



**1990
Linear Applications Handbook
Volume I**

A Guide to Linear Circuit Design



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Linear Technology Corporation

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INTRODUCTION

Why Write Applications?

This is seemingly an odd and unlikely way to begin an applications publication, but it is a valid question. As such, the components of the decision to produce this book are worth reviewing.

Producing linear application material requires an intensive, extended effort. Development costs for worthwhile material are extraordinarily high, absorbing substantial amounts of engineering time and money. Further, these same resources could be directed towards product development, the contribution of which is much more easily measured at the corporate coffers. These are serious issues in any environment, but are particularly critical in a rapidly growing company, where resources must be thoughtfully allocated.

Linear Technology Corporation's commitment to a concerted applications effort was made despite these concerns. Specifically, the nature of linear circuit design is so diverse, the devices so sophisticated, and user requirements so demanding that designers require (or at least welcome) assistance. Ultimately, the procurement and use of linear ICs is tied to the user's ability to solve the problems confronting them. Anything which enhances this ability, in both specific and general cases, obviously benefits user and vendor.

This is a very simple but powerful argument, and is the basis of LTC's commitment to applications. Additional benefits include occasional new product concepts and a way to test products under "real world" conditions, but the basic justification is as described.

Traditionally, application work has involved reviewing considerations for successful use of a specific product. Additionally, basic circuit suggestions or concepts are sometimes offered. Although this approach is useful and necessary, some expansion is possible. LTC's applications are centered on detailed, systems-oriented circuits, (hopefully) similar to the types of designs users are working with. There is a broad tutorial content, reflected in the form of frequent text digressions and liberal use of graphics. Discussions of trade-offs, options and techniques are emphasized, as opposed to brief descriptions of circuit operation. Many of the application notes contain appended sections which examine related or pertinent topics in detail. Ideally, this treatment provides enough background to allow readers to modify the circuits presented into solutions to their specific problems.

Some comment about the circuit examples is appropriate. They range from relatively simple to quite complex and sophisticated. Emphasis is on high performance, in keeping with the capabilities of LTC's products and the market we serve. The circuit's primary function is to serve as a catalyst—once the reader has started thinking, the material has accomplished its mission.

Substantial effort has been expended in working out and documenting these circuits, but they are not finessed to the highest possible degree. All of the circuits have been breadboarded and bench-tested at the prototype level. Specifications and performance levels quoted in the text represent measured and extrapolated data derived from the breadboard prototype. The volume of material generated prohibits formal worst-case review or tolerance analysis for production. Additionally, despite our best efforts, errors of various sorts do occasionally creep in along the way to publication. Because of these considerations, readers should contact LTC when preparing to use a circuit in a production situation. This allows us to advise on specific areas of the circuit which may require a "second look" before going to production. Updates, suggested modifications and just plain mistakes can also be discussed at this time.

We have received numerous comments and questions since this books first (1987) edition. The most frequent query concerns topic selection. The topics presented are survivors of a selection process involving a number of disparate considerations. These include reader needs, suitability for magazine publication, LTC's short and long term commercial aspirations, time constraints and author interest in doing the work. Additionally, we seek a 10 year useful lifetime for application notes. This generally precludes narrowly focused effort towards individual IC's. Topics are broad, with a tutorial and design emphasis that (ideally) reflects the readers long term interests. While the circuits presented unabashedly favor our products, they must be conceptually applicable to succeeding generations of devices (hopefully ours). Similarly, the circuits should represent a relatively complete and interdisciplinary approach to solving the problem at hand. Solving a problem is usually the readers/customers overwhelming motivation. The selection and integration of tools and methods towards this end is *the* priority. For this reason the examples and accompanying text are as complete and practical as possible. This may necessitate effort in areas where we have no direct economic stake, e.g., the software presented in AN28 or the magnetics developed for AN25, AN29 and AN35. In some circumstances this policy necessitates use of competitors products (horrors!) where appropriate. Such gallant objectivity is not without calculation; the goal is to have readers associate LTC with realistic advice, useful products and satisfactory results, regardless of the problem encountered. The long term task is establishing and maintaining credibility and customer loyalty. If unabused, these are powerful sales tools. Maintaining this stance involves a significant amount of negotiation and compromise with issues and individuals, but the results are usually favorable for everyone.

A second common question addresses the time and effort required to produce an individual application note. The work invested varies considerably. AN29 required a year to complete. It involved endless laboratory hours, close coordination with our magnetics supplier and over 300 changes, corrections,

band-aids and tweaks before the manuscript was finally released. Conversely, AN31 and AN32 were finished (perhaps therapeutically) within three weeks. In all cases the actual writing time is a miniscule percentage of the total work time. AN29's year of effort was written up in a week. AN31 and AN32 required less than five hours.

Another common question involves our photographic documentation. We have received hundreds of inquiries requesting details on instrumentation, particularly for multi-trace oscilloscope photography. Almost all photographic work is done with four (Tektronix 547 with a four trace 1A4 plug-in) or eight (Tektronix 556 with two 1A4 plug-ins) trace oscilloscopes. Photographs with more than eight traces utilize multiple exposure or splicing techniques. Tektronix C-12 and C-27 cameras are used on both instruments, with modified graticule illumination on the 556. AN29's Appendix F provides additional discussion.

A final recurring question concerns use of this book as text in university level courses. We certainly welcome this, and find it rewarding. However, we cannot develop, or collaborate in the development of, supplementary material for problem sets and laboratory manuals. This simply strays too far from our charter.

Some significant additions since the 1987 edition are "Design Notes" and the open format used in AN26, AN27 and AN36. "Design Notes" provide a way to cover a specific topic in concise form and get the material to the reader quickly. Most of these notes are stand-alone efforts. In some cases they are excerpted from application note work in progress and fed directly to print. When the application note becomes available the material appears in unabridged form. Another change is the format used for AN26, AN27 and AN36. The segmented approach allows convenient updating and additions at some sacrifice in text flow. Subjects amenable to this treatment avoid the disruptive surgery required to revise a conventional manuscript.

In response to reader requests we have included macromodels of components. The present list includes 28 IC's, all amplifiers. This inventory will grow and diversify into other part types. Significant effort has gone towards making these models realistic and usable. They are intended as powerful adjunct tools in the design process, and should not be abused. More specifically, they are meant to augment actual breadboards, not eliminate them. Bypassing breadboarding is an extraordinarily hazardous process with a high fatality rate, even among veteran designers. Although these macromodels cannot eliminate the cold realities involved in making something work, they ease the task and save time. As such, we encourage readers to use them and invite your comments.

Also new is the inclusion of application notes from other sources. These notes, found in the "Reference Reading" section, have proven particularly useful to readers. The information they contain is pertinent to problem areas that concern our readers. As such, they merit inclusion. If this approach is well received this section will be enlarged in succeeding editions. The cooperation of the contributors is appreciated.

Finally, the appearance of new authors is applauded, particularly by the undersigned. There is plenty of work to do and many pens (and probes) ease the task while broadening perspective.

Acknowledgements

A number of people with a wide variety of talents contributed to this book. LTC's senior management, most notably R. Swanson, B. Dobkin and B. Ehsam, provided continuous support and encouragement. M. J. Yuhas showed special skill in converting the worst form of "chicken tracks" into legible, expertly prepared and edited manuscripts and is due special recognition.

B. Essaff prepared some beautiful breadboards (until I corrupted his construction technique) and was a major contributor to the lab work. C. Nelson, T. Redfern, G. Erdi, W. Rempfer, D. O'Neill, N. Sevastopoulos, and B. Huffman contributed useful comments, most of which were not diluted by tact.

In the final analysis, however, the ultimate acknowledgement must be reserved for our customers, who are both the beneficiaries and benefactors of this book. Their requests and requirements define our work, and hence this book. If we have listened carefully, they should be pleased.



James M. Williams
November, 1989
Milpitas, California

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The index is organized so that application circuits and subject tutorials are easily found. The major categories are broken up into specialized topics to help isolate a particular application. The subject index works as follows, i.e. AN8, Pg. 8 = Application Note 8 page 8; LTC1044 DS = LTC1044 Data Sheet; DN17, Pg. 1 = Design Note 17 page 1.

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ACCELEROMETER—See Signal Conditioning

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Precision Absolute Value Circuit: OP05 DS

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Large Signal Voltage Follower: LT1001 DS

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Clamping Techniques

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Fast DC Stabilized FET Amplifier (100V/ μs , 1MHz FPB): AN21, Pg. 2

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Fast Precision Inverter: LTC1052 DS

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- “Current Mode Feedback” (Son of Godzilla Amplifier) (3000V/ μ s, 25MHz FPB): AN21, Pg. 8; AN22, Pg. 13; LT1088 DS

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- Simple Pre-Amplifier for the Comparator: AN17, Pg. 4
- “No Trims” 12 Bit Multiplying DAC Output Amplifier: LT1012 DS; LT1022 DS; LT1055 DS
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- Advantages of Matched Dual Op Amps: LT1002 DS; OP227 DS; LT1024 DS
- Gain 1000 Amplifier with 0.01% DC Accuracy: LT1007 DS
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- Stabilized FET Buffer (FET Probe): AN9, Pg. 9

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- “Current Mode Feedback” Amplifier (1MHz FPB): AN21, Pg. 7; AN22, Pg. 12; LT1088 DS

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LT1102 DS

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Amplifier: LTC1100 DS

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HELP

Linear Technology Corporation

Call Applications: 408-432-1900

HEWLETT, W. R.

Oscillator

“A New Type Resistance-Capacity Oscillator” M.S. Thesis,
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- Wein Bridge Sine Wave Oscillator: LM101 DS
- Ultra Pure Sine Wave Generator: LT1007 DS; LT1022 DS
- Super Low Distortion Variable Sine Wave Oscillator: LT1028 DS
- Low Distortion, Crystal Stabilized Oscillator: LT1057 DS

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Half Sine Wave

A Half-Sine Reference Generator: AN35, Pg. 28

REFERENCE-CURRENT—See Also Current

Sink

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Source

Precision Current Source: LT1001 DS

Precision Current Source (1 μ A): LT1019 DS

REFERENCE-VOLTAGE

2-Terminal

10V Buffered Reference Using a Single Supply: LM129 DS;
OP07 DS

6.9V Reference: LM129 DS

1.235V Micropower Reference: LT1004 DS; LT1034 DS

1.25V Reference: LT1004 DS

2.5V Reference: LT1004 DS; LM185 DS

Low Noise Reference: LT1004 DS

3-Terminal

Wide Supply Range: LM136 DS

2.5V Reference, \pm 5V Trim Range: LT1009 DS; LM136 DS

Low Noise 2.5V Buffered Reference: LT1009 DS; LM136 DS

Switchable \pm 1.25V Bipolar Reference: LT1009 DS; LM136 DS

Wide Supply Range, Adjustable Reference: LT1009 DS

Split \pm 2.5V References: LT1029 DS

Trimming Output to 5.120V: LT1029 DS

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Precision High Current Reference (1.5A): AN2, Pg. 7

Handling Higher Load Currents: LT1019 DS; LT1021 DS;
LT1031 DS

Output Current Boost with Current Limit: LT1019 DS; LT1021 DS;
LT1031 DS

Boosted Output Current with No Current Limit: LT1021 DS;
LT1031 DS

Discussion

Heat Mode Reduces Temperature Drift to Less Than 2ppm/ $^{\circ}$ C:
LT1019 DS

Output Trimming: LT1019 DS

Effects of Air Movement on Low Frequency Noise: LT1021 DS

Trimming Output Voltage: LT1021 DS

Application Hints for Ultra-Precision Reference: LTZ1000 DS

High Voltage

Ultra Precision Variable Voltage Reference (7.45ppm/ $^{\circ}$ C):
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Low Noise Reference: LT1004 DS

2-Pole Lowpass Filtered Reference: LT1021 DS; LT1031 DS

Low Noise Reference: LTZ1000 DS

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Self-Buffered Micropower Reference: DN23, Pg. 1; LT1178 DS

Micropower 5V Reference: LM185 DS; LM134 DS

1.235V Micropower Reference: LT1004 DS

2.5V Micropower Reference: LT1004 DS

Micropower 5V Reference: LT1004 DS

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Ultra Precision Inverter: AN3, Pg. 14

Negative 10V Reference for CMOS DAC: LT1019 DS; AD580 DS

Negative Series Reference: LT1019 DS; LT1021 DS; AD580 DS

Basic Negative Reference: LT1021 DS; LT1031 DS; AD580 DS

CMOS DAC with Low Drift Full Scale Trimming: LT1021 DS

Negative Shunt Reference Driven by Current Source:
LT1021 DS; LT1031 DS

Negative Voltage Reference: LTZ1000 DS

Precision

10V Buffered Reference: LM199 DS

6.95V Reference: LM199 DS

Portable Calibrator: LM199 DS

Standard Cell Replacement: LM199 DS

Precision \pm 10V Reference: LT1002 DS

Buffered Reference for A to D Converters: LT1012 DS

Heat Mode Reduces Temperature Drift to Less than 2ppm/ $^{\circ}$ C:
LT1019 DS

Operating 5V Reference from 5V Supply: LT1021 DS

Precision DAC Reference with System TC Trim: LT1021 DS;
LT1031 DS

Restricted Trim Range for Improved Resolution: LT1021 DS;
LT1019 DS

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Standard Grade Variable Voltage Reference: AN9, Pg. 5

Saturated Standard Cell Amplifier: LT1008 DS; LT1012 DS

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- Ultra Precision Variable Voltage Reference (7.45ppm/°C): AN6, Pg. 6; LT1001 DS; LT1002 DS
- 7V Positive Reference: LTZ1000 DS
- Adjusting Temperature Coefficient in Unstabilized Application: LTZ1000 DS
- Averaging Reference Voltages for Lower Noise and Better Stability: LTZ1000 DS
- Low Noise Reference: LTZ1000 DS

REGULATOR-CURRENT—See Also Current

Source

- Two Terminal Current Regulator: LM10 DS
- Current Regulator: LT1033 DS

REGULATOR-SWITCHING

Boost

- Single Cell Up Converter (1.5V to 5V): AN8, Pg. 8; AN30, Pg. 8
- Up Converter (6V to 15V): AN8, Pg. 9; LT1013 DS; AN30, Pg. 7
- Single Inductor, Dual Polarity Regulator (6V to ± 15V): AN8, Pg. 10; LT1013 DS; AN30, Pg. 9
- Boost Converter (1.5V to 5V): AN15, Pg. 7; AN30, Pg. 8; LT1018 DS
- Boost Converter (5V to 12V): AN19, Pg. 13; AN25, Pg. 2; AN30, Pg. 5
- Voltage Boosted Boost Converter (15V to 100V): AN19, Pg. 37; AN30, Pg. 5; LT1070 DS
- Negative Boost Regulator (– 15V to – 28V): AN19, Pg. 38; AN30, Pg. 5; LT1070 DS
- Current Boosted Boost Converter (16V–24V to 28V): AN19, Pg. 40; AN30, Pg. 5; LT1070 DS
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- Low Quiescent Current Flyback Regulator (150μA, 6V to 12V): AN29, Pg. 9; DN11, Pg. 2; AN30, Pg. 6
- 200mA Output Converter (1.5V to 5V): AN29, Pg. 15; AN30, Pg. 7
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- High Repetition Rate Vp-p Pulse Generator (5V to 12.75V or 12.00V): DN17, Pg. 2; AN30, Pg. 43
- Up Converter (1.5V to 5V): LM10 DS; AN30, Pg. 8
- Regulated Up Converter (5V to 10V): LT1018 DS; AN30, Pg. 8
- Negative Boost Converter (– 4.5V to – 15V to – 15V): LT1074 DS
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- Switching Pre-Regulator Linear Regulator (9V to 5V): AN8, Pg. 5; AN30, Pg. 17; LT1013 DS
- Negative Buck Converter (– 20V to – 5.2V): AN19, Pg. 17; AN30, Pg. 16; LT1070 DS
- Positive Buck Converter: AN19, Pg. 23; AN30, Pg. 15; LT1070 DS
- Micropower Switching Regulator (5.8V–10V to 5V): AN23, Pg. 15; AN30, Pg. 17
- Micropower Post Regulated Switching Regulator (6V–10V to 5V): AN23, Pg. 16; AN30, Pg. 32
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- High Power Switched Capacitor Voltage Converter (12V to 5V):
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- Regulated Negative Voltage Converter: AN8, Pg. 2;
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Telecom

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 1A Regulator with Current Limit: LT1020 DS
 Current Limited 1A Regulator: LT1020 DS
 Improving Ripple Rejection: LT1038 DS; LT117 DS; LT138 DS
 Regulator with Reference: LT117 DS; LT117HV DS

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 Adjustable Regulator 0V-10V @5A: LT1003 DS
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SEEBECK EFFECT

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SEEBECK, THOMAS

Temperature

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ZOO

San Francisco

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SECTION 1—APPLICATION NOTES

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AN26J	Interfacing the LTC1091 to the TMS7742 MCU	AN26J-1
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AN26M	Interfacing the LTC1090 to the TMS320C25 DSP	AN26M-1
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AN36D	Interfacing the LTC1290 to the COP820C MCU	AN36D-1
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AN36F	Interfacing the LTC1290 to the COP402N MCU	AN36F-1
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Understanding and Applying the LT1005 Multifunction Regulator

Jim Williams

The number of voltage regulators currently available makes the introduction of another regulator seem almost unnecessary. However, a new device, the LT1005, offers auxiliary functions which help solve problems often associated with voltage regulation in circuits.

The LT1005 (Figure 1) consists of a 5V, 1A* regulator, which is controlled by a positive logic enable pin, and a 5V auxiliary regulator. The auxiliary regulator's output is

unaffected by the state of the main regulator. Thermal overload protection and current limiting round out the device. The enable pin is a high impedance input which floats in a high state. $10\mu\text{A}$ * of current pulled from the pin will force it below its 1.6V turn-off threshold, shutting down the main output. Figure 2A shows a simple but useful application. Here, the regulator's enable pin is controlled by the state of a toggling flip-flop which is triggered by a pushbutton on a computer keyboard. The

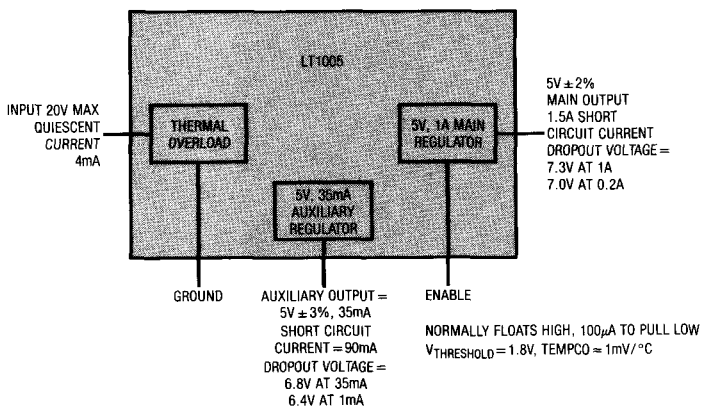


Figure 1

*A 3A version of the LT1005 is also available. See LT1035.

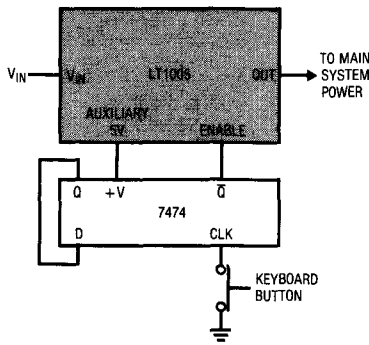
Application Note 1

auxiliary 5V output powers the flip-flop when the computer has been shut down. This arrangement allows the normal separate power switch to be eliminated. Although the enable pin interfaces directly to CMOS and TTL, its relatively high impedance allows it to implement a number of diverse functions.

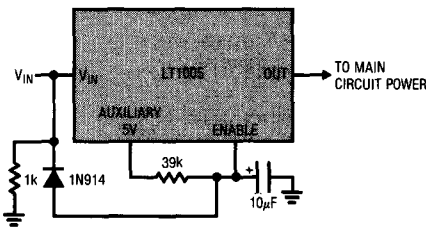
Figure 2B is a power-on delay circuit. Upon application of power, the output is held low until the capacitor charges beyond the 1.6V threshold of the enable pin. In this case, the time required is about 100ms. The diode-1k combination drains the capacitor quickly when power is removed.

Figure 2C shows a simple arrangement which will latch down the main regulator output if a short circuit occurs in

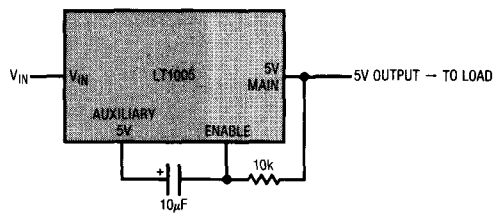
the load. When power is applied to the regulator, the 5V auxiliary output comes up, transferring charge through the 10 μ F unit. This forces the enable pin high, allowing the main regulator to come up and power the load. If a load short occurs, the regulator goes into current limit and the main output falls to zero. This pulls the enable pin low, completing a positive feedback latch which disables the main regulator output. Under these conditions the output will remain at zero, even after the load short is removed. Also, the regulator will not have to dissipate power for the duration of the short circuit. The output may be reset by removing regulator input power or forcing the enable pin.



(A)



(B)



(C)

Figure 2

Figure 3 illustrates a circuit which takes advantage of this operation to achieve a cost-effective solid-state equivalent of a circuit breaker. This circuit will turn off the main regulator's output within 700ns of an over-load. The trip current and breaker delay times are settable over a wide range. Under normal conditions the current through the 1Ω shunt is insufficient to bias Q1 into conduction. Q2 is also off and the regulator functions. When an overload occurs (Trace A, Figure 4 is the regulator's output current), the potential across the 1Ω resistor rises, turning on Q1. Q1's collector drives Q2's base (Trace B, Figure 4) via the $1k$ resistor and the $100pF$ speed-up capacitor. This turns on Q2, pulling the enable pin (Trace C, Figure 4) to ground and shutting down the regulator output (Trace D, Figure 4). The $10k$ value from the main output to the enable pin latches the regulator down in a fashion similar to Figure 1 and the $4.7\mu F$ capacitor shown in dashed lines may be added (delete the $100pF$ unit) for applications where fast response is not desirable. The 1Ω value can be selected to accommodate any desired current trip point.

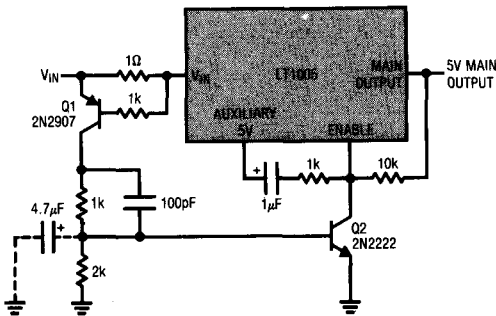


Figure 3

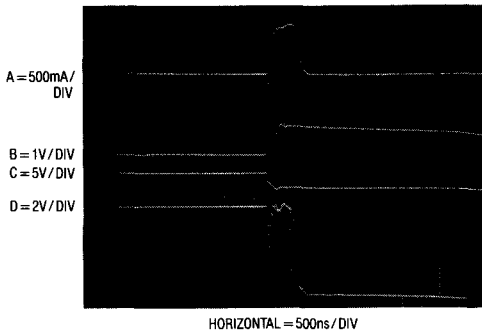


Figure 4

Figure 5 shows another circuit which uses the enable pin to shut down the regulator under abnormal conditions.

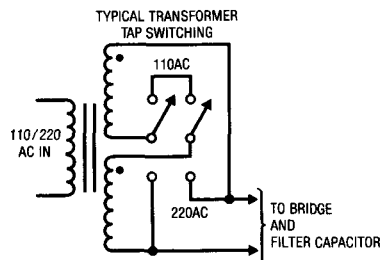
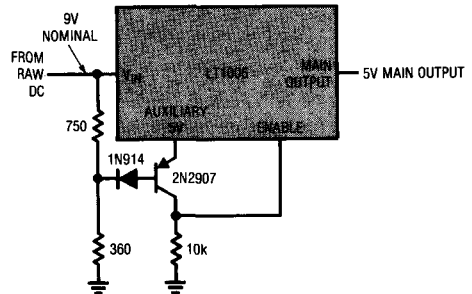


Figure 5

This configuration is useful in instruments or systems meant to be powered from 110VAC or 220VAC. Powering a regulator from a 220VAC primary when the secondary transformer tap switch is set for 110VAC forces excessive dissipation in the regulator, leading to thermal shutdown. The circuit shown prevents this by sensing the abnormally high input voltage and shutting down the regulator. Under normal operating conditions the input voltage is low enough to keep the transistor on, pulling the enable pin toward the auxiliary output and maintaining regulator output. If the circuit is inadvertently powered from 220VAC without moving the transformer tap switch, the regulator's input voltage rises. This cuts off the transistor and the $10k$ resistor pulls the enable pin to ground, shutting down the regulator. The diode in the transistor's base line prevents V_{BE} zenering during the reverse bias condition which exists during the shutdown. For the values given, this circuit will function properly over ranges of 88VAC–135VAC and 180VAC–260VAC (110VAC–220VAC $\pm 20\%$).

Application Note 1

Figure 6 shows the LT1005 in another circuit where operation depends on input conditions. This circuit is useful in systems where it is necessary to bring up and power-down circuitry in a sequence. It is particularly applicable in situations where it is desirable to transfer and store data into nonvolatile memory during power outages. It functions by taking advantage of the differing dropout voltages between the main and auxiliary outputs. When power is first applied, the LT1005 input (Trace A, Figure 7) starts to ramp up. The auxiliary output (Trace D, Figure 7) follows this ramping action and clamps at its 5V regulated output. During this interval, C1 monitors the difference between the regulator input and the 5V auxiliary output. The resistor ratios at its inputs are scaled so that the enable pin (Trace B, Figure 7) will be clamped until the regulator input is high enough to support main output regulation. (The small ramp segments visible at the enable pin are

due to the comparator output's failure to clamp under very low supply voltage conditions. They do not influence overall circuit operation.) When this point is reached, the main output (Trace C, Figure 7) comes up quickly. Because the auxiliary output precedes the main output, it can be used to preset conditions in the circuitry being powered by the regulator. When power falls below the threshold point, C1 pulls the enable pin (Trace B, Figure 7) low, forcing the regulator's main output to go off rapidly. The auxiliary output, however, maintains regulation after the main output has gone off. This allows the main output to be used as a logic signal to alert auxiliary-powered non-volatile memory to store data. The amount of time the auxiliary output will maintain regulation on power-down may be controlled by regulator filter capacitor size. The diode-4.7k combination provides regenerative action to assure a clean turn-off for the main output.

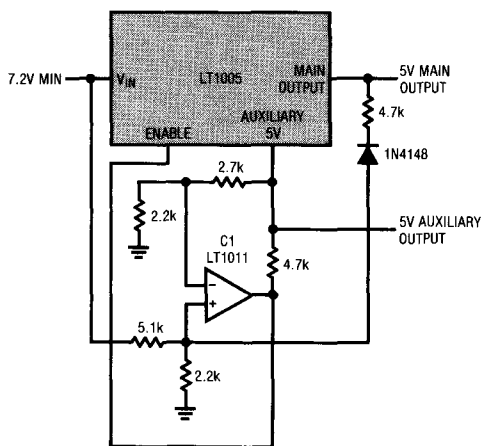


Figure 6

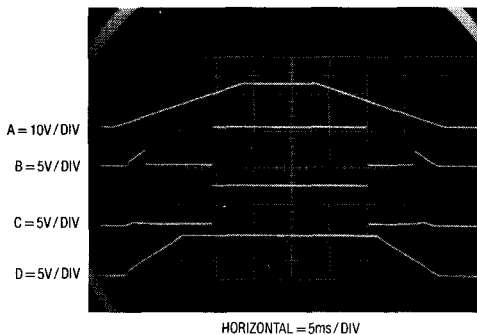


Figure 7

In some systems it is more convenient, or advantageous, to detect power outages by directly monitoring the AC line. Figure 8's circuit does this by connecting an optoisolator across the AC output of the power transformer. Normally, the AC line (Trace A, Figure 9) turns on the LED every 8ms ($\frac{1}{2}$ cycle of the line), causing the Darlington output transistor to reset the $0.01\mu\text{F}$ capacitor to $V_{CE(SAT)}$. When the line drops out (Trace B, Figure 9), the capacitor charges at a rate dependent upon the setting of the 20k potentiometer. This ramping voltage is compared by C1 to a refer-

ence derived from the auxiliary output. When C1 goes low, the regulator output goes low (Trace C, Figure 9). This occurrence can be used as a logic signal to flag circuitry which is powered by the auxiliary output. The "trip set" potentiometer and the value of the capacitor can be used to determine the number of missing line cycles required to shut down the regulator. When using this circuit it is important to recognize that the hold-up time of the raw supply must be taken into account to determine how long the auxiliary output will remain regulated.

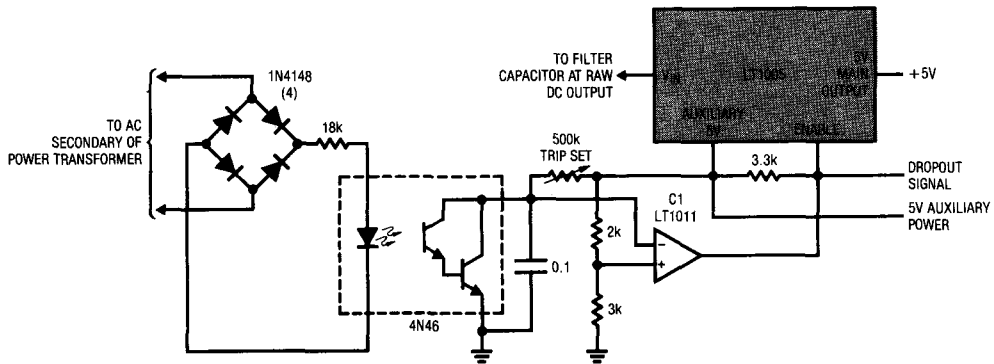


Figure 8

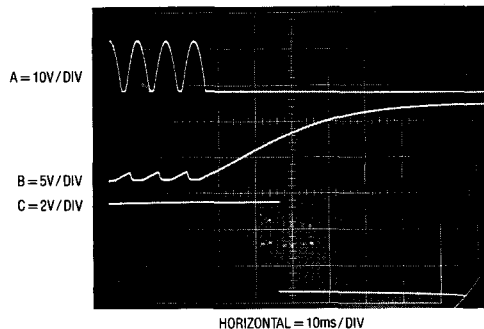


Figure 9

Application Note 1

Figure 10 shows a latching circuit similar to Figure 2, except that a negative temperature coefficient (NTC) sharp transition thermistor runs from the enable pin to ground.

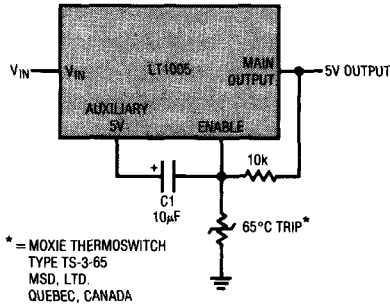


Figure 10

This circuit will provide latching protection for circuitry under thermal overloads due to blocked vents or fan failures. The NTC device resistance decreases from 200k at 60°C to 10k at 65°C, cutting off the regulator. The thermistor is biased from the output, so latch-off occurs when the trip temperature is reached. C1 ensures starting. Unfortunately, the transition and hysteresis points of NTC devices are fixed and cannot be user-varied. Figure 11 takes advantage of the relatively high impedance of the enable input to circumvent this problem. A standard thermistor (negative temperature coefficient) allows the trip point and hysteresis band to be set at any desired point. For the example shown, the regulator will shut down at 58°C ambient (8k thermistor resistance) and come back up at 42°C (15.2k thermistor resistance). Other characteristics are obtainable by shifting resistor and thermistor values.

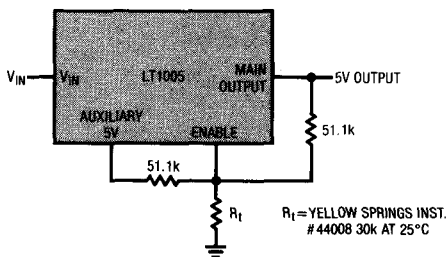


Figure 11

Figure 12 shows another thermally-related use of the regulator. The highest crystal oscillator stabilities are achieved by temperature-stabilizing the crystal. In frequency-measuring equipment and communications work it is often important that the crystal frequency be stabilized before the equipment is used. In this circuit, the LT1005 combines with a typical commercial crystal oven to prevent equipment use until oven temperature has stabilized. When power is applied, pin 6 of the crystal oven is high, biasing Q1. Simultaneously, the SCR gate is triggered by auxiliary-generated output current coming through the 4.7µF unit. This disables the main regulator output. When the oven reaches temperature, the thermoswitch opens, removing bias from Q1. This commutates the SCR and the regulator comes up, allowing its load to operate. The 4.7k resistor eliminates false SCR triggering and the diode suppresses reverse gate current when regulator input power is removed.

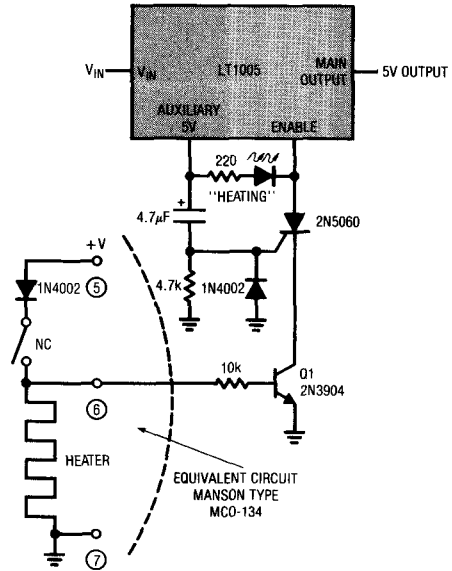
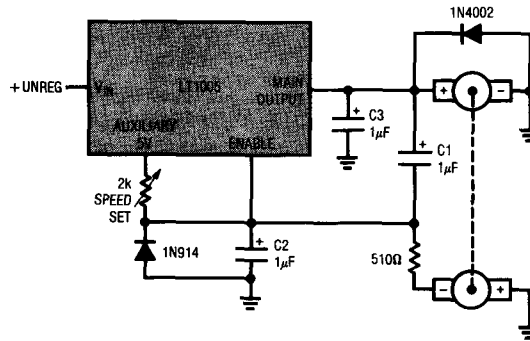


Figure 12

The latching action used in many of the preceding applications is one form of feedback. *Negative* feedback to the enable pin can be used to make closed loop servos. Figure 13 shows a way to make a simple switched-mode motor speed controller with the LT1005. This circuit uses a tachometer to generate a feedback signal which is compared to a reference supplied by the auxiliary output. When power is applied, the tachometer output is zero and the regulator output (Trace A, Figure 14) comes on, forcing current (Trace C, Figure 14) into the motor. As motor rotation increases, the negative tachometer output pulls the enable pin (Trace B, Figure 14) toward ground. When the enable pin's threshold voltage is reached, the regulator output goes down and the motor slows. The regulator provides positive feedback, ensuring clean transitions. In this fashion, the motor's speed is servo-controlled at a point

determined by the 2k potentiometer setting. The regulator free-runs at whatever frequency and duty cycle are required to maintain the enable pin at its threshold. Loop bandwidth and stability are set by C2 and C3. The 1N914 diode prevents the negative output tachometer from pulling the enable pin below ground while the 1N4002 commutates the motor's negative flyback pulse. The servo-controlled pulse mode excitation allows the motor to furnish excellent torque characteristics, even when operating at 5% of its full speed rating. For example, the small motor listed, with a shaft torque rating of 20 gram-cMs at 3300RPM, is almost unstopable by the unaided human hand at 150RPM. The thermal and current limiting in the regulator prevents either the motor or the regulator from burning up in the event of a shaft overload.



MOTOR-TACH = CANON #EF-26-R1-N1

Figure 13

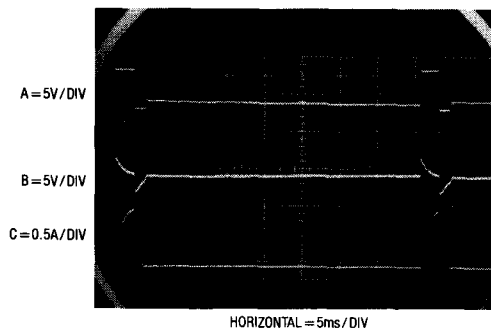


Figure 14

Application Note 1

Figure 15 shows a way to run higher voltage motors. In this mode the motor is placed in the regulator input line and the output is terminated into a 3.3Ω load. The servo loop operates in a similar fashion to the one in Figure 13. In this case, however, a large capacitor is placed at the regulator to filter the transients generated by motor switching. When the tachometer output (Trace A, Figure 16) calls for power, the regulator comes on, allowing current to flow through the motor. This forces the regulator input toward ground (Trace B, Figure 16) for the duration of the on-time. The

circuit's advantage is that it allows higher voltage motors (up to 20V) to be controlled. In common with the previous circuit, the regulator provides thermal and current overload protection for the motor. Its disadvantage is that for servo setpoints which require high motor power, the regulator's DC input will go below dropout and the auxiliary output will fall, destabilizing the servo setpoint. Each of these circuits offers a simple, cost-effective, one package solution to speed control of small motors at the expense of efficiency.

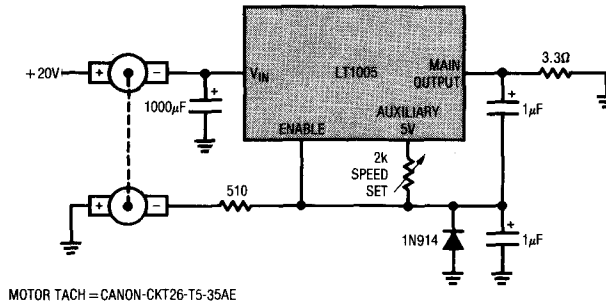


Figure 15

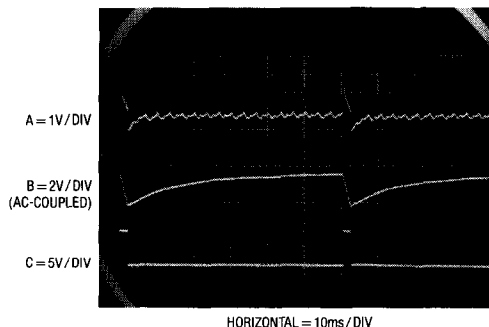


Figure 16

Performance Enhancement Techniques for Three-Terminal Regulators

Jim Williams

Three terminal regulators provide a simple, effective solution to voltage regulation requirements. In many situations the regulator can be used with no special considerations. Some applications, however, require special techniques to enhance the performance of the device.

Probably the most common modification involves extending the output current of regulators. Conceptually, the simplest way to do this is by paralleling devices. In practice, the voltage output tolerance of the regulators can cause problems. Figure 1 shows a way to use two regulators to achieve an output current equal to their sum. This circuit capitalizes on the 1% output tolerance of the specified regulators to achieve a simple paralleled configuration. Both regulators sense from the same divider string and the small value resistors provide ballast to account for the slightly differing output voltages. This added impedance degrades total circuit regulation to about 1%.

Figure 2 shows another way to extend current capability in a regulator. Although this circuit is more complex than Figure 1, it eliminates the ballasting resistor's effects and has a fast-acting logic-controlled shutdown feature. Additionally, the current limit may be set to any desired value. This circuit extends the 1A capacity of the LT1005 multi-function regulator to 12A, while retaining the LT1005's enable feature and auxiliary 5V output. Q1, a booster transistor, is servo-controlled by the LT1005, while Q2 senses the current dependent voltage across the 0.05Ω shunt. When the shunt voltage is large enough, Q2 comes on, biasing Q3 and shutting down the regulator via the LT1005's enable pin. The shunt's value can be selected for the desired current limit. The 100°C thermoswitch limits dissipation in Q1 during prolonged short circuits by disabling the LT1005. It should be mounted on Q1's heat sink.

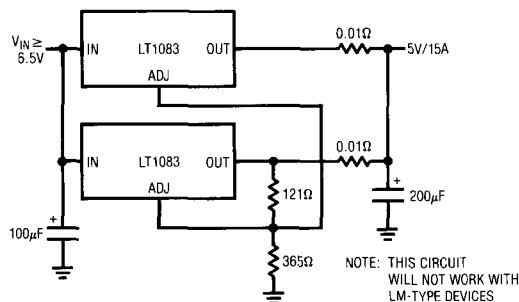


Figure 1

Application Note 2

Boosted regulator schemes of this type are often poorly dynamically damped. Such improper loop compensation results in large output transients for shifts in the load. In particular, because Q1's common emitter configuration has voltage gain, transients approaching the input voltage are possible when the load drops out. Here, the 100 μ F capacitor damps Q1's tendency to overshoot, while the 20 Ω value provides turn-off bias. The 250 μ F unit maintains Q1's emitter at DC. Figure 3 shows that this "brute force" compensation works quite well. Normally the regulator sees no load. When Trace A goes high, a 12A load (regulator output current is Trace C) is placed across the output terminals. The regulator output voltage recovers quickly, with minimal aberration.

While the 100 μ F output capacitor aids stability, it prevents the regulator output from dropping quickly when the enable command is given. Because Q1 cannot sink current, the 100 μ F unit's discharge time is load limited. Q4 corrects this problem, even when there is no load. When the enable command is given (Trace A, Figure 4) Q3 comes on, cutting off the LT1005 and forcing Q1 off. Simultaneously, Q4 comes on, pulling down the regulator output (Trace B), and sinks the 100 μ F capacitor's discharge current (Trace C). If fast turn-off is not needed, Q4 may be omitted.

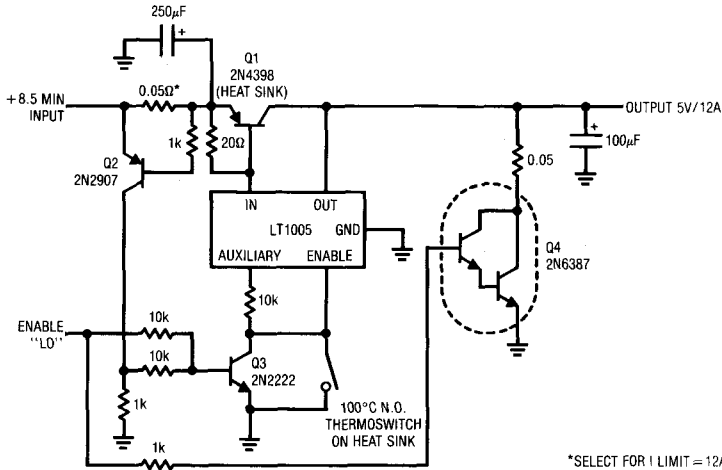


Figure 2

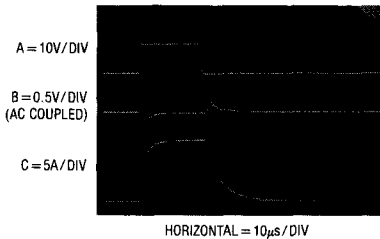


Figure 3

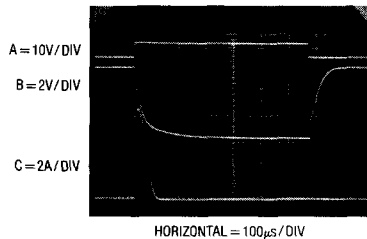


Figure 4

Power dissipation control is another area where regulators can be helped by additional circuitry. Increasing heat sink area can be used to offset dissipation problems, but is a wasteful and inefficient approach. Instead, the regulator can be placed within a switched-mode loop that servo-controls the voltage across the regulator. In this arrangement the regulator functions normally while the switched-mode control loop maintains the voltage across it at a minimal value, regardless of line or load changes. Although this approach is not quite as efficient as a classical switching regulator, it offers lower noise and the fast transient response of the linear regulator. Figure 5 details a DC driven version of the

circuit. The LT350A functions in the conventional fashion, supplying a regulated output at 3A capacity. The remaining components form the switched-mode dissipation limiting control. This loop forces the potential across the LT350A to equal the 3.7V value of V_Z . When the input of the regulator (Trace A, Figure 6) decays far enough, the LT1018 output (Trace B) switches low, turning on Q1 (Q1 collector is Trace D). This allows current flow (Trace C) from the circuit input into the 4500 μ F capacitor, raising the regulator's input voltage. When the regulator input rises far enough, the comparator goes high, Q1 cuts off and the capacitor ceases charging.

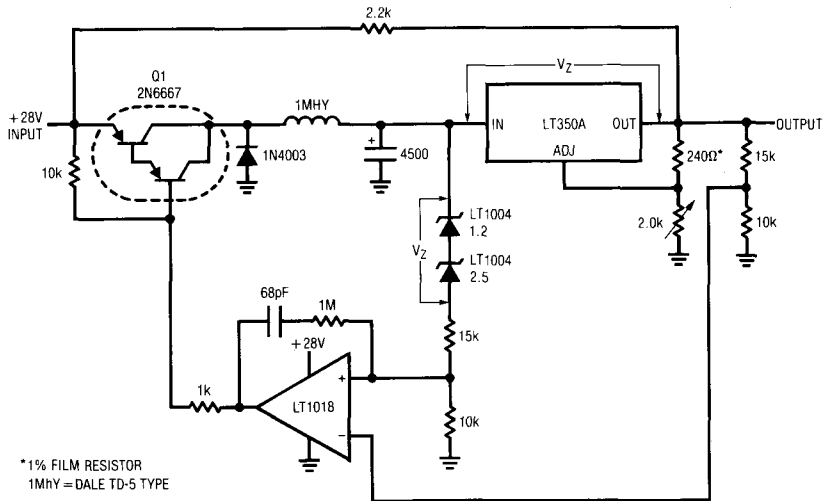


Figure 5

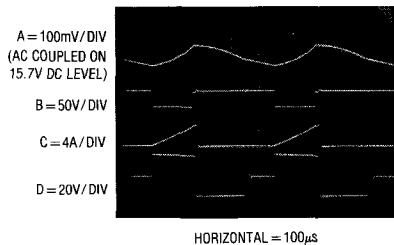


Figure 6

Application Note 2

The 1N4003 damps the flyback spike of the current limiting inductor. The 4.7kΩ unit ensures circuit start-up and the 68pF-1MΩ combination sets loop hysteresis at about 80mVp-p. This free-running oscillation control mode substantially reduces dissipation in the regulator, while preserving its performance. Despite changes in the input voltage, different regulated outputs or load shifts, the loop always ensures the minimum possible dissipation in the regulator.

Figure 7 shows the dissipation limiting technique applied in a more sophisticated circuit. This AC powered version provides 0V-35V, 10A regulation under high line-low line (90VAC-140VAC) conditions with good efficiency. In this version, two SCRs and a center tapped transformer source power to the inductor-capacitor combination. The transformer output is also diode rectified (Trace A, Figure 8), divided down, and used to reset the 0.1μF unit (Trace B)

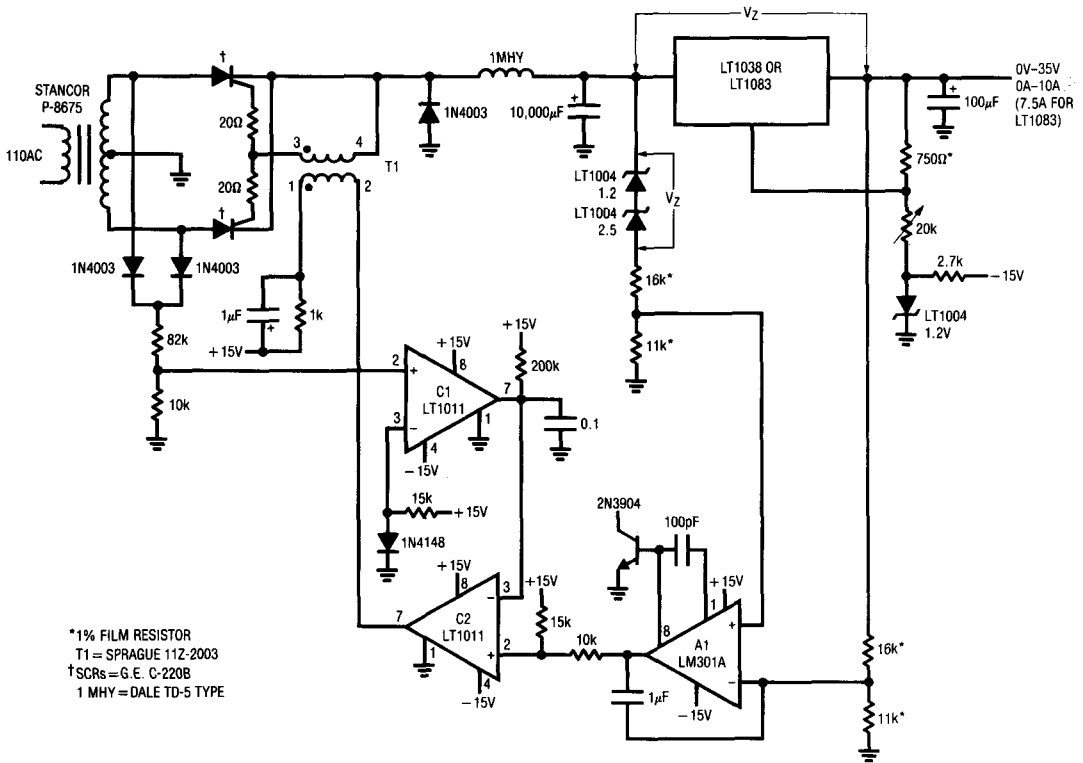


Figure 7

via C1. The resulting AC line synchronous ramp at C1's output is compared to A1's offset output by C2. A1's output represents the deviation from the V_Z value that the loop is trying to force across the LT1038. When the ramp output exceeds C2's "+" input value, C2 pulls low, dumping current through T1's primary (Trace C). This fires the appropriate SCR and a path from the main transformer to the LC pair occurs (Trace D). The resultant current flow (Trace E) is limited by the inductor and charges the capacitor. When the AC line cycle drops low enough, the SCR commutates and charging ceases. On the next half-cycle the process repeats, except that the alternate SCR does the work. In this fashion, the loop controls the phase angle at which the SCRs fire to keep the voltage across the

LT1038 at V_Z (3.7V). As a result, the circuit functions over all line, load and output voltage conditions with good efficiency. The 1.2V LT1004 at the LT1038 allows the output voltage to be set down to 0.00 and the 2N3904 clamp at A1 prevents loop "hangup". Figure 7A shows a way to trigger the SCRs without using a transformer.

Although A1's output is an analog voltage, the AC driven nature of the circuit makes it approximate a smoothed, sampled loop response. Conversely, the regulator constitutes a true linear system. Because these two feedback systems are interlocked, frequency compensation can be difficult.

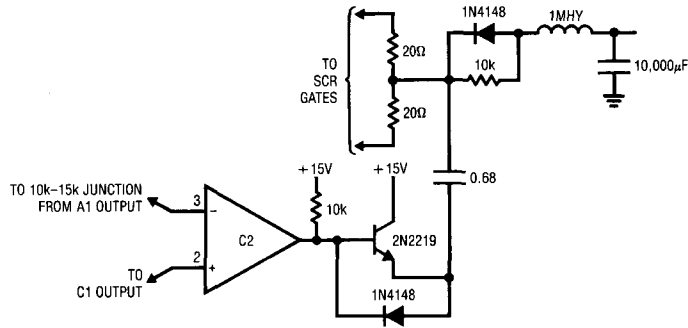


Figure 7A

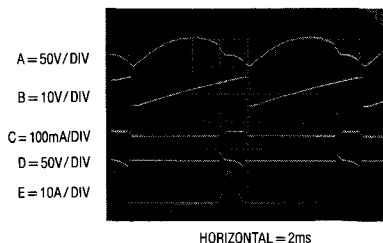


Figure 8

Application Note 2

In practice, A1's 1 μ F capacitor keeps dissipation loop gain at a low enough frequency for stable characteristics, without influencing the LT1038's transient response characteristic. Trace A, Figure 9 shows the output noise while the circuit is operating at 35V into a 10A load (350W). Note the absence of fast switching transients and harmonics. The output noise is made up of residual 120Hz ripple and regulator noise. Reflected noise into the AC power line is also negligible (Trace B) because the inductor limits current rise time to about 1ms, much slower than the normal switching supplies. Figure 10 shows a plot of efficiency versus output voltage for a 10A load. At low output voltages, where the static losses across the regulator and SCRs are significant, efficiency suffers, but 85% is attained at the upper extreme.

High voltage output is another area for regulator enhancement. In theory, because the regulator does not have a ground pin, it can regulate high voltages. In normal operation the regulator floats at the supply's upper level, and as long as the $V_{IN}-V_{OUT}$ maximum differential is not exceeded there are no problems. However, if the output is shorted, the $V_{IN}-V_{OUT}$ maximum is exceeded and device destruction will occur. The circuit of Figure 11 shows a complete high voltage regulator that delivers 100V at 100mA and withstands shorts to ground. Even at 100V output the LT317A functions in the normal mode, maintaining 1.2V between its output and adjustment pin.

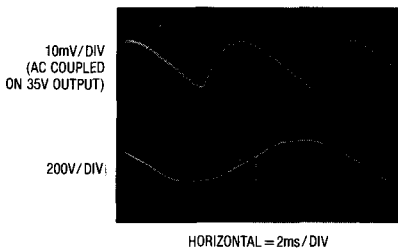


Figure 9

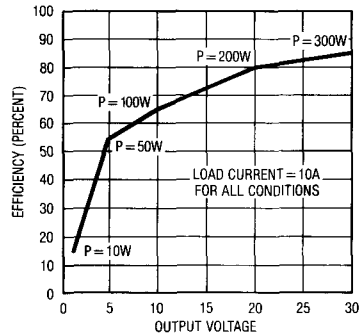


Figure 10

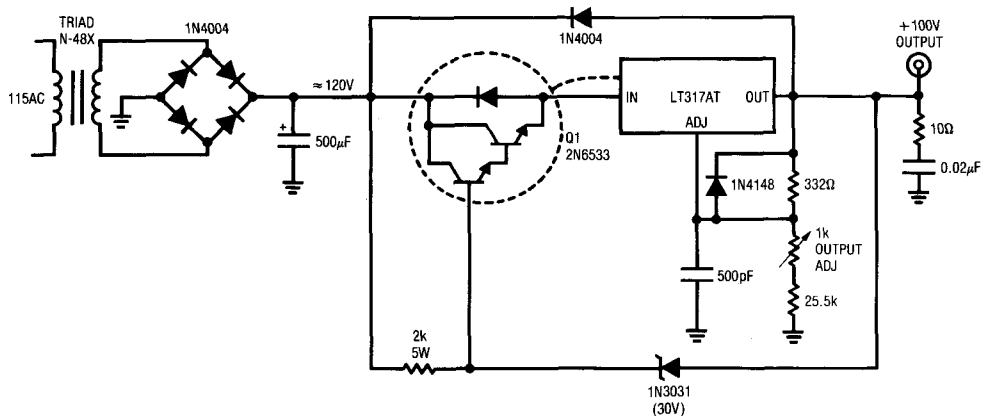


Figure 11

Under these conditions the 30V zener is off and Q1 conducts. When an output short occurs, the zener conducts, forcing Q1's base to 30V. This causes Q1's emitter to clamp $2 V_{BE}$ s below V_Z , well within the $V_{IN}-V_{OUT}$ rating of the regulator. Under these conditions, Q1, a high voltage device, sustains 90V V_{CE} at whatever current the transformer and the regulator's current limit will support. The transformer specified saturates at 130mA, keeping Q1 well within its safe area as it dissipates 12W. If Q1 and the LT317A are thermally coupled, the regulator will soon go into thermal shutdown and oscillation will commence. This action will continue, protecting the load and the regulator as long as the output remains shorted. The 500pF capacitor and the $10\Omega-0.02\mu F$ damper aid transient response and the diodes provide safe discharge paths for the capacitors.

This approach to high voltage regulation is primarily limited by the power dissipation capability of the device in series with the regulator. Figure 11A uses a vacuum tube in series with the regulator. (remember them?) to achieve very high short circuit dissipation capability. The tube allows high voltage operation and is extremely tolerant of overloads. This circuit allows the LT317A to control 600W at 2000V (V_1 's plate limit is 300mA) with full short circuit protection.

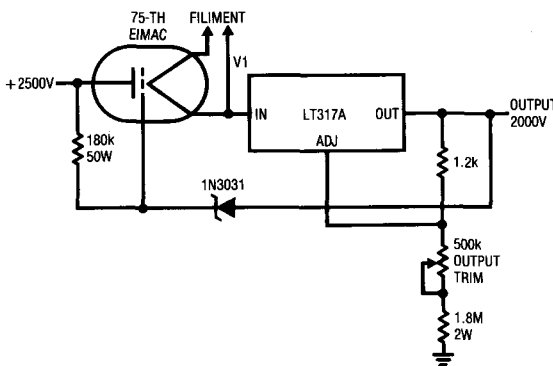
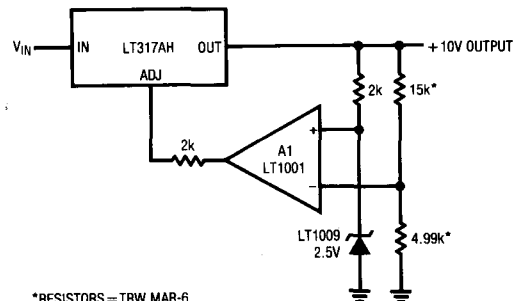


Figure 11A

Power is not the only area in which regulator performance can be augmented. Figure 12 shows a way to increase the stability of a regulator's output over time and temperature. This is particularly useful in powering strain gauge-based transducers. In this circuit the output voltage is divided down and compared to the 2.5V reference by A1, a precision amplifier. A1's output is used to force the LT317A's adjustment pin to whatever voltage is required to maintain the 10V output. A1 contributes negligible error. The resistors specified will track within 5ppm/ $^{\circ}C$ and the reference contributes about 20ppm/ $^{\circ}C$. The regulator's internal circuitry protects against short circuits and thermal overload.

Figure 13's circuit allows a regulator to remotely sense the feedback voltage, eliminating the effects of voltage drop in the supply lines. This is a concern where high currents must be transmitted over relatively long supply rails or PC traces. Figure 13's circuit uses A1 to sense the voltage at the point of load. A1's output, summed with the regulator's output, modifies the adjustment pin voltage to compensate for the voltage lost across R_{DROP} . The feedback divider is returned through a separate lead from the load, completing the remote sensing scheme. The $5\mu F$ capacitor filters noise and the 1k value limits bypass capacitor discharge when power is turned off.



*RESISTORS = TRW MAR-6

Figure 12

Application Note 2

A final circuit allows voltage regulator-powered circuitry to run from 110VAC or 220VAC without having to switch transformer windings. Regulator dissipation does not increase for 220VAC inputs. In Figure 14, when T1 is driven from 110VAC, the LT1011 output goes high, allowing the SCR to receive gate bias through the 1.2k resistor. The 1N4002 is off. T1's output is rectified by the SCR and the regulator sees about 8.5V at its input. If T1 is plugged into a 220VAC source, the negative input at the LT1011 is driven beyond 2.5V and the device's output clamps low. This steers the SCR's gate bias to ground through the LT1011's output transistor. The diodes in the

LT1011 output line prevent reverse voltages from reaching the SCR or the LT1011 output. Now, the SCR goes off and the 1N4002 sources current to the regulator from T1's center tap. Although T1's input voltage has doubled, its output potential has halved and regulator power dissipation remains the same. Figure 15 shows the AC line input versus regulator input voltage transfer function. The switch to center tap drive occurs midway between 110VAC and 220VAC. The hysteresis, a desirable characteristic, occurs because T1's output voltage shifts with the step change in loading.

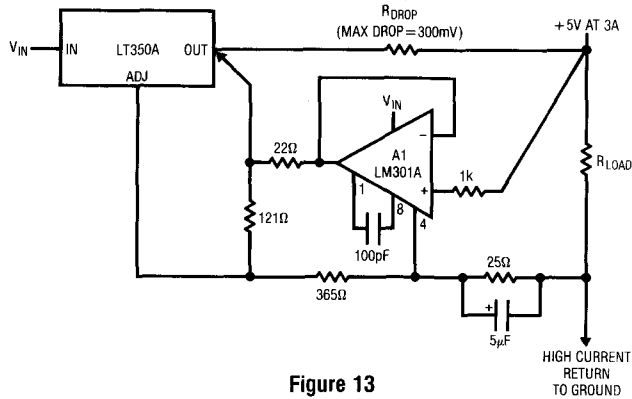


Figure 13

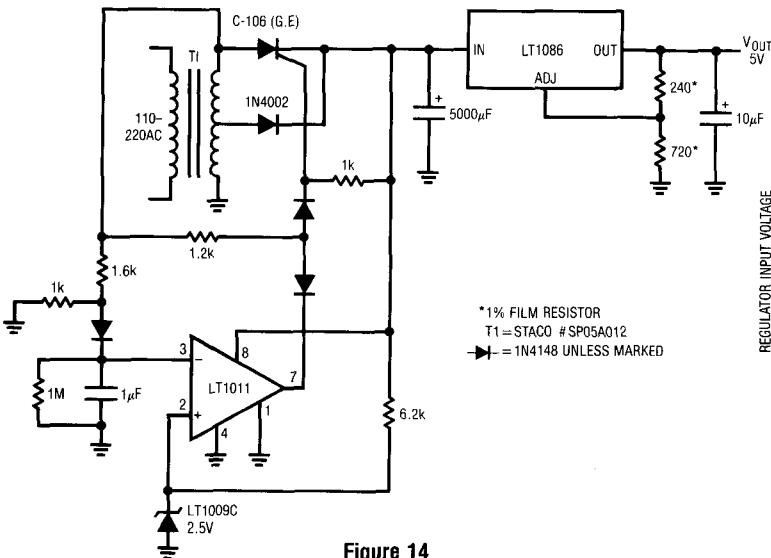


Figure 14

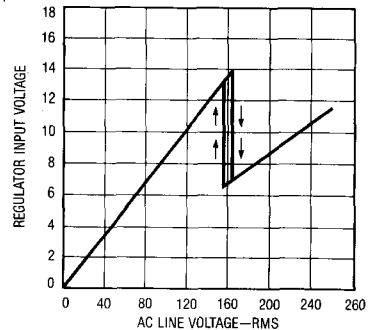


Figure 15

Applications for a Switched-Capacitor Instrumentation Building Block

Jim Williams

CMOS analog IC design is largely based on manipulation of charge. Switches and capacitors are the elements used to control and distribute the charge. Monolithic filters, data converters and voltage converters rely on the excellent characteristics of IC CMOS switches. Because of the importance of switches in their circuits, CMOS designers have developed techniques to minimize switch induced errors, particularly those associated with stray capacitance and switch timing. Until now, these techniques have been used only in the internal construction of monolithic devices. A new device, the LTC1043, makes these switches available for board level use. Multi-pole switching and a self-driven, non-overlapping clock allow the device to be used in circuits which are impractical with other switches.

Conceptually, the LTC1043 is simple. Figure 1 details its features. The oscillator, free-running at 200kHz, drives a non-overlapping clock. Placing a capacitor from pin 16 to ground shifts the oscillator frequency downward to any desired point. The pin may also be driven from an external source, synchronizing the switches to external circuitry. A non-overlapping clock controls both DPDT switch sections. The non-overlapping drive prevents simultaneous conduction in the series connected switch sections.

Charge balancing circuitry cancels the effects of stray capacitance. Pins 1 and 10 may be used as guard points for pins 3 and 12 in particularly sensitive applications.

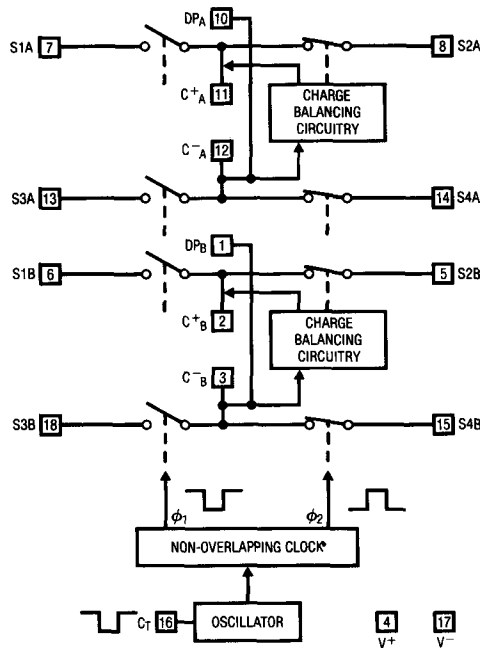


Figure 1. Block Diagram of LTC1043 Showing Individual Switches

Application Note 3

Although the device's operation is simple, it permits surprisingly sophisticated circuit functions. Additionally, the careful attention paid to switching characteristics makes implementing such functions relatively easy. Discrete timing and charge-balance compensation networks are eliminated, reducing component count and trimming requirements.

Classical analog circuits work by utilizing continuous functions. Their operation is usually described in terms of voltage and current. Switched-capacitor based circuits are sampled data systems which approximate continuous functions with bandwidth limited by the sampling frequency. Their operation is described in the distribution of charge over time. To best understand the circuits which follow, this distinction should be kept in mind. Analog sampled data and carrier based systems are less common than true continuous approaches, and developing a working familiarity with them requires some thought.

Switched-capacitor approaches have greatly aided analog MOS IC design. The LTC1043 brings many of the freedoms and advantages of CMOS IC switched-capacitor circuits to the board level, providing a valuable addition to available design techniques.

Instrumentation Amplifier

Figure 2 uses the LTC1043 to build a simple, precise instrumentation amplifier. An LTC1043 and an LT1013 dual op amp are used, allowing a dual instrumentation amplifier using just two packages. A single DPDT section converts the differential input to a ground referred single-ended signal at the LT1013's input. With the input switches closed, C1 acquires the input signal. When the input switches open, C2's switches close and C2 receives charge. Continuous clocking forces C2's voltage to equal the difference between the circuit's inputs. The 0.01 μ F capacitor at pin 16 sets the switching frequency at 500Hz. Common-mode voltages are rejected by over 120dB and drift is low.

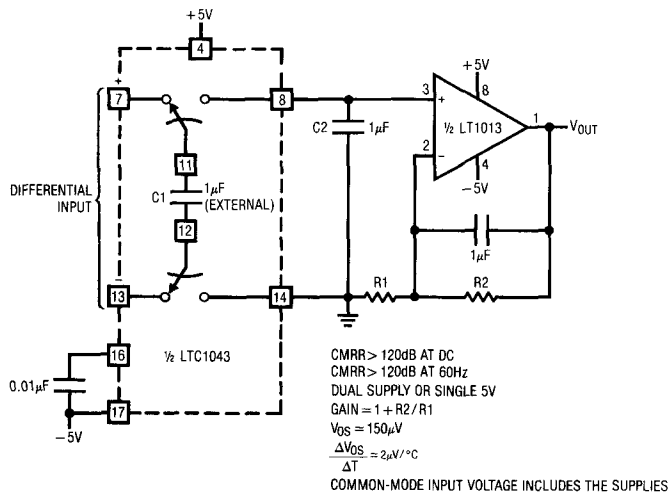


Figure 2. $\pm 5V$ Precision Instrumentation Amplifier

Amplifier gain is set in the conventional manner. This circuit is a simple, economical way to build a high performance instrumentation amplifier. Its DC characteristics rival any IC or hybrid unit and it can operate from a single 5V supply. The common-mode range includes the supply rails, allowing the circuit to read across shunts in the supply lines. The performance of the instrumentation amplifier depends on the output amplifier used. Specifications for an LT1013 appear in the figure. Lower figures for offset, drift and bias current are achievable by employing type LT1001, LT1012, LT1056 or the chopper-stabilized LTC1052.

Ultra-High Performance Instrumentation Amplifier

Figure 3 is similar to Figure 2, but utilizes the remaining LTC1043 section to construct a low drift chopper amplifier. This approach maintains the true differential inputs while achieving $0.1\mu\text{V}/^\circ\text{C}$ drift. The differential input is converted to a single-ended potential at pin 7 of the LTC1043. This voltage is chopped into a 500Hz square wave by the switching action of pins 7, 11, and 8. A1, AC coupled, amplifies this signal. A1's square wave output, also AC coupled, is synchronously demodulated by switches 12, 14, and 13. Because this switch section is

synchronously driven with the input chopper, proper amplitude and polarity information is presented to A2, the DC output amplifier. This stage integrates the square wave into a DC voltage to provide the output. The output is divided down and fed back to pin 8 of the input chopper where it serves as the zero signal reference. Because the main amplifier is AC coupled, its DC terms do not affect overall circuit offset, resulting in the extremely low offset and drift noted in the specifications. This circuit offers lower offset and drift than any commercially available instrumentation amplifier.

Lock-In Amplifier

The AC carrier approach used in Figure 3 may be extended to form a "lock-in" amplifier. A lock-in amplifier works by synchronously detecting the carrier modulated output of the signal source. Because the desired signal information is contained within the carrier, the system constitutes an extremely narrow-band amplifier. Non-carrier related components are rejected and the amplifier passes only signals which are coherent with the carrier. In practice, lock-in amplifiers can extract a signal 120dB below the noise level.

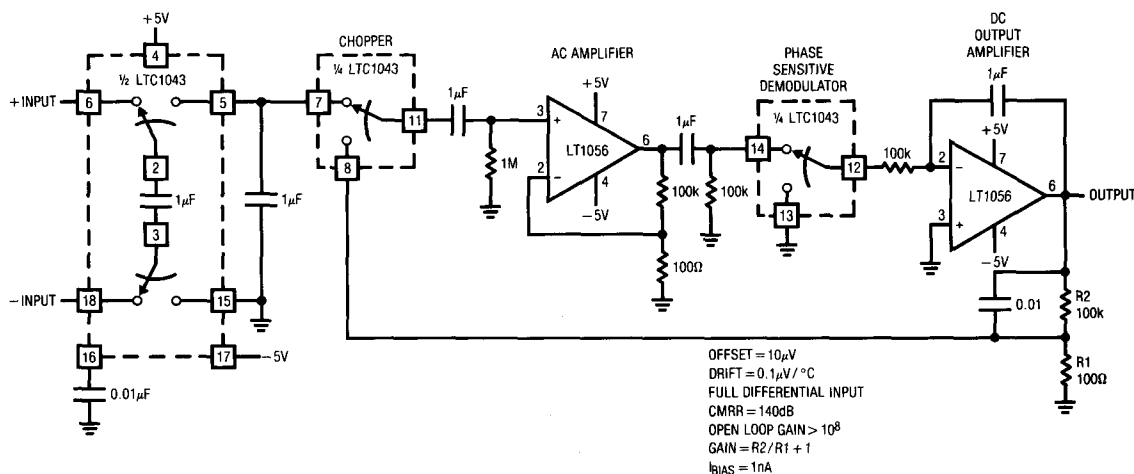


Figure 3. Chopper-Stabilized Instrumentation Amplifier

Application Note 3

Figure 4 shows a lock-in amplifier which uses a single LTC1043 section. In this application, the signal source is a thermistor bridge which detects extremely small temperature shifts in a biochemical microcalorimetry reaction chamber.

The 500Hz carrier is applied at T1's input (Trace A, Figure 5). T1's floating output drives the thermistor bridge, which presents a single-ended output to A1. A1 operates at an AC gain of 1000. A 60Hz broadband noise source is also deliberately injected into A1's input (Trace B). The carrier's zero crossings are detected by C1. C1's

output clocks the LTC1043 (Trace C). A1's output (Trace D) shows the desired 500Hz signal buried within the 60Hz noise source. The LTC1043's zero-cross-synchronized switching at A2's positive input (Trace E) causes A2's gain to alternate between plus and minus one. As a result, A1's output is synchronously demodulated by A2. A2's output (Trace F) consists of demodulated carrier signal and non-coherent components. The desired carrier amplitude and polarity information is discernible in A2's output and is extracted by filter-averaging at A3. To trim this circuit, adjust the phase potentiometer so that C1 switches when the carrier crosses through zero.

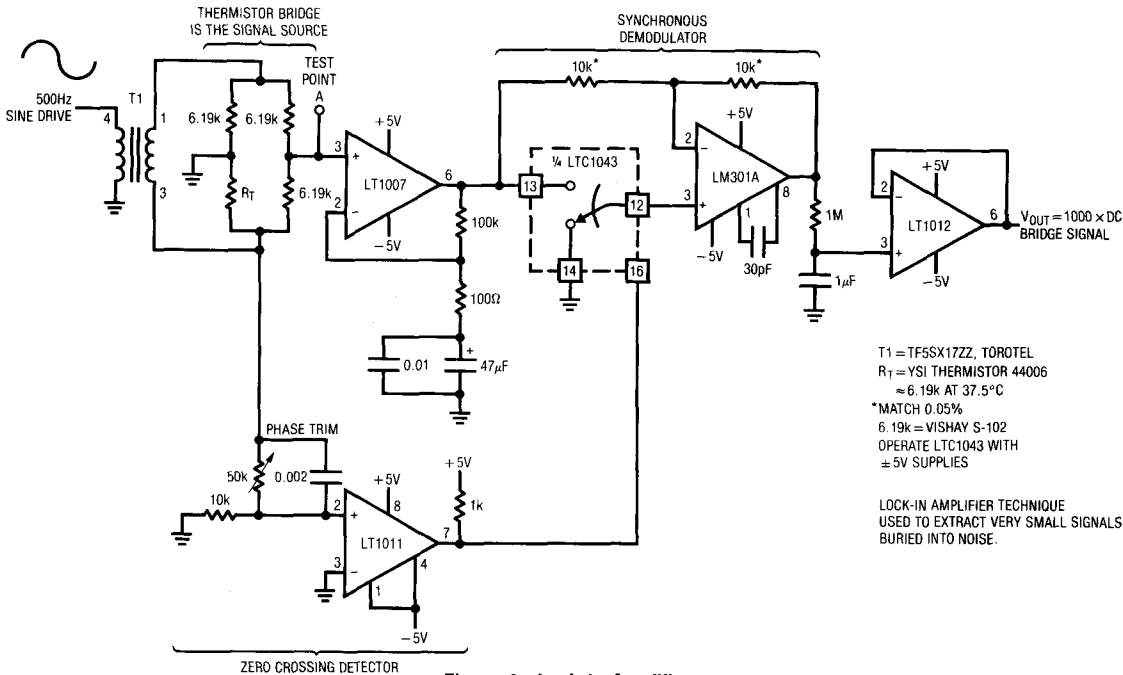


Figure 4. Lock-In Amplifier

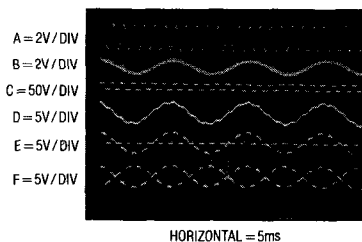


Figure 5

Wide Range, Digitally Controlled, Variable Gain Amplifier

Aside from low drift and noise rejection, another dimension in amplifier design is variable gain. Designing a wide range, digitally variable gain block with good DC stability is a difficult task. Such configurations usually involve relays or temperature compensated FET networks in expensive and complex arrangements. The circuit shown in Figure 6 uses the LTC1043 in a variable gain amplifier which features continuously variable gain from 0-1000, gain stability of 20ppm/°C and single-ended or differential input. The circuit uses two separate LTC1043s. Unit A is clocked by a frequency input which could be derived from a host processor. LTC1043B is continuously clocked by a 1kHz source which could also be processor supplied. Both LTC1043s function as the sampled data equivalent of a resistor within the bandwidth set by A1's 0.01μF value and the switched-capacitor equivalent feedback resistor. The time-averaged current delivered to the summing point by LTC1043A is a function of the 0.01μF capacitor's input-derived voltage and the commutation frequency at pin 16. Low commutation frequen-

cies result in small time-averaged current values, approximating a large input resistor. Higher frequencies produce an equivalent small input resistor. LTC1043B, in A1's feedback path, acts in a similar fashion. For the circuit values given, the gain is simply:

$$G = \frac{f_{IN}}{10} \times \frac{0.01\mu F}{100pF}$$

Gain stability depends on the ratiometric stability between the 1kHz and variable clocks (which could be derived from a common source) and the ratio stability of the capacitors. For polystyrene types, this will typically be 20ppm/°C. The circuit input, determined by the pin connections shown in the figure, may be either single-ended or fully differential. Additionally, although A1 is connected as an inverter, the circuit's overall transfer function may be either positive or negative. As shown, with pins 13A and 7A grounded and the input applied to 8A, it is negative.

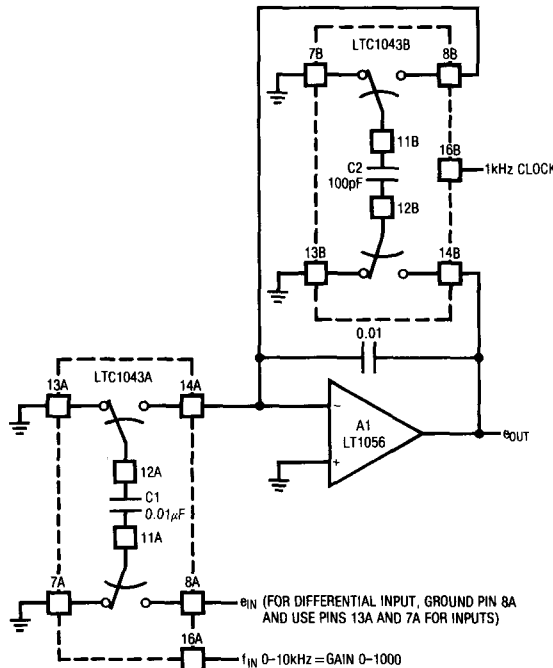


Figure 6. Variable Gain Amplifier

Application Note 3

Precision, Linearized Platinum RTD Signal Conditioner

Figure 7 shows a circuit which provides complete, linearized signal conditioning for a platinum RTD. One side of the RTD sensor is grounded, often desirable for noise considerations. This LTC1043 based circuit is considerably simpler than instrumentation or multi-amplifier based designs and will operate from a single 5V supply. A1 serves as a voltage-controlled ground referred current source by differentially sensing the voltage across the 887Ω feedback resistor. The LTC1043 section which does this presents a single-ended signal to A1's negative input, closing a loop. The 2k-0.1μF combination sets amplifier roll-off well below the LTC1043's switching frequency and the configuration is stable. Because A1's loop forces a fixed voltage across the 887Ω resistor, the current through R_p is constant. A1's operating point is primarily fixed by the 2.5V LT1009 voltage reference.

The RTD's constant current forces the voltage across it to vary with its resistance, which has a nearly linear positive temperature coefficient. The non-linearity could cause several degrees of error over the circuit's 0°C–400°C operating range. A2 amplifies R_p's output, while simultaneously supplying non-linearity correction. The correction is implemented by feeding a portion of A2's output back to A1's input via the 10k–250k divider. This causes the current supplied to R_p to slightly shift with its operating point, compensating sensor non-linearity to within ±0.05°C. The remaining LTC1043 section furnishes A2 with a differential input. This allows an offsetting potential, derived from the LT1009 reference, to be subtracted from R_p's output. Scaling is arranged so 0°C equals 0V at A2's output. Circuit gain is set by A2's feedback values and linearity correction is derived from the output.

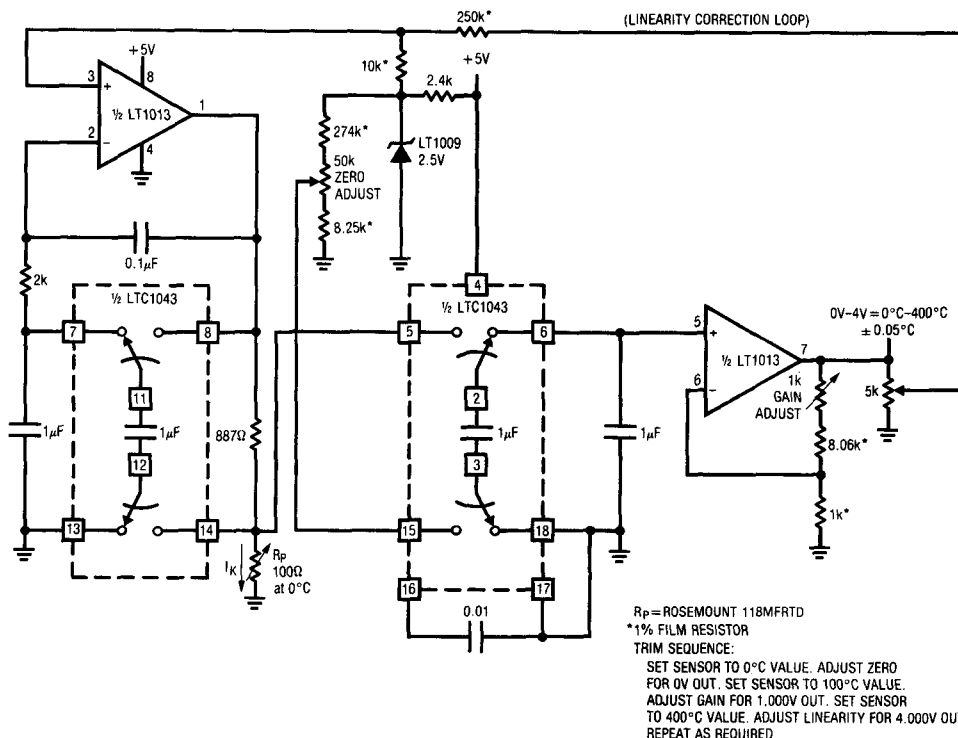


Figure 7. Linearized Platinum Signal Conditioner

To calibrate this circuit, substitute a precision decade box (e.g., General Radio 1432k) for R_p . Set the box to the 0°C value (100.00Ω) and adjust the offset trim for a 0.00V output. Next, set the decade box for a 140°C output (154.26Ω) and adjust the gain trim for a 1.400V output reading. Finally, set the box to 249.0°C (400.00°C) and trim the linearity adjustment for a 4.000V output. Repeat this sequence until all three points are fixed. Total error over the entire range will be within $\pm 0.05^\circ\text{C}$. The resistance values given are for a nominal 100.00Ω (0°C) sensor. Sensors deviating from this nominal value can be used by factoring in the deviation from 100.00Ω . This deviation, which is manufacturer specified for each individual sensor, is an offset term due to winding tolerances during fabrication of the RTD. The gain slope of the platinum is primarily fixed by the purity of the material and is a very small error term.

Note that A1 constitutes a voltage controlled current source with input and output referred to ground. This is a difficult function to achieve and is worthy of separate mention.

Relative Humidity Sensor Signal Conditioner

Relative humidity is a difficult physical parameter to transduce, and most transducers available require fairly complex signal conditioning circuitry. Figure 8 combines two LTC1043s with a recently introduced capacitively based humidity transducer in a simple charge-pump based circuit.

The sensor specified has a nominal 500pF capacitance at $\text{RH} = 76\%$, with a slope of $1.7\text{pF}/\% \text{RH}$. The average voltage across this device must be zero. This provision prevents deleterious electrochemical migration in the sensor. LTC1043A inverts a resistively scaled portion of the LT1009 reference, generating a negative potential at pin 14A. LTC1043B alternately charges and discharges the humidity sensor via pins 12B, 13B, and 14B. With 14B and 12B connected, the sensor charges via the $1\mu\text{F}$ unit to the negative potential at pin 14A. When the 14B-12B pair opens, 12B is connected to A1's summing point via 13B. The sensor now discharges into the summing point through the $1\mu\text{F}$ capacitor. Since the charge

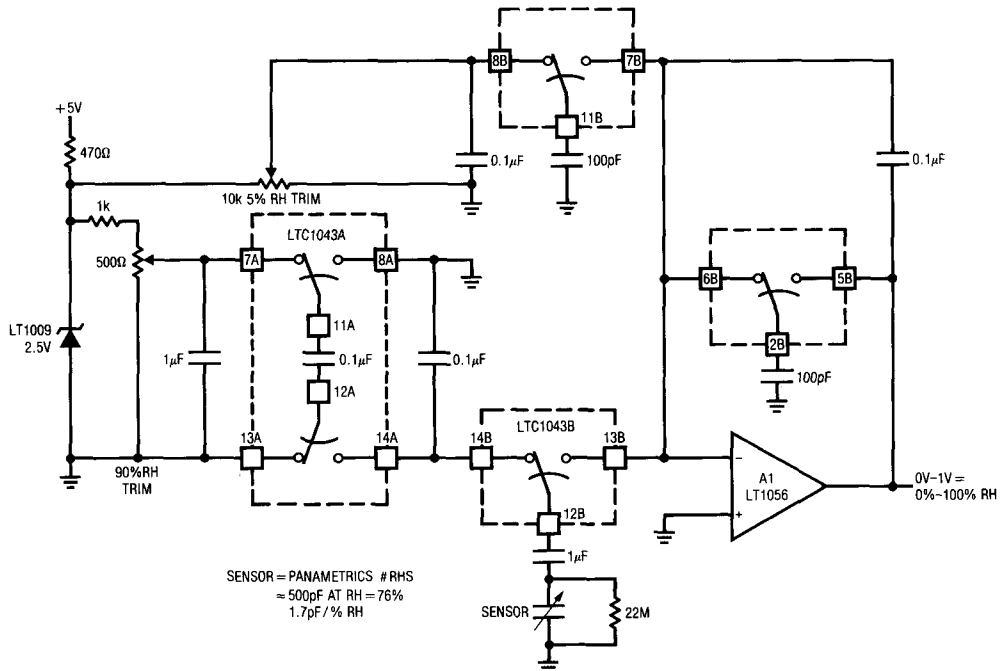


Figure 8. Relative Humidity Signal Conditioner

Application Note 3

voltage is fixed, the average current into the summing point is determined by the sensor's humidity related value. The $1\mu\text{F}$ value AC couples the sensor to the charge-discharge path, maintaining the required zero average voltage across the device. The 22M resistor prevents accumulation of charge, which would stop current flow. The average current into A1's summing point is balanced by packets of charge delivered by the switched-capacitor network in A1's feedback loop. The $0.1\mu\text{F}$ capacitor gives A1 an integrator-like response, and its output is DC.

To allow 0% RH to equal 0V, offsetting is required. The signal and feedback terms biasing the summing point are expressed in charge form. Because of this, the offset must also be delivered to the summing point as charge, instead of a simple DC current. If this is not done, the circuit will be affected by frequency drift of LTC1043B's oscillator. Section 8B-11B-7B serves this function, delivering LT1009-referenced offsetting charge to A1.

Drift terms in this circuit include the LT1009 and the ratio stability of the sensor and the 100pF capacitors. These terms are well within the sensor's 2% accuracy specification and temperature compensation is not required. To calibrate this circuit, place the sensor in a known 5% RH environment and adjust the "5% RH trim" for 0.05V output. Next, place the sensor in a 90% RH environment and set the "90% RH trim" for 900mV output. Repeat this procedure until both points are fixed. Once calibrated, this circuit is accurate within 2% in the 5%–90% RH range.

Figure 9 shows an alternate circuit which requires two op amps but needs only one LTC1043 package. This circuit retains insensitivity to clock frequency while permitting a DC offset trim. This is accomplished by summing in the offset current after A1.

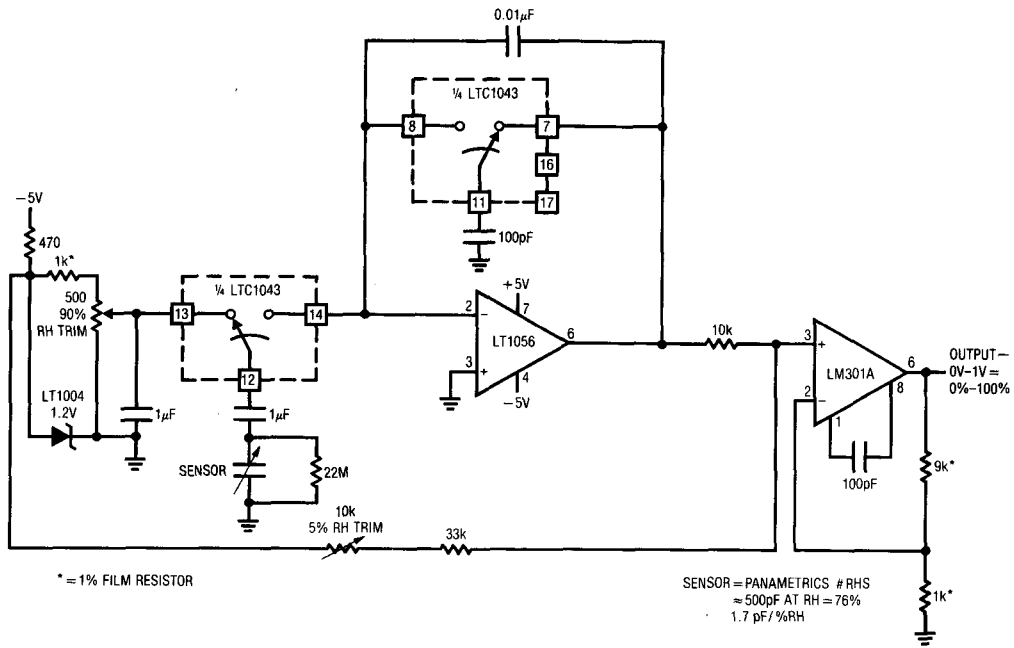


Figure 9. Relative Humidity Signal Conditioner

LVDT Signal Conditioner

LVDTs (Linear Variable Differential Transformers) are another example of a transducer which the LTC1043 can signal condition. An LVDT is a transformer with a mechanically actuated core. The primary is driven by a sine wave, usually amplitude stabilized. Sine drive eliminates error inducing harmonics in the transformer. The two secondaries are connected in opposed phase. When the core is positioned in the magnetic center of the transformer, the secondary outputs cancel and there is no output. Moving the core away from the center position unbalances the flux ratio between the secondaries, developing an output. Figure 10 shows an LTC1043

based LVDT signal conditioner. A1 and its associated components furnish the amplitude stable sine wave source. A1's positive feedback path is a Wein bridge, tuned for 1.5kHz. Q1, the LT1004 reference, and additional components in A1's negative loop unity-gain stabilize the amplifier. A1's output (Trace A, Figure 11), an amplitude stable sine wave, drives the LVDT. C1 detects zero crossings and feeds the LTC1043 clock pin (Trace B). A speed-up network at C1's input compensates LVDT phase shift, synchronizing the LTC1043's clock to the transformer's output zero crossings. The LTC1043 alternately connects each end of the

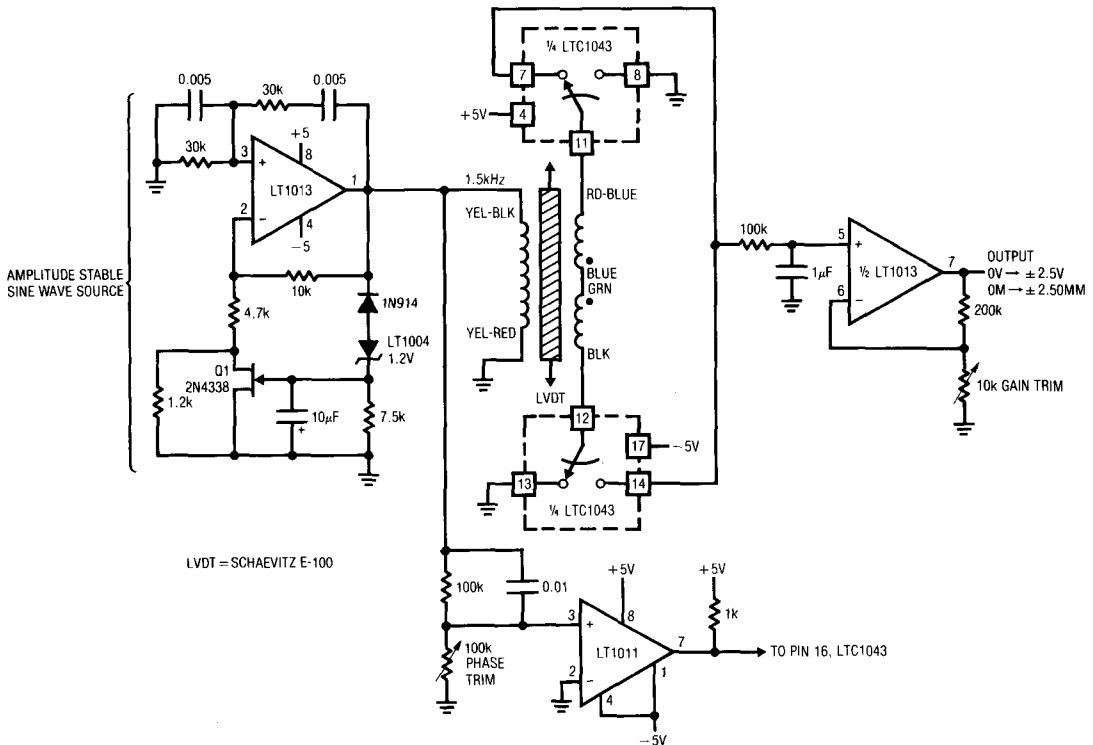


Figure 10. LVDT Signal Conditioner

Application Note 3

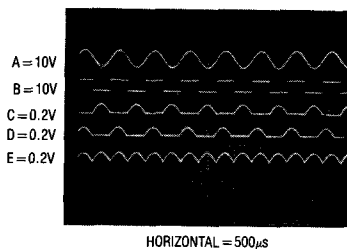


Figure 11

transformer to ground, resulting in positive half-wave rectification at pins 7 and 14 (Traces C and D, respectively). These points are summed (Trace E) at a low pass filter which feeds A2. A2 furnishes gain scaling and the circuit's output.

The LTC1043's synchronized clocking means the information presented to the low pass filter is amplitude and phase sensitive. The circuit output indicates how far the core is from center and on which side.

To calibrate this circuit, center the LVDT core in the transformer and adjust the phase trim for 0V output. Next, move the core to either extreme position and set the gain trim for 2.50V output.

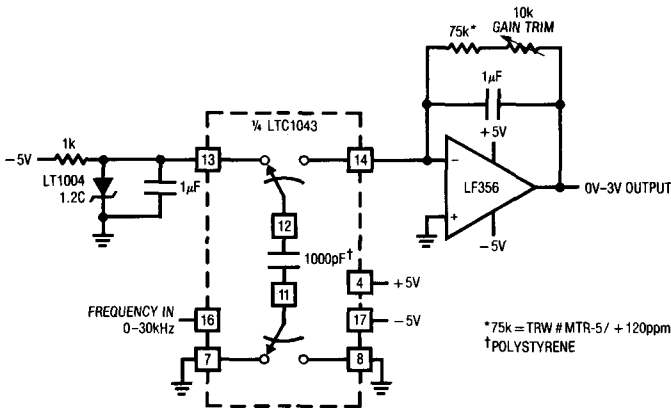
Charge Pump F → V and V → F Converters

Figure 12 shows two related circuits, both of which show how the LTC1043 can simplify a precision circuit function. Charge pump F → V and V → F converters usually require substantial compensation for non-ideal charge gating behavior. These examples equal the performance of such circuits, while requiring no compensations. These circuits are economical, component count is low, and the 0.005% transfer linearity equals that of more complex designs. Figure 12A is an F → V converter. The LTC1043's clock pin is driven from the input (Trace A, Figure 13). With the input high, pins 12 and 13 are shorted and 14 is open. The 1000pF capacitor receives charge from the 1µF unit, which is biased by the LT1004. At the input's negative-going edge, pins 12–13 open and 12–14 close. The 1000pF capacitor quickly removes current (Trace B) from A1's summing node. Initially, current

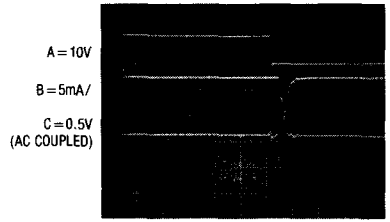
is transferred through A1's feedback capacitor and the amplifier output goes negative (Trace C). When A1 recovers, it slews positive to a level which resets the summing junction to zero. A1's 1µF feedback capacitor averages this action over many cycles and the circuit output is a DC level linearly related to frequency. A1's feedback resistors set the circuit's DC gain. To trim the circuit, apply 30kHz in and set the 10kΩ gain trim for exactly 3V output. The primary drift term in this circuit is the 120ppm/°C tempco of the 1000pF capacitor, which should be polystyrene. This can be reduced to within 20ppm/°C by using a feedback resistor with an opposing tempco (e.g., TRW # MTR-5/ + 120ppm). The input pulse width must be low for at least 100ns to allow complete discharge of the 1000pF capacitor.

In Figure 12B, the LTC1043 based charge pump is placed in A1's feedback loop, resulting in a V → F converter. The clock pin is driven from A1's output. Assume that A1's negative input is just below 0V. The amplifier output is positive. Under these conditions, LTC1043's pins 12 and 13 are shorted and 14 is open, allowing the 0.01µF capacitor to charge toward the negative 1.2V LT1004. When the input-voltage-derived current forces A1's summing point (Trace A, Figure 13) positive, its output (Trace B) goes negative. This reverses the LTC1043's switch states, connecting pins 12 and 14. Current flows from the summing point into the 0.01µF capacitor (Trace C). The 30pF-22k combination at A1's positive input (Trace D) ensures A1 will remain low long enough for the 0.01µF capacitor to completely reset to zero. When the 30pF-22k positive feedback path decays, A1's output returns positive and the entire cycle repeats. The oscillation frequency of this action is directly related to the input voltage with a transfer linearity of 0.005%.

Start-up or overdrive conditions could force A1 to go to the negative rail and stay there. Q1 prevents this by pulling the summing point negative if A1's output stays low long enough to charge the 1µF-330k RC. Two LTC1043 switch sections provide complementary sink-source outputs. Similar to the F → V circuit, the 0.01µF capacitor is the primary drift term, and the resistor type noted above will provide optimum tempco cancellation. To calibrate this circuit, apply 3V and adjust the gain trim for a 30kHz output.

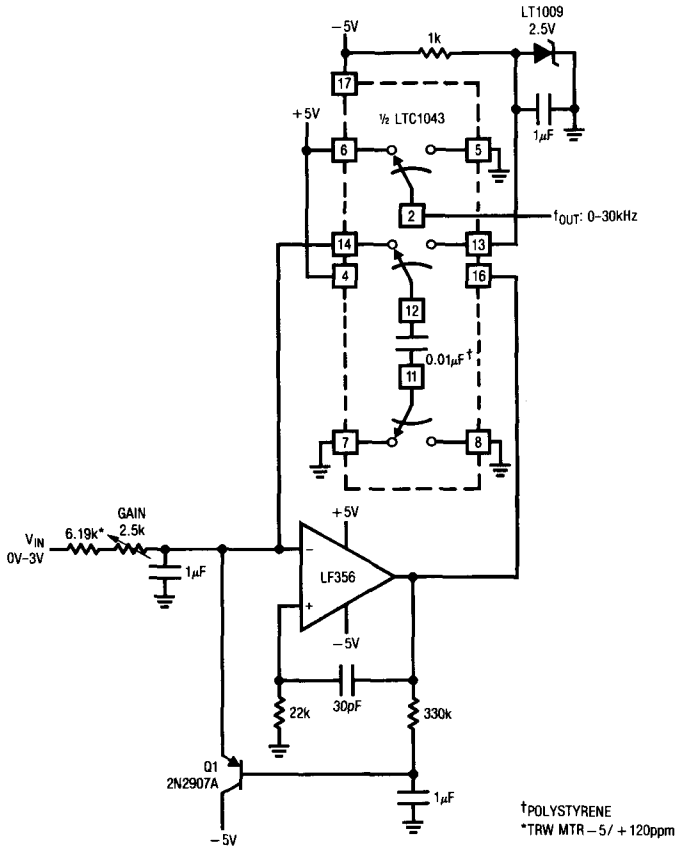


A. Frequency to Voltage Converter

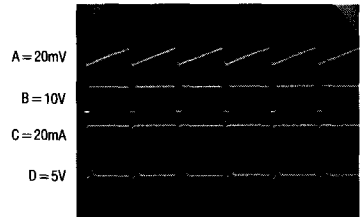


HORIZONTAL = 50ns / DIV

Figure 13



B. Voltage to Frequency Converter
Figure 12



HORIZONTAL = 20μs / DIV

Figure 14

Application Note 3

12-Bit A → D Converter

Figure 15 shows the LTC1043 used to implement an economical 12-bit A → D converter. The circuit is self-clocking, has a serial output, and completes a full-scale conversion in 25ms.

Two LTC1043s are used in this design. Unit A free-runs, alternately charging the 100pF capacitor from the LT1004

reference source and then dumping it into A1's summing point. A1, connected as an integrator, responds with a linear ramp output (Trace B, Figure 16). This ramp is compared to the input voltage by C1B. When the crossing occurs, C1B's output goes low (Trace C, just faintly visible in the photograph), setting the flip-flop high (Trace D). This pulls LTC1043's pin 16 high, resetting A1's integrator

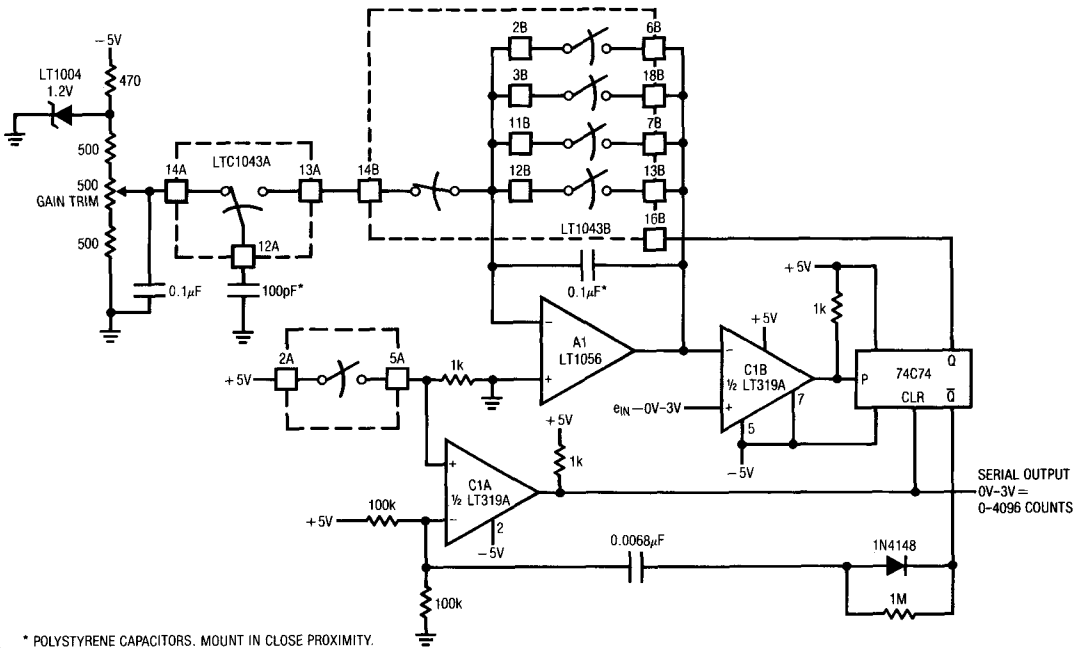
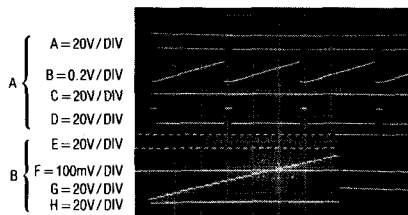


Figure 15. 12-Bit A → D Converter



A HORIZONTAL = 500μs / DIV
 B HORIZONTAL = 20μs / DIV

Figure 16

capacitor via the paralleled switches. Simultaneously, pin 14B opens, preventing charge from being delivered to A1's summing point during the reset. The flip-flop's Q output, low during this interval, causes an AC negative-going spike at C1A. This forces C1A's output high, inserting a gap in the output clock pulse stream (Trace A). The width of this gap, set by the components at C1A's negative input, is sufficient to allow a complete reset of A1's integrating capacitor. The number of pulses between gaps is directly related to the input voltage. The actual conversion begins at the gap's negative edge and ends at its positive edge. The flip-flop output may be used for resetting. Alternately, a processor driven "time-out" routine can determine the end of conversion. Traces E through H offer expanded scale versions of Traces A through D, respectively. The staircase detail of A1's ramp output reflects the charge pumping action at its summing point. Note that drift in the 100pF and 0.1μF capacitors, which should be polystyrene, ratiometrically cancels. Full-scale drift for this circuit is typically 20ppm/°C, allowing it to hold 12-bit accuracy over 25°C + 10°C. To calibrate the circuit, apply 3V in and trim the gain potentiometer for 4096 pulses out between data stream gaps.

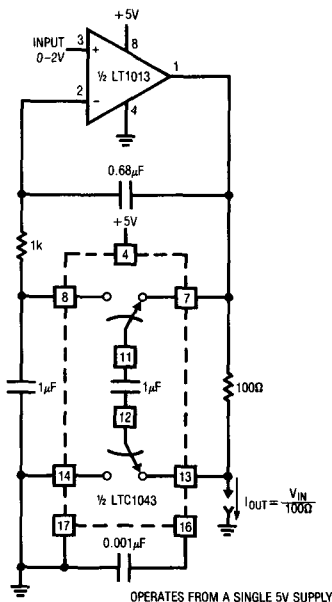


Figure 17. Voltage Controlled Current Source with Ground Referred Input and Output

Miscellaneous Circuits

Figures 17–22 show a group of miscellaneous circuits, most of which are derivations of applications covered in the text. As such, only brief comments are provided.

Voltage-Controlled Current Source—Grounded Source and Load

This is a simple, precise voltage-controlled current source. Bipolar supplies will permit bipolar output. Configurations featuring a grounded voltage control source and a grounded load are usually more complex and depend upon several components for stability. In this circuit, accuracy and stability are almost entirely dependent on the 100Ω shunt.

Current Sensing in Supply Rails

The LTC1043 can sense current through a shunt in either of its supply rails (Figure 18). This capability has wide application in battery and solar-powered systems. If the ground-referred voltage output is unloaded by an amplifier, the shunt can operate with very little voltage drop across it, minimizing losses.

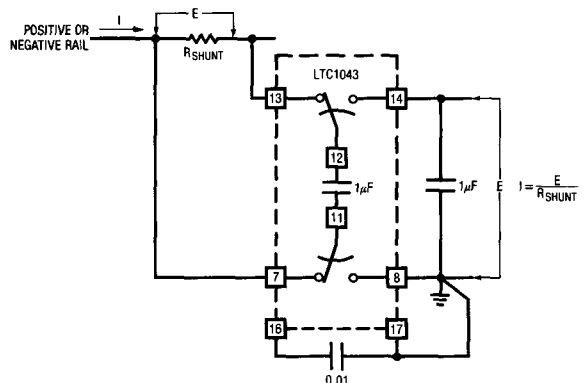


Figure 18. Precision Current Sensing in Supply Rails

Application Note 3

0.01% Analog Multiplier

Figure 19, using the $V \rightarrow F$ and $F \rightarrow V$ circuits previously described, forms a high precision analog multiplier. The $F \rightarrow V$ input frequency is locked to the $V \rightarrow F$ output because the LTC1043's clock is common to both sections. The $F \rightarrow V$'s reference is used as one input of the multiplier, while the $V \rightarrow F$ furnishes the other. To calibrate, short the X and Y inputs to 1.7320V and trim for a 3V output.

Inverting a Reference

Figure 20 allows a reference to be inverted with 1ppm accuracy. This circuit features high input impedance and requires no trimming.

Low Power, 5V Driven, Temperature Compensated Crystal Oscillator

Figure 21 uses the LTC1043 to differentiate between a temperature sensing network and a DC reference. The single-ended output biases a varactor tuned crystal oscillator to compensate drift. The varactor-crystal network has high DC impedance, eliminating the need for an LTC1043 output amplifier.

Simple Thermometer

Figure 22's circuit is conceptually similar to the platinum RTD example of Figure 7. The thermistor network specified eliminates the requirement for a linearity trim, at the expense of accuracy and range of operation.

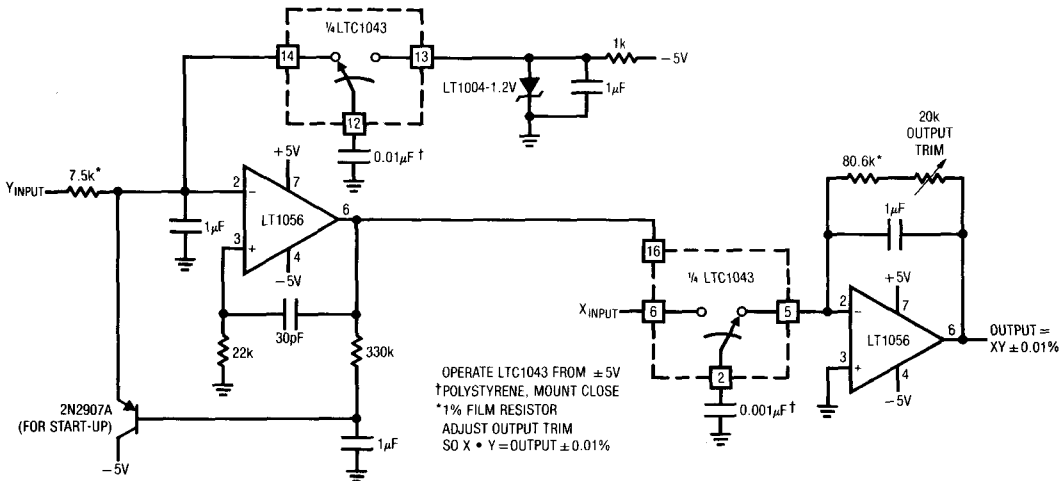


Figure 19. Analog Multiplier with 0.01% Accuracy

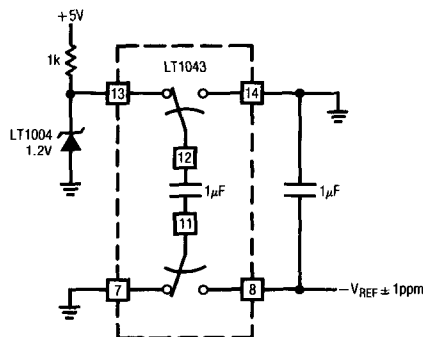


Figure 20. Precision Voltage Inverter

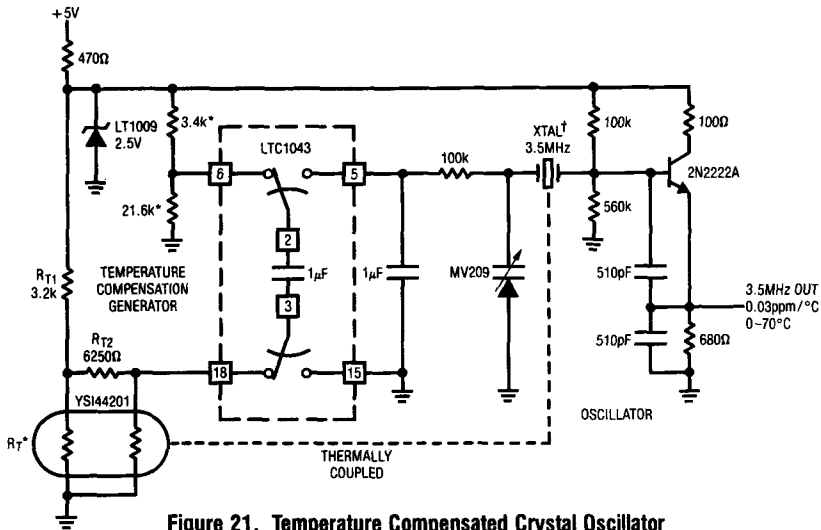


Figure 21. Temperature Compensated Crystal Oscillator

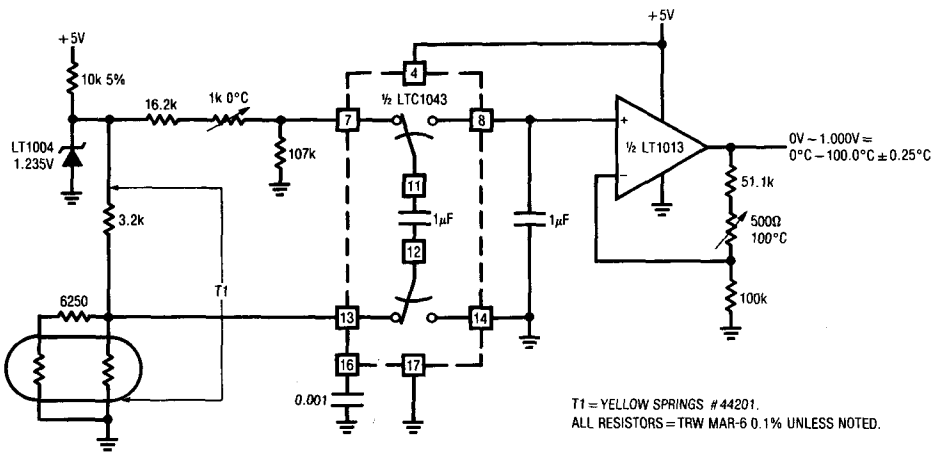


Figure 22. Linear Thermometer

High Current, "Inductorless," Switching Regulator

Figure 23 shows a high efficiency battery driven regulator with a 1A output capacity. Additionally, it does not require an inductor, an unusual feature for a switching regulator operating at this current level.

The LTC1043 switched-capacitor building block provides non-overlapping complementary drive to the Q1-Q4 power MOSFETs. The MOSFETs are arranged so that C1 and C2 are alternately placed in series and then in parallel. During the series phase, the +12V battery's current flows

through both capacitors, charging them and furnishing load current. During the parallel phase, both capacitors deliver current to the load. Traces A and B, Figure 24, are the LTC1043-supplied drives to Q3 and Q4, respectively. Q1 and Q2 receive similar drive from pins 3 and 11. The diode-resistor networks provide additional non-overlapping drive characteristics, preventing simultaneous drive to the series-parallel phase switches. Normally, the output would be one-half of the supply voltage, but C1 and its associated components close a feedback loop, forcing the

Application Note 3

output to 5V. With the circuit in the series phase, the output (Trace C) heads rapidly positive. When the output exceeds 5V, C1 trips, forcing the LTC1043 oscillator pin (Trace D) high. This truncates the LTC1043's triangle wave oscillator cycle. The circuit is forced into the parallel phase and the output coasts down slowly until the next LTC1043 clock cycle begins. C1's output diode prevents the triangle down-slope from being affected and the 100pF

capacitor provides sharp transitions. The loop regulates the output to 5V by feedback controlling the turn-off point of the series phase. The circuit constitutes a large scale switched-capacitor voltage divider which is never allowed to complete a full cycle. The high transient currents are easily handled by the power MOSFETs and overall efficiency is 83%.

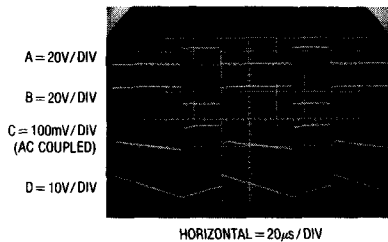
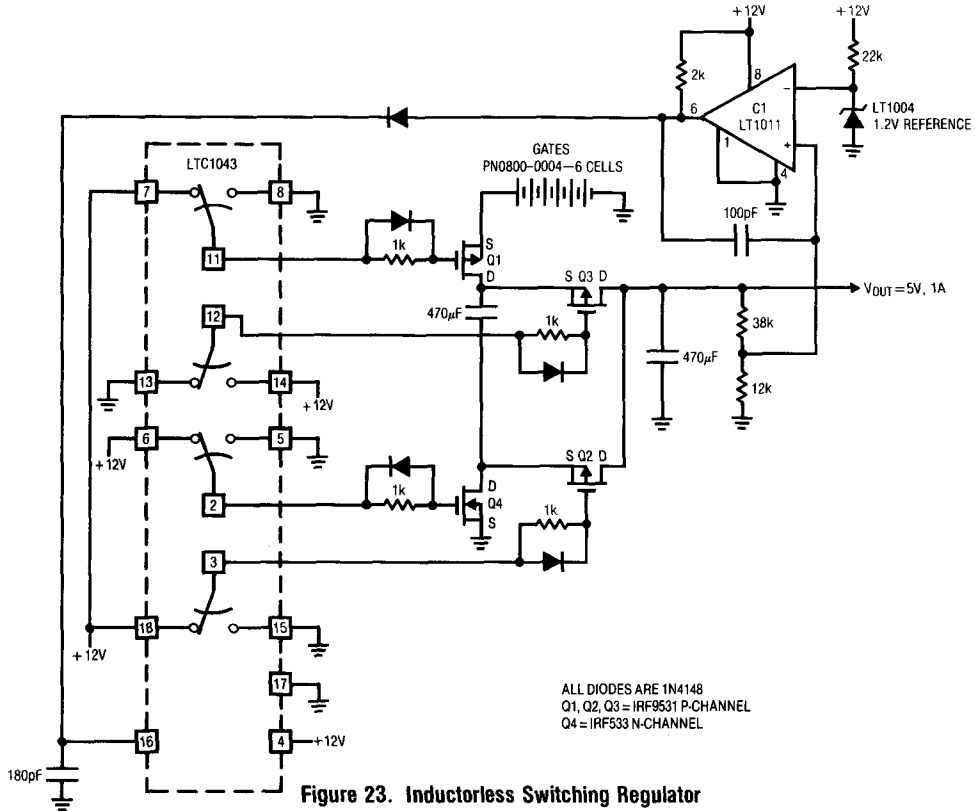


Figure 24

Applications for a New Power Buffer

Jim Williams

A frequent requirement in systems involves driving analog signals into non-linear or reactive loads. Cables, transformers, actuators, motors, and sample-and-hold circuits are examples where the ability to drive difficult loads is required. Although several power buffer amplifiers are available, none have been optimized for driving difficult loads. The LT1010 can isolate and drive almost any reactive load. It also offers current limiting and thermal overload protection which protect the device against output fault conditions. The combination of good speed, output protection, and reactive load driving capability (see

Box Section, "The LT1010 at a Glance") make the device useful in a variety of practical situations.

Buffered Output Line Driver

Figure 1 shows the LT1010 placed within the feedback loop of an operational amplifier. At lower frequencies, the buffer is within the feedback loop and its offset voltage and gain error are negligible. At higher frequencies, feedback is through C_F so that phase shift from load capacitance acting against the buffer's output resistance does not cause loop instability.

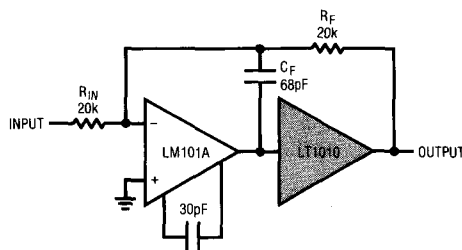


Figure 1. Practical LT1010 Based Boosted Op Amp

Application Note 4

Figure 2 shows this configuration driving a 50Ω - $0.33\mu\text{F}$ load. The waveform is clean, with controlled damping. With C load increased to a brutal $2\mu\text{F}$, the circuit is still stable (Trace A, Figure 3), even though the large capacitance requires substantial current (Trace B) from the LT1010. Adjustment of the R_F - C_F time constant would allow improved damping.

Although this circuit is useful, its speed is limited by the op amp.

Fast, Stabilized Buffer Amplifier

Figure 4 shows a way to eliminate this restriction, while maintaining good DC characteristics. Here, the LT1010 is combined with a wideband gain stage, Q1-Q3, to form a fast inverting configuration. The LT1008 op amp DC stabilizes this stage by biasing the Q2-Q3 emitters to force a zero DC potential at the circuit's summing junction. The roll-offs of the fast stage and the op amp are arranged to provide smooth overall circuit response.

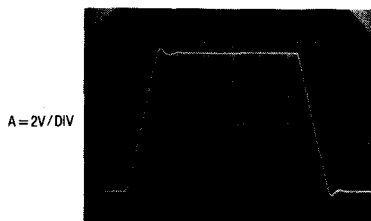


Figure 2

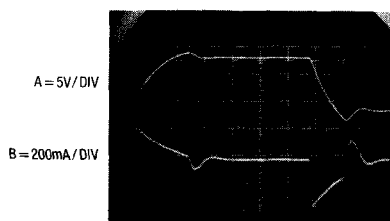


Figure 3

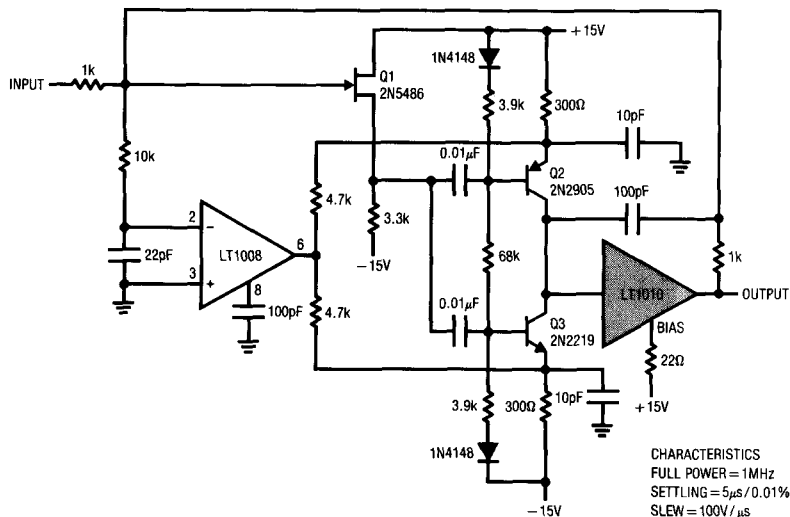


Figure 4. Fed Forward, Wideband DC Stabilized Buffer

Because the circuit's DC stabilization path occurs in parallel with the buffer, higher speed is obtainable. Figure 5 shows the circuit driving a 600Ω-2500pF load. Despite the heavy load, the output (Trace B) does a good job of following the input (Trace A) at a gain of -1.

single-ends into the LT1010. The capacitively terminated feedback divider gives the circuit a DC gain of 1, while allowing AC gains up to 10. Using a 20Ω bias resistor (see Box Section), the circuit delivers 1Vp-p into a typical 75Ω video load. For applications sensitive to NTSC requirements, dropping the bias resistor value will aid performance.

Video Line Driving Amplifier

In many applications, DC stability is unimportant and AC gain is required. Figure 6 shows how to combine the LT1010's load handling capability with a fast, discrete gain stage. Q1 and Q2 form a differential stage which

At A=2, the gain is within 0.5dB to 10MHz with the -3dB point occurring at 16MHz. At A=10, the gain is flat (± 0.5 dB to 4MHz) with a -3dB point at 8MHz. The peaking adjustment should be optimized under loaded output conditions.

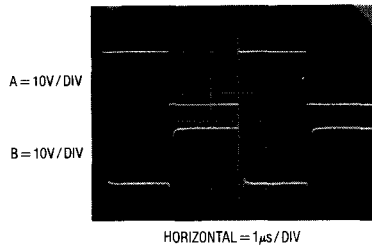


Figure 5

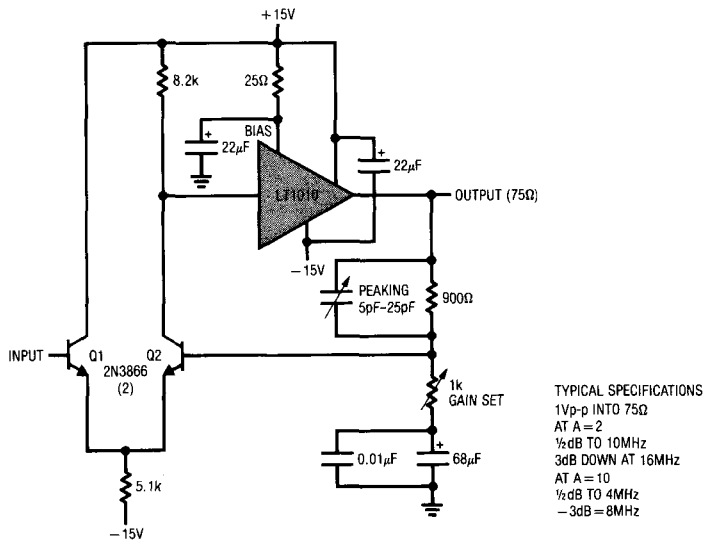


Figure 6. Video Line Driving Amplifier

Application Note 4

Figure 7 shows a video distribution amplifier. In this example, resistors are included in the output line to isolate reflections from unterminated lines. If the line characteristics are known, the resistors may be deleted. To meet NTSC gain-phase requirements, a small value boost resistor is used. Each 1Vp-p channel output is essentially flat through 6MHz into a 75Ω load.

Fast, Precision Sample-Hold Circuit

Sample-hold circuits require high capacitive load driving capability to achieve fast acquisition times. Additionally, other tradeoffs must be considered to achieve a good design. The conceptual circuit of Figure 8 illustrates some of the issues encountered. Fast acquisition requires high charge currents and dynamic stability, which

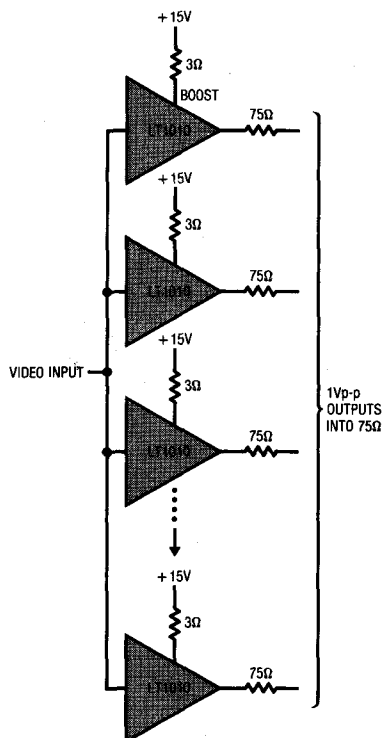


Figure 7. Video Distribution Amplifier

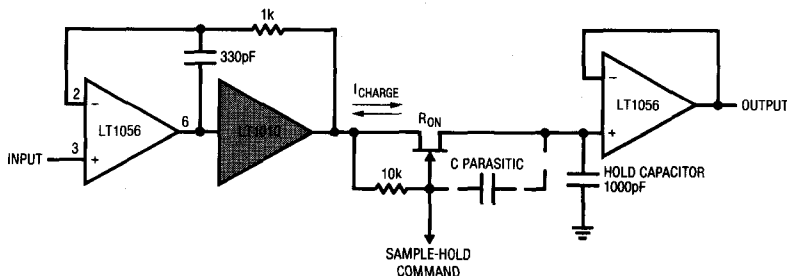


Figure 8. Conceptual Sample-Hold

the LT1010 can provide. To get reasonable droop rate, the hold capacitor must be appropriately sized, but too large a value means FET switch on-resistance will effect acquisition time. If very low on-resistance FETs are used, the parasitic gate-source capacitance becomes significant and a substantial amount of charge is removed from the hold capacitor when the gate is switched off. This charge removal causes the stored voltage to abruptly change when the circuit is switched into the hold mode. This phenomenon, called "hold step", limits accuracy. It can be combated by increasing the hold capacitor's value, but then acquisition time suffers. Finally, since a TTL compatible input is desirable, the FET requires a level shift. This level shift must provide adequate pinch-off voltage over the entire range of circuit inputs and must also be fast. Delays will result in aperture errors, introducing dynamic sampling inaccuracies.

Figure 9 shows a circuit which combines the LT1010 with some techniques to produce a fast, precise sample-and-hold circuit. Q1 through Q4 constitute a very fast TTL compatible level shift. Total delay from the TTL input switching into hold to Q6 turning off is 16ns. Baker clamped Q1 biases Q3's emitter to switch level shifter Q4. Q2 drives a heavy feedforward network, speeding Q4's switching. This stage affords low aperture errors, while providing the necessary level shift for Q6's gate. The hold step error due to Q6's parasitic gate-source capacitance is compensated for by Q5 and the LT318A amplifier (A3).

The amount of charge removed by Q6's parasitic capacitance is signal dependent ($Q = CV$). To compensate this error, A3 measures the circuit output and biases the Q5 switch. Each time the circuit switches into hold mode, an appropriate amount of charge is delivered through the

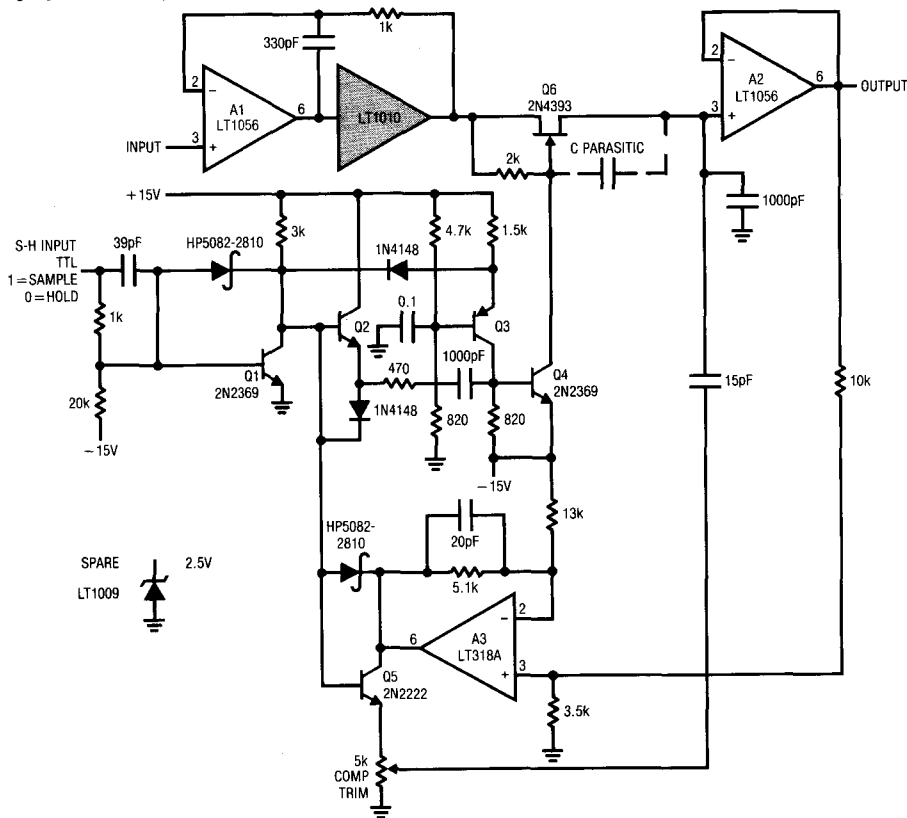


Figure 9. Fast Sample-Hold with Hold Step Compensation

Application Note 4

potentiometer—15pF network in Q5's emitter. The amount of charge is scaled to compensate for charge removal due to Q6's parasitic term. A3's inverting input is biased so that negative supply shifts, which alter the charge removed through C parasitic, are accounted for in the compensating charge. Compensation is set by grounding the signal input, clocking the S-H line and adjusting the potentiometer for minimum disturbance at the circuit's output.

Figure 10 shows the circuit at work. When the sample-hold input (Trace A, Figure 10) goes into hold, charge cancellation occurs and the output (Trace B) sees less than 250μV of hold step error within 100ns. Without compensation, the error would be 50mV (Trace B, Figure 11—Trace A is the sample-hold input).

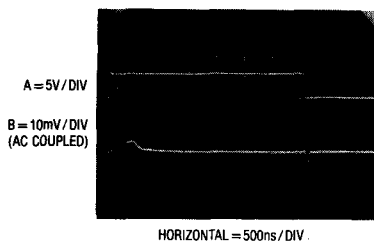
Figure 12 shows the LT1010's contribution to fast acquisition. The circuit acquires a 10V signal in this photograph. Trace A is the sample-hold input. Trace B shows the LT1010 delivering over 100mA to the hold capacitor and Trace C depicts the output value slewing

and settling to final value. Note that the acquisition time is limited by amplifier settling time and not capacitor charge time. Pertinent specifications include:

Acquisition time:	2μs to 0.01%
Hold settling time:	< 100ns to 1mV
Aperture time:	16ns

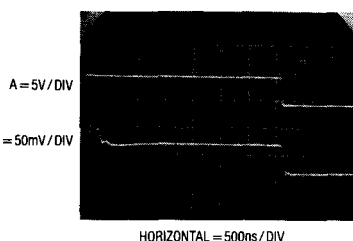
Motor Speed Control

The LT1010's ability to drive difficult loads is exploited in Figure 13's circuit. Here, the buffer drives a motor-tachometer combination. The tachometer signal is fed back and compared to a reference current and the 301A amplifier closes a control loop. The 0.47μF capacitor provides stable compensation. Because the tachometer output is bipolar, the speed is controllable in both directions, with clean transitions through zero. The LT1010's thermal protection is particularly useful in this application, preventing device destruction in the event of mechanical overload or malfunction.



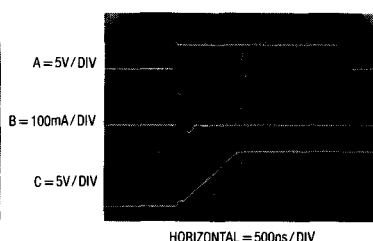
HORIZONTAL = 500ns / DIV

Figure 10



HORIZONTAL = 500ns / DIV

Figure 11



HORIZONTAL = 500ns / DIV

Figure 12

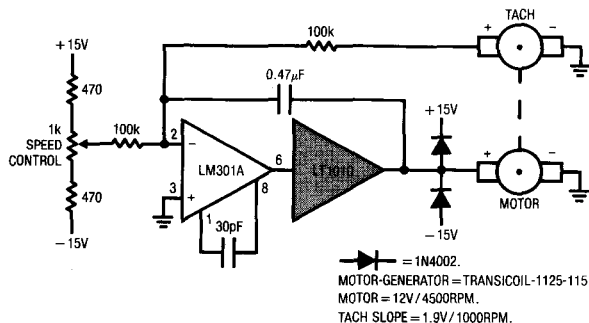


Figure 13. Overload Protected Motor Speed Controller

Fan-Based Temperature Controller

Figure 14 shows a way to use the LT1010 to control a fan motor's speed to regulate instrument temperature. The fan employed is one of the new electrostatic types which has very high reliability because it contains no wearing parts. These devices require high voltage drive. When power is applied, the thermistor (located in the fan's exhaust stream) is at a high value. This unbalances the A3 amplifier driven bridge, A1 receives no power, and the fan does not run. As the instrument enclosure warms, the thermistor value decreases until A3 begins to oscillate.

A2 provides isolation and gain and A4 drives the transformer to generate high voltage for the fan. In this fashion, the loop acts to maintain a stable instrument temperature by controlling the fan's exhaust rate. The 100 μ F time constant across the error amplifier pins will produce audibly annoying "hunting" in the servo. Optimal values for this time constant and gain depend upon the thermal and airflow characteristics of the enclosure being controlled.

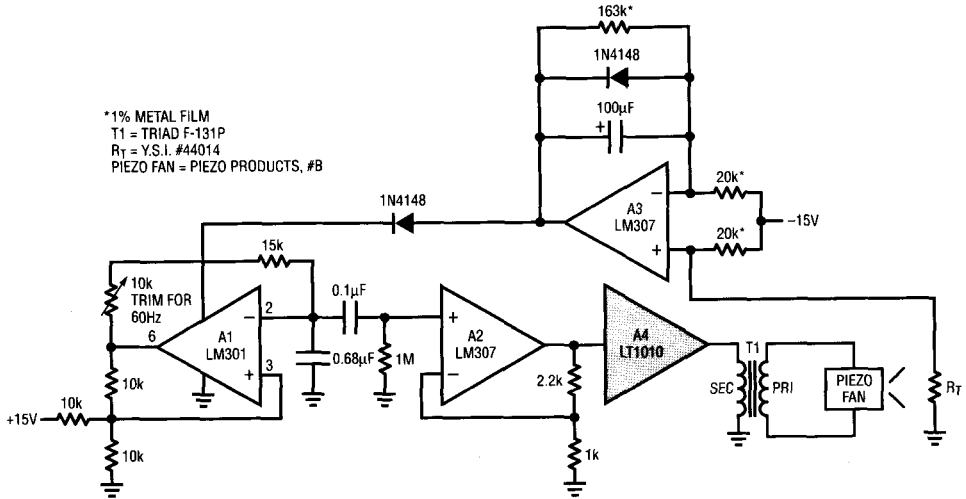


Figure 14. Piezo-Electric Fan Servo

The LT1010 at a Glance

By R. J. Widar

The schematic describes the basic elements of the buffer design. The op amp drives the output sink transistor, Q3, such that the collector current of the output follower never drops below the quiescent value (determined by I and the area ratio of D1 and D2). As a result, the high frequency response is essentially that of a simple follower, even when Q3 is supplying the load current. The internal feedback loop is isolated from the effects of capacitive loading in the output lead.

The scheme is not perfect in that the rate of rise of sink current is not nearly as fast as source current. This can be mitigated by connecting a resistor between the bias terminal and V+, raising quiescent current. A feature of the final design is that the output resistance is largely independent of the follower quiescent current or the output load current. The output will also swing to the negative rail, which is particularly useful with single supply operation.

Application Note 4

The buffer is no more sensitive to supply bypassing than slower op amps as far as stability is concerned. The $0.1\mu\text{F}$ disc ceramic capacitors usually recommended for op amps are certainly adequate for low frequency work. As always, keeping the capacitor leads short and using a ground plane are prudent, especially when operating at high frequencies.

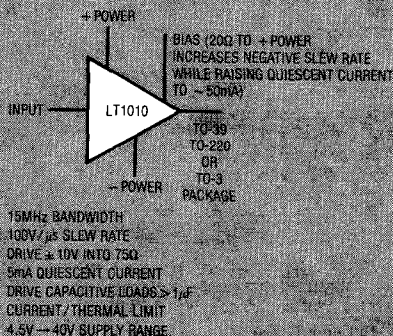
The buffer slew rate can be reduced by inadequate supply bypass. With output current changes much above $100\text{mA}/\mu\text{s}$, using $10\mu\text{F}$ solid tantalum capacitors on both supplies is good practice, although bypassing from the positive to the negative supply may suffice.

When used in conjunction with an op amp and heavily loaded (resistive or capacitive), the buffer can couple into supply leads common to the op amp, causing stability problems with the overall loop. Adequate bypassing can usually be provided by $10\mu\text{F}$ solid tantalum capacitors. Alternately, smaller capacitors could be used with decoupling resistors. Sometimes the op amp has much better high frequency rejection on one supply, so bypass requirements are less on this supply.

Power Dissipation

In many applications, the LT1010 will require heat sinking. Thermal resistance, junction to still air, is $150^\circ\text{C}/\text{W}$ for the TO-39 package and $60^\circ\text{C}/\text{W}$ for the TO-3 package. Circulating air, a heat sink or mounting the TO-3 package to a printed circuit board will reduce thermal resistance.

The LT1010 at a Glance



In DC circuits, buffer dissipation is easily computed. In AC circuits, signal waveshape and the nature of the load determine dissipation. Peak dissipation can be several times average with reactive loads. It is particularly important to determine dissipation when driving large load capacitance.

Overload Protection

The LT1010 has both instantaneous current limit and thermal overload protection. Foldback current limiting has not been used, enabling the buffer to drive complex loads without limiting. Because of this, it is capable of power dissipation in excess of its continuous ratings.

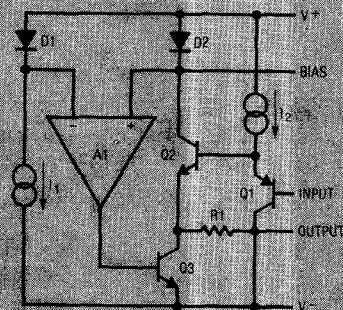
Normally, thermal overload protection will limit dissipation and prevent damage. However, with more than 30V across the conducting output transistor, thermal limiting is not quick enough to ensure protection in current limit. The thermal protection is effective with 40V across the conducting output transistor as long as the load current is otherwise limited to 150mA.

Drive Impedance

When driving capacitive loads, the LT1010 likes to be driven from a low source impedance at high frequencies. Some low power op amps are marginal in this respect. Some care may be required to avoid oscillations, especially at low temperatures.

Bypassing the buffer input with more than 200pF will solve the problem. Raising the operating current also works, but this can be done only on the TO-3 package.

LT1010 Conceptual Schematic



Thermal Techniques in Measurement and Control Circuitry

Jim Williams

Designers spend much time combating thermal effects in circuitry. The close relationship between temperature and electronic devices is the source of more design headaches than any other consideration.

In fact, instead of eliminating or compensating for thermal parasitics in circuits, it is possible to utilize them. In particular, applying thermal techniques to measurement and control circuits allows novel solutions to difficult problems. The most obvious example is temperature control. Familiarity with thermal considerations in temperature control loops permits less obvious, but very useful, thermally based circuits to be built.

Temperature Controller

Figure 1 shows a precision temperature controller for a small components oven. When power is applied, the thermistor, a negative TC device, is at a high value. A1

saturates positive. This forces the LT3525A switching regulator's output low, biasing Q1. As the heater warms, the thermistor's value decreases. When its inputs finally balance, A1 comes out of saturation and the LT3525A pulse-width modulates the heater via Q1, completing a feedback path. A1 provides gain and the LT3525A furnishes high efficiency. The 2kHz pulse-width modulated heater power is much faster than the thermal loop's response and the oven sees an even, continuous heat flow.

The key to high performance control is matching the gain-bandwidth of A1 to the thermal feedback path. Theoretically, it is a simple matter to do this using conventional servo-feedback techniques. Practically, the long time constants and uncertain delays inherent in thermal systems present a challenge. The unfortunate relationship between servo systems and oscillators is very apparent in thermal control systems.

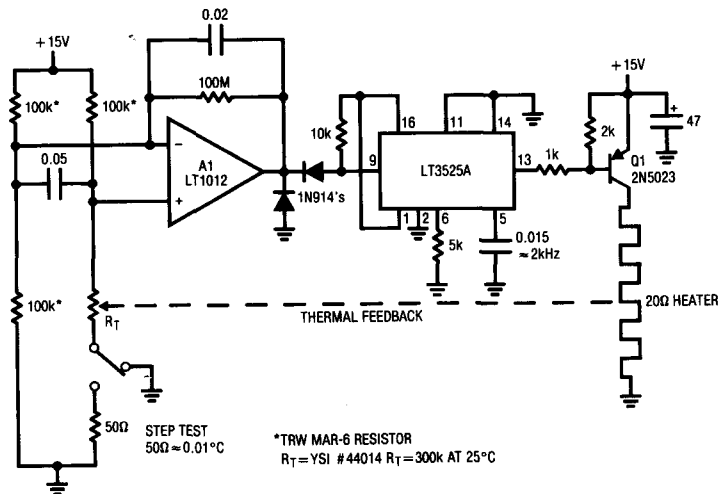


Figure 1. Precision Temperature Controller

Application Note 5

The thermal control loop can be very simply modeled as a network of resistors and capacitors. The resistors are equivalent to the thermal resistance and the capacitors equivalent to thermal capacity. In Figure 2 the heater, heater-sensor interface, and sensor all have RC factors that contribute to a lumped delay in the ability of a thermal system to respond. To prevent oscillation, A1's gain-bandwidth must be limited to account for this delay. Since high gain-bandwidth is desirable for good control, the delays must be minimized. The physical size and electrical resistivity of the heater selected give some element of control over the heater's time constant. The heater-sensor interface time constant can be minimized by placing the sensor in intimate contact with the heater.

The sensor's RC product can be minimized by selecting a sensor of small size relative to the capacity of its thermal environment. Clearly, if the wall of an oven is 6" thick aluminum, the tiniest sensor available is not an absolute

necessity. Conversely, if one is controlling the temperature of a 1/16" thick glass microscope slide, a very small sensor (i.e., fast) is in order.

After the thermal time constants relating to the heater and sensor have been minimized, some form of insulation for the system must be chosen. The function of insulation is to keep the loss rate down so the temperature control device can keep up with the losses. For any given system, the higher the ratio between the heater-sensor time constants and the insulation time constants, the better the performance of the control loop.

After these thermal considerations have been attended to, the control loop's gain-bandwidth can be optimized. Figures 3A, 3B, and 3C show the effects of different compensation values at A1. Compensation is trimmed by applying small steps in temperature setpoint and observing the loop response at A1's output. The 50Ω resistor and

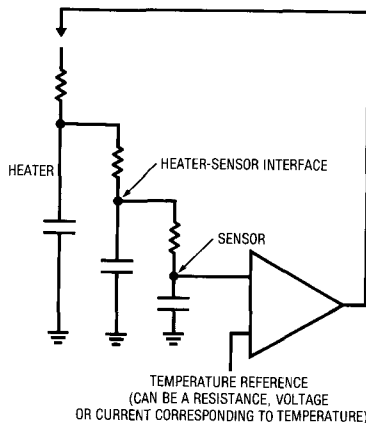
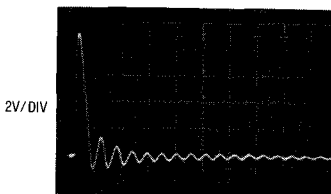
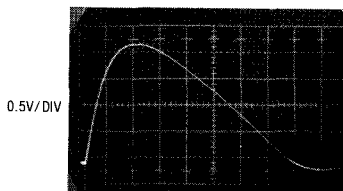


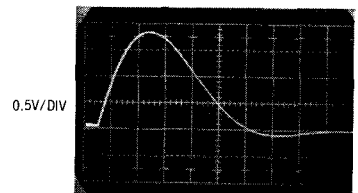
Figure 2. Thermal Control Loop Model



A



B



C

Figure 3. Loop Response for Various Gain Bandwidths

switch in the thermistor leg of the bridge furnish a 0.01°C step generator. Figure 3A shows the effects of too much gain-bandwidth. The step change forces a damped, ringing response over 50 seconds in duration! The loop is marginally stable. Increasing A1's gain-bandwidth (GBW) will force oscillation. Figure 3B shows what happens when GBW is reduced. Settling is much quicker and more controlled. The waveform is overdamped, indicating that higher GBW is achievable without stability compromises. Figure 3C shows the response for the compensation values given and is a nearly ideal critically damped recovery. Settling occurs within 4 seconds. An oven optimized in this fashion will easily attenuate external temperature shifts by a factor of thousands without overshoots or excessive lags.

Thermally Stabilized PIN Photodiode Signal Conditioner

PIN photodiodes are frequently employed in wide range photometric measurements. The photodiode specified in Figure 4 responds linearly to light intensity over a 100dB

range. Digitizing the diode's linearly amplified output would require an A-D converter with 17 bits of range. This requirement can be eliminated by logarithmically compressing the diode's output in the signal conditioning circuitry. Logarithmic amplifiers utilize the logarithmic relationship between V_{BE} and collector current in transistors. This characteristic is very temperature-sensitive and requires special components and layout considerations to achieve good results. Figure 4's circuit logarithmically signal conditions the photodiode's output with no special components or layout.

A1 and Q4 convert the diode's photocurrent to a voltage output with a logarithmic transfer function. A2 provides offsetting and additional gain. A3 and its associated components form a temperature control loop which maintains Q4 at constant temperature (all transistors in this circuit are part of a CA3096 monolithic array). The $0.033\mu\text{F}$ value at A3's compensation pins gives good loop damping if the circuit is built using the array's transistors in the locations shown. These locations have been selected for optimal control at Q4, the logging transistor. Because of the

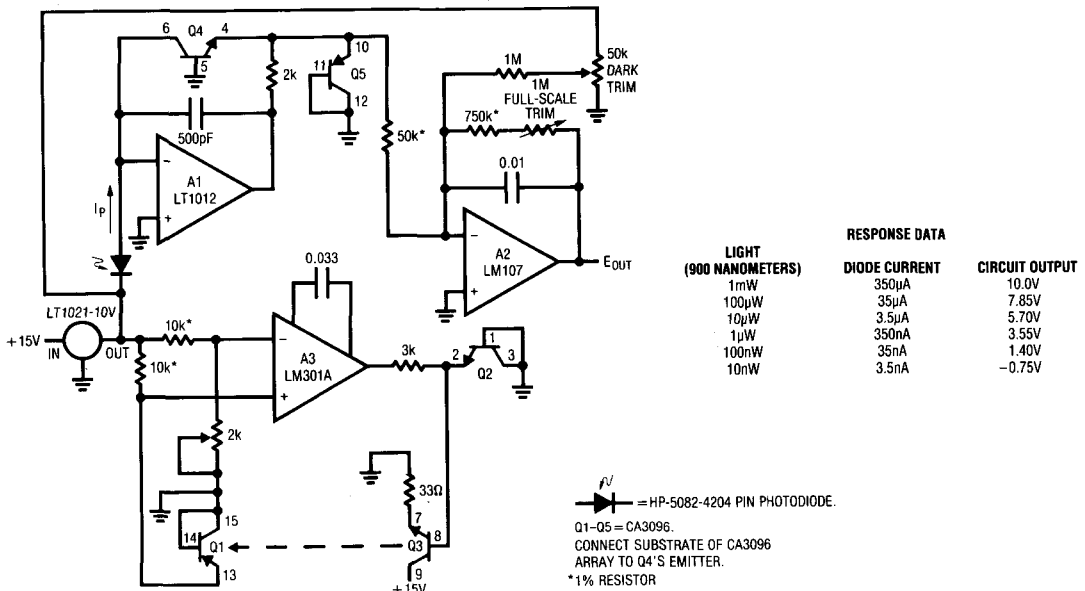


Figure 4. 100dB Range Logarithmic Photodiode Amplifier

Application Note 5

array die's small size, response is quick and clean. A full-scale step requires only 250ms to settle (photo, Figure 5) to final value. To use this circuit, first set the thermal control loop. To do this, ground Q3's base and set the 2k pot so A3's negative input voltage is 55mV below its positive input. This places the servo's setpoint at about 50°C (25°C ambient + 2.2mV/°C × 25°C rise = 55mV = 50°C). Unground Q3's base and the array will come to temperature. Next, place the photodiode in a completely dark environment and adjust the "dark trim" so A2's output is 0V. Finally, apply or electrically simulate (see chart, Figure 4) 1mW of light and set the "full-scale" trim for 10V out. Once adjusted, this circuit responds logarithmically to light inputs from 10nW to 1mW with an accuracy limited by the diode's 1% error.

50MHz Bandwidth Thermal RMS → DC Converter

Conversion of AC waveforms to their equivalent DC power value is usually accomplished by either rectifying and averaging or using analog computing methods. Rectification-averaging works only for sinusoidal inputs. Analog computing methods are limited to use below 500kHz. Above this frequency, accuracy degrades beyond the point of usefulness in instrumentation applications. Additionally, crest factors greater than 10 cause significant reading errors.

A way to achieve wide bandwidth and high crest factor performance is to measure the true power value of the waveform directly. The circuit of Figure 6 does this by measuring the DC heating power of the input waveform.

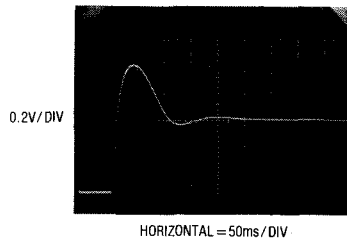


Figure 5. Figure 4's Thermal Loop Response

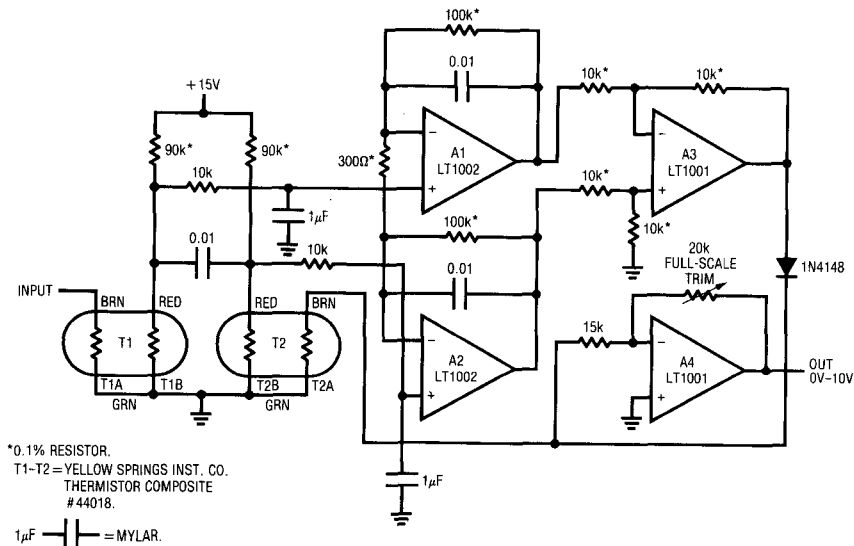


Figure 6. 50MHz Thermal RMS → DC Converter

By using thermal techniques to integrate the input waveform, 50MHz bandwidth is easily achieved with 2% accuracy. Additionally, because the thermal integrator's output is at low frequency, no wideband circuitry is required. The circuit uses standard components and requires no special trimming techniques. It is based on measuring the amount of power required to maintain two similar but thermally decoupled masses at the same temperature. The input is applied to T1, a dual thermistor bead. The power dissipated in one leg (T1A) of this bead forces the other section (T1B) to shift down in value, unbalancing the bridge formed by the other bead and the 90kΩ resistors. This imbalance is amplified by the A1-A2-A3 combination. A3's output is applied to a second thermistor bead, T2. T2A heats, causing T2B to decay in value. As T2B's resistance drops, the bridge balances. A3's output adjusts drive to T2A until T1B and T2B have equal values. Under these conditions, the voltage at T2A is equal to the RMS value of the circuit's input. In fact, slight mass imbalances between T1 and T2 contribute a gain error, which is corrected at A4. RC filters at A1 and A2 and the 0.01μF capacitor eliminate possible high frequency error due to capacitive coupling between T1A and T1B. The diode in A3's output line prevents circuit latch-up.

Figure 7 details the recommended thermal arrangement for the thermistors. The styrofoam block provides an isothermal environment and coiling the thermistor leads attenuates heat pipe effects to the outside ambient. The two inch distance between the devices allows them to see identical thermal conditions without interaction. To calibrate this circuit, apply 10V_{DC} to the input and adjust the full-scale trim for 10 volts out at A4. Accuracy remains within 2% from DC to 50MHz for inputs of 300mV to 10V.

Crest factors of 100:1 contribute less than 0.1% additional error and response time to rated accuracy is five seconds.

Low Flow Rate Thermal Flowmeter

Measuring low flow rates in fluids presents difficulties. "Paddle wheel" and hinged vane type transducers have low and inaccurate outputs at low flow rates. If small diameter tubing is required, as in medical or biochemical work, such transduction techniques also become mechanically impractical. Figure 8 shows a thermally based flowmeter which features high accuracy at rates as low as 1mL/minute and has a frequency output which is a linear function of flow rate. This design measures the differential temperature between two sensors (Figure 9). One sensor, T1, located before the heater resistor, assumes the fluid's temperature before it is heated by the resistor. The second sensor, T2, picks up the temperature rise induced into the fluid by the resistor's heating. The sensor's difference signal appears at A1's output. A2 amplifies this difference with a time constant set by the 10MΩ adjustment. Figure 10 shows A2's output versus flow rate. The function has an inverse relationship. A3 and A4 linearize this relationship, while simultaneously providing a frequency output (Figure 10). A3 functions as an integrator which is biased from the LT1004 and the 383k input resistor. Its output is compared to A2's output at A4. Large inputs from A2 force the integrator to run for a long time before A4 can go high, turning on Q1 and resetting A3. For small inputs from A2, A3 does not have to integrate very long before resetting action occurs. Thus, the configuration oscillates at a frequency which is inversely proportional to A2's output voltage. Since this voltage is inversely related to flow rate, the oscillation frequency linearly corresponds to flow rate.

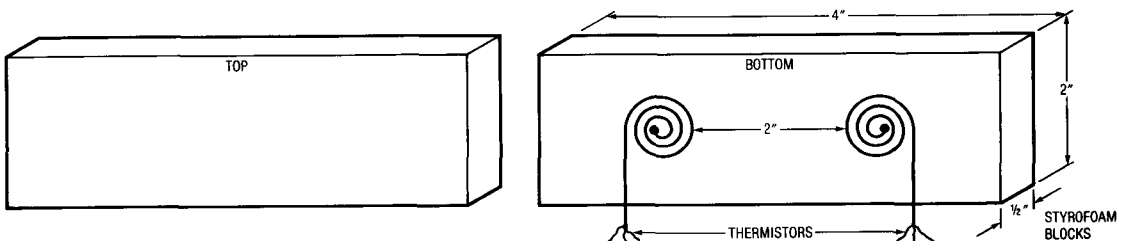


Figure 7. Thermal Arrangement for RMS → DC Converter

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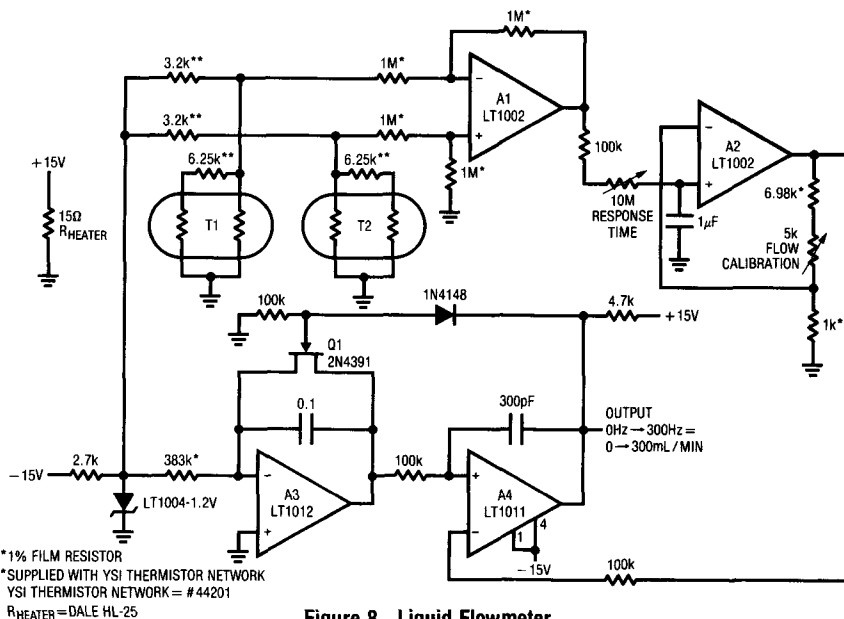


Figure 8. Liquid Flowmeter

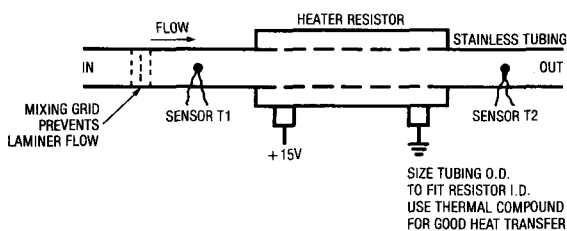


Figure 9. Flowmeter Transducer Details

Several thermal considerations are important in this circuit. The amount of power dissipated into the stream should be constant to maintain calibration. Ideally, the best way to do this is to measure the VI product at the heater resistor and construct a control loop to maintain constant wattage dissipation. However, if the resistor specified is used, its drift with temperature is small enough to assume constant dissipation with a fixed voltage drive. Additionally, the fluid's specific heat will affect calibration. The curves shown are for distilled water. To calibrate this circuit, set a flow rate of 10mL/minute and

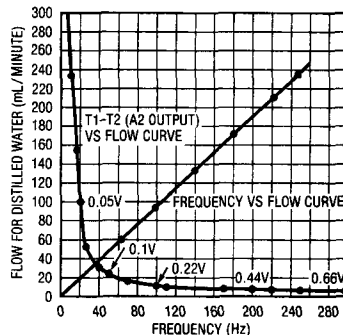


Figure 10. Flowmeter Response Data

adjust the flow calibration trim for 10Hz output. The response time adjustment is convenient for filtering flow aberrations due to mechanical limitations in the pump driving the system.

Thermally Based Anemometer (Air Flowmeter)

Figure 11 shows another thermally based flowmeter, but this design is used to measure air or gas flow. It works by measuring the energy required to maintain a heated resistance wire at constant temperature. The positive temperature coefficient of a small lamp, in combination with

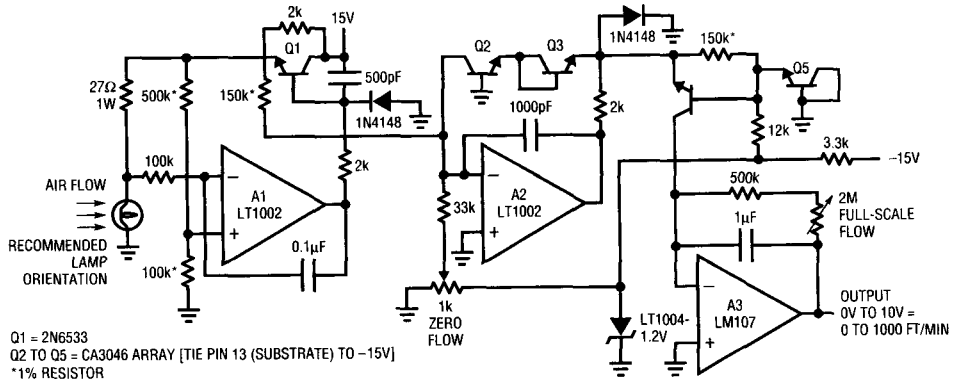


Figure 11. Thermal Anemometer

its ready availability, makes it a good sensor. A type 328 lamp is modified for this circuit by removing its glass envelope. The lamp is placed in a bridge which is monitored by A1. A1's output is current amplified by Q1 and fed back to drive the bridge. The capacitors and 220Ω resistor ensure stability. The 2k resistor furnishes start-up. When power is applied, the lamp is at a low resistance and Q1's emitter tries to come full on. As current flows through the lamp, its temperature quickly rises, forcing its resistance to increase. This action increases A1's negative input potential. Q1's emitter voltage decreases and the circuit finds a stable operating point. To keep the bridge balanced, A1 acts to force the lamp's resistance, hence its temperature, constant. The 10k-2k bridge values have been chosen so that the lamp operates just below the incandescence point. This high temperature minimizes the effects of ambient temperature shifts on circuit operation. Under these conditions, the only physical parameter which can significantly influence the lamp's temperature is a change in dissipation characteristic. Air flow moving by the lamp provides this change. Moving air by the lamp tends to cool it and A1 increases Q1's output to maintain the lamp's temperature. The voltage at Q1's emitter is non-linearly, but predictably, related to air flow by the lamp. A2, A3 and the array transistors form a circuit which squares and amplifies Q1's emitter voltage to give a linear, calibrated output versus air flow rate. To use this circuit, place the lamp in the air flow so that its filament is at a 90° angle to the flow. Next, either shut off the air flow or shield the lamp from it and adjust the zero flow potentiometer for a circuit output of 0V. Then, expose the lamp to air flow of 1000 feet/minute and trim the full flow potentiometer for 10V output.

Repeat these adjustments until both points are fixed. With this procedure completed, the air flowmeter is accurate within 3% over the entire 0-1000 foot/minute range.

Low Distortion, Thermally Stabilized Wien Bridge Oscillator

The positive temperature coefficient of lamp filaments is employed in a modern adaptation of a classic circuit in Figure 12. In any oscillator it is necessary to control the gain as well as the phase shift at the frequency of interest. If gain is too low, oscillation will not occur. Conversely, too much gain will cause saturation limiting. Figure 12 uses a variable Wien Bridge to provide frequency tuning from 20Hz to 20kHz. Gain control comes from the positive temperature coefficient of the lamp. When power is applied, the lamp is at a low resistance value, gain is high and oscillation amplitude builds. As amplitude builds, the lamp current increases, heating occurs and its resistance goes up. This causes a reduction in amplifier gain and the circuit finds a stable operating point. The lamp's gain-regulating behavior is flat within 0.25dB over the 20Hz-20kHz range of the circuit. The smooth, limiting nature of the lamp's operation, in combination with its simplicity, gives good results. Trace A, Figure 13 shows circuit output at 10kHz. Harmonic distortion is shown in Trace B and is below 0.003%. The trace shows that most of the distortion is due to second harmonic content and some crossover disturbance is noticeable. The low resistance values in the Wein network and the 3.8nV/√Hz noise specification of the LT1037 eliminate amplifier noise as an error term.

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At low frequencies, the thermal time constant of the small normal mode lamp begins to introduce distortion levels above 0.01%. This is due to "hunting" as the oscillator's frequency approaches the lamp thermal time constant. This effect can be eliminated, at the expense of reduced output amplitude and longer amplitude settling time, by switching to the low frequency, low distortion mode. The four large lamps give a longer thermal time constant and distortion is reduced. Figure 14 plots distortion versus frequency for the circuit.

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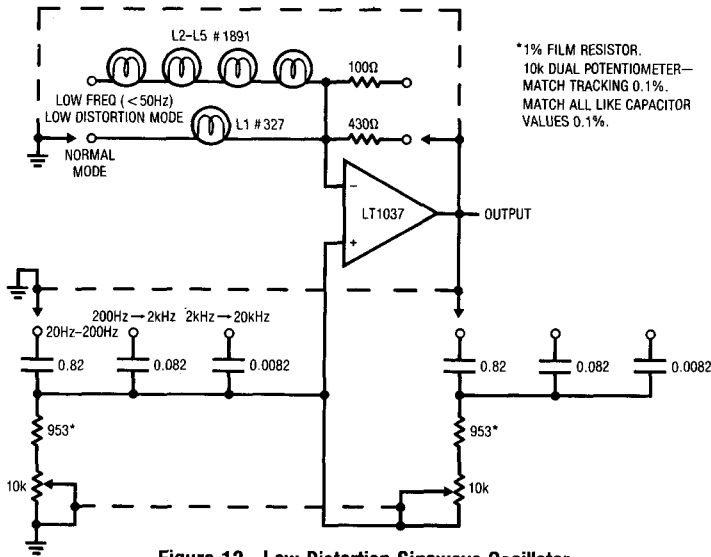


Figure 12. Low Distortion Sinewave Oscillator

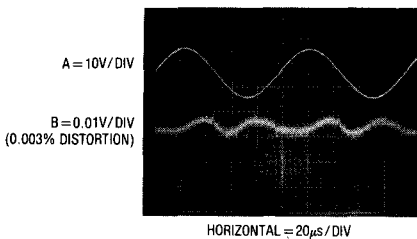


Figure 13. Oscillator Waveforms

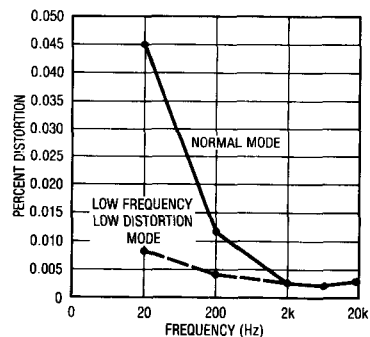


Figure 14. Oscillator Distortion vs Frequency

Applications of New Precision Op Amps

Jim Williams

Two new precision bipolar op amps, the LT1001 and a dual version, the LT1002, expand applications possibilities for designers of measurement and control circuits. These devices will find use where high accuracy and/or microvolt level capability are required. A summary of the new op-amp specifications appears in Table A. The high performance of these devices makes them useful as building blocks in precision circuitry. Figure 1 furnishes an excellent example.

Table A. LT1001A Specifications

OFFSET VOLTAGE	
Initial	25 μ V Max
vs Temperature	1 μ V/ $^{\circ}$ C Max
vs Time	1 μ V/Month Max
BIAS CURRENT	
Initial	2nA Max
Offset	2nA Max
OPEN LOOP GAIN	400,000 Min
COMMON-MODE REJECTION (+13V)	114dB Min
POWER SUPPLY REJECTION	110dB Min
SLEW RATE	0.15V/ μ s Min
GAIN-BANDWIDTH PRODUCT	0.5MHz Min
NOISE (Voltage)	
0.1Hz-10Hz	0.5 μ V/p-p
10Hz	18nV/ \sqrt Hz Max
100Hz	13nV/ \sqrt Hz Max
1000Hz	11nV/ \sqrt Hz Max
NOISE (Current)	
0.1Hz-10Hz	30pAp-p Max
10Hz	0.8pAp-p Max
100Hz	0.23pAp-p Max
1000Hz	0.17pAp-p Max

Instrumentation Amplifier with $V_{CM} = 300V$ and $CMRR > 160dB$

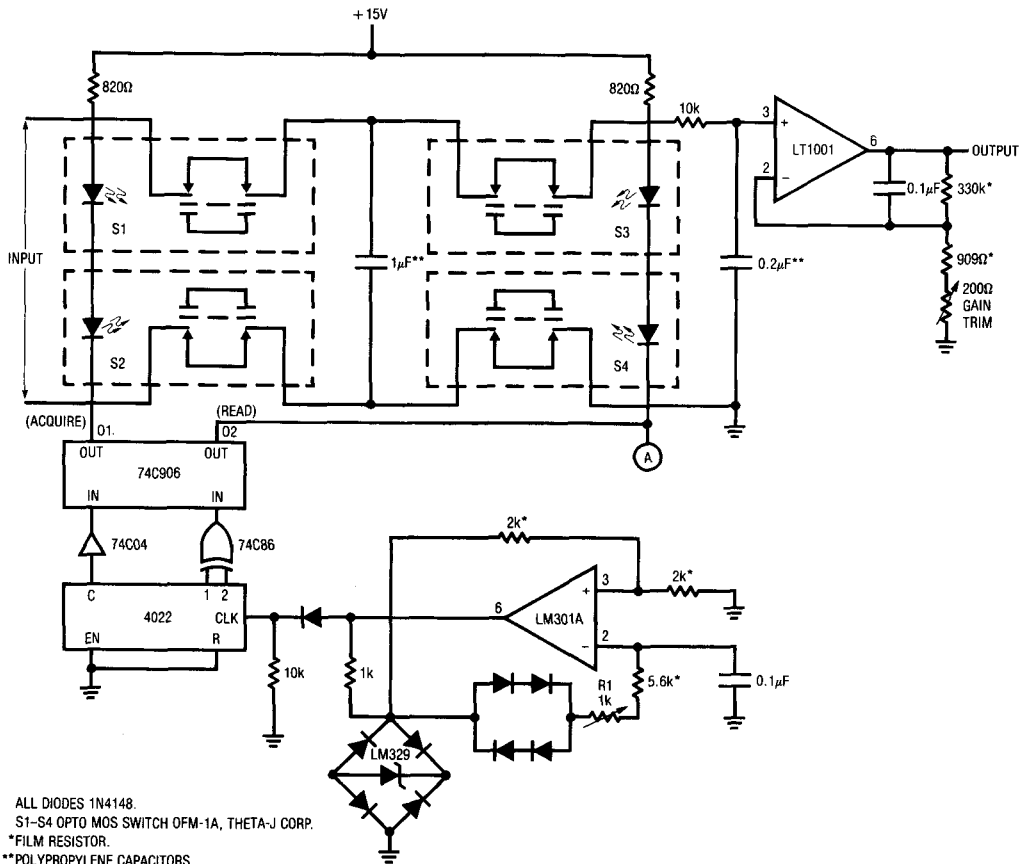
The circuit of Figure 1 may be used wherever differential inputs are required. It is particularly applicable to transducer signal conditioning where high common-mode voltages may exist. The circuit has the low offset and drift of the LT1002, but also incorporates a novel switched-capacitor "front end" to achieve some specifications not available in an instrumentation amplifier.

Common-mode rejection ratio at DC for the front end exceeds 160dB. The amplifier will operate over a $\pm 300V$ common-mode range and gain accuracy and stability are limited only by external resistors. The high common-mode voltage capability of the design allows it to withstand transient and fault conditions often encountered in industrial environments.

The circuit's inputs are fed to LED-driven optically-coupled MOSFET switches, S1 and S2. Two similar switches, S3 and S4, are in series with S1 and S2. A2, a precision oscillator, and its associated CMOS logic functions generate non-overlapping clock outputs which drive the switch's LEDs. When the "acquire pulse" is low, S1 and S2 are on and the 1 μ F capacitor acquires the differential voltage at the bridge's output. During this interval, S3 and S4 are off. When the acquire pulse rises, S1 and S2 begin to go off. After a delay to allow S1 and S2 to fully open, the "read pulse" goes low, turning on S3 and S4. Now, the 1 μ F capacitor appears as a ground-referred voltage source which is read by the main amplifier, A3. The 10k-0.2 μ F network allows A3's input to retain the 1 μ F unit's value when the circuit returns to the acquire mode. A3 provides the circuit's output. Its gain is set in normal fashion by feedback resistors. The 0.1 μ F feedback capacitor sets a rolloff of 5Hz. Several features aid circuit operation. A2 is trimmed for a 93Hz clock output. This frequency inhibits power line-originated noise from interacting with the switching action because it is not harmonically related to 60Hz. Such interaction may cause DC errors.

The differential-to-single-ended transition performed by the switches and capacitors means that A3 never sees the input's common-mode signal. The 300V breakdown specification of the optically-driven MOSFET switch allows the circuit to withstand and operate at common-mode levels of $\pm 300V$ (switch leakage typically rises above 1nA over 100V, causing some circuit performance degradation). In addition, the optical drive to the

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ALL DIODES 1N4148.
 S1-S4 OPTO MOS SWITCH OFM-1A, THETA-J CORP.
 *FILM RESISTOR.
 **POLYPROPYLENE CAPACITORS.
 ADJUST R1 FOR 93Hz AT TEST POINT A.
 A FLYING CAPACITOR CHARGED BY CLOCKED PHOTO-DRIVEN FET SWITCHES CONVERTS A DIFFERENTIAL SIGNAL AT A HIGH COMMON-MODE VOLTAGE TO A SINGLE-ENDED SIGNAL AT THE LT1001 OUTPUT.

Figure 1. Instrumentation Amplifier with 300V Common-Mode Range

MOSFETs eliminates the charge injection problems common to FET switched capacitive networks. The 750µs switching speed of the optical switch limits the circuit carrier to low frequencies, but most transducer circuits do not require any substantial bandwidth.

Linearized Platinum RTD Signal Conditioner

Platinum resistance temperature detectors (RTD) are generally accepted as the best choice for high accuracy and stability in temperature measurements. Unfortunately, they exhibit a non-linear temperature versus

resistance characteristic which complicates signal conditioning. Over a 0°C to 100°C range this non-linearity amounts to 0.4°C. Figure 2 shows a thermometer circuit which corrects for this error and achieves ±0.025°C absolute accuracy over the 0°C-100°C range.

A1 functions as a negative gain inverter to drive a constant current through the platinum sensor. The LT1009 and the 10k resistor provide the current reference. Because A1 operates at negative gain, the voltage across the RTD is low and self-heating induced errors are reduced. A1's output potential, which varies with the

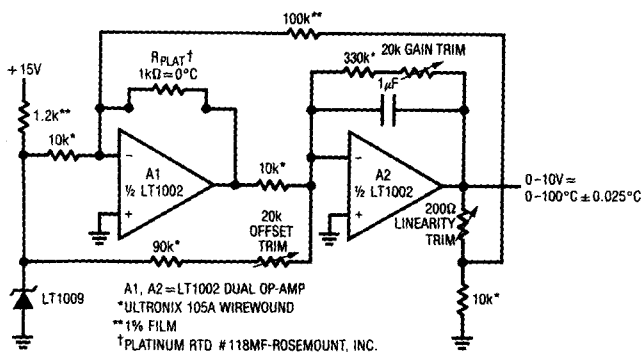


Figure 2. Linear Thermometer

platinum sensor's temperature, feeds A2. A2 provides scaled gain and offsetting so that its output will swing from 0.00V to 10.000V for a 0.00°C to 100.00°C temperature swing at the RTD. The $1\mu\text{F}$ capacitor limits noise pick-up. Normally, this circuit would exhibit a 0.4°C non-linearity error due to the RTD's imperfect response. This term is corrected by returning a small portion of the circuit's output to A1's negative input. This varies the reference current, causing compensatory changes in the circuit's gain slope. To calibrate this circuit, substitute a precision decade box (e.g., General Radio 1432-K) for the sensor. Set the box to the 0°C value (1000.0Ω) and adjust the offset trim for a 0.000V output. Next, set the decade box for a 35°C output (1138.7Ω) and adjust the gain trim for a 3.500V output reading. Finally, set the box to 1392.6Ω (100.00°C) and trim the linearity adjustment. Repeat this sequence until all three points are fixed. Total error over the entire range will be within $\pm 0.025^\circ\text{C}$. The resistance values given are for a nominal 1000.0Ω (0°C) sensor. Sensors deviating from this nominal value can be used by factoring in the deviation from 1000.0Ω . This deviation, which is manufacturer specified for each individual sensor, is an offset term due to winding tolerances during fabrication of the RTD. The gain slope of the platinum is primarily fixed by the purity of the material and is a very small error term.

Thermally Controlled Ni Cad Charger

Charging Ni Cad batteries at high current rates is desirable because it allows short charge time. The difficulty with such operations is that excessive internal heating degrades the batteries and can cause gas venting to the outside atmosphere. Schemes based on monitoring cell voltage during charge suffer because cell voltage is not necessarily indicative of the charge state of the battery. Open loop techniques involving high charge rates for a fixed time do not account for battery characteristic shifts over life and ambient temperature.

One way to charge batteries rapidly without abuse is to measure cell temperature and taper the charge accordingly. Figure 3 uses a thermocouple for this function. A second thermocouple nulls out the effects of ambient temperature. The LT1001 amplifier furnishes the low level capability necessary to work with the microvolt level thermocouple signals. To understand the circuit's operation, assume a discharged battery pack in the Darlington collector line. The battery and ambient thermocouples are at the same temperature. The battery thermocouple is directly mounted to one of the cells in the pack. The ambient thermocouple is exposed to ambient temperature and mounted to a thermal mass which approximates that

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of the battery pack. Under these conditions, the thermocouple voltages cancel and the positive input is at zero volts. The negative current through the 620kΩ resistor to the summing junction causes the amplifier to swing positive, turning on the Darlington pair. Current flows from the +15V supply, through the battery pack and to ground via the 0.6Ω shunt. The voltage across the shunt rises to 1V, balancing the summing junction, and the amplifier servo controls about 1.6A through the battery pack. As the battery charges, it heats. This heat is picked up by the battery-mounted thermocouple. The temperature difference between the two thermocouples determines the voltage which appears at the amplifier's positive input. As battery temperature rises, this small negative voltage (1°C difference between the thermocouples equals 40μV) becomes larger. The amplifier, operating at a gain of 4300, gradually reduces the current through the bat-

tery to maintain its inputs at balance. The effect of this action is shown in Figure 4. The battery charges at a high rate until heating occurs and the circuit then tapers the charge. The values given in the circuit limit the battery surface temperature rise over ambient to about 5°C.

Precision Adjustable Dead Zone Circuit

Figure 5 details a precision adjustable dead zone circuit. This is particularly useful in motor driven position servo circuits. In such applications it is desirable to generate an adjustable, symmetrical dead band so that the servo motor's degree of stiffness and hunting characteristics around null may be controlled. In addition, because stages of this type are usually followed by very high gain servo amplifiers, it is necessary that low voltage offsets be maintained when inside the dead band zone.

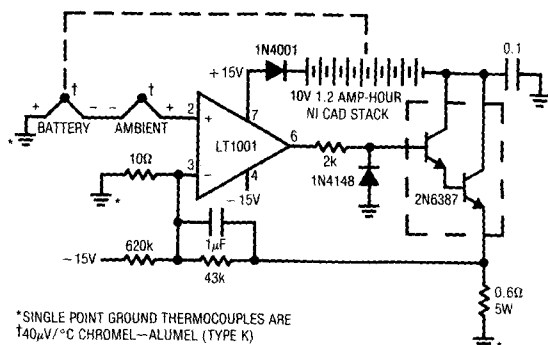


Figure 3. Thermally Controlled Ni Cad Battery Charger

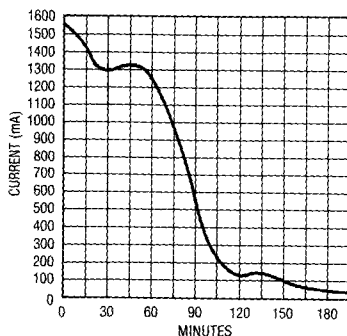


Figure 4. Charging Current vs Time for a 1.2A-Hour Cell

The circuit is made up of a synchronous rectifier (A1, C1), a variable unipolar dead zone cell composed of A2A and Q2-Q4, and a demodulator (A2B). When a circuit input (Trace A, Figure 6), in this case a triangle wave, is applied, the C1 crossing detector determines its polarity. C1's output (Trace B, Figure 6) drives Q1. When the input is negative, C1 goes high and Q1 conducts, grounding A1's positive input (Trace C, Figure 6). This turns A1 into a unity-gain inverter and its output (Trace D, Figure 6) inverts the input signal. For positive inputs, C1's output is low, cutting Q1 off and A1 unity-gain follows the input. This synchronous rectification presents the dead zone cell with a unipolar signal. Q2 forms a voltage adjustable current control at A2A's summing junction. Q3 provides V_{BE} temperature compensation and Q4 protects Q2's V_{BE} against reverse bias. When the dead zone command input is above A1's output, Q2 (Q2 emitter is Trace E, Figure 6) is off and A2A's output (Trace F, Figure 6) goes

to zero. When A1's output rises above the dead zone input, Q2 conducts, A2A functions as a current-to-voltage converter, and an inverted version of A1's output appears at A2A's output. This signal feeds synchronous demodulator A2B, which recovers the bipolar input signal. Q6 is switched by Q5's phase inverted version of C1's output. When the circuit signal input is positive, Q6 is on, grounding A2B's positive input (Trace G, Figure 6) and A2B's output inverts. The opposite action occurs for negative signal inputs. In this fashion, A2B's output recovers the bipolar input signal while preserving the adjustable dead zone. Because the same device (Q2) is used for positive and negative signals, dead zone symmetry is nearly ideal. Q2's V_{BE} drop limits the minimum dead zone to 600mV. Thus, A1's offsets will never be seen when the circuit is in dead band and the effects of delay time and offset in C1 are similarly eliminated. Only A2A and A2B need to be low offset devices.

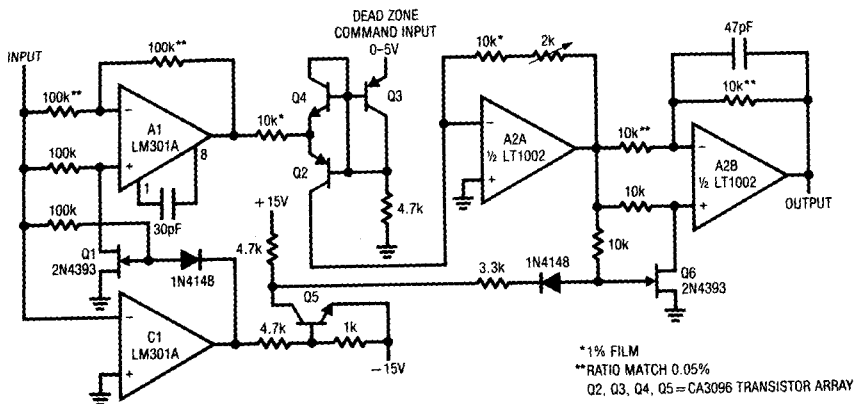


Figure 5. Precision Adjustable Dead Zone Generator

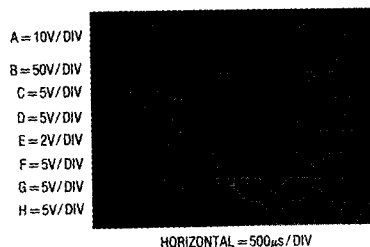


Figure 6

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Ultra-Precision Variable Voltage Reference

Figure 7 combines an LT1002 with a MOSFET switched toroid to create a precision variable voltage reference with a wide dynamic range of outputs. The reference has two outputs. The low voltage range spans 0V to 10V and is settable in 100 μ V (10ppm at full scale) increments. The high voltage range runs from 0V to 100V in 1mV steps (also 10ppm at full scale). The low voltage range is derived from A1, the LM199A voltage reference, and the panel mounted Kelvin-Varley Divider (KVD). A1 is a follower with gain, with the 2N2219 used for a boosted output. The selected value, typically in the 43k Ω range, and the 100 Ω potentiometer are used to trim the output to 10.0000V with the KVD dials set to full scale. The low offset of the LT1002 op amp eliminates the need for an offset trim. The non-inverting configuration used permits the 100k Ω KVD to be unloaded by the amplifier. The low bias current and high CMRR of the LT1002 are required to read the KVD without introducing error. The 100 Ω resistor is a short circuit limit and the low range output is taken at the 2N2219 emitter.

The circuit achieves its high voltage output without resorting to separate high voltage power supplies. Instead, the DC input to a chopped step-up toroidal transformer is servo-controlled by an op amp. The C1 multivibrator generates a 40kHz clock, which is divided into a complementary 20kHz square wave by the 74C74 flip-flop. These waveforms bias the VMOS FETs. A2 compares the divided down output of the transformer's rectifier-filter against the low voltage output. The amplified difference voltage biases the power Darlington, which drives the transformer's primary center tap, completing a feedback loop around the transformer. The 0.1 μ F unit is used for loop stability. A2 servos whatever voltage is required to balance its inputs. The loop is calibrated so a precise 0V-100.00V output corresponds to the setting of the KVD dials. The VMOS choppers are the key to maintaining the wide dynamic range of settings on the high voltage scale. Their resistive saturation characteristic allows the control range to extend to within an LSB (1mV) of 0V. The 2N2907 serves as a simple coarse voltage clamp on the high voltage range. The potentiometer allows a voltage ceiling to

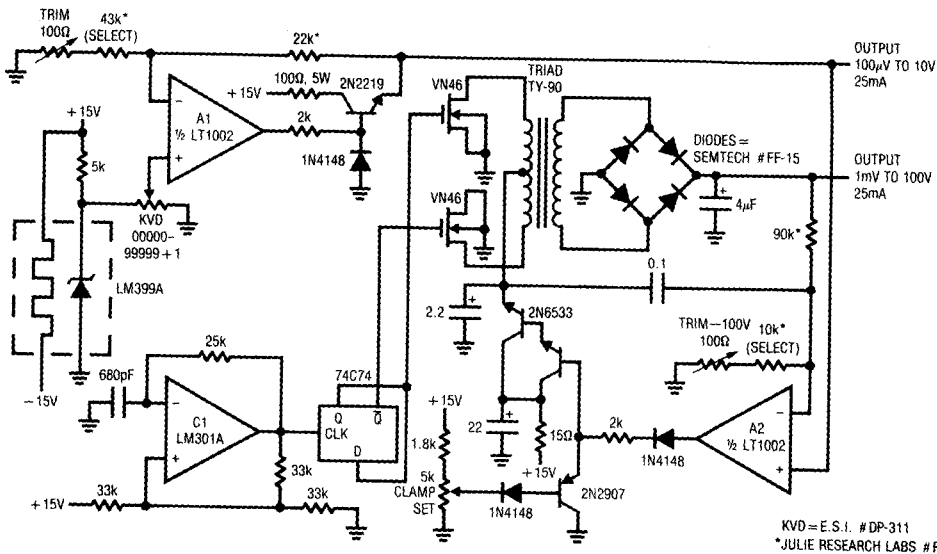


Figure 7. Ultra-Precision Variable Voltage Reference

be set for safety or other reasons when using the reference. To calibrate this circuit, select the 43kΩ value and adjust the 100Ω trim for a precise 10.0000V output at the low voltage output. Next, select the 10kΩ value and trim the 100Ω unit in the high voltage divider string. The typical stability of this circuit under laboratory conditions (25°C ± 5°C) may be estimated from the following data:

10V Range

Zener drift— temperature 5°C × 0.2ppm/°C	= 1ppm
Zener drift—time (per year)	= 25ppm
A1 op amp E _{OS} drift 0.5μV/°C × 5°C × A = 1.4 = 2.5μV	= 0.25ppm
A1 op amp E _{OS} drift— 1 year = 10μV/year	= 1ppm
KVD—2ppm/°C ratio shift × 5°C	= 10ppm
<u>37.25ppm over ± 5°C and 1 year at full scale</u>	

100V Range

All above errors	= 37.25ppm
A2 time and temperature	= 0.5ppm
<u>37.75ppm at full scale</u>	

Precision High Speed Op Amp

The design requirements to achieve high DC accuracy in an amplifier such as the LT1001/1002 preclude high speed performance. Additionally, it is difficult to design a precision monolithic amplifier which will drive large currents because of internal die heating problems. Some applications do call for speed, accuracy and output drive capability. Figure 8 shows a circuit which can be used to meet these conflicting requirements. In this arrangement, the LT1001 is used to stabilize a broadband stage to build an op amp with the DC precision of the LT1001 and high speed capability. This composite amplifier

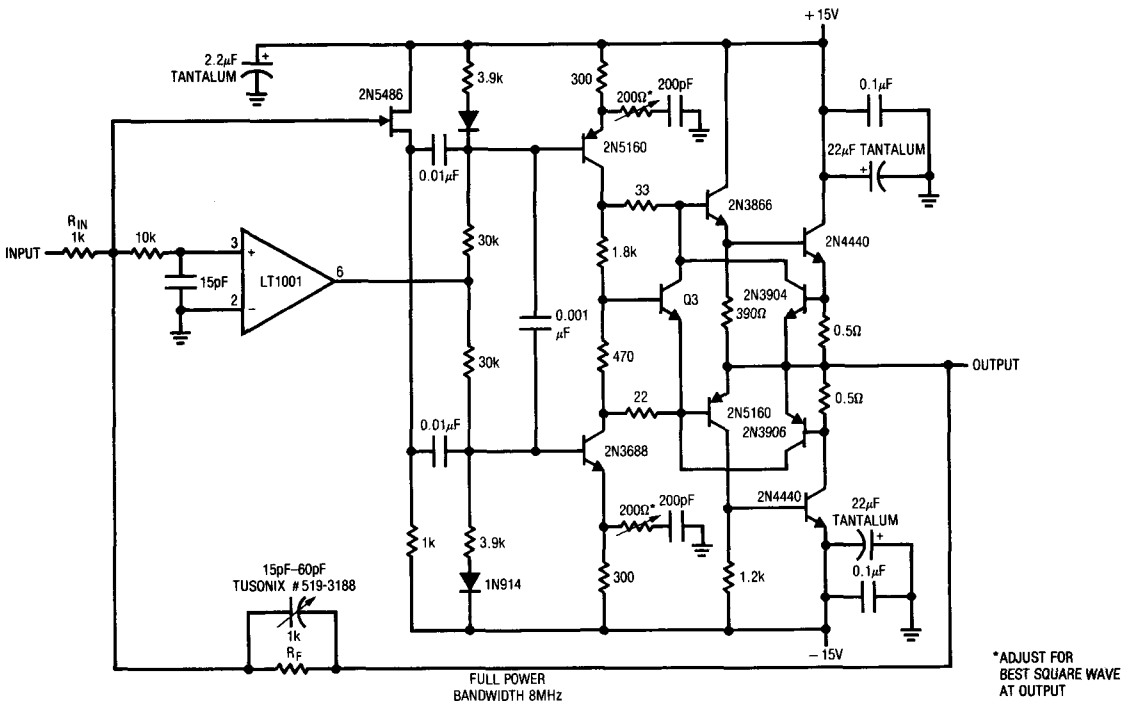


Figure 8. 1000V/μs 1A Op Amp

Application Note 6

features a $1500\text{V}/\mu\text{s}$ slew rate, full output to 8MHz and will drive $\pm 10\text{V}$ into a 10Ω load. It is short circuit protected at $\pm 1\text{A}$. The offset and drift specifications are controlled by the LT1001. High speed signals are fed-forward around the LT1001 through Q10 and directly drive the wideband stage. The LT1001 operates at low frequency to DC stabilize the fast stage. The high frequency rolloff of the LT1001 is matched to the low frequency rolloff of the discrete stage.

The high speed stage is composed of transistors with F_t 's approaching 1GHz. The output devices are NPN RF power transistors in a quasi-complementary arrangement. This is necessary because PNP RF power transistors are not available. Q8 and Q9 limit short circuit

current by sensing across 0.5Ω shunts. They apply degenerative feedback around the output stage when turned on, thereby limiting current. The 200Ω potentiometers and the variable feedback capacitor should be adjusted for a compromise between slew rate and output waveform clarity. Typically, the highest slew rate will sacrifice clean transitions. Figure 9 shows the response of the amplifier (Trace B) to a fast input pulse (Trace A), with the adjustments optimized for clean transitions. Slew rate is still $1000\text{V}/\mu\text{s}$ and the output appears clean within the 275MHz bandpass of the monitoring oscilloscope. In setting up and using this circuit, RF layout techniques and a ground plane are mandatory and the 2N4440s must be heat sunk.

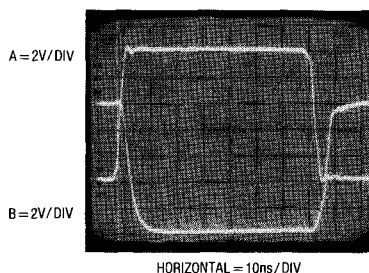


Figure 9. Op Amp Response

Some Techniques for Direct Digitization of Transducer Outputs

Jim Williams

Almost all transducers produce low level signals. Normally, high accuracy signal conditioning amplifiers are used to boost these outputs to levels which can easily drive cables, additional circuitry, or data converters. This practice raises the signal processing range well above the error floor, permitting high resolution over a wide dynamic range.

Some emerging trends in transducer-based systems are causing the use of signal conditioning amplifiers to be re-evaluated. While these amplifiers will always be useful, their utilization may not be as universal as it once was. In particular, many industrial transducer-fed systems are employing digital transmission of signals to eliminate noise-induced inaccuracies in long cable runs. Additionally, the increasing digital content of systems, along with pressures on board space and cost, make it desirable to digitize transducer outputs as far forward in the signal chain as possible. These trends point toward direct digitization of transducer outputs—a difficult task.

Classical A→D conversion techniques emphasize high level input ranges. This allows LSB step size to be as large as possible, minimizing offset and noise caused errors. For this reason, A→D LSB size is almost always above a millivolt, with 100 μ V–200 μ V per LSB available in a few 10V full-scale devices. The requirements to directly A→D convert the output of a typical strain gauge transducer are illuminating. The transducer's full-scale

output is 30mV, meaning a 10-bit A→D converter must have an LSB increment of only 30 μ V. Performing a 10-bit conversion on a type K thermocouple monitoring a 0°C–60°C environment proves even more stringent. The type K thermocouple puts out 41.4 μ V/°C over the 0°C–60°C range. The LSB increment is found by:

$$\frac{60^{\circ}\text{C} \times 41.4\mu\text{V}/^{\circ}\text{C}}{1024} = 2.42\mu\text{V}/\text{LSB}$$

These examples furnish extraordinarily small step sizes, far below commercially available A→D units and seemingly impossible to digitize without DC preamplification. In fact, both transducers' outputs may be directly digitized to stable 10-bit resolution using circuitry specifically designed for the function.

This application note details circuit techniques which directly digitize the low level outputs of a variety of transducers. The approaches described are unique in that they do not utilize any DC gain stage. The transducer outputs receive no DC signal conditioning; A→D conversion is directly performed at low level. The circuits produce a serial data output which may be transmitted over a single wire with the characteristic noise immunity of digital systems. By eliminating the traditional DC gain stage, these circuits furnish a direct, economical way to digitize low level transducer outputs without sacrificing performance.

Application Note 7

Figure 1 shows a simple way to convert the current output of an LM334 temperature sensor to a corresponding output frequency. The sensor pulls a temperature-dependent current ($0.33\%/^{\circ}\text{C}$) from A1's positive input node. This point, biased from the LM329-driven resistor string, responds with a varying, temperature-dependent voltage. The voltage varies the operating point of A1, configured as a self-resetting integrator. A1 integrates the LM329 referenced current into its summing point, producing a negative-going ramp at its output. When the ramp amplitude becomes large enough, the transistors turn on, resetting the feedback capacitor and forcing A1's output to zero. When the capacitor's reset current goes to zero, the transistors go off and A1 begins to integrate negatively again. The frequency of this oscillation action is dependent on A1's DC operating point, which varies with the LM334's temperature. The circuit's DC biasing values are arranged so that a 0°C to 100°C sensor temperature excursion produces 0kHz-to-1kHz at the output. Additionally, only 2V appear across the LM334, minimizing sensor power dissipation related errors. The differentiator-transistor network at A1's output provides a TTL compatible output. To calibrate this circuit, place the LM334 in a 0°C environment and trim the "0°C adjust" for 0Hz. Next, put the LM334 in a 100°C environment and set the "100°C adjust" for 1kHz output.

Repeat this procedure until both points are fixed. This circuit has a stable 0.1°C resolution with $\pm 1.0^{\circ}\text{C}$ accuracy.

Figure 2 shows another temperature-to-frequency converter, but this circuit uses the popular type K thermocouple as a sensor. The design includes cold junction compensation for the thermocouple over a 0°C – 60°C range. Accuracy is $\pm 1^{\circ}\text{C}$ and resolution is 0.1°C .

The thermocouple's extremely low output ($41.4\mu\text{V}/^{\circ}\text{C}$) and the requirement for cold junction compensation make it one of the most difficult transducers to directly digitize. The approach used is based on the $50\text{nV}/^{\circ}\text{C}$ input offset drift performance of the LTC1052 chopper-stabilized amplifier.

In this circuit, A1's positive input is biased by the thermocouple. A1's output drives a crude $V \rightarrow F$ converter, comprised of the 74C04 inverters and associated components. Each $V \rightarrow F$ output pulse causes a fixed quantity of charge to be dispensed into the $1\mu\text{F}$ capacitor from the 100pF capacitor via the LTC1043 switch. The larger capacitor integrates the packets of charge, producing a DC voltage at A1's negative input. A1's output forces the $V \rightarrow F$ converter to run at whatever frequency is required to balance the amplifier's inputs. This feedback action

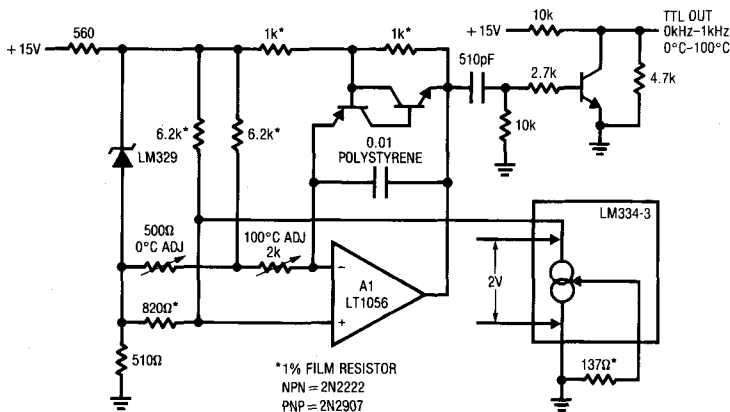


Figure 1. Temperature-to-Frequency Converter

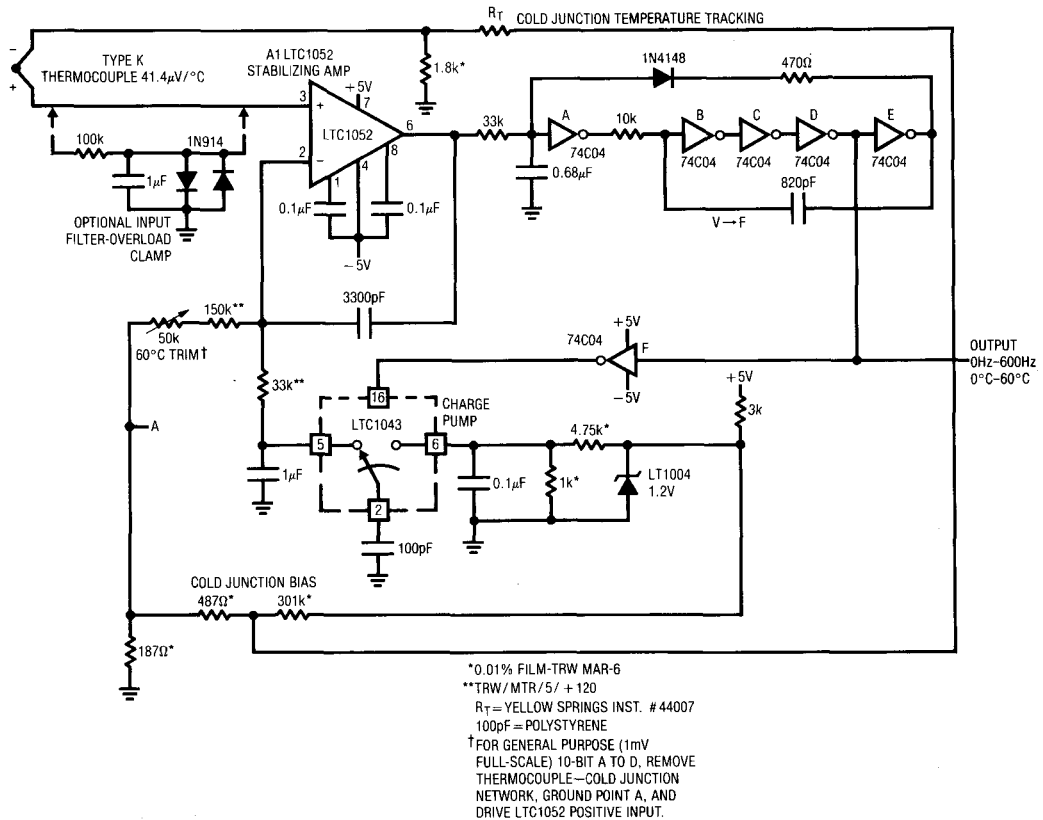


Figure 2. Thermocouple-to-Frequency Converter

eliminates drift and nonlinearities in the V→F converter as an error term and the output frequency is solely a function of the DC conditions at A1's inputs. The 3300pF capacitor forms a dominant response pole at A1, stabilizing the loop.

A1's low drift eliminates offset errors in the circuit, despite an LSB value of only 4.14µV(0.1°C)!

R_T, a thermistor, and the 1.8k, 187Ω, 487Ω and 301k values form a cold junction compensation network which is biased from the LT1004 1.2V reference. In addition to cold junction compensation, the network provides offsetting, permitting a 0°C sensor temperature to yield 0Hz at the output.

Figure 3 details circuit operation. A1's output drives the 33k-0.68µF combination, producing a ramp (Trace A, Figure 3) across the capacitor. When the ramp crosses inverter A's threshold, the cascaded inverter chain switches, producing a low output at E (Trace B). This causes the 0.68µF capacitor to discharge through the diode, resetting the capacitor to 0V. The 820pF unit provides positive AC feedback to inverter B's input (Trace C), assuring a clean reset. The frequency of this ramp-and-reset sequence varies with A1's output. Inverter F's output controls the LTC1043 switch. When the inverter output is high, pins 2 and 6 are connected, allowing the 100pF capacitor to charge to a potential derived from the LT1004 1.2V reference. When the inverter goes low, pin 2

Application Note 7

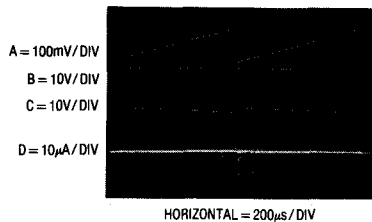


Figure 3. Thermocouple Digitizer Waveforms

is connected to pin 5. During this interval, the 100pF capacitor completely discharges (Trace D) into the 1µF unit. The amount of charge delivered is constant over each cycle ($Q = CV$), so the voltage the 1µF capacitor charges to is a function of frequency and discharge path resistance. This voltage is summed with the LT1004-derived offsetting potential at A1's negative input, closing a loop around A1. The $-120\text{ppm}/^\circ\text{C}$ drift of the 100pF charge-dispensing polystyrene capacitor is compensated by the opposing tempco of the specified resistors used in the 1µF's discharge path. Typical circuit gain is $20\text{ppm}/^\circ\text{C}$, allowing less than 1 LSB (0.1°C) output drift over a 0°C – 70°C ambient operating range.

The thermocouple's known characteristics, combined with A1's low offset and the cold junction/offsetting network components specified, eliminate zero trimming. Calibration is accomplished by placing the thermocouple in a 60°C environment and adjusting the 50kΩ potentiometer for a 600Hz output. Beyond 60°C the cold junction network departs from the thermocouple's response and output error increases rapidly. Although the digital output will be a function of the thermocouple's temperature over hundreds of degrees, linearization by a monitoring processor is required.

It is worth noting that this circuit can directly convert any low level, single-ended signal. If the offsetting/cold junction network is removed and the 50kΩ potentiometer returned directly to ground, inputs may be applied to A1's positive terminal. The circuit produces a 10-bit accurate output with a full-scale range of only 1mV ($1\mu\text{V}$ per LSB)! The high impedance of A1's input allows filtering or overload clamping of the input signal without introducing error.

Figure 4 is another temperature measuring circuit, but the transducer used is unusual. The circuit measures temperature by utilizing the relationship between the speed of sound and temperature in a medium. In dry air the relationship is governed by:

$$C = 331, 5 \sqrt{\frac{T}{273}} \text{ meters/second}$$

where C = speed of sound.

Acoustic thermometry is used where extremes in operating temperature are encountered, such as cryogenics and nuclear reactors. Additionally, acoustic temperature standards have been built by operating the acoustic transducer inside a sealed, known medium.

The inherent time domain operation of acoustic thermometers allows a direct conversion into a digital output. Figure 4 shows a circuit that does this. A1, the inductor, and their associated components for a simple flyback type regulated 200V supply which biases the transducer. The transducer is composed of the Polaroid ultrasonic element noted, mounted at one end of a sealed, 6 inch long Invar tube. The Invar material minimizes mechanical tube deformation with temperature. The medium inside the tube is dry air. The transducer may be thought of as a capacitor, composed of an insulating disc with a conductive coating on each side.

Each time the TTL clock (Trace A, Figure 5) goes high, the transducer receives AC drive via the $0.22\mu\text{F}$ capacitor. This drive causes mechanical movement of the disc and ultrasonic energy is emitted. The clock input simultaneously sets the 74C74 flip-flop output (Trace E) low and pulls the $0.01\mu\text{F}$ capacitor to ground. This cuts off drive to C1's 3kΩ output pull-up resistor (Trace C), forcing C1's output (Trace D) to zero. During the clock pulse's period, A2's output (Trace B) is saturated due to excessive signal at its input. When the clock pulse ceases, A2 comes out of bound and amplifies in its linear region. The ultrasonic transducer now acts like a capacitance microphone, with the 200V supply providing bias. Residual disc ringing is picked up and appears at A2's output. This signal cannot trigger C1, however, because the $0.01\mu\text{F}$ capacitor has not charged high enough to allow the inverter chain output to bias C1's output pull-up resistor.

The ultrasonic energy emitted by the transducer travels down the tube, bounces off the far end and heads toward the transducer. Before it returns, the $0.01\mu\text{F}$ capacitor crosses the inverter's threshold and C1's $3\text{k}\Omega$ resistor (Trace C) receives bias. Upon returning, the sonic energy causes a mechanical displacement of the transducer, forcing a shift in capacitance. This capacitance shift causes charge to be displaced into C2's summing point,

and the output responds with an amplified version of this signal (Trace B). C1's output (Trace D) triggers, resetting the flip-flop. The flip-flop's output pulse (Trace E) represents the transit time down the tube and will vary with temperature according to the equation given. A monitoring processor can convert this pulse width into the desired temperature information.

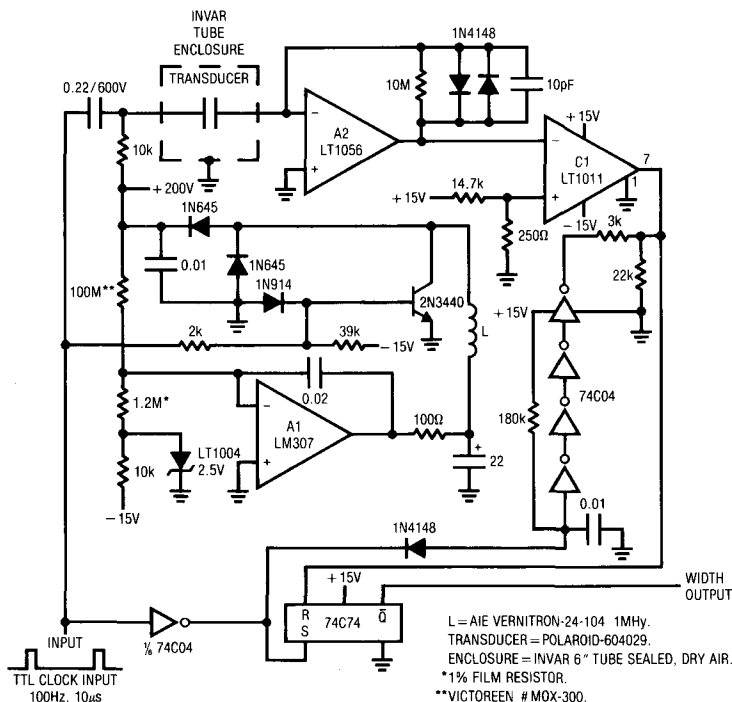


Figure 4. Acoustic Thermometer

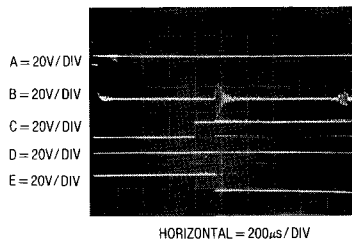


Figure 5. Acoustic Thermometer Waveforms

Application Note 7

In the photograph another received signal, lower in amplitude, is visible at the extreme right hand side of Trace B. Its position in time identifies it as a second bounce return from the tube's far end. Also, note the increased detected noise level after the return of the first bounce. This is due to sonic energy dispersion inside the tube. The transducer picks up energy deflected from the tube walls, which is phase shifted from the desired signal. C1 is seen to respond to these unwanted signal sources, but the circuit's final pulse output is unaffected. Additionally, the time window gating supplied to C1's pull-up resistor greatly reduces the likelihood of false triggering due to noise coming from outside the tube.

Temperature sensors are not the only transducers which can be directly digitized. Strain gauge transducers account for a large class of pressure and force measurements. Typically, a strain gauge bridge-based transducer produces 3mV of full-scale output per volt of bridge drive. Figure 6 shows a way to directly digitize a strain gauge bridge's output to 10-bit accuracy. For a 7.5V bridge drive, an LSB increment is 25 μ V, considerably larger than the thermocouple example but still far below conventional A \rightarrow D converters. The bridge's differential output complicates the required converter input structure, but is accommodated.

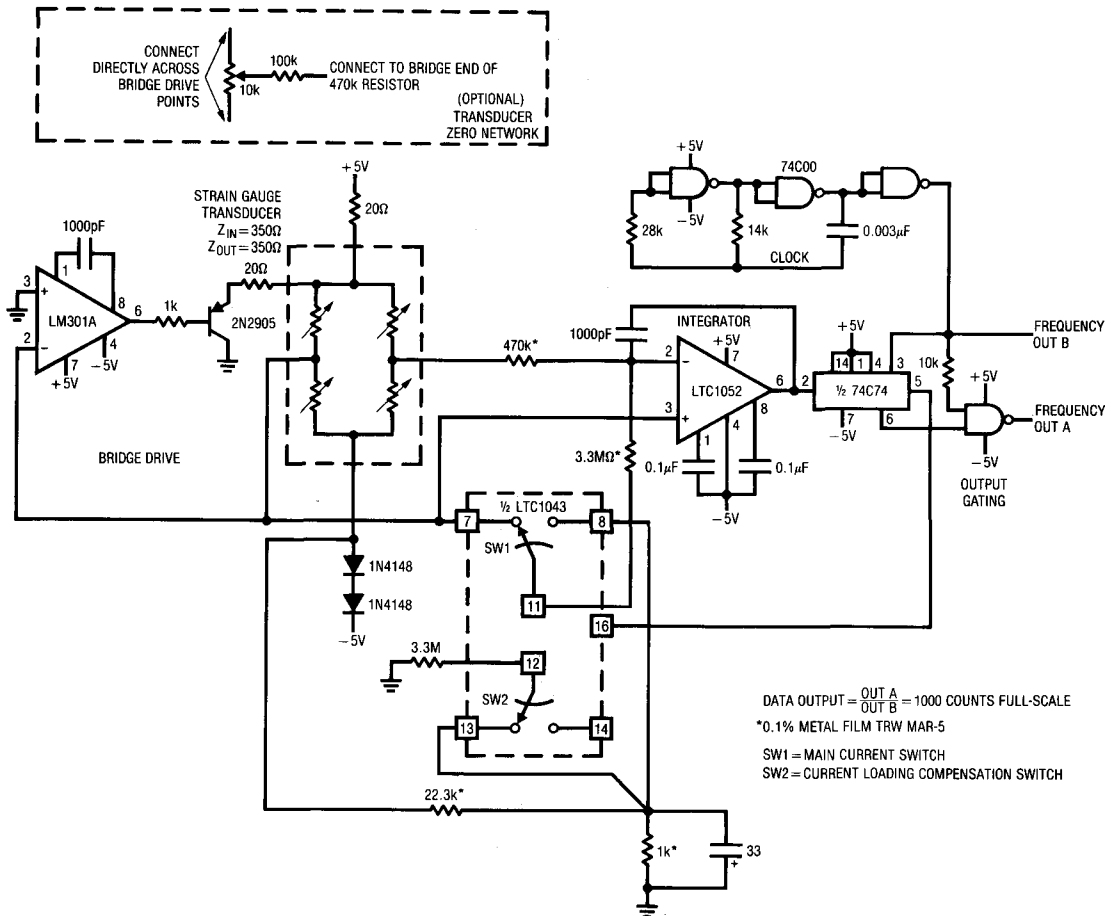


Figure 6. Strain Gauge Digitizer

A1 and the transistor provide bridge excitation. One signal output of the bridge is connected to A1's negative input. A1's positive input is at ground. A1 drives the transistor to bias the bridge at whatever voltage is required to bring its negative input to ground potential. The diode drops in the bridge's $-5V$ return line allow the transistor to force the bridge's positive end far enough to servo A1's inputs. This arrangement allows the bridge's other output to be sensed in a single-ended, ground-referred fashion. In practice, a slight error exists due to A1's offset voltage. This error is eliminated by referring the A \rightarrow D converter input to A1's negative input instead of ground.

The A \rightarrow D converter is made up of A2, a flip-flop and some gates. It is based on a current balancing technique. Once again, the chopper-stabilized LTC7652's $50nV/^{\circ}C$ input drift is required to implement the low level input A \rightarrow D. Figure 7 details key A \rightarrow D waveforms. Assume the flip-flop's Q output (Trace B) is low, connecting LTC1043 pins 11 and 12 to pins 7 and 13, respectively. The main current switch passes no current, as the $3.3M\Omega$ resistor is placed across A2's inputs. The current loading compensation switch puts a $3.3M\Omega$ value across the $1k$ divider resistor, lowering the voltage across it by 0.03%.

Under these conditions the only current into A2's summing point is from the bridge via the $470k\Omega$ resistor. This positive current forces A2's output (Trace A, Figure 7) to integrate in a negative direction. The negative ramp continues and finally passes the 74C74 flip-flop's switching threshold. At the next clock pulse (clock is Trace C), the flip-flop changes

state (Trace B), causing the LTC1043 switch positions to reverse. Pin 12 connects to pin 14 and pin 11 to pin 8. In this case, the $3.3M\Omega$ resistor controlled by the current loading compensation switch is disconnected from the $1k$ unit, but the $3.3M\Omega$ value controlled by the main current switch replaces it. The 0.03% loading of the $3.3M\Omega$ resistor, combined with this switching scheme, eliminate any sag or loading effects across the $1k\Omega$ resistor during switching. The result is a quickly rising, precise current flow out of A2's summing point.

This current, scaled to be greater than the bridge's maximum output, forces A2's output movement to reverse and integrate in the positive direction. At the first clock pulse after A2's output has crossed the flip-flop's triggering threshold, switching occurs and the entire cycle repeats. Because the reference current is fixed, the flip-flop's duty cycle is solely a function of the bridge signal current into A2's summing point. Additionally, the reference current is supplied from the $22.3k-1k$ divider, which is derived from the bridge drive. Thus, the A \rightarrow D's reference current varies ratiometrically with the bridge output, eliminating bridge drive variations as an error source. The flip-flop's output gates the clock, producing the "frequency output A" waveform (Trace D). The $10k$ resistor combines with the output gate's input capacitance to slightly delay the clock signal, eliminating spurious output pulses due to flip-flop delay. The circuit's data output, the ratio of output A to the clock frequency, may be extracted with counters. Because the output is expressed as a ratio, clock frequency stability is unimportant.

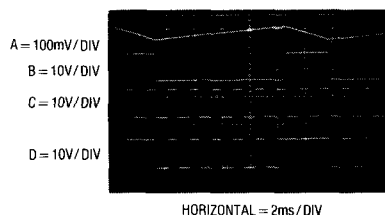


Figure 7. Strain Gauge Digitizer Waveforms

Application Note 7

Several subtle factors are critical in setting up and using this circuit. The 470k Ω input resistor at A2 has been selected to produce less than 1 LSB loading error on the strain gauge bridge. The bridge receives only about 7.5V of drive due to the deliberate resistor and diode drops in its supply lines. At 3mV output per volt of bridge drive, full-scale signal is 22.5mV. This produces a signal current of only:

$$I = \frac{0.0225V}{470k} = 48nA.$$

To maintain 10-bit accuracy, leakage and amplifier bias current into A2's summing point must be less than 0.1% of this figure or:

$$I = \frac{48nA}{1000} = 48pA.$$

Although A2's bias current is much lower than this, board leakage can cause trouble. At a minimum, careful layout and a clean PC board are required. The best practice is to use a teflon stand-off for all summing point connections. The 470k Ω and 3.3M Ω resistors associated with A2's negative input should be placed as close as possible to the IC pin. Note also that the 3.3M Ω current summing resistor is switched to A2's positive input when it is not sourcing current to the summing point. This seemingly unnecessary connection prevents minute stray 60Hz and noise currents from being coupled to A2's summing point when the current reference is off. Failure to utilize this connection will cause jitter in the LSB. Gain trimming of this circuit may be accomplished by varying the 22.3k value. If the particular strain gauge transducer used requires zero trimming, use the optional network shown. Over a 0°C–70°C range the circuit will typically maintain its 10-bit output within 1 LSB accuracy. The tracking errors of the starred resistors are the primary contributors to this small error.

Because of their extremely wide dynamic range, photo diodes present a difficult challenge for signal conditioning circuitry. A high quality device furnishes a linear current output over a 100dB range, requiring a 17-bit A \rightarrow D converter as well as a current-to-voltage input amplifier. A

common approach employs a logarithmically responding current-to-voltage input amplifier to nonlinearly compress the photodiode's output, allowing a much lower resolution A \rightarrow D converter to be used. Although this scheme saves the cost of the 17-bit A \rightarrow D, it has the inconvenience of a nonlinear output. Also, logarithmic amplifiers respond relatively slowly, which may be detrimental in some photometric measurements. Figure 8's circuit directly converts a photodiode's current output into an output frequency with 100dB of dynamic range. Optical input power of 20nW–2mW produces a linear, calibrated 20Hz-to-2MHz output. Output response to input light steps is fast and cost is low.

The photodiode's output current feeds a highly modified, high frequency version of a Pease type charge pump I \rightarrow F converter. Diode output current biases A1's negative input, causing its output (Trace A, Figure 9) to ramp in a negative direction. When A1's output crosses zero, C1's output (Trace B) goes low, causing the LT1009 diode bridge to bound at –3.7V. The 200pF–1.8k lead network at C1's positive input aids comparator high frequency response. C1's output going low also provides AC positive feedback to its positive input (Trace D). Additional AC positive feedback is supplied by output transistor Q3's collector (Trace C). During this interval, charge is pulled from A1's summing point via the 47pF–5pF capacitors (Trace E). This causes A1's output to move quickly positive, switching C1 after the positive feedback around it has decayed. The LT1009 diode bridge now bounds at +3.7V. The 47pF–5pF pair receives charge, A2's summing junction recovers and the entire cycle repeats at a frequency linearly related to photodiode output current. D1 and D2 compensate the bridge diodes. Diode connected Q1 compensates steering diode Q2. The diode connected transistors provide lower leakage than simple diodes. C2 provides circuit latch-up protection, necessary because of the circuit's AC coupled feedback loop. If latch-up occurs, A1's output saturates low, causing C2's emitter-follower connected output to go high. This forces A1's output positive, initiating normal circuit action.

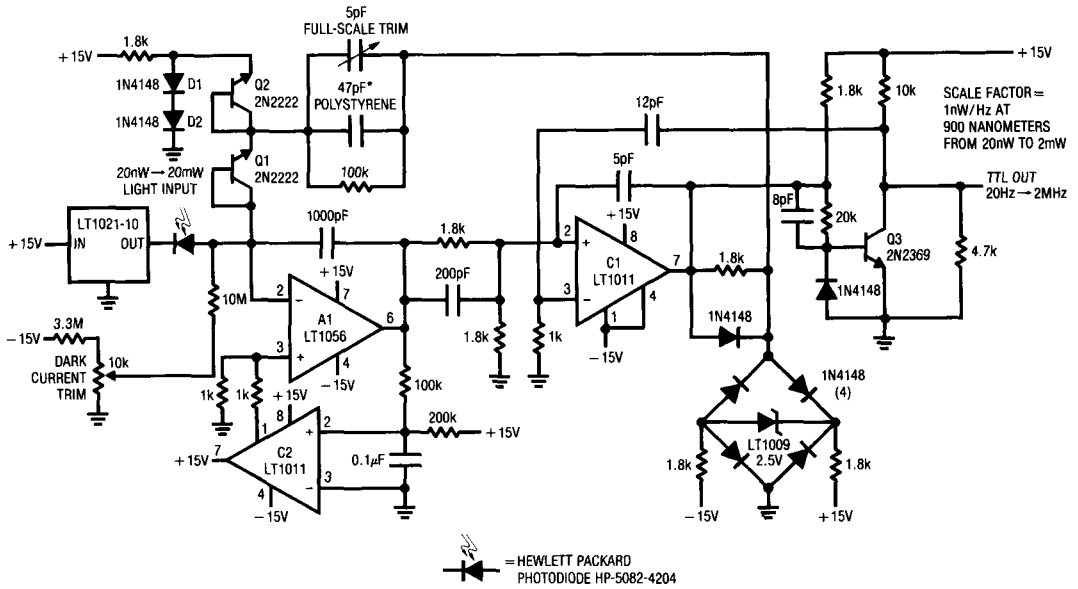
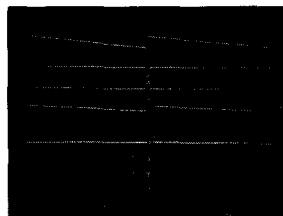


Figure 8. Photodiode Digitizer

A = 0.5V/DIV
B = 50V/DIV
C = 20V/DIV
D = 0.5V/DIV
E = 10mA/DIV



HORIZONTAL = 2µs/DIV

Figure 9. Photodiode Digitizer Waveforms

Application Note 7

The LT1021-10 reference biases the photodiode, providing optimum optical current response characteristics. To trim this circuit, place the photodiode in a *completely* dark environment. Trim the "dark current" adjustment so the circuit oscillates at the lowest possible frequency, typically 1Hz–2Hz. Next, apply or electrically simulate (see manufacturer's data sheet for light input versus output current data) a 2mW optical input. Trim the 5pF adjustment for an output frequency of 2MHz. If the adjustment is outside the range of the trimmer, alter the 47pF capacitor's value appropriately. Once calibrated, this circuit will maintain 1% accuracy over the photodiode's entire 100dB range. The accuracy obtained is limited by photodiode characteristics and not the circuit. Figure 10 shows dynamic response of the circuit to a fast light pulse (Trace A, Figure 10). The frequency output settles within $1\mu\text{s}$ on both edges.

One of the most difficult physical parameters to transduce is relative humidity. A recently introduced humidity transducer, based on a capacitance shift versus relative humidity (RH), offers good accuracy, fast response, wide range and linear response. The transducer features a nominal $+1.7\text{pF}$ per percent RH capacitance shift with a 500pF value at RH = 76%. It does not require temperature compensation. A significant consideration in signal conditioning this transducer is that the average voltage across the device must be zero. No net DC may pass through the transducer. Figure 11's circuit converts the RH transducer's capacitive shifts directly into a calibrated frequency output. The LTC1043 switched-capacitor instrumentation building block IC free runs at 150kHz. Pin 2 (Figure 12, Trace A) is alternately connected between the LT1004 negative reference and A1's summing junction. The $1\mu\text{F}$ -22M Ω combination associated with the RH transducer ensures the device's required pure AC biasing.

When pin 2 is connected to pin 6, the transducer receives a negative charge. When the LTC1043's internal clock switches, pin 2 is tied to pin 5, depositing all of the transducer's charge into A1's summing point. A1's input (Trace B), just faintly visible, shows transducer current, while Trace C is A1's output. A1, an integrator, ramps up in stepped fashion as successive discrete packets of charge are deposited into its summing point. Concurrent with this action, a second set of LTC1043 switches (pins 7, 8, 11, 12, 13, and 14) works to synchronously transfer a fixed amount of charge of opposing polarity into A1's summing junction. The amount of fixed charge is set to cancel the sensor offset (e.g., 0% RH does not extrapolate to 0pF sensor capacitance). Thus, the slope of the stepped ramp at A1's output is a function of the sensor's value minus its offset term. A1 continues to ramp positive until it equals the voltage at C1's negative input. This triggers C1's output high (Trace D). AC positive feedback holds C1's output high long enough for the 2N4393 FET to completely discharge A1's feedback capacitor. A1's output drops to zero and the entire cycle repeats. The frequency of repetition is a function of the RH transducer's capacitance. C1's input voltage is derived from the LT1004 reference. LTC1044 pins 3, 18, and 15 and the 330pF value form a simple charge pump which biases A2's summing point. A2's output assumes whatever value is required to maintain its summing point at zero. The 0.22 μF capacitor integrates A2's response to DC, while the feedback resistors establish the operating point. Because A2's output voltage determines ramp height, its feedback resistor's value sets the circuit's gain slope. Traces E, F, and G, time and amplitude expansions of Traces A, B, and C, permit a detailed look at the effects of the transducer's charge dumping on A1's output ramp.

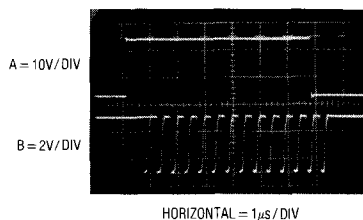


Figure 10. Step Response of Photodiode Digitizer

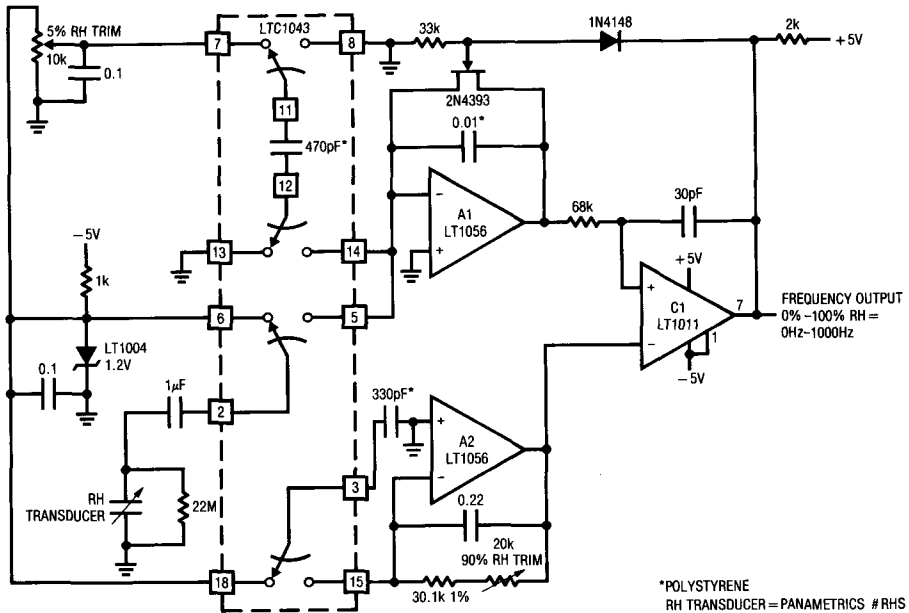


Figure 11. Humidity-to-Frequency Converter

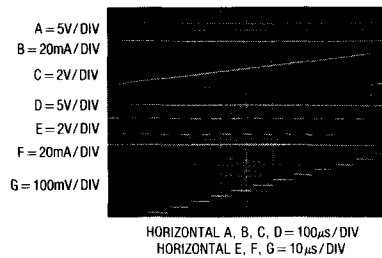


Figure 12. Humidity → Frequency Converter Waveforms

Application Note 7

Circuit temperature dependence is low because the 330pF and 0.01 μ F polystyrene capacitors' (both gain terms) -120 ppm drifts ratiometrically cancel. Further ratiometric error cancellation occurs because the transducer's charge source and A2's output voltage are both derived from the LT1004 reference. The sole uncompensated term in the circuit is the 470pF capacitor which supplies the offsetting charge. Its -120 ppm/ $^{\circ}$ C drift is well below the transducer's 2% accuracy specification, and circuit temperature independence is assured.

To calibrate this circuit, place the transducer in a 5% RH environment and adjust the 5% trim for 50Hz output. Next, place the transducer in a 90% RH environment and adjust the 90% trim for a 900Hz output. Repeat this procedure until both points are fixed. Relative humidity accuracy will be 2% over the 5%–90% RH range. If RH standards are not available, the circuit may be approximately calibrated against using fixed capacitors in place of the sensor. Ideal values are 5% RH = 379.3pF and 90% = 523.8pF. Note that these values assume an ideal sensor. An actual device may depart from them by as much as 10%.

Another frequently required physical parameter is level. Level transducers which measure angle from ideal level are employed in road construction, machine tools, inertial navigation systems and other applications requiring a gravity reference. One of the most elegantly simple level transducers is a small tube nearly filled with a partially conductive liquid. Figure 13 shows such a device. If the tube is level with respect to gravity, the bubble resides in the tube's center and the electrode resistances to common are identical. As the tube shifts away from level, the resistances increase and decrease proportionally. By controlling the tube's shape at manufacture it is possible to obtain a linear output signal when the transducer is incorporated into a bridge circuit.

Transducers of this type must be excited with an AC waveform to avoid damage to the partially conductive liquid inside the tube. Signal conditioning involves generating this excitation as well as extracting angle information and polarity determination (e.g., which side of level the tube is on). Figure 14 shows a circuit which does this, directly producing a calibrated frequency output corresponding to level. A sign bit, also supplied at the output, gives polarity information.

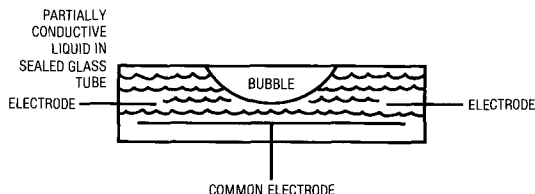


Figure 13. Bubble Based Level Transducer

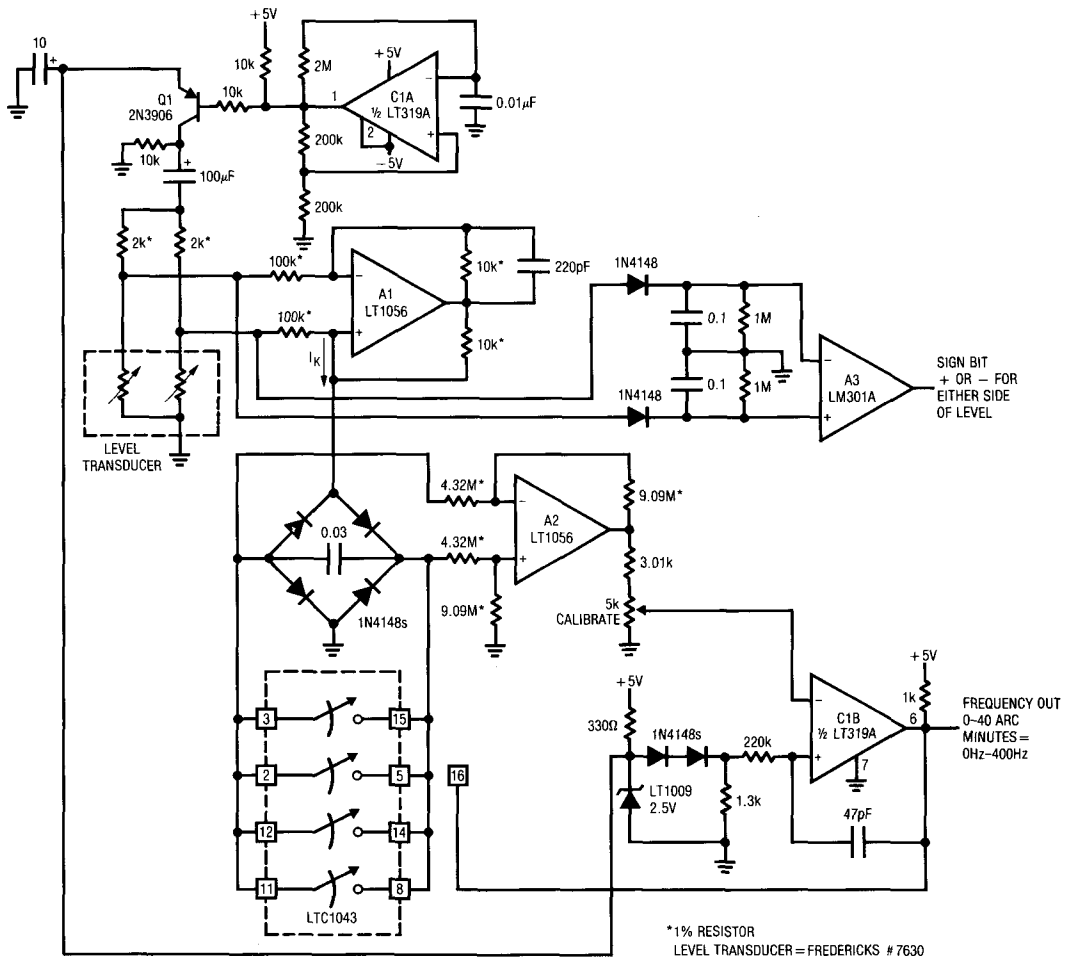


Figure 14. Level Transducer Digitizer

Application Note 7

The level transducer is configured with a pair of $2k\Omega$ resistors to form a bridge. The required AC bridge excitation is developed at C1A, which is configured as a multi-vibrator. C1 biases Q1, which switches the LT1009's 2.5V potential through the $100\mu\text{F}$ capacitor to provide the AC bridge drive. The bridge differential output AC signal is converted to a current by A1, operating as a Howland current pump. This current, whose polarity reverses as bridge drive polarity switches, is rectified by the diode bridge. Thus, the $0.03\mu\text{F}$ capacitor receives unipolar charge. A2, running at a differential gain of 2, senses the voltage across the capacitor and presents its single-ended output to C1B. When the voltage across the $0.03\mu\text{F}$ capacitor becomes high enough, C1B's output goes high, turning on the paralleled sections of the LTC1043 switch. This discharges the capacitor. The 47pF capacitor provides enough AC feedback around C1B to allow a complete zero reset for the capacitor. When the AC feedback ceases, C1B's output goes low and the LTC1043 switch goes off. The $0.03\mu\text{F}$ unit again receives constant current charging and the entire cycle repeats. The frequency of this oscillation is determined by the magnitude of the constant current delivered to the bridge-capacitor configuration. This current's magnitude is determined by the transducer bridge's offset, which is level related.

Figure 15 shows circuit waveforms. Trace A is the AC bridge drive, while Trace B is A1's output. Observe that when the bridge drive changes polarity, A1's output flips sign rapidly to maintain a constant current into the bridge-capacitor configuration. A2's output (Trace C) is a

unipolar, ground-referred ramp. Trace D is C1B's output pulse and the circuit's output. The diodes at C1B's positive input provide temperature compensation for the sensor's positive tempco, allowing C1B's trip voltage to ratiometrically track bridge output over temperature.

A3, operating open loop, determines polarity by comparing the rectified and filtered bridge output signals with respect to ground.

To calibrate this circuit, place the level transducer at a known 40 arc-minute angle and adjust the $5k\Omega$ trimmer at C1B for a 400Hz output. Circuit accuracy is limited by the transducer to about 2.5%.

The final example concerns direct digitization of a piezoelectric accelerometer. These transducers rely on the property of ceramic materials to produce charge when mechanically excited. In this device a mass is coupled to the ceramic element. An acceleration acting on the mass causes charge to be dispensed from the ceramic element. Sensitivity and frequency response are related to the characteristics of the ceramic used and the mechanical design of the transducer. The best way to signal condition a piezoelectric output is to unload it directly into the virtual ground of an op amp's summing point. This method provides no voltage difference between the center conductor and the shield of the coaxial cable connecting the accelerometer and the signal conditioning amplifier. This eliminates cable capacitance as a parasitic term, an important consideration in any charge output transducer. Because the accelerometer produces AC outputs, a direct digitization of its output must produce a sign bit as well as amplitude data.

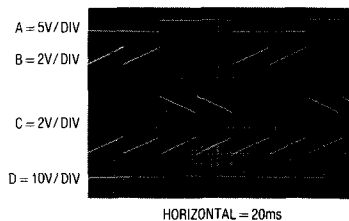


Figure 15. Level Transducer Digitizer Waveforms

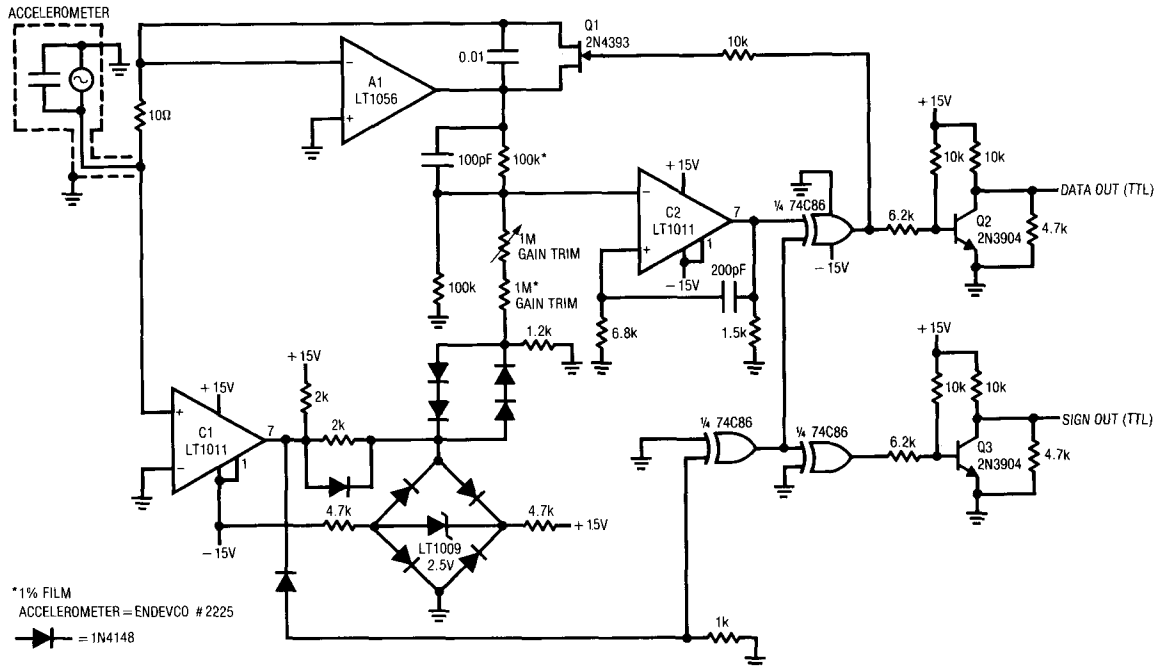


Figure 16. Accelerometer Digitizer

Figure 16's circuit accomplishes a complete, direct A → D conversion on the piezoelectric accelerometer noted and is generally applicable to other devices in this class. To understand the circuit it is convenient to replace the accelerometer with a square wave source coming through a resistor. When the square wave is positive, the A1 integrator responds with a negative-going ramp output (Trace A, Figure 17). C1, detecting the square wave polarity, goes high and the LT1009 diode bridge (Trace B) limits at +3.7V. A1's ramp output is summed with the bridge's output at C2's negative input. The series diodes temperature-compensate the bridge diodes. When A1's output goes far enough negative, C2's (Trace C) output goes high. The output gating is arranged so that with C1's output low and C2 high, Q1's gate (Trace D) receives turn-on bias. Q1 comes on, discharging A1's feedback capacitor and resetting A1's output to zero. Local AC positive feed-

back at C2 ensures adequate time for a complete zero reset of A1's feedback capacitor. The 100pF capacitor at C2's input aids high frequency response. When the AC feedback decays away, Q1 goes off, A1 begins to ramp negative again and the cycle repeats as long as the input square wave is positive. The frequency of oscillation is directly proportional to the current into A1's summing point. When the input square wave goes negative, A1 abruptly begins to ramp in the positive direction. Simultaneously, the C1 input polarity detector output goes negative, forcing the LT1009 bridge output negative. C2's output now switches when A2's output exceeds a positive limit. The output gating, directed by C1's polarity signal, inverts C2's output to supply proper drive to Q1's gate. Q1 turns on and resetting occurs. Thus, the loop maintains oscillation, but with all signs reversed. The Q2 and Q3 level shifters supply TTL data outputs for data and sign.

Application Note 7

This circuit constitutes an I→F converter which responds to AC inputs. If the square wave source is replaced with a piezoelectric accelerometer, direct digitization results. Figure 18 shows circuit response when an acceleration (Trace A), in this case a damped sinusoid, is applied to the transducer. The sign bit (Trace B) keeps track of acceleration polarity, while the frequency output supplies amplitude data. Observe the drop in output fre-

quency as the input waveform damps. A monitoring processor, sampling the sign and frequency waveforms faster than twice the highest acceleration frequency of interest, can extract desired acceleration waveform data. To trim the circuit, apply a known amplitude acceleration and adjust the 1MΩ gain trim at C2. Alternately, the accelerometer may be electrically simulated (see manufacturer's data sheet for scale factors).

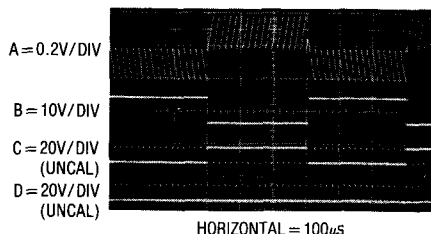


Figure 17. Accelerometer Digitizer Waveforms with Square Wave Test Drive

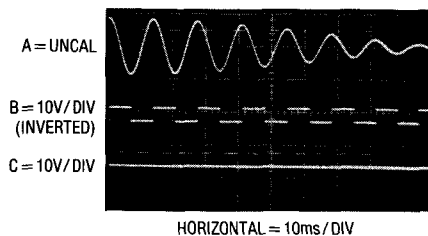


Figure 18. Accelerometer Digitizer Response

Power Conditioning Techniques for Batteries

Jim Williams

Declining power requirements for circuitry have made battery operation desirable and common. In many circumstances the battery voltage may be applied directly to circuitry with no special considerations. Other situations require some form of battery power conditioning to supply necessary voltages. At present, most IC regulators are not suitable for battery regulation because of high quiescent current and/or inability to operate at low input voltages. In particular, some switching regulators consume 20mA, many times the total power drain of some low power systems.

Designing battery regulator circuitry involves numerous considerations including efficiency, power output, battery life, circuit complexity, PC board space and cost.

Various linear and switching regulation techniques are applicable, with the best approach determined by specific requirements. Most circuit types provide DC outputs, although AC is sometimes required. General classes of regulators include voltage inverters, step-down circuits and step-up converters.

Negative Voltage Generators

Generating a negative voltage is a common requirement. Figure 1 shows a simple way to do this. The LTC1044 switched-capacitor voltage converter's internal switches synchronously transfer charge from C1 to C2, the output capacitor. When SW1 is closed, C1 charges to 9V. When SW1 opens, SW2 closes, charging C2, which assumes a negative potential with respect to ground. Continuous clocking

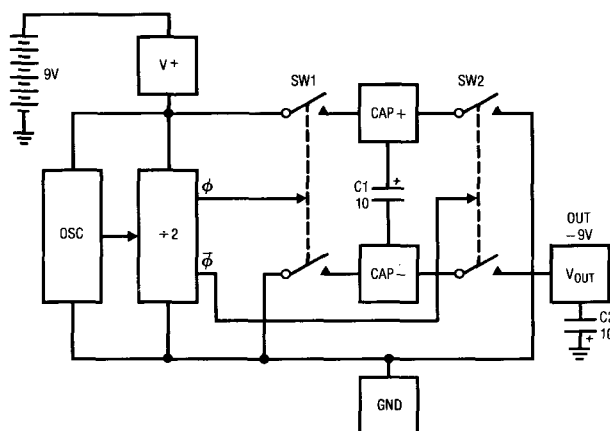


Figure 1. Negative Voltage Generator

keeps V_{OUT} at DC. Due to finite output impedance, loading the output causes a drop in voltage. Figure 2 plots output voltage deviation versus load current. In low current applications or where regulation is not critical, this circuit is adequate. To improve regulation, it is necessary to decrease output impedance. Figure 3 encloses the LTC1044 within the LM10's feedback loop. Because of the LTC1044's voltage inversion, the loop is closed at the op amp's positive input. The voltage converter's losses are compensated by increased drive from the LM10. The $0.1\mu\text{F}$ capacitor stabilizes the loop and the $47\mu\text{F}$ unit keeps LM10 output impedance low at the LTC1044's switching frequency. LM10 output swing restrictions limit circuit output to 8.5V. Output regulation, plotted in Figure 2, improves upon Figure 1's basic circuit.

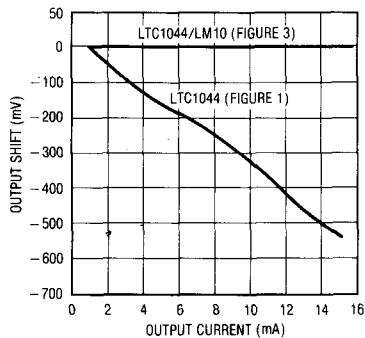


Figure 2

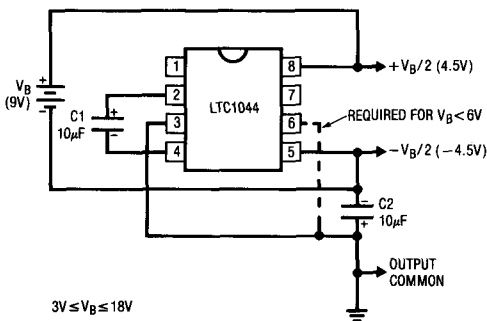


Figure 4. Battery Splitter

Battery Splitter

A common need in many systems is to obtain positive and negative supplies from a single battery. Where current requirements are small, the circuit shown in Figure 4 is a simple solution. It provides symmetrical \pm output voltages, both equal to one half the input voltage. The output voltages are referenced to pin 3 (output common). If the input voltage between pin 8 and pin 5 exceeds 6V, pin 6 should also be connected to pin 3, as shown by the dashed line. Higher current requirements are served by an LT1010 buffer. The splitter circuit shown in Figure 5 can source or sink up to $\pm 150\text{mA}$ with only 5mA quiescent current. The output capacitor, C2, can be made as large as necessary to absorb current transients. An input capacitor is also used on the buffer to avoid high frequency instability that can be caused by high source impedance.

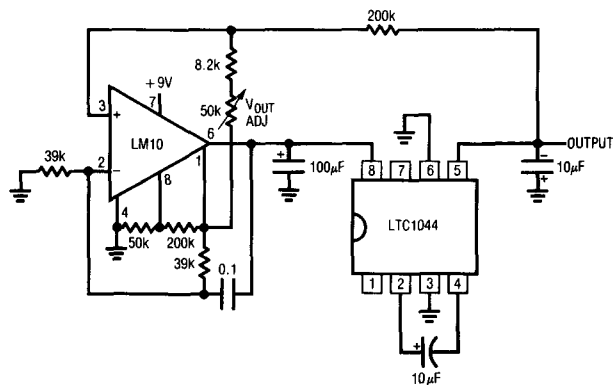


Figure 3. Regulated Negative Voltage Converter

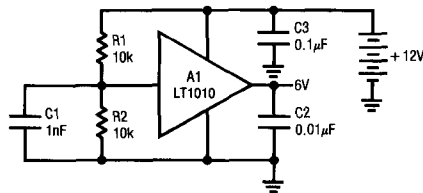


Figure 5. High Current Battery Splitter

Low Dropout Regulator

Linear regulators for batteries are a good way to get low noise, fast transient response regulation. It is desirable to achieve this performance with a very low regulator dropout voltage to maximize battery life. This can be done with PNP pass elements, but their base current never arrives at the load, decreasing efficiency. Additionally, the PNP's voltage gain complicates loop dynamics, often resulting in relatively poor transient response.

The circuit illustrated in Figure 6 offers extremely low dropout and the fast transient response of an NPN pass element. Quiescent current is $760\mu\text{A}$ and the 100mA capacity output is short circuit protected. Normally, NPN pass-based regulators have high dropout voltages because of voltage drops in the emitter-follower connected pass transistor. This 6V powered design drives the NPN pass base from a 12V source generated by the LTC1044

voltage doubler. The transistor operates as a voltage overdriven emitter-follower. The emitter's ability to follow the collector is limited only by $V_{CE\text{SAT}}$. The voltage overdriven base removes V_{BE} drop, normally the dominant loss, as a consideration. The LTC1044 doubles the battery voltage and powers the LT1013 dual op amp. A1, with 12V output capability, feedback controls the 6V collector-biased transistor. The 100Ω resistor prevents parasitic high frequency oscillation and the LT1004 serves as a reference. The output is trimmed by varying A1's feedback divider and the $0.003\mu\text{F}$ capacitor compensates the loop. A2 provides short circuit protection by forcing A1's output low if battery current exceeds 150mA. A2's low offset and high open loop gain allow using the 0.01Ω current sense resistor, reducing voltage drop losses. At 100mA output, the shunt has only 1mV across it.

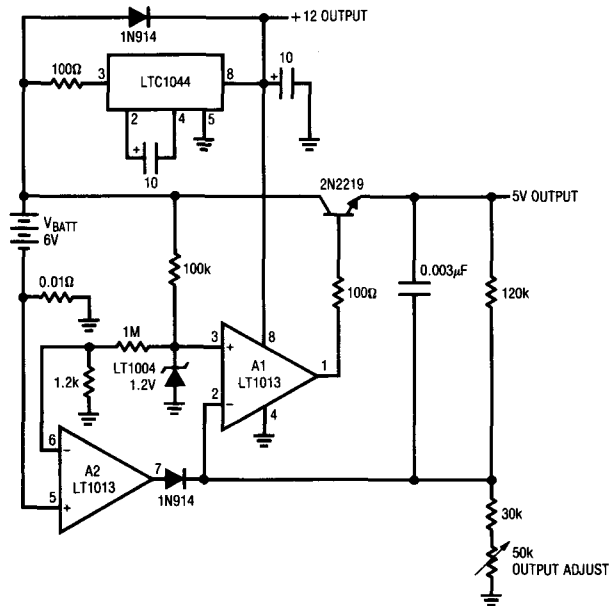


Figure 6. Low Dropout 5V Regulator

Application Note 8

Figure 7 illustrates dropout data for the regulator. At 10mA load, dropout is only 0.016V, with 0.94V occurring at 100mA loading. Transient response is shown in Figure 8. Waveform A controls an output load which is either zero or 100mA. Waveform B is the regulator's AC-coupled output. Transient response is clean and quick, with little tailing or aberration.

Low Power Switching Regulator

The low dropout linear regulator is efficient only when its input and output voltages are close. Situations requiring substantial voltage drop to achieve the desired regulated output need switching techniques to maintain good efficiency. Figure 9 shows a simple battery-powered switching regulator. It provides 5V out from a 9V source with 80%

efficiency and 50mA output capability. Assume Q1 is on. Its collector (Trace A, Figure 10) voltage rises, forcing current (Trace B) through the inductor. The output voltage (Trace C) rises, causing A1's output to rise. Q1 cuts off and the output decays through the load. The 100pF capacitor ensures clean switching. The cycle repeats when the output drops low enough for A1 to turn on Q1. The 1μF capacitor ensures low battery impedance at high frequencies, preventing "sag" during switching. Short circuit protection is as shown in Figure 6's circuit. In some applications the switching-induced noise on the regulated output may be troublesome. Figure 11 eliminates the noise by adding a low-dropout series regulator at the switching circuit's output. The switching loop's operation is similar to Figure 9 except that the voltage across the 2N5434 FET series pass element is controlled. The switching loop

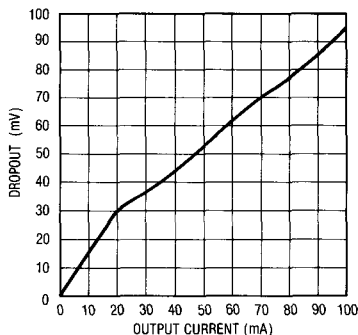


Figure 7. Dropout vs Load for Figure 6

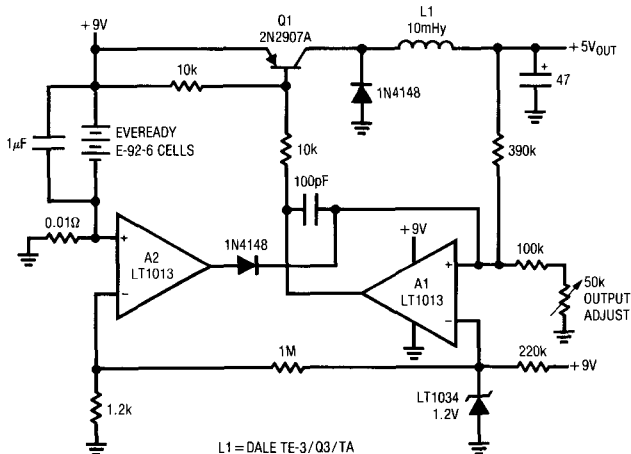


Figure 9. Low Power Switching Regulator

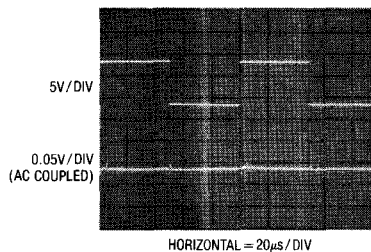


Figure 8. Transient Response of Figure 6's Circuit

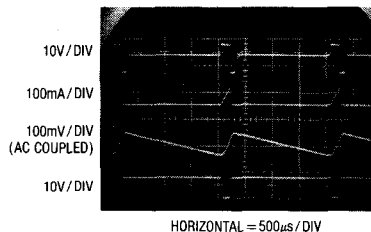


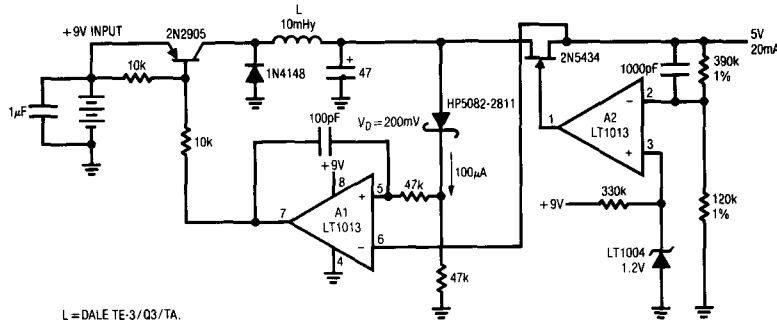
Figure 10. Figure 9's Operating Waveforms

forces this voltage to equal V_D , regardless of input or loading conditions. The FET, a low R_{ON} , low pinch-off unit, combines with A2 to form a simple, low dropout series pass regulator. The LT1004 is the reference and the 1000pF capacitor provides roll-off. This circuit will supply 25mA of noise-free, regulated power with short circuit current set by the FET's 30mA I_{DSS} . The overall 75% effi-

ciency is not quite as good as the basic switching circuit due to the 6mW ($0.250V \times 0.025A$) dissipated in the FET.

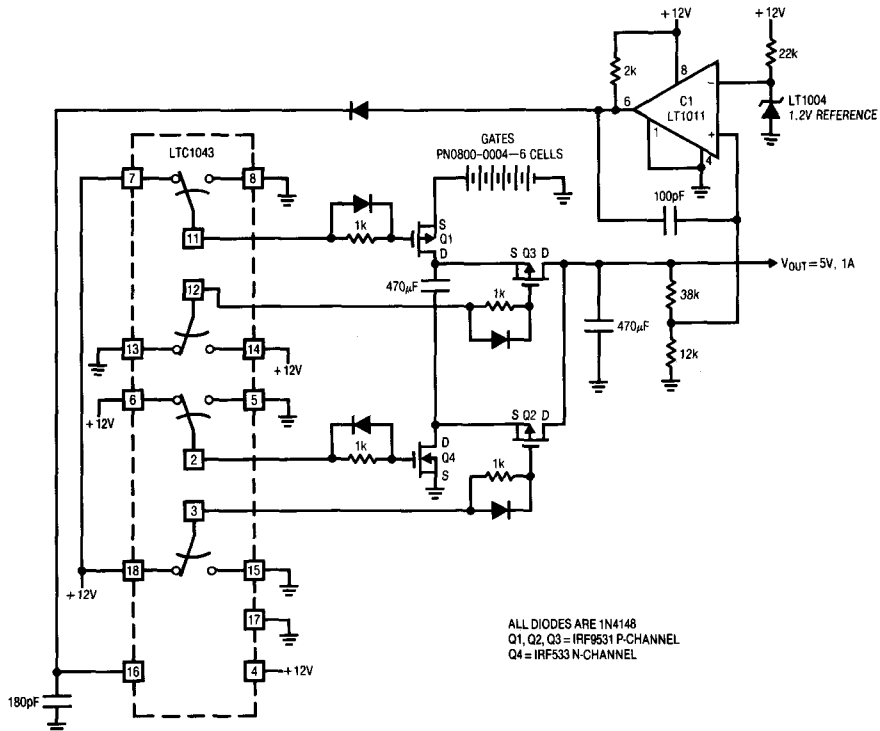
High Current, "Inductorless," Switching Regulator

Figure 12 shows another high efficiency battery-driven regulator, but this circuit features a 1A output capacity.



L = DALE TE-3/Q3/TA.

Figure 11. Switching Preregulated Linear Regulator



ALL DIODES ARE 1N4148
Q1, Q2, Q3 = IRFP531 P-CHANNEL
Q4 = IRFS33 N-CHANNEL

Figure 12. "Inductorless" High Current Switching Regulator

Application Note 8

Additionally, it does not require an inductor, an unusual feature for a switching regulator operating at this current level.

The LTC1043 switched-capacitor building block provides non-overlapping complementary drive to the Q1-Q4 power MOSFETs. The MOSFETs are arranged so that C1 and C2 are alternately placed in series and then in parallel. During the series phase, the +12V battery's current flows through both capacitors, charging them and furnishing load current. During the parallel phase, both capacitors deliver current to the load. Traces A and B, Figure 13, are the LTC1043-supplied drives to Q3 and Q4 respectively. Q1 and Q2 receive similar drive from pins 3 and 11. The diode-resistor networks provide additional non-overlapping drive characteristics, preventing simultaneous drive to the series-parallel phase switches. Normally, the output would be one half of the supply voltage, but C1 and its associated components close a feedback loop, forcing the output to 5V. With the circuit in the series phase, the output (Trace C) heads rapidly positive. When the output exceeds 5V, C1 trips, forcing the LTC1043 oscillator pin (Trace D) high. This truncates the LTC1043's triangle wave oscillator cycle. The circuit is forced into the parallel

phase and the output coasts down slowly until the next LTC1043 clock cycle begins. C1's output diode prevents the triangle down-slope from being affected and the 100pF capacitor provides sharp transitions. The loop regulates the output to 5V by feedback-controlling the turn-off point of the series phase. The circuit constitutes a large scale switched-capacitor voltage divider which is never allowed to complete a full cycle. The high transient currents are easily handled by the power MOSFETs and overall efficiency is 83%.

Voltage Step-Up Circuits—Simple Voltage Doubler

All of the previous circuits condition battery output to a lower voltage. Many applications call for a voltage above the battery output. Figure 14 shows a simple way to double available battery voltage using the LTC1044 switched-capacitor voltage converter. As shown, the IC functions in similar fashion to Figure 12's circuit, at greatly reduced power levels. This circuit will drive low power 74-CMOS loads (V_{SUPPLY} 3V-15V) for extended periods of time from two small cells. Efficiency exceeds 90% for load currents below 1.75mA. Figure 15 plots output voltage versus loading.

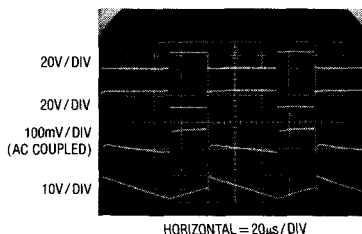


Figure 13. "Inductorless" Regulator's Waveforms

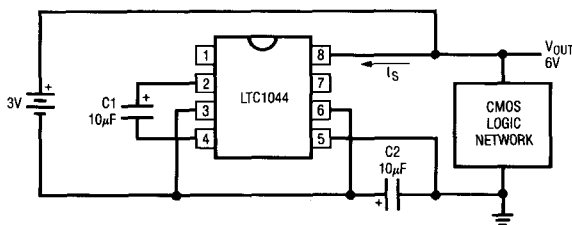


Figure 14. Voltage Doubler

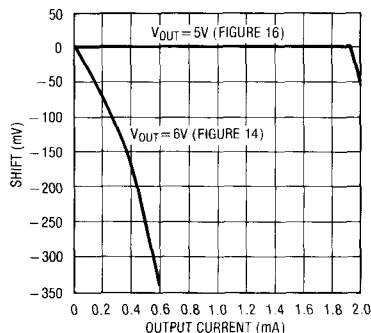


Figure 15

Figure 16 addresses Figure 14's regulation fall-off with increasing current. As in Figure 12, feedback techniques are used to compensate for the voltage converter's output impedance. The LTC1044 is connected in a voltage doubler mode, with the $10\mu\text{F}$ value used to pump up the $100\mu\text{F}$ capacitor. Q1 and Q2 serve as a bidirectional switch, allowing the pump up action to be interrupted. The circuit regulates by using an LM10 op amp reference to control the switch. When output voltage decays low enough (Figure 17, Trace A), the LM10's reference ampli-

fier swings high (Trace B), driving the op amp negative (Trace C) and both transistors come on. This allows the LTC1044 to pump charge to the $100\mu\text{F}$ capacitor. For each charge cycle, the output takes a voltage step. When the output steps high enough, the LM10 switches and the cycle repeats. Repetition rate is load dependent, with typical values of 1Hz-400Hz. Response hysteresis is set by the loop's gain-bandwidth to 40mV. The feedback network fixes the 5V output within 0.025V for loads up to 2mA (plotted in Figure 15).

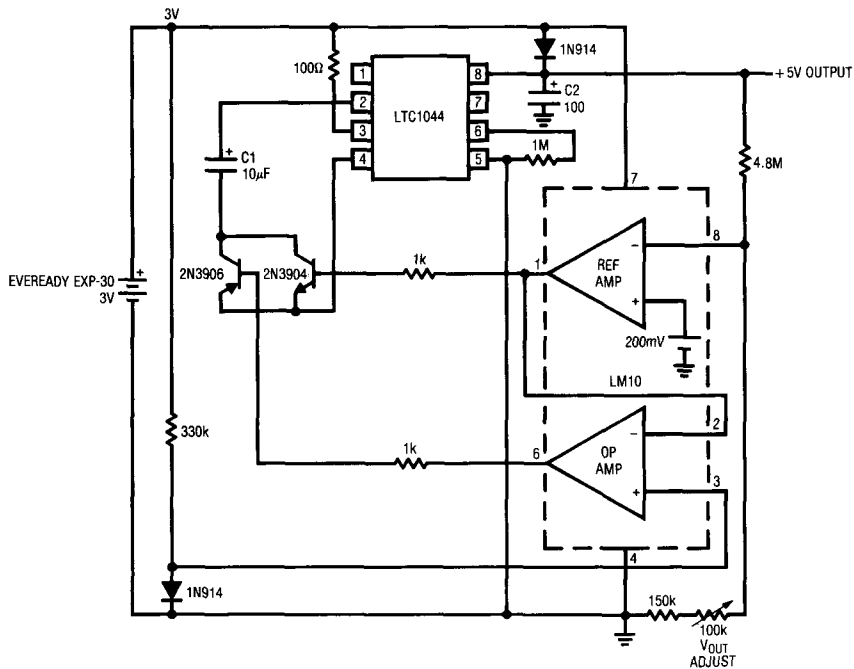


Figure 16. Regulated Voltage Up Converter

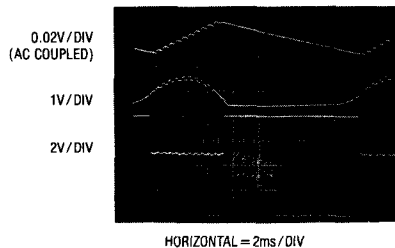


Figure 17. Up Converter's Waveforms

Application Note 8

The circuit in Figure 18 is conceptually similar, but uses a transformer to get greater voltage gain. This allows a 5V output from a single 1.5V cell. Q2, Q3 and T1 form a self-oscillating DC-DC converter, controlled by the Q1 switch. As in Figure 16, an LM10 closes feedback around this battery step-up converter. With only 1.5V at the input, particular attention must be paid to switch saturation losses. The Germanium transistors specified have under 50mV drop, less than silicon types. Germanium output diodes also contribute low forward drop losses. The 0.004 μ F capacitor sets hysteresis at 20mV, preventing erratic loop dynamics. An RC damper in T1's primary

eliminates parasitic high frequency oscillation modes. Figure 19 shows operation, with Q1's collector (Trace A) going high when circuit output voltage (Trace D) falls below the loop setpoint. Traces B and C are the LM10 output and Q2's collector, respectively. Note that the output's ramp steps up in similar fashion to Figure 16's capacitively-driven circuit. As with Figure 16, loop oscillation frequency is directly load dependent, with typical values of 1Hz-250Hz. This circuit will supply a 5V, 150 μ A load (about 25 CMOS SSI ICs) for 3000 hours from a single 1.5V "D" battery.

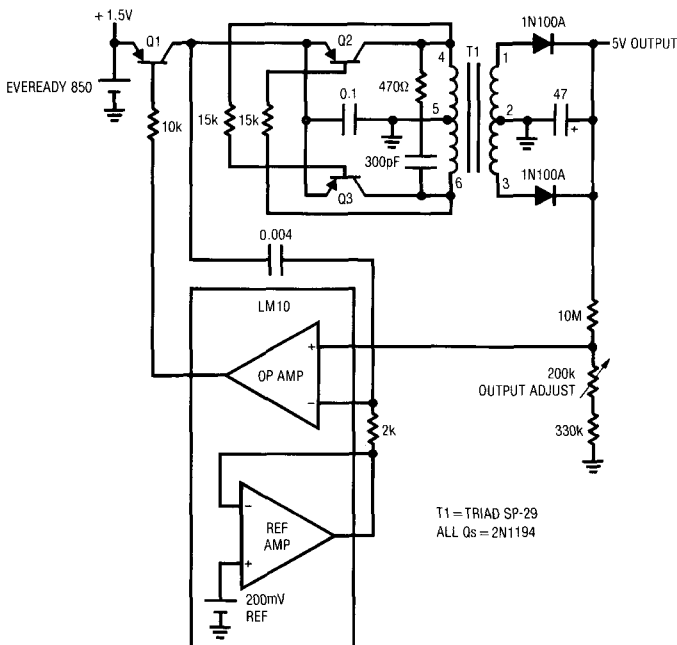


Figure 18. Single Cell Up Converter

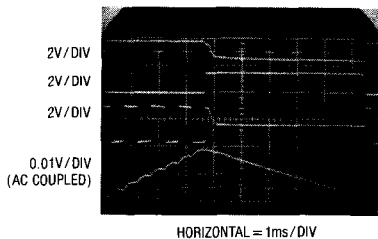


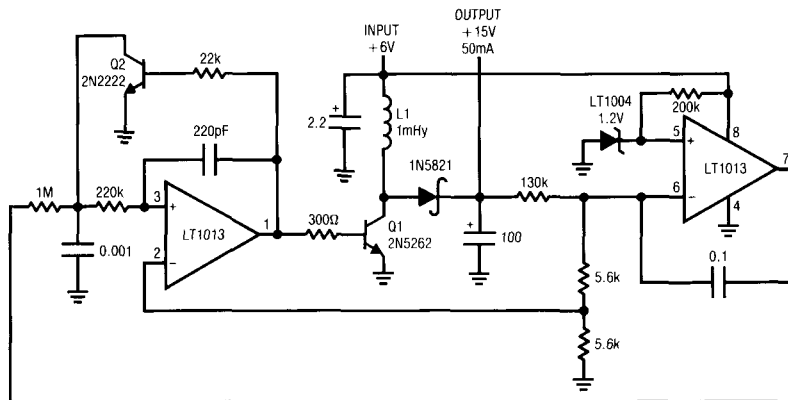
Figure 19. Figure 18's Waveforms

Regulated, 15V_{OUT}, 6V Driven Converter

Figure 20 shows a 15V output converter which delivers up to 50mA from a 6V battery. Efficiency is 78%. This flyback class converter functions by feedback-controlling the frequency of inductive flyback events. The inductor's output, rectified and filtered to DC, biases the feedback loop to establish a stable output. If the converter's output is below the loop setpoint, A2's inputs unbalance and current is fed through the 1MΩ resistor at A1. This ramps the 1000pF value positive (Trace A, Figure 21). When this ramp exceeds the 0.5V potential at A1's positive input, the amplifier switches high (Trace B). Q2 comes on, discharging the capacitor to ground. Simultaneously, regenerative feedback through the 220pF value causes a positive-going pulse at A1's positive input (Trace C), sustaining A1's positive output. Q1 comes on, allowing inductor (L1) current (Trace D) to flow. When A1's feedback pulse

decays, its output goes low, turning off Q1. Q1's collector (Trace E) is pulled high by the inductor's flyback and the energy is stored in the 100μF capacitor. The capacitor's voltage, which is the circuit output, is sampled by A2 to close a loop around the A1-Q1 combination. This loop forces A1 to oscillate at whatever frequency is required to maintain the 15V output. A1's fixed width output pulse prevents L1 from ever saturating, preventing destructive Q1 currents. The 0.1μF capacitor at A2 furnishes stable loop compensation, with the LT1004 serving as a reference. Regulation is within 0.05% over a wide range of output loads and temperature coefficient is typically 50ppm/°C.

The relatively high voltage-high power output of this circuit suits mixed linear-digital systems requirements well.



L1 = AIE—VERNITRON 24-104
78% EFFICIENCY

Figure 20. +6V-to-+15V Converter

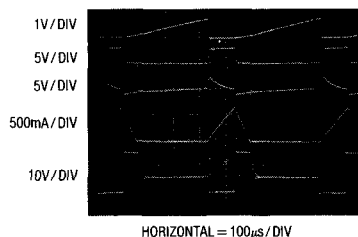


Figure 21. Figure 20's Waveforms

Application Note 8

Bipolar Output Flyback Converter

Figure 22 shows a way to obtain positive and negative 15V outputs from a single inductor. The circuit works by alternately determining which end of the inductor is allowed to flyback. The resultant positive and negative peaks are rectified, stored and regulated to produce a bipolar output. The 30kHz clock drives the 74C74 flip-flop, producing a square wave at Q1 (Trace A, Figure 23).

This waveform is fed to the 74C00 gate network. The RC networks prevent unwanted pulses due to flip-flop delay. G2 and G3's outputs appear as Traces B and C, respectively, and bias Q1 and Q2. The logic alternately turns Q1

and Q2 off when the inductor flies back. Although inductor drive current (Trace D) always flows in the same direction, the alternate switching allows positive and negative flyback action at the transistor's collectors. Trace E shows Q1's collector and Trace E is Q2's output. The ringing, due to incomplete damping, is common at low power converter outputs and is not deleterious to circuit operation. The LT1013 dual op amp and the FETs form a dual low dropout $\pm 15V$ regulator with 30mA output capability. These mirror image circuits function similarly to the one shown in Figure 11.

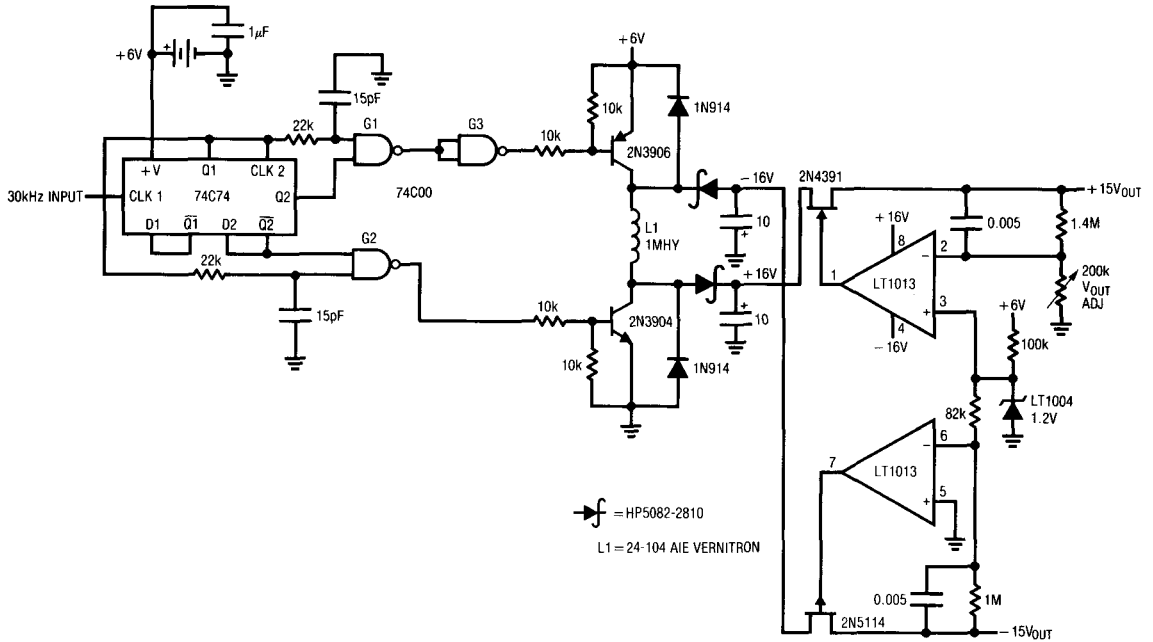


Figure 22. Single Inductor, Dual Polarity Regulator

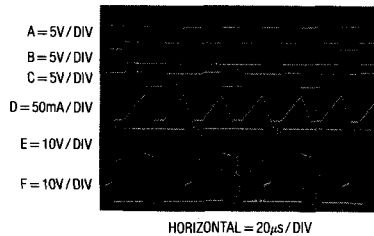


Figure 23. Figure 22's Waveforms

115VAC Sine Wave Output Converter

Not all battery converters must produce a DC output. Some battery-driven systems utilize high voltage, sine wave-driven devices such as small motors, gyros, and syncros. Deriving high voltage sine waves from a battery

supply is possible with linear techniques but efficiency is poor. Figure 24 shows a circuit which obtains 78% efficiency by sequentially switching segments of a 28V battery stack into a fixed gain, step-up voltage chopper.

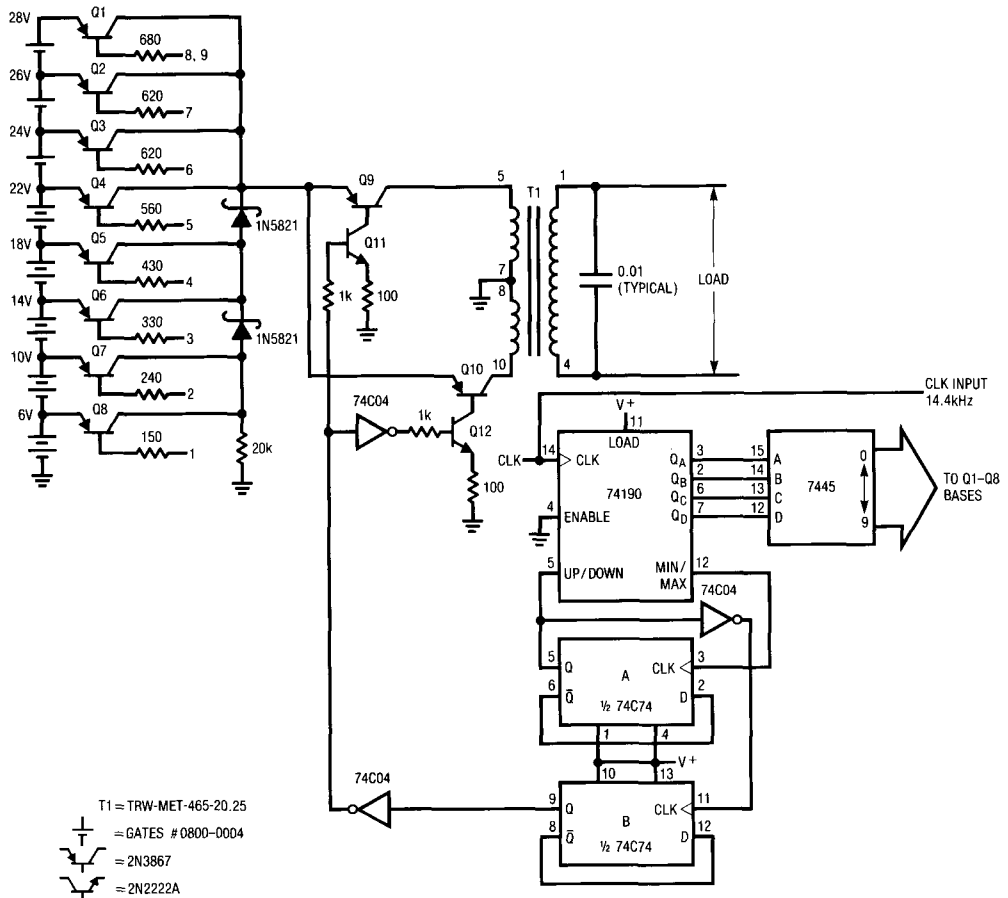


Figure 24. Sine Wave Output Converter

Application Note 8

Figure 25 illustrates the voltage presented to the chopper as a function of the sequencing logic's state. The battery stack segments are arranged to provide the best sine wave fit. Figure 26 details waveforms of operation. Trace A is the 14.4kHz clock, which feeds the logic network. The logic generates 9 discrete states, which bias Q1-Q8. These transistors sequentially place portions of the battery stack at the input of the Q9-Q10-T1 chopper. The 74C74 flip-flop "A" directs the 74190 up-down counter to reverse direction each time it reaches zero, resulting in a repetitive, rectified sine wave at the chopper input (Trace B). The diodes in the transistor's collector line prevent reverse breakdown. Q9 and Q10's bias are a

divided version of flip-flop A's output (Trace C) and T1 receives alternating drive. T1's output approximates a sine wave, (Trace D) with voltage step-up furnished by the transformer ratio. In this case, the output is 115VAC, 400Hz with a power capability of about 20W. The $0.01\mu\text{F}$ capacitor shown filters residual harmonics and may not be required for some loads. Traces E, F, and G are increased resolution representations of Traces A, B and C. They clearly show the relationship between the clock and the chopper input stepping. The dissimilar amplitude step heights are discernible, in accordance with the protocol presented in Figure 25.

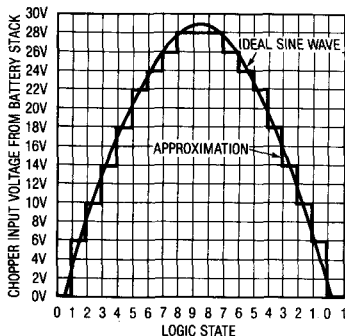


Figure 25

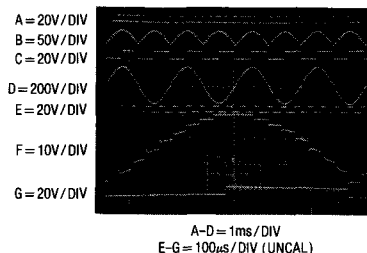


Figure 26. Figure 24's Waveforms

Application Considerations and Circuits for a New Chopper-Stabilized Op Amp

Jim Williams

A great deal of progress has been made in op amp DC characteristics. Carefully executed designs currently available provide sub-microvolt V_{OS} ΔT drift, low bias currents and open loop gains exceeding one million. Considerable design and processing advances were required to achieve these specifications. Because of this, it is interesting to note that amplifiers with even better DC specification were available in 1963 (Philbrick Researches Model SP656). Although these modular amplifiers were large and expensive ($\approx 3" \times 2" \times 1.5"$ at \$195.00 1963 dollars) by modern standards, their DC performance anticipated today's best monolithic amplifiers while using relatively primitive components. This was accomplished by employing chopper-stabilization techniques (see Box, "Choppers, Chopper-Stabilization and the LTC1052") instead of the more common DC-differential stage approach.

The chopper-stabilized approach, developed by E. A. Goldberg in 1948, uses the amplifier's input to amplitude modulate an AC carrier. This carrier, amplified and synchronously demodulated back to DC, furnishes the ampli-

fier's output. Because the DC input is translated to and amplified as an AC signal, the amplifier's DC terms have no effect on overall drift. This is the reason chopper-stabilized amplifiers are able to achieve significantly lower time and temperature drifts than classic differential types. Additionally, the AC processing of the signal aids low frequency amplifier noise performance and eliminates many of the careful design and layout procedures necessary in a classic differential approach. The most significant trade-off is increased complexity. The chopping circuitry and sampled data operation of these amplifiers require significant attention for good results. Additionally, the AC dynamics of chopper-stabilized amplifiers are complex if bandwidths greater than the chopping carrier frequency are required.

The LTC1052 is a third generation monolithic chopper-stabilized amplifier. As the table in Figure 1 shows, it is significantly better than previous monolithic chopper-stabilized amplifiers in several areas. For comparison purposes, conventional FET input and bias current compensated bipolar types are also listed. Noise has been a

PARAMETER	LTC1052 CHOPPER- STABILIZED	ICL7652 CHOPPER- STABILIZED	HA2904/5 CHOPPER- STABILIZED	AD547 FET	LM11 LOW I_B BIPOLAR	LT1012 LOW I_B BIPOLAR
$E_{OS} - 25^\circ C$	$\pm 5\mu V$	$\pm 5\mu V$	$\pm 50\mu V$	$\pm 250\mu V$	$\pm 300\mu V$	$\pm 35\mu V$
$E_{OS} \Delta T / ^\circ C$	$0.05\mu V / ^\circ C$	$0.05\mu V / ^\circ C$	$0.4\mu V / ^\circ C$	$1\mu V / ^\circ C$	$3\mu V / ^\circ C$	$1.5\mu V / ^\circ C$
Noise (1Hz BW)	$0.5\mu V_{p-p}$ Typ	$0.2\mu V_{p-p}$ Typ*	Specified as $900nV/\sqrt{Hz}$ at 10Hz**	$4\mu V_{p-p}$	$6\mu V_{p-p}$ $R_S = 100k\Omega$	$0.5\mu V_{p-p}$
Open Loop Gain	120dB	120dB (25°C)	5×10^8 Typ	2.5×10^5	2.5×10^5	3×10^5
Bias Current—25°C	30pA	30pA	150pA Typ	25pA	50pA	100pA
CMRR	120dB	110dB (25°C)	120dB	80dB	110dB	114dB
PSRR	120dB	110dB (25°C)	120dB	100dB	100dB	114dB
Input Common-Mode Range	$V^+ / - 2.3V$ $V^- / + 0V$	$V^+ / - 1.5V$ $V^- / + 0.7V$	$\pm 10V$ at $\pm 15V$ Supply	$V^+ / - 2V$ $V^- / + 3V$	$V^+ / - 0.5V$ $V^- / + 1.5V$	$V^+ / - 1.5V$ $V^- / + 1.5V$
Slew Rate	$4V/\mu s$	$0.5V/\mu s$	$2.5V/\mu s$	$3V/\mu s$	$0.3V/\mu s$	$0.1V/\mu s$
GBW	1MHz	0.45MHz	3MHz	1MHz	0.8MHz	0.8MHz

*Unable to verify by laboratory testing.
Measured at $0.7\mu V_{p-p}$.

**Measured at $5\mu V_{p-p}$ in a 1Hz bandwidth.

Figure 1

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particular concern with previous monolithic chopper designs and Figure 2 is a strip chart of the LTC1052's performance at two measurement bandwidths. Additionally, the LTC1052's input common-mode range includes V^- , making single-supply operation more practical.

Considerable attention to DC parasitics, particularly thermal EMFs, is required if the LTC1052's ultra low drift is to be fully utilized. Any connection of dissimilar metals produces a potential which varies with the junction's temperature (Seebeck effect). As temperature sensors, thermocouples exploit this phenomenon to produce useful information. In low drift amplifier circuits the effect is probably the primary source of error. Connectors, switches, relay contacts, sockets, wire, and even solder are all candidates for thermal

EMF generation. It is relatively clear that connectors and sockets can form thermal junctions. However, it is not at all obvious that junctions of wire from different manufacturers can easily generate $200\text{nV}/^\circ\text{C}$ —four times the LTC1052's drift specification! Figure 3 shows a plot obtained for such a wire junction. Even solder can become an error term at low levels, creating a junction with copper or Kovar wires or PC traces (see Figure 4).

Minimizing thermal EMF induced errors is possible if judicious attention is given to circuit board layout. In general, it is good practice to limit the number of junctions in the amplifier's input signal path. Avoid connectors, sockets, switches and other potential error sources to the extent possible. In some cases this will not be possible.

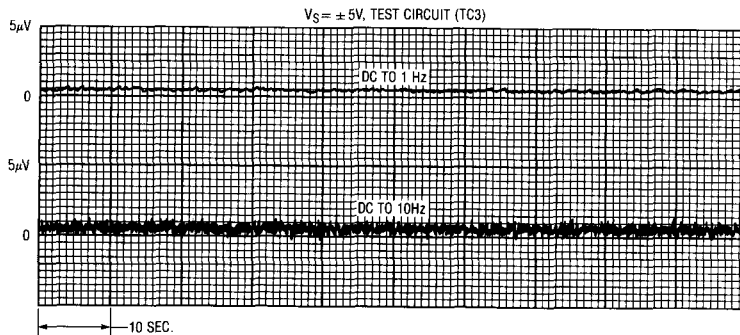


Figure 2 LTC1052 Input Noise Voltage

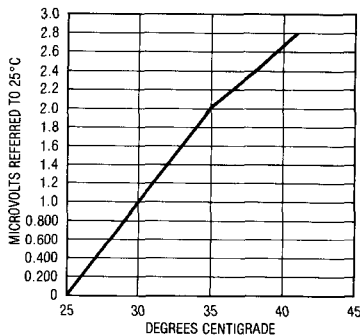


Figure 3. Thermal EMF Generated by Two Wires

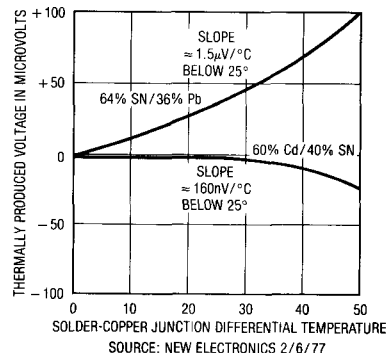


Figure 4. Solder-Copper Thermal EMFs

In these instances, attempt to balance the number and type of junctions in the amplifier inputs so that differential cancellation occurs. Doing this may involve deliberately creating and introducing junctions to offset unavoidable junctions. This practice, borrowed from standard lab procedures, can be quite effective in reducing thermal EMF originated drifts. Figure 5 shows a simple example where a nominally unnecessary resistor is included to promote such thermal balancing. For remote signal sources such as transducers, connectors may be unavoidable. In these cases choose a connector specified for relatively low thermal EMF activity and ensure a similarly balanced approach in routing signals through the connector, along the circuit board and to the amplifier. If some imbalance is unavoidable, deliberately introduce an intentional counterbalancing junction. In all cases maintain the junctions in close physical proximity, which will keep them at the same temperature. Avoid drafts and temperature gradients, which can introduce thermal imbalances and cause problems. Figure 6 shows the LTC1052 set up in a test circuit to measure its temperature stability. The lead lengths of the resistors connected to the amplifier's inputs are identical. The thermal capacity each input sees is also balanced because of the symmetrical connection of the resistors and their identical size. Thus, thermal EMF induced shifts are equal in phase and amplitude and cancellation occurs. Very slight air currents can still affect

even this arrangement. Figure 7 shows strip charts of output noise with the circuit covered by a small styrofoam cup (HANDI-KUP Company Model H8-S) and with no cover in "still" air. This data illustrates why it is often prudent to enclose the LTC1052 and its attendant components inside some form of thermal baffle.

Thermal EMFs are the most likely, but not the only, potential low level error source. Electrostatic and electromagnetic shielding may be required. Power supply transformer fields are notorious sources of errors often mistakenly attributed to amplifier DC drift and noise. A transformer's magnetic field impinging on a PC trace can easily generate microvolts across that conductor in accordance with well-known magnetic theory. The amplifier cannot distinguish between this spurious signal and the desired input. Attempts to eliminate the problem by rolling off amplifier gain with a feedback capacitor may work, but often the filtered version of the undesired pickup masquerades as an unstable DC term in the output. The most direct approach is to use shielded transformers, but careful layout may be equally effective and less costly. A circuit which requires the transformer to be close by to achieve a good quality grounding scheme may be disturbed by the transformer's magnetic field. An RF choke connected across a scope probe can determine the presence and relative intensity of transformer fields, aiding layout experimentation.

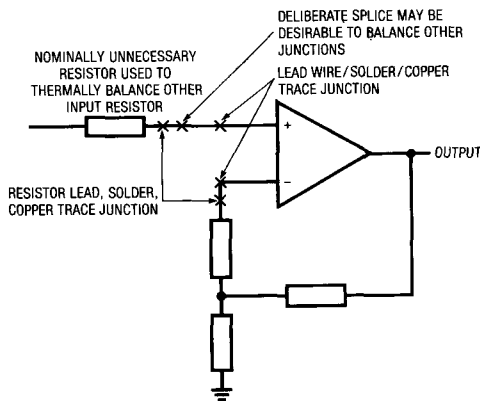


Figure 5. Typical Thermal Layout Considerations

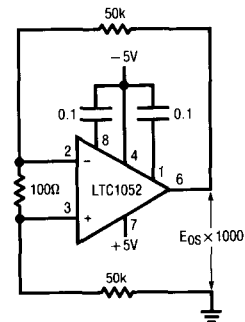


Figure 6. Recommended Drift Test Circuit

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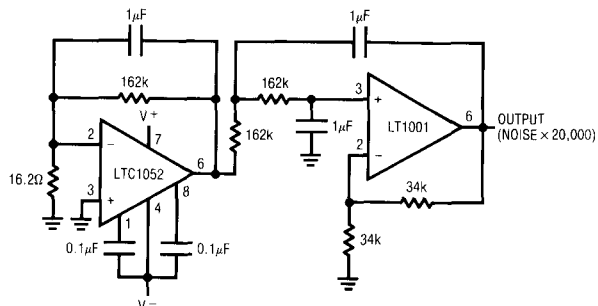
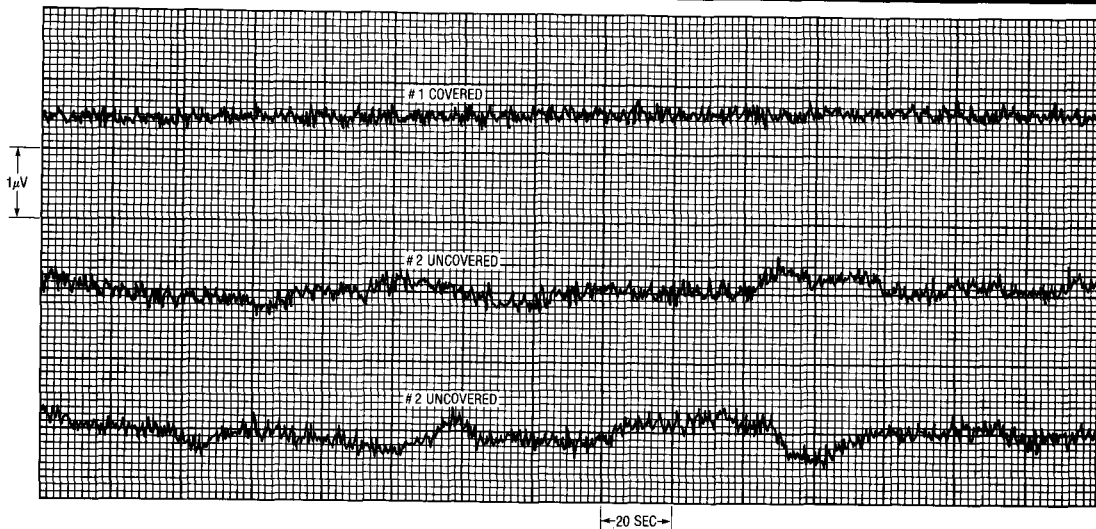


Figure 7. DC to 1Hz Noise Test Circuit

Another source of parasitic error is stray leakage current. The LTC1052's 30pA bias current allows operation from very high source impedances. In such cases it is desirable to prevent stray leakage currents from reaching the inputs. The simplest way to do this is to connect the amplifier inputs directly to the signal source via a teflon stand-off. Because the amplifier inputs never contact the PC board, stray leakage currents do not affect them. Although this approach is effective, its implementation may not be acceptable in production. Guarding is another technique to minimize board leakage effects. The guard is a PC trace completely encircling the input. This trace is driven (see Figure 8) at a potential equal to that of the input, preventing leakage to the amplifier input terminal. On PC boards, the guard should enclose the input(s) to be protected, with signal connections made directly to the amplifier input.

A final form of parasitic is one particular to all carrier-based amplifiers. If the amplifier is operating in a circuit which contains clocking or oscillation with substantial harmonic content at or near its carrier frequency (e.g., from another LTC1052), erratic operation is possible. This is particularly the case if inductors or transformers radiate magnetic fields related to the clocking or oscillation. The undesired interaction between the amplifier's chopping sequence and the externally generated AC signals may cause mixing and beat frequencies to occur, resulting in errors in the output. The LTC1052 is not particularly sensitive in this regard, but synchronizing its internal oscillator with external circuit clocking precludes this problem. The 14-pin version of the LTC1052 features a pin which allows the internal clock to be synchronized to an external signal. Input signals containing substantial AC content may also cause this problem if the AC signal

has strong spectral components related to the chopping frequency. In applications where such AC input components exist, it may be necessary to drive the LTC1052 from an external clock source at a frequency which has no harmonic relationship with the input signal. For example, a 372Hz clock frequency will prevent 60Hz input components from affecting amplifier operation.

Applications

Once alerted to the potential problems previously outlined, the engineer is prepared to design circuits around the LTC1052. The most obvious applications are at low level DC, where the low drift will improve performance over other amplifiers. More subtly, it is possible to exploit the LTC1052's low offset uncertainties to extend the dynamic

range of circuit operation. The circuits which follow demonstrate these points, using relatively straightforward examples of improvements in low level, precision performance. Additional, less obvious, circuits use the LTC1052 to stabilize and enhance the performance of a variety of functions including data converters, buffers and comparators.

Standard Grade Variable Voltage Reference

Figure 9 diagrams a standard lab grade variable voltage reference. This circuit combines a pair of LTC1052s with high grade saturated standard cells and other components to produce an extremely stable reference source. The circuit may be used to calibrate 6½ digit voltmeters, ultra high resolution data converters and other apparatus requiring high order traceability to primary standards.

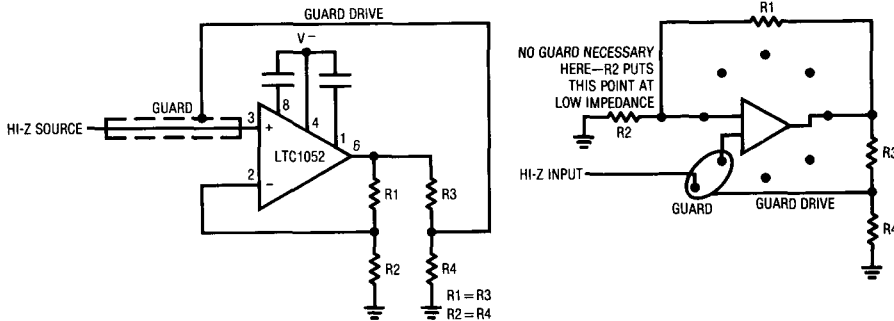


Figure 8. Guarding Technique and Typical Layout

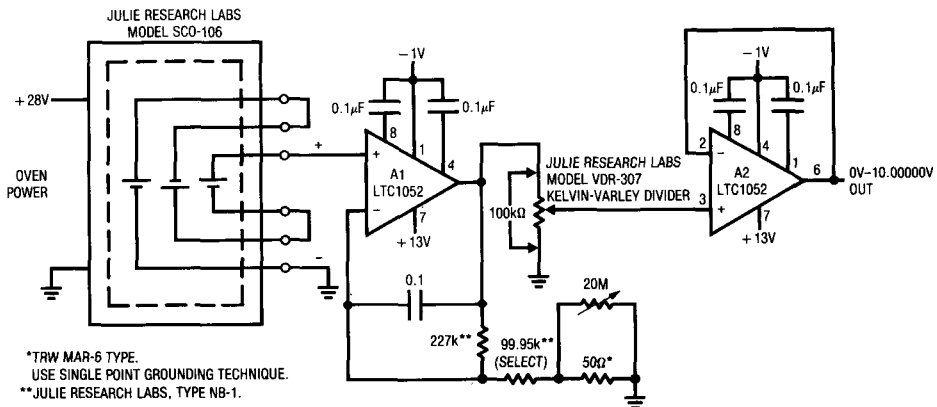


Figure 9. Standard Grade Variable Voltage Reference

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The SCO-106 saturated cells furnish a reference voltage which is buffered and amplified to precisely 10V by A1. A1's output drives a seven place settable Kelvin-Varley divider with 1ppm accuracy. A2's low bias current and high CMRR allow it to unload the divider without introducing significant error. To calibrate this circuit, adjust A1's output for exactly 10V by selecting the feedback resistor and fine trimming the 20MΩ potentiometer. A1's output should be measured with equipment having order traceability to primary NBS standards. Once calibrated, this

circuit will provide *worst-case* 0.0014% accuracy over one year's time and $\pm 5^{\circ}\text{C}$ temperature excursions. Figure 10 details error sources. Note that the amplifiers contribute only about 1.3ppm (0.00013%) of the total.

Ultra-Precision Instrumentation Amplifier

An ultra-precision instrumentation amplifier appears in Figure 11. This circuit offers greater accuracy and lower drift than any commercially available IC, hybrid or module.

SCO-106 Reference / 2ppm / Year		= 2ppm
A1 - $0.05\mu\text{V}/^{\circ}\text{C} \times \text{A} = 3 \times 5^{\circ}\text{C} = 0.75\mu\text{V}$		= 0.075ppm
A2 - $0.05\mu\text{V}/^{\circ}\text{C} \times \text{A} = 1 \times 5^{\circ}\text{C} = 0.25\mu\text{V}$		= 0.025ppm
A1 + A2 Time Drift / Year = $2\mu\text{V}$		= 0.02ppm
KVD - $0.5\text{ppm}/^{\circ}\text{C} \times 5^{\circ}\text{C} + 1\text{ppm} / \text{Year} = 3.5\text{ppm}$		= 3.5ppm
Resistors - $0.1\text{ppm}/^{\circ}\text{C} \text{ Ratio } 5^{\circ}\text{C} + 2\text{ppm} / \text{Year} = 2.5\text{ppm}$		= 2.5ppm
A2 CMRR Error	= 1ppm	1.2ppm
A2 Loading Error	= 0.2ppm	<u>9.32ppm</u>

Figure 10. Error Sources for Ultra-Precision Voltage Reference

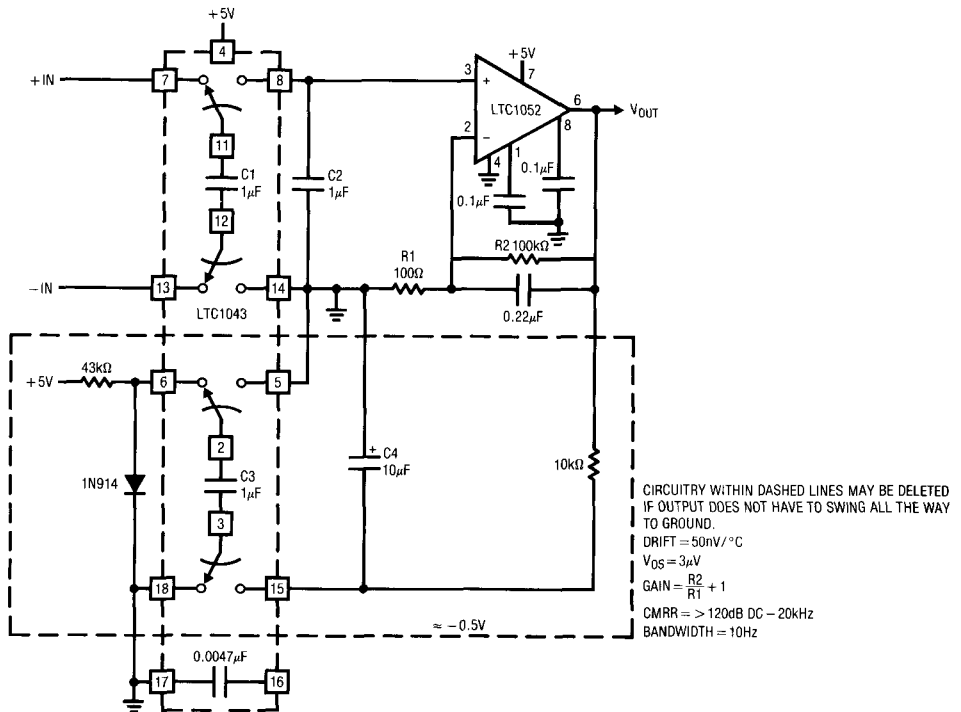


Figure 11. Ultra-Precision Instrumentation Amp

Additionally, it will run from a single 5V power supply. The LTC1043 switched-capacitor instrumentation building block provides a differential-to-single-ended transition using a flying capacitor technique. C1 alternately samples the differential input signal and charges ground referred C2 with this information. The LTC1052 measures the voltage across C2 and provides the circuit's output. Gain is set by the ratio of the amplifier's feedback resistors. Normally, the LTC1052's output stage can swing within 15mV of ground. If operation all the way to zero is required, the circuit shown in dashed lines may be employed. This configuration uses the remaining LTC1043 section to generate a small negative voltage by inverting the diode drop. This potential drives the 10k Ω pull-down resistor, forcing the LTC1052's output into class A operation for voltages near zero. Note that the circuit's switched-capacitor front end forms a sampled data filter allowing common-mode rejection ratio to remain high, even with increasing frequency. The 0.0047 μ F unit sets front end switching frequency at a few hundred hertz. The chart details circuit performance.

High Performance Isolation Amplifier

Instrumentation amplifiers cannot be used to signal condition all differential signals. In factory and process control environments, severe grounding and common-mode voltages often mandate the requirement for isolation amplifiers. Isolation amplifiers feature inputs which are galvanically isolated from their output and power connections. This allows the amplifier to ignore the effects of ground loops and operate at input common-mode voltages many times the power supply voltage. Implementing a precise, low drift isolation amplifier is not easy, and commercial units are quite expensive. Figure 12 shows a circuit with 0.03% transfer accuracy and the 50nV/ $^{\circ}$ C input drift of the LTC1052. As shown, the circuit provides a gain of 1000 and will operate at 250V input common-mode levels.

The circuit works by amplitude modulating the output of a signal conditioning amplifier through a transformer. A synchronous demodulator filter reconstructs the amplifier's original output and furnishes the circuit's output. A separate oscillator and transformer provide power to the amplifier, preserving galvanic isolation between the circuit's input and output ports.

Three 74C04 gates and their associated components form an oscillator which provides complementary drive to Q5 and Q6. These devices energize L1, which generates floating power on the input side of the dashed barrier shown. Simultaneously, the oscillator provides slightly delayed complementary drive to the Q1–Q2 FET switches via the 330 Ω –100pF network and the additional inverters. The floating power produced by L1 is rectified and filtered and drives the LTC1052 (A1) via the zener drops of the transistors. The \pm 15V floating power is brought out so it can be used to power transducers or other loads. Interaction between the transformer's chopping carrier and A1's internal oscillator is avoided by synchronizing the amplifier to the carrier via the two decade counters. Q3 and Q4, driven by opposing phase carrier signals derived from L1, chop A1's output into L2. This modulated signal information is received at L2's other winding. Because Q1 and Q2 are driven synchronously with Q3 and Q4, they demodulate the amplitude and phase (e.g., plus or minus polarity) information in the carrier. The 330 Ω –100pF network compensates for the slight skew in switch drive signals on opposing sides of L2, minimizing gain error. L2's output (pin 2) is RC filtered at A2, which also provides the circuit's output. Slight switching errors in the modulator-demodulator result in very small gain differences between positive and negative outputs at pin 2 of L2. This effect is compensated by the diode-resistor network in A2's output, which provides a small decrease in gain for negative outputs.

Figure 13 shows the response of the isolation amplifier to a sine wave input. For this test, the floating common and circuit grounds are tied together. Trace A is the input applied to A1. Trace B, taken at pin 4 of L2, shows A1's amplified output being modulated into the transformer. Trace C, obtained at pin 1 of L2, depicts the received modulated waveform as it is synchronously demodulated. The filtered and final output of A2 appears in Trace D. The 25kHz carrier limits full power bandwidth of this circuit to about 500Hz, adequate for process control and transducer applications. The transformers used set a voltage breakdown specification of 250V, although higher levels are achievable with different devices. As shown, circuit gain is 1000, allowing amplification of a \pm 5mV signal riding on 250V of common-mode to a \pm 5V output. Gain accuracy is 0.03% with a gain drift of typically 50ppm/ $^{\circ}$ C. Input referred drift is set by the LTC1052's 50nV/ $^{\circ}$ C specification.

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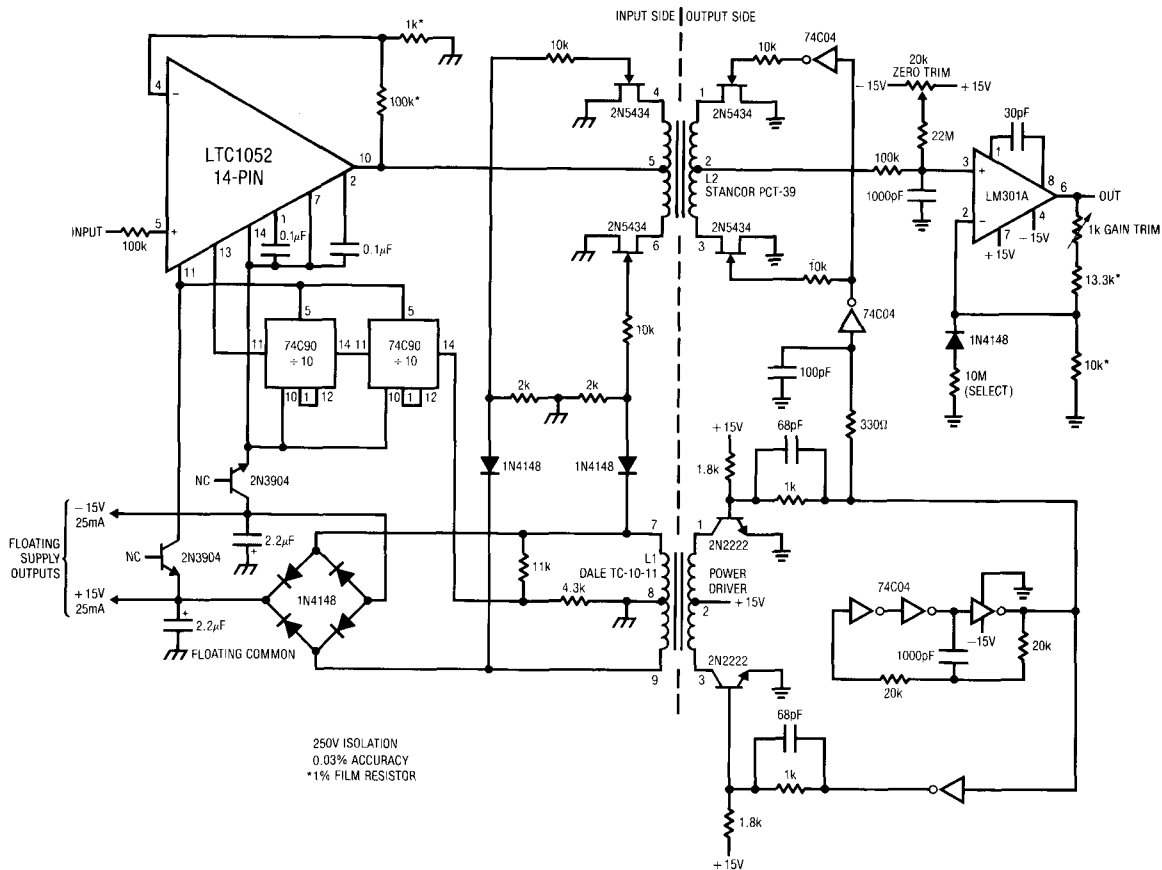


Figure 12. Precision Isolation Amplifier

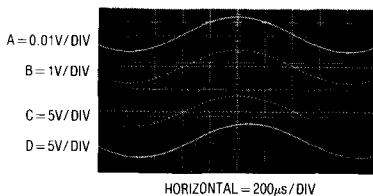


Figure 13. Waveforms for Isolation Amplifier

To trim this circuit, tie A1's input to floating common and adjust the zero trim for 0V output. Next, connect A1's input to a +5mV source and adjust the gain trim at A2 for exactly $+5.000V_{OUT}$. Finally, connect A1's input to a -5mV source and select the 10M Ω value in A2's feedback path for a -5.000V output reading. Repeat this procedure until all three points are fixed.

Stabilized, Low Input Capacitance Buffer (FET Probe)

A recurring requirement in automatic semiconductor testing and probing equipment is for a highly stable unity-gain buffer amplifier with low input capacitance. Such an amplifier is also useful for other circuit chores where it is desirable to accurately monitor a point without introducing any significant AC or DC loading terms. Figure 14 shows such a circuit. Q1 and Q2 constitute a simple, high speed FET input buffer. Q1 functions as a source follower, with the Q2 current source load setting the drain-source

channel current. The LT1010 buffer provides output drive capability for cables or whatever load is required. Normally, this open loop configuration would be quite drifty because there is no DC feedback. The LTC1052 contributes this function to stabilize the circuit. It does this by comparing the filtered circuit output to a similarly filtered version of the input signal. The amplified difference between these signals is used to set Q2's bias, and hence Q1's channel current. This forces Q1's V_{GS} to whatever voltage is required to match the circuit's input and output potentials. The diode in Q1's source line ensures that the gate never forward biases and the 2000pF capacitor at A1 provides stable loop compensation. The RC network in A1's output prevents it from seeing high speed edges coupled through Q2's collector-base junction. A2's output is also fed back to the shield around Q1's gate lead, bootstrapping the circuit's effective input capacitance down to less than 1pF.

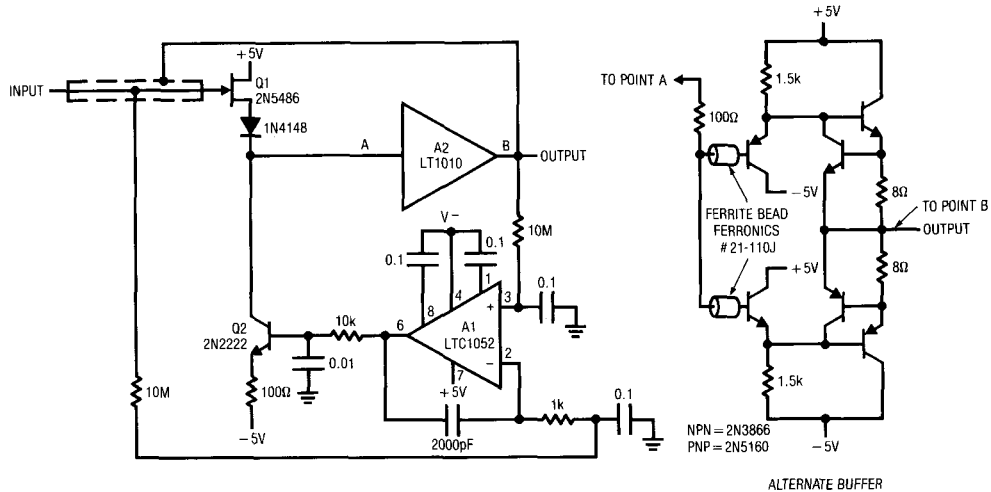


Figure 14. Fast, Stabilized FET Buffer

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The LT1010's 15MHz bandwidth and 100V/ μ s slew rate, combined with its 150mA output, are fast enough for most circuits. For very fast requirements, the alternate discrete component buffer shown will be useful. Although its output is current limited at 75mA, the GHz range transistors employed provide exceptionally wide bandwidth, fast slewing and very little delay. Figure 15 shows the LTC1052 stabilized buffer circuit's response using the discrete stage. Response is clean and quick, with delay inside 4ns. Note that rise time is limited by the pulse generator and not the circuit. For either stage, offset is set by the LTC1052 at 3 μ V, with gain about 0.95. It is worth noting that this circuit performs the same function as commercial FET probes in the \$1,000.00 range.

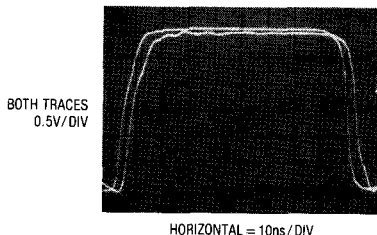


Figure 15. Stabilized Buffer Delay

Chopper-Stabilized Comparator

It is often desirable to use a reasonably fast voltage comparator with low input offset drift. Such a device is useful in high resolution A \rightarrow D converters, crossing detectors and anywhere else a precise, stable, high speed comparison must be made. Unfortunately, obtaining reasonable comparator speed and low input drift in a design is difficult and monolithic comparators must be constructed around this trade-off. Figure 16 shows a way to use the LTC1052 to eliminate offset and drift in a comparator without sacrificing speed or differential input versatility. This circuit is applicable only in situations where some dead time is available for zeroing action to occur.

The circuit functions by periodically shorting the comparator inputs together and forcing the comparator into its linear region via its offset pins. The voltage at the offset

pins required to do this is stored. When the comparator inputs are returned to their normal states, the stored voltage is maintained at the comparator's offset pins, effectively controlling the device's offset. Periodic updating ensures long term stability of the correction. In this circuit, A1 is the stabilizing amplifier for C1. C1's inputs are controlled by a dual DPDT switch section furnished by the LTC1043. When LTC1043 pin 16 is high, pins 12 and 11 are connected to pins 13 and 7, respectively. Pin 3, at C1's output, is connected to pin 18. Under these conditions, A1 is effectively connected in a negative feedback loop between C1's output and its offset pin 5 (see detail of LT1011 input stage in Figure 16). This forces C1 into its linear region and its output oscillates at a high frequency between the rail voltages. A1, connected as a low frequency integrator, filters this action, compares its DC equivalent value to ground (its positive input potential) and drives C1's offsets to zero. When pin 16 of the LTC1043 goes low, all switch states reverse and C1's inputs are free to compare the signals present at LTC1043 pins 14 and 8 in the normal fashion. During this interval, A1's output remains fixed at the voltage stored in its feedback capacitor. A1's low bias current allows long durations between correction cycles—periods of seconds are practical—while maintaining effective comparator offset well within 5 μ V with negligible temperature drift.

Figure 17 shows the circuit's response to a sine wave (Trace A) applied to C1's positive input at LTC1043 pin 14. C1's negative input, LTC1043 pin 8, is grounded. With the circuit's zero command low (Trace B), C1's output (Trace C) responds in the normal fashion. During this period, the status output (Trace D) is low, indicating C1 is in its normal mode. When the zero command occurs (Trace B, just to the right-center of the screen), C1 is forced into its linear region, where it oscillates. During this time, A1 updates the correction voltage stored in its feedback capacitor. When the zero command pulse falls, normal comparator action is seen to resume. Note that the circuit's status output reflects the true operating mode of the circuit, because its timing includes the 50ns delay of the LTC1043 switch. For this reason the status output, and not the zero command, should be used to indicate the circuit's actual operating state.

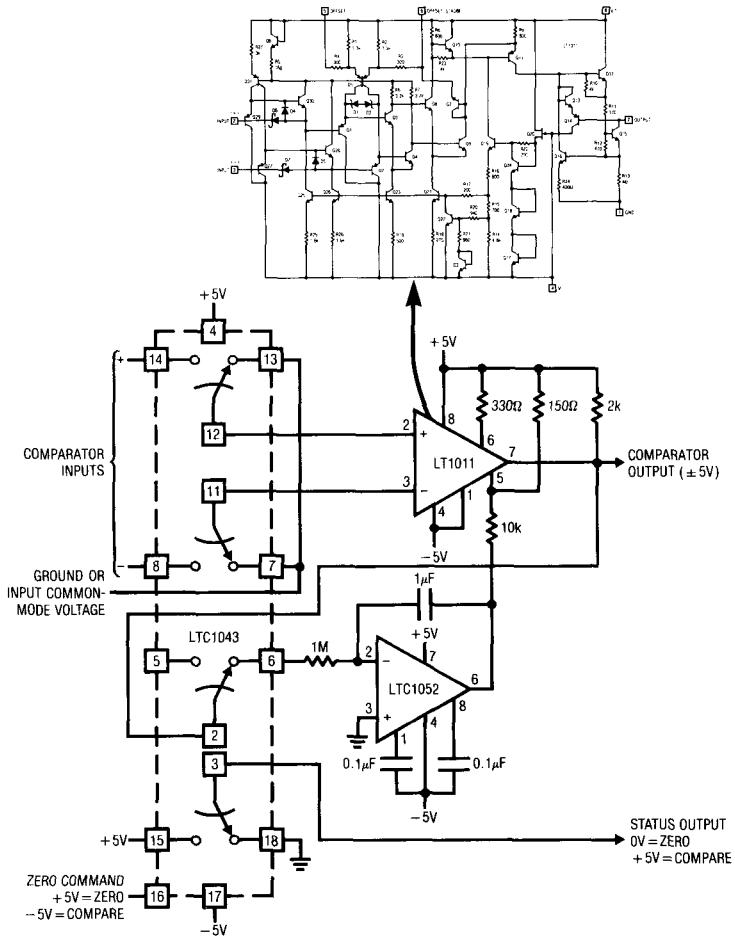


Figure 16. Offset Stabilized Comparator

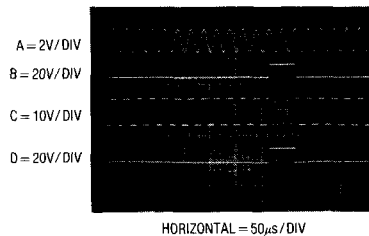


Figure 17. Stabilized Comparator Waveforms

Stabilized Data Converter

Amplifiers and comparators are not the only elements which can benefit from chopper-stabilization by the LTC1052. Figure 18 shows a way to offset-stabilize a data converter, thereby doubling its dynamic range of operation, eliminating the necessity for an offset trim and reducing zero drift to negligible levels. In this circuit, the LTC1052 corrects for offset deficiencies in the AD650 V → F converter. Although specified for 1MHz full-scale operation, this device's 4mV input offset limits untrimmed dynamic range of operation to only 3½ decades of output frequency. Under normal operating conditions, the AD650's positive input is grounded and its negative input is driven via the resistor string shown. Obtaining more than 3½ decades of operation requires an offset trim at pins 13 and 14. Even after trimming, the input amplifier's $30\mu\text{V}/^\circ\text{C}$ drift contributes a $3\text{Hz}/^\circ\text{C}$ zero point error. The LTC1052

corrects these problems by measuring the offset voltage at the circuit's summing node, comparing it to ground and driving the AD650 positive input (normally grounded in the manufacturer's recommended circuit configuration) with the appropriate stabilizing correction voltage. The dual FETs eliminate bias current caused errors. The LTC1052's integrator configuration keeps its gain at low frequency and DC, preserving the AD650's fast dynamic response while eliminating its offset errors. The divider network in the LTC1052's output is scaled to allow enough correction range to zero the AD650's offsets without causing overdrive during start-up and transients. With this scheme in use, the circuit does not require any zero trim to achieve full 6 decade operation. To calibrate, apply 10V and trim the output for exactly 1MHz.

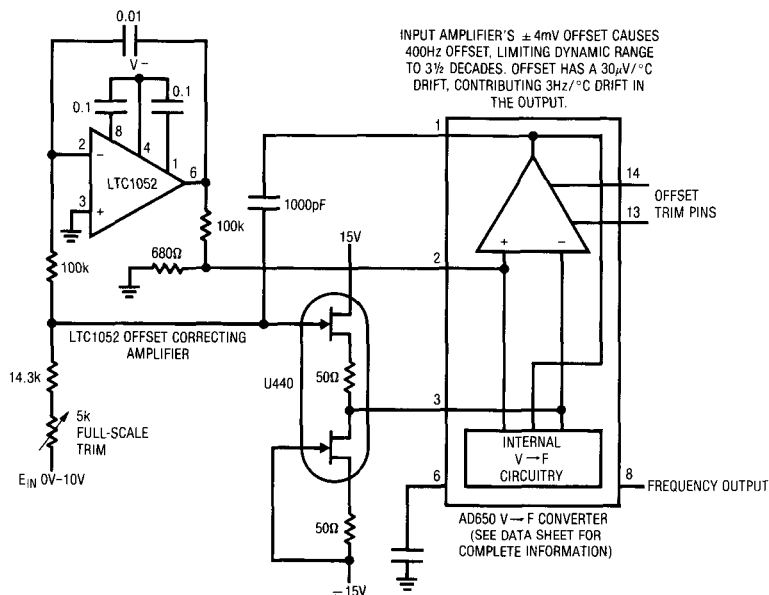


Figure 18. Offset Stabilizing a V → F Converter

Wide Range V → F Converter

Figure 19 shows another stabilized V → F converter. It features 1Hz–1.25MHz operation, 0.05% linearity, and a temperature coefficient of typically 20ppm/°C, all substantially better than Figure 18's circuit. Additionally, it is less expensive and runs from a single 5V supply. Trade-offs include slower step response and a larger component

count. This circuit uses a charge feedback scheme to allow the LTC1052 to close a loop around the entire V → F converter, instead of simply controlling offset. This approach enhances linearity and stability but introduces the loop's settling time into the overall V → F step response characteristic. Figure 20 shows waveforms of operation.

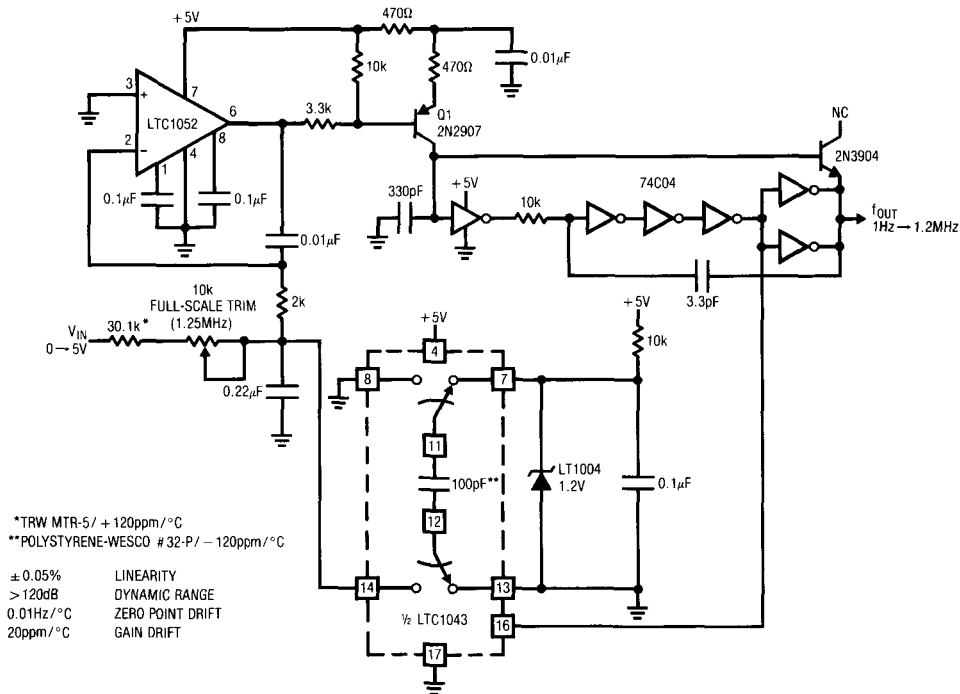


Figure 19. 1Hz-1.25MHz Voltage-to-Frequency Converter

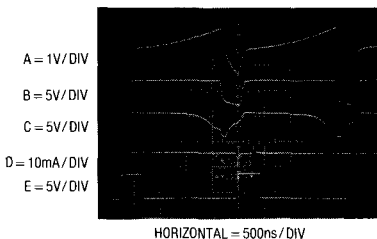


Figure 20. V → F Waveforms

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A positive input voltage directs A1's output to go negative, biasing the Q1 current source. Q1's collector puts current into the 330pF capacitor, causing it to rise in voltage (Trace A, Figure 20). The low input current CMOS inverter changes state when the ramp crosses $\frac{1}{2}$ of the supply voltage. This causes all of the inverters to switch. The two paralleled inverters at the end of the chain go low (Trace B), simultaneously supplying positive feedback at the 10k-3.3pF junction (Trace C) and forcing the 330pF capacitor to a lower voltage by removing current from it (Trace D) via the diode connected 2N3904. During the ramping interval, LTC1043 switch pins 11 and 12 are connected to pins 8 and 14 discharging the 100pF capacitor into pin 14. When the output inverters go low, the LTC1043's control pin (16) also switches, placing the charged 100pF capacitor across pins 7 and 13. Thus, each time the inverters switch, a fixed quantity of charge is dispensed into the 2k-0.22 μ F-10k potentiometer junction ($Q = CV$). The LTC1043's switching is arranged so that this charge is of opposite polarity to the positive input current. The 0.22 μ F capacitor integrates the discrete charge dumps to DC. A1 servo controls the Q1 inverter oscillator to run at whatever frequency is required to force its negative input to 0V. In this manner, drift and non-linear response in the Q1 inverter oscillator are compensated by A1's closed loop control. The circuit's frequency output is delivered by another LTC1043 section (Trace E).

Several factors contribute to this circuit's performance. The low input current of the CMOS inverter, combined with the low leakage of the 2N3904 base-emitter diode and the circuit's servo action, allows operation to well below 1Hz, despite the small 330pF integrating capacitor. In the lower frequency ranges, currents at this junction are small and board leakage can cause jitter. A clean board will work well, but the best approach is to mount the capacitor, Q1's collector, the inverter input and the transistor base connection on a teflon stand-off, using short connections. The resistor and capacitor specified in the figure, both gain terms, have opposing temperature coefficients, aiding gain drift performance. The LTC1052's low offset eliminates the need for a zero trim while preserving the circuit's >120dB dynamic range of operation. To trim the circuit, apply +5.000V and adjust the 1.25MHz trim for 1.2500MHz out.

1Hz-30MHz V \rightarrow F Converter

Although Figure 19's circuit is impressive, it still does not tax the LTC1052's dynamic range of operation. Figure 21 shows a highly modified version of Figure 19. It has a 1Hz to 30MHz output (150dB dynamic range) for a 0V to 3V input. This is by far the widest dynamic range and highest operating frequency of any V \rightarrow F discussed in the literature at the time of writing*. It is a good application of the extremely wide signal processing range afforded by the LTC1052. The circuit maintains 0.08% linearity over its entire $7\frac{1}{3}$ decade range with a full-scale drift of about 20ppm/ $^{\circ}$ C. Zero point error is 0.3Hz/ $^{\circ}$ C and is directly related to the LTC1052's 50nV/ $^{\circ}$ C drift specification.

To get the additional bandwidth, Figure 19's CMOS inverters are replaced with a fast JFET buffer driving a Schottky TTL Schmitt trigger. The Schottky diode prevents the Schmitt trigger from ever seeing negative voltage at its input. The diode connected 2N3904 is retained for resetting the capacitor, which has a smaller value. Figure 19's positive AC feedback, with its attendant recovery time constant, is avoided in this circuit. Instead, the Schmitt's input voltage hysteresis provides the limits which the oscillator runs between. The 30MHz full-scale output is much faster than the LTC1043 can accept, so the digital divider stages are used to reduce the feedback frequency signal by a factor of 20. Remaining Schmitt sections furnish complementary outputs. Good high frequency wiring techniques should be used when constructing the current source-buffer-Schmitt trigger sections.

Figure 22 shows the key waveforms with the circuit loafing at 20MHz. Trace A is the Schmitt trigger input, which is seen to ramp between two voltage limits, while Trace B is the Schmitt output. The closed loop approach results in very low output jitter and noise over the entire 150dB operating range. Figure 23 plots this, showing frequency jitter versus output frequency. Jitter does not rise above 0.01% until 20kHz, which is only 0.05% of scale. Even at 1ppm of scale (30Hz), jitter is still about 1%, finally rising to 10% at 1Hz (0.00003% of full-scale). As V \rightarrow F operating frequency decreases toward the LTC1052's feedback loop roll-off, the loop dominates the jitter characteristic. In the high frequency ranges the loop

*1Hz-100MHz circuit is under development and will be discussed in AN-14, "Designs for High Performance V \rightarrow F Converters."

poles are not a factor and current source and Schmitt trigger switching noise dominate. As with Figure 19's circuit, the feedback loop slows step response. Figure 24 shows this, with a full-scale input step requiring almost

50ms to settle. To trim this circuit, ground the input and adjust the 1Hz trim until oscillation just starts. Next, apply 3.000V and set the 30MHz trim for a 30.00MHz output. Repeat this procedure until both points are fixed.

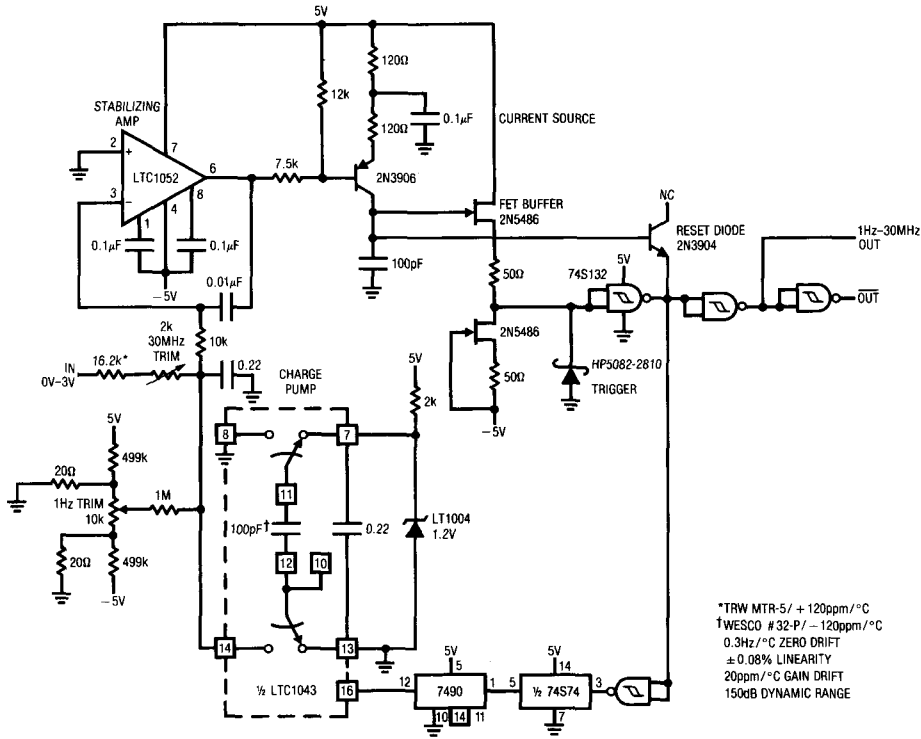


Figure 21. 1Hz-30MHz V→F Converter

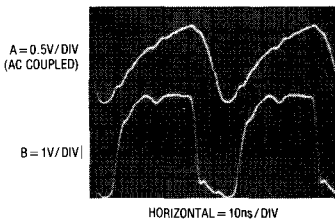


Figure 22. Fast V→F Ramp-Reset Detail

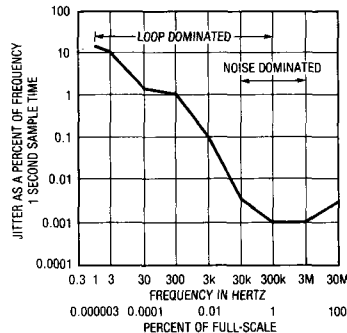


Figure 23

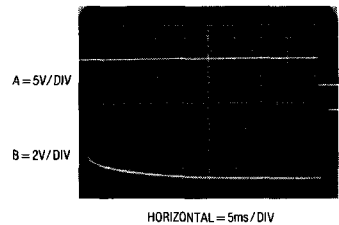


Figure 24. Fast V→F Step Response

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16-Bit A → D Converter

V → F converters are not the only types of data converters which can benefit from the LTC1052's performance. Figure 25 shows a 16-bit A → D converter (overrange to 100,000 counts is provided).

The A → D converter, made up of A2, a flip-flop, some gates and a current sink, is based on a current balancing technique. Once again, the chopper-stabilized LTC1052's 50nV/°C input drift is required to eliminate offset errors in the A → D. Figure 26 details key A → D waveforms. Assume the flip-flop's Q output (Trace B) is low, connecting LTC1043 pins 3 and 18. The current sink switch directs its output to ground.

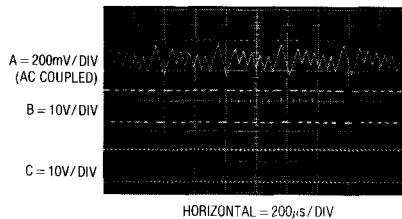


Figure 26. 16-Bit A → D Waveforms

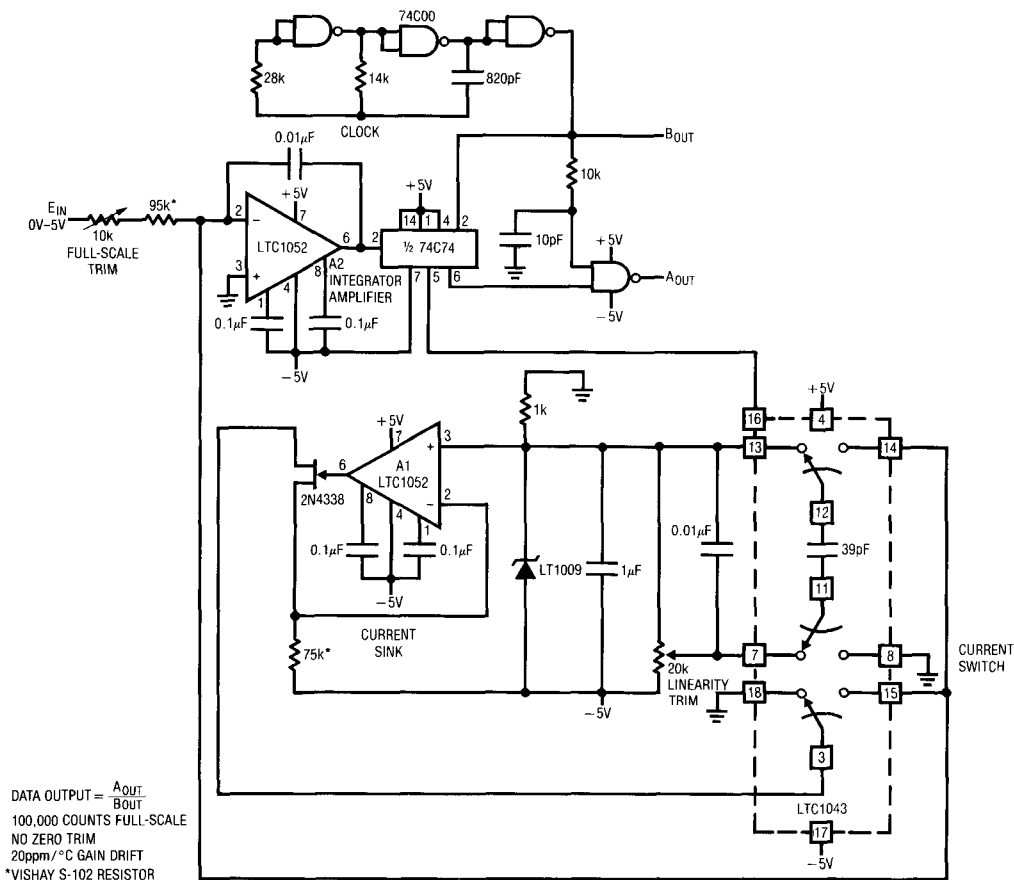


Figure 25. 16-Bit A → D Converter

Under these conditions, the only current into A2's summing point is from the input via the 95kΩ resistor. This positive current forces A2's output (Trace A, Figure 26) to integrate in a negative direction. The negative ramp continues and finally passes the 74C74 flip-flop's switching threshold. At the next clock pulse (clock is Trace C), the flip-flop changes state (Trace B), causing the LTC1043 switch positions to reverse. Pin 3 connects to pin 15, allowing the current sink to bias A2's summing point.

This results in a quickly rising, precise current flow out of A2's summing point. This current, scaled to be greater than the maximum input derived current, forces A2's output movement to reverse and integrate in the positive direction. At the first clock pulse after A2's output has crossed the flip-flop's triggering threshold, switching occurs and the entire cycle repeats. Because the reference current is fixed, the flip-flop's duty cycle is solely a function of the input signal current into A2's summing point. The flip-flop's output gates the clock, producing the "frequency output A" output. The 10k-10pF RC slightly delays the clock signal, eliminating spurious output pulses due to flip-flop delay. The circuit's data output, the ratio of output A to the clock frequency, may be extracted with counters. Because the output is expressed as a ratio, clock frequency stability is unimportant.

Slight parasitic charge pumping at the current switch introduces an error term which varies with loop operating frequency. This effect will cause a small nonlinearity in the A → D's transfer function unless compensated. The

remaining LTC1043 sections accomplish this by inverting the reference and returning a very small, compensatory charge to the current sink output each time circuit switching occurs. The charge delivered is scaled by the linearity trim to cancel the parasitic term. To calibrate this circuit, apply 5.00000V and adjust the full-scale trim for 100,000 counts out. Next, set the input to 1.25000V and adjust the linearity trim for 25,000 counts out. Repeat this procedure until both points are fixed. Converter accuracy is ± 1 count with a temperature coefficient of typically 15ppm/°C. Better TC is possible by employing a more stable reference. The high offset stability of the LTC1052 at A2 eliminates zero errors and trimming.

Simple Remote Thermometer

Although many remote thermometer circuits have appeared, few allow the temperature transducer's output to be directly transmitted over an unshielded wire. The relatively high output impedance of most temperature transducers makes their outputs sensitive to noise on the line and shielding is required. The low offset drift of the LTC1052 permits the circuit of Figure 27, which offers one solution to this problem. Here, the low output impedance of a closed loop op amp gives ideal line-noise immunity, while the op amp's offset voltage drift provides a temperature sensor. Using the op amp in this way requires no external components and has the additional advantages of a hermetic package and unit-to-unit mechanical uniformity if replacement is ever required.

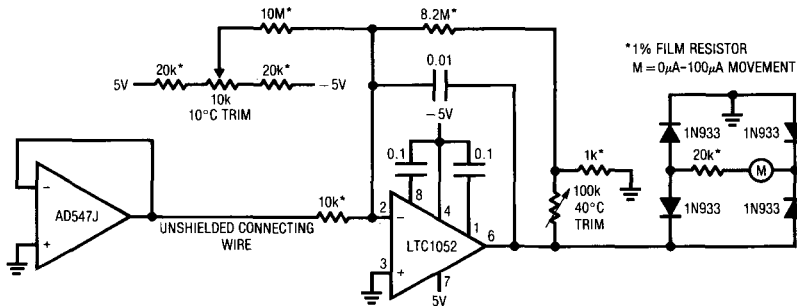


Figure 27. High Noise Rejection Thermometer

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The op amp's offset drift is amplified to drive the meter by the LTC1052. The diode bridge connection allows either positive or negative op amp temperature sensor offsets to interface directly with the circuit. In this case, the circuit is arranged for a +10°C to +40°C output, although other ranges are easily accommodated. To calibrate this circuit, subject the op amp sensor to a +10°C environment and adjust the 10°C trim for an appropriate meter indication. Next, place the op amp sensor in a +40°C environment and trim the 40°C adjustment for the proper reading. Repeat this procedure until both points are fixed. Once calibrated, this circuit will typically provide accuracy within $\pm 2^\circ\text{C}$, even in high noise environments.

Output Stages

In some circumstances it may be required to obtain more output current or swing from the LTC1052 than it can provide. The CMOS output stage cannot provide the current

levels of bipolar op amps. Additionally, it may be necessary to run the device off $\pm 15\text{V}$ supplies and to obtain increased voltage and current outputs. Figure 28 parallels a package of CMOS inverters to obtain 10mA–20mA output current capability. The inversion in the loop requires the feedback connection to go to the amplifier's positive input. The RC damper eliminates oscillation in the inverter stage, which is running in its linear region. The local capacitive feedback at the amplifier gives loop compensation. Figure 29 shows a way to run the LTC1052 from +15V supplies while obtaining the increased current and voltage output capabilities of the LT318A amplifier. The transistors run in zener mode, dropping the supply to about $\pm 7\text{V}$ at the LTC1052. The LT318A serves as an output stage with a voltage gain of 4. The output swing is that of the LT318A, typically, $\pm 13\text{V}$ into $2\text{k}\Omega$ with a short circuit current of 20mA. This circuit is dynamically stable at any gain in either the inverting or noninverting configuration, although the LTC1052's input common-mode range (-7V to $+5\text{V}$ with the $\pm 15\text{V}$ power supply used) must not be exceeded.

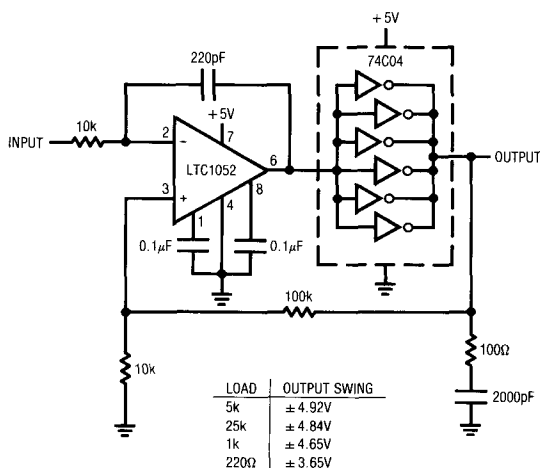


Figure 28. Increasing Output Current

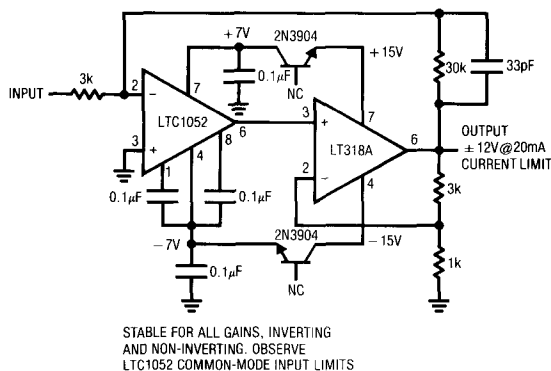


Figure 29. Increasing Output Current and Voltage ($V_{\text{SUPPLY}} = \pm 15\text{V}$)

Box Section—Choppers.**Chopper-Stabilization and the LTC1052**

All chopper-stabilized amplifiers achieve high DC stability by converting the DC input into an AC signal. An AC gain stage amplifies this signal. After amplification it is converted back to DC and presented as the amplifier's output. Figure B1 shows a conceptual chopper amplifier.

The AC amplifier's input is alternately switched between the signal input and the feedback divider network. The AC amplifier's output amplitude represents the difference between the feedback signal and the circuit's input. This output is converted back to DC by a phase sensitive demodulator composed of a second switch, synchronously driven with the input switch. The output integrator stage smooths the switch output to DC and presents the final output. Drifts in the output integrator stage are of little consequence because they are preceded by the AC gain stage. The DC drifts in the AC stage are also irrelevant because they are isolated from the rest of the amplifier by the coupling capacitors. Overall DC gain is extremely high, being the product of the gains of the AC stage and the DC gain of the integrator. Although this approach easily yields drifts of $100\text{ nV}/^\circ\text{C}$ and open loop gains of 100 million, there are some drawbacks. The amplifier has a single-ended, non-inverting input and cannot accept differential signals without additional circuitry added at the front end. Also, the carrier-based approach constitutes a sampled data system and overall amplifier bandwidth is limited to a small fraction of the carrier frequency. Carrier frequency, in turn, is restricted by AC

amplifier gain-phase limitations and errors induced by switch response time. Maintaining good DC performance involves keeping the effects of these considerations small and carrier frequencies are usually in the low kilohertz range, dictating low overall bandwidth.

The classic chopper-stabilized amplifier solves the chopper amplifier's low bandwidth problem. It uses a parallel path approach (Figure B2) to provide wider bandwidth while maintaining good DC characteristics. The stabilizing amplifier, a chopper type, biases the fast amplifier's positive terminal to force the summing point to zero. Fast signals directly drive the AC amplifier, while slow ones are handled by the stabilizing chopper amplifier. The low frequency cut-off of the fast amplifier must coincide with the high frequency roll-off of the stabilizing amplifier to achieve smooth overall gain-frequency characteristics. With proper design, the chopper-stabilized approach yields bandwidths of several megahertz with the low drift characteristic of the chopper amplifier. Unfortunately, because the stabilizing amplifier controls the fast amplifier's positive terminal, the classic chopper-stabilized approach is restricted to inverting operation only.

The LTC1052 uses a different approach which permits full differential input operation, good bandwidth and retains ultra-low drift. It relies on an auto-zero technique.

During the LTC1052's auto-zero cycle, the inputs are shorted together and a feedback path is closed around

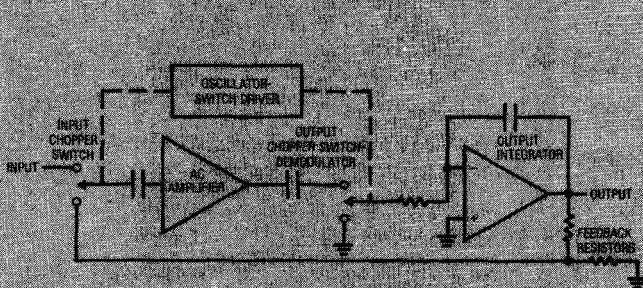


Figure B1. Chopper Amplifier

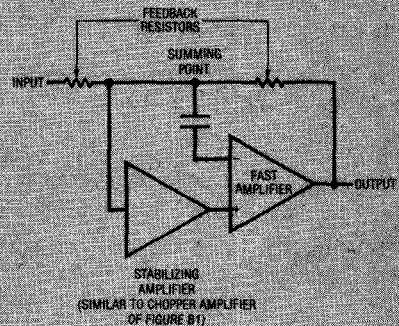


Figure B2. Classic Chopper-Stabilized Amp

Application Note 9

the input stage to null its offset. Switch S2 (Figure B3) and capacitor C_{EXTA} act as a sample and hold to store the nulling voltage during the sampling cycle.

In the sampling cycle, the now almost ideal amplifier is used to amplify the differential input voltage. Switch S2 connects the amplified input voltage to C_{EXTB} and the output gain stage. C_{EXTB} and S2 act as a sample and hold to store the amplified input signal during the auto-zero cycle. By switching between these two states at a frequency much higher than the signal frequency, a continuous output results.

Notice that during the auto-zero cycle the inputs are not only shorted together, but are also shorted to the negative input. This forces nulling with the common-mode voltage present. The same argument applies to power supply variations and accounts for the extremely good CMRR and PSRR specifications on the LTC1052.

The complete amplifier contains stabilizing elements, feed-forward for high frequency signals, and anti-aliasing circuitry, but the superior DC performance is completely described by this simple loop.

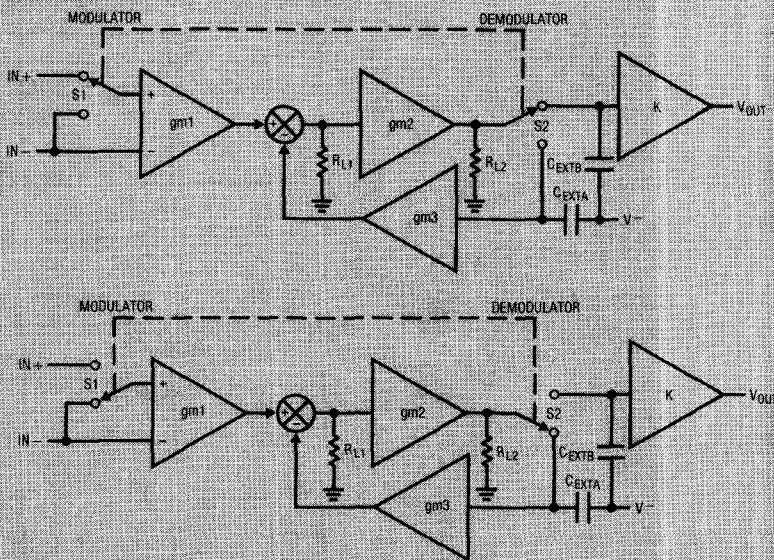


Figure B3. LTC1052 Conceptual Amplifier (Simplified)

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Methods for Measuring Op Amp Settling Time

Jim Williams

Servo, DAC and data acquisition amplifiers all require good dynamic response. In particular, the time required for an amplifier to settle to final value after an input step is especially important. This specification allows setting a circuit's timing margins with confidence that the data produced is accurate. The settling time is the total length of time from input step application until the amplifier remains within a specified error band around the final value.

Figure 1 shows one way to measure amplifier settling time (see References 1, 2, and 3). The circuit uses the "false sum node" technique. The resistors and amplifier form a bridge-type network. Assuming ideal resistors, the amplifier output will step to $-V_{IN}$ when an input pulse is applied. During slew, the oscilloscope probe is bounded by the diodes, limiting voltage excursion. When settling occurs, the oscilloscope probe voltage should be zero. Note that the resistor divider's attenuation means the probe's output will be one-half of the actual settled voltage.

In theory, this circuit allows settling to be observed to small amplitudes. In practice, it cannot be relied upon to produce useful measurements. Several flaws exist. The circuit requires the input pulse to have a flat top within the

required measurement limits. Typically, settling within 10mV or less for a 10V step is of interest. No general purpose pulse generator is meant to hold output amplitude and noise within these limits. Generator output-caused aberrations appearing at the oscilloscope probe will be indistinguishable from amplifier output movement, producing unreliable results. The oscilloscope connection presents additional problems. As probe capacitance rises, AC loading of the resistor junction will influence observed settling waveforms. The 20pF probe shown alleviates this problem but its 10X attenuation sacrifices oscilloscope gain. 1X probes are not suitable because of their excessive input capacitance. An active 1X FET probe will work, but another issue remains.

The clamp diodes at the probe point are intended to reduce swing during amplifier slewing, preventing excessive oscilloscope overdrive. Unfortunately, oscilloscope overdrive recovery characteristics vary widely among different types and are not usually specified. The diodes' 600mV drop means the oscilloscope may see an unacceptable overload, bringing displayed results into question (for a discussion of oscilloscope overdrive considerations, see Box Section A, "Evaluating Oscilloscope Overload Response").

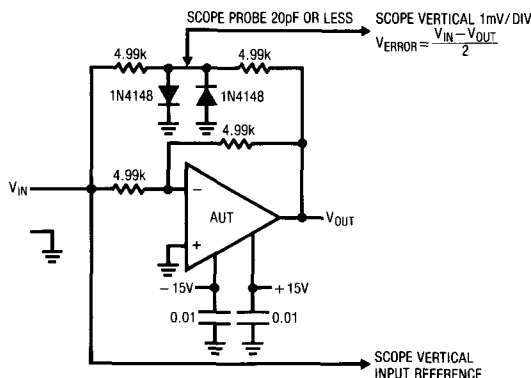


Figure 1. Typical Settling Time Test Circuit

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Figure 2 shows a practical settling time test circuit which addresses the problems discussed. Combined with a careful evaluation of the test oscilloscope used, it permits reliable settling time measurements in the 0.1% to 0.01% region. The input pulse does not drive the amplifier, but switches a Schottky bridge via a clamp. The bridge is biased from two low noise LT1021-10V references. Depending on input pulse polarity, current flows through the appropriate 10k resistor to bias the amplifier's summing point. The bridge switches cleanly and quickly, producing a flat-topped current pulse into the AUT. The circuit's input pulse characteristics do not influence the measurement. A second clamp-bridge arrangement supplies an opposite polarity signal which is nulled against the amplifier's output at point B. Schottky

clamp diodes limit this point's voltage excursion to $\pm 300\text{mV}$.

The Q1-Q5 configuration forms a low input capacitance, high speed buffer to drive the oscilloscope. Q1A's 1-2pF input capacitance provides very light AC loading, eliminating probe-caused problems. Q1B, running as a current sink, compensates Q1A's V_{GS} drop. Q2-Q5 form a complementary emitter-follower which can drive substantial cable capacitance without distortion.

The circuit should be built on a ground planed board with particular care taken to ensure low stray capacitance at points A and B. The AUT socket should be selected for short pin lengths. Very high speed amplifiers ($t_{SETTLE} < 200\text{ns}$) should be directly soldered into the circuit.

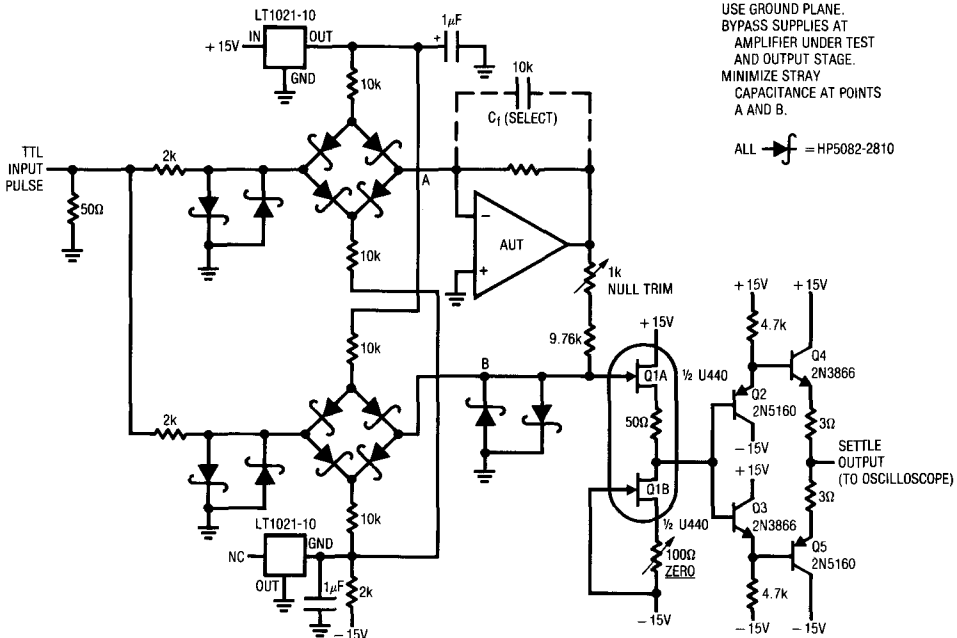


Figure 2. Improved Settling Time Test Circuit

This circuit, combined with a judiciously chosen oscilloscope, allows observation of amplifier settling to a millivolt (0.01%) for a 10V step. A good way to gain confidence in the circuit is to test a very fast UHF amplifier. Figure 3 shows response for an amplifier (Teledyne Philbrick 1435) specified to settle in 70ns within a millivolt for a 10V step. Trace A is the input pulse, Trace B is the amplifier output and Trace C is the settle signal. Settling occurs inside 70ns, indicating good agreement between the circuit and the AUT specification. Since most amplifiers are not nearly this fast, it is reasonable to assume that the circuit will always provide reliable results.

Because this circuit works by nulling opposite polarity sources, it seems unable to test followers—but it can. The AUT is battery-powered and completely floated from the circuit's power supply (Figure 4). The AUT output is connected to circuit ground and the battery center tap becomes the output. The positive input is driven from the Schottky bridge. The floating power supply lets the follower fool the circuit into thinking it is testing an inverter. The AUT's output appears inverted, but this is not a significant penalty.

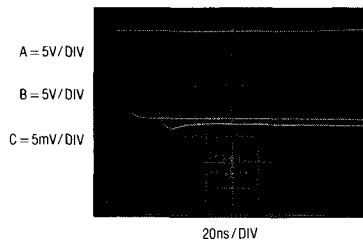


Figure 3. Settling Detail for a Fast Amplifier

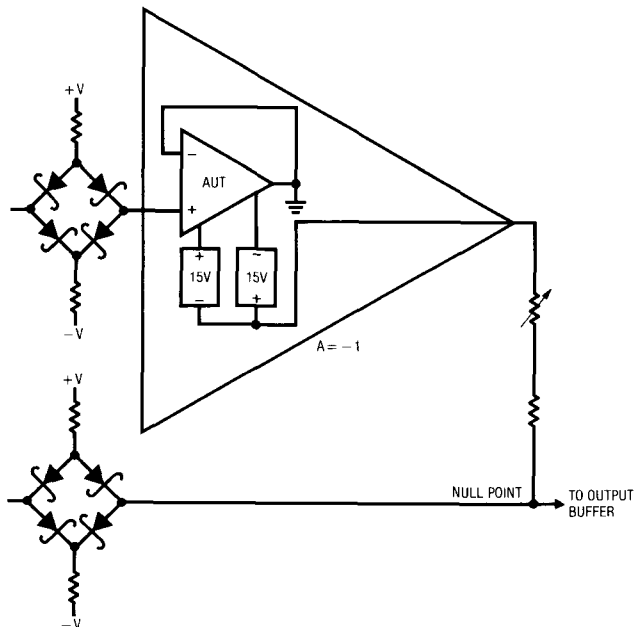


Figure 4. Circuit for Testing Followers

Application Note 10

To calibrate this circuit, ground point B and adjust the "zero trim" for 0V output. Next, temporarily tie the pulse input to +15V through 680Ω and adjust the "null trim" for 0V output. Remove the 680Ω resistor and the circuit is ready for use. When measuring settling times remember to experiment with the value of C_F to obtain best performance (see Box Section B, "Amplifier Compensation").

In the past, amplifier settling measurements below 1mV were not required. Recently, 16-bit and 18-bit D→A converters have become relatively common, requiring users to consider sub-millivolt settling time performance. Also, the offset specifications of current generation monolithic amplifiers are good enough to make very high precision settling time data worthwhile. Previously, being able to see an amplifier settle within 50μV wasn't interesting because its thermal drift swamped this figure.

The newer amplifier's substantially lower drift means very high precision settling time measurement data is useful. Figure 2's circuit is limited to 0.01% (1mV out of 10V) resolution by the 300mV Schottky clamp potential at point B. Simply increasing oscilloscope gain to get higher resolution will not work because of severe overload problems. With the oscilloscope set at 50μV/division, the

Schottky bound allows a 6000:1 overdrive. This is much more than any vertical amplifier is designed to accommodate. The oscilloscope's overload recovery will completely dominate the observed waveform and all measurements will be meaningless.

One way to obtain higher precision settling time measurements is to clip the incoming waveform in *time*, as well as amplitude. If the oscilloscope is prevented from seeing the waveform until settling is nearly complete, overload is avoided. Doing this requires placing a switch at the settle circuit's output and controlling it with an input-triggered, variable delay. FET switches are not suitable because of their gate-source capacitance. This capacitance will allow gate drive artifacts to corrupt the oscilloscope display, producing confusing readings. In the worst case, gate drive transients will be large enough to induce overload, defeating the switch's purpose.

Figure 5 shows a way to implement the switch which largely eliminates these problems. This circuit, connected to the basic settle circuit of Figure 2, allows settling within 10μV to be observed. The Schottky sampling bridge is the actual switch. The bridge's inherent balance, combined with matched diodes and very high

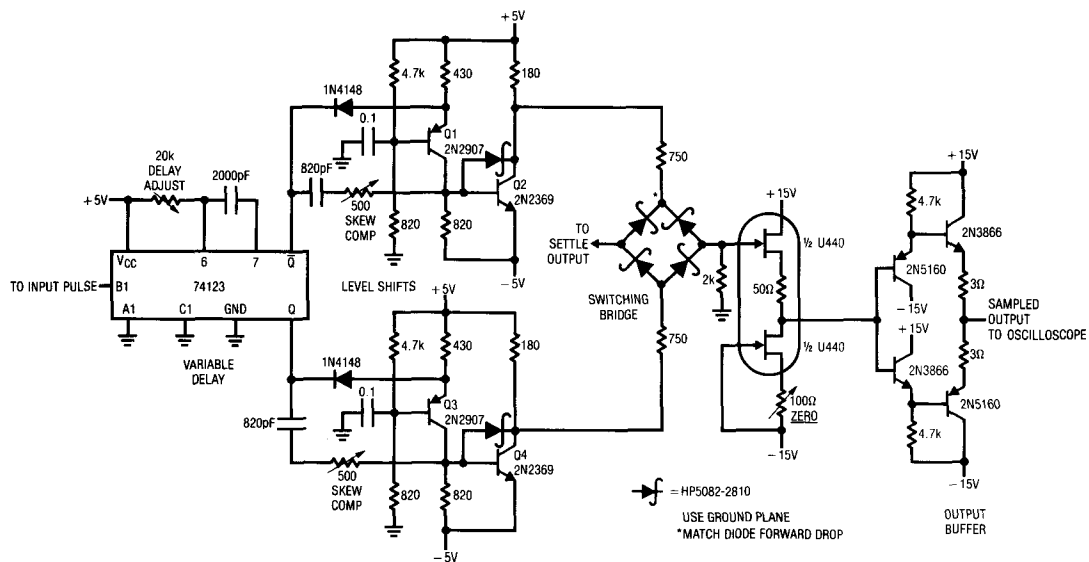


Figure 5. Sampling Switch for Ultra Precision Settling Time Measurement

speed complementary bridge switching, yields a clean, switched output. An output buffer stage, identical to the one used in Figure 2, unloads the bridge and drives the oscilloscope.

The complementary bridge switching drive is supplied from the Q1–Q2 and Q3–Q4 level shifters. Each circuit converts the delay one-shot's TTL output to $\pm 5V$ levels. The identical stages are comprised of an emitter-switched current source feeding a Baker-clamped common emitter output. Feedforward capacitance to the output transistor aids speed and overall delays are about 3ns. The level shifters must switch simultaneously to minimize drive-induced disturbances in the bridge's output. The "skew compensation" trims permit very small phasing adjustments in each level shifter, compensating skew in the 74123 one-shot's outputs. To trim this circuit, ground the bridge input and pulse the 74123's C1 input. Next, set the oscilloscope to $100\mu V$ /division and adjust the skew trims for minimum indication on the screen. Connect the bridge input back to the settle circuit's output and the circuit is ready for use.

Construction of this circuit requires care. A ground plane is mandatory and all bridge connections should be as

short and symmetrical as possible. To maintain low noise, the bridge's output ground return should be routed away from high current returns such as the 74123's ground pin.

This switch circuit, carefully constructed and used with the basic settle circuit, provides good results. Figure 6 shows an LT1001 precision op amp as the AUT. Trace A is the input pulse, while Trace B is the AUT output. During the AUT's slewing period the 74123 is fired (Trace C is Q), turning off the bridge. The bridge input appears in Trace D. The 74123 delay is adjusted so the bridge is switched when settling is nearly complete. Trace E is the circuit's final output, showing settling details at $100\mu V$ /division. The narrow peaking at the waveform's leading edge is due to switching residue. Figure 7 lists measured settling times to $50\mu V$ (0.0005% of a 10V step) for a group of precision amplifiers.

Some poorly designed amplifiers exhibit a substantial "thermal tail" after responding to an input step. This phenomenon, due to die heating, can cause the output to wander outside desired limits long after settling has apparently occurred. After checking settling at high speed it

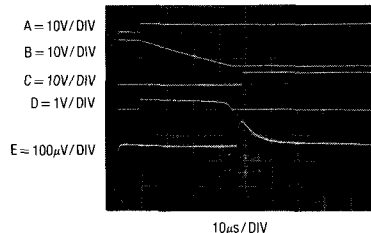


Figure 6. Sampling Switch Waveforms

Amplifier	Settling Time	Remarks
LT1001	65µs	
LT1007	18µs	
LT1008	65µs	Standard Compensation
LT1008	35µs	Feedforward Compensation
LT1012	70µs	
LT1055	6µs	
LT1056	5µs	

Figure 7. Measured Settling Times to 0.0005%

Application Note 10

is always a good idea to slow the oscilloscope sweep down and look for thermal tails. Often the thermal tail's effect can be accentuated by loading the amplifier's out-

put. Figure 8 shows the thermal tail of an amplifier which appears to have settled in a much shorter time than it actually has.

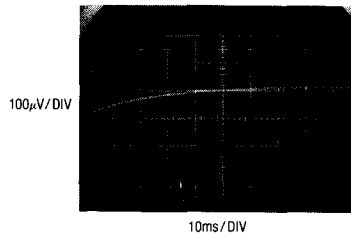


Figure 8. Typical Thermal Tail

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BOX SECTION A

Evaluating Oscilloscope Overload Performance

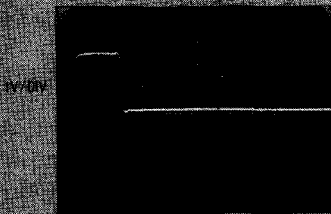
Settling time measurement relies heavily on the oscilloscope used. In many cases the oscilloscope is required to supply an accurate waveform after the display has been driven off screen. How long must one wait after an overload before the display can be taken seriously? The answer to this question is quite complex. Factors involved include the degree of overload, its duty cycle, its magnitude in time and amplitude and other considerations. Oscilloscope response to overload varies widely between types and markedly different behavior can be observed in any individual instrument. For example, the recovery time for a 100X overload at 0.005V/division may be very different than at 0.1V/division. The recovery characteristic may also vary with waveform shape, DC content and repetition rate. With so many variables, it is clear that measurements involving oscilloscope overload must be

approached with caution. Nevertheless, a simple test can indicate when the oscilloscope is being deleteriously affected by overdrive.

The waveform to be expanded is placed on the screen at a vertical sensitivity which eliminates all off-screen activity. Figure A1 shows the display. The lower right hand portion is to be expanded. Increasing the vertical sensitivity by a factor of two (Figure A2) drives the waveform off-screen, but the remaining display appears reasonable. Amplitude has doubled and waveshape is consistent with the original display. Looking carefully, it is possible to see small amplitude information presented as a dip in the waveform at about the third vertical division. Some small disturbances are also visible. This observed expansion of the original waveform is believable. In Figure A3, gain has

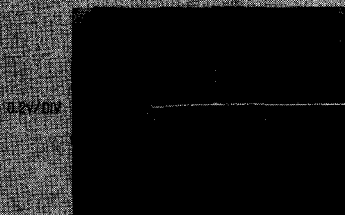
been further increased, and all the features of Figure A2 are amplified accordingly. The basic waveshape appears clearer and the dip and small disturbances are also easier to see. No new waveform characteristics are observed. Figure A4 brings some unpleasant surprises. This increase in gain causes definite distortion. The initial negative-going peak, although larger, has a different shape. Its bottom appears less broad than in Figure A3. Additionally, the peak's positive recovery is shaped slightly differently. A new rippling disturbance is visible in the center of the screen. This kind of change indicates that the oscilloscope is having trouble. A further test can

confirm that this waveform is being influenced by overloading. In Figure A5 the gain remains the same but the vertical position knob has been used to reposition the display at the screen's bottom. This shifts the oscilloscope's DC operating point which, under normal circumstances, should not affect the displayed waveform. Instead, a marked shift in waveform amplitude and outline occurs. Repositioning the waveform to the screen's top produces a differently distorted waveform (Figure A6). It is obvious that for this particular waveform, accurate results cannot be obtained at this gain.



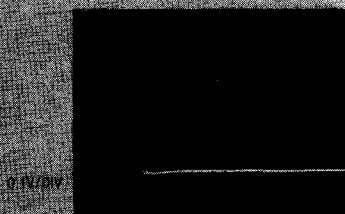
100ns/DIV

A1



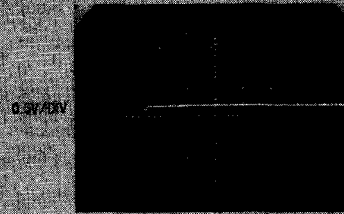
100ns/DIV

A3



100ns/DIV

A5



0.5V/DIV

100ns/DIV

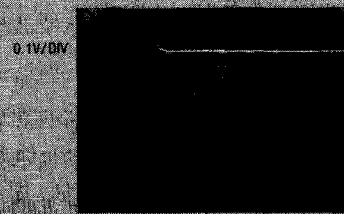
A2



0.1V/DIV

100ns/DIV

A4



0.1V/DIV

100ns/DIV

A6

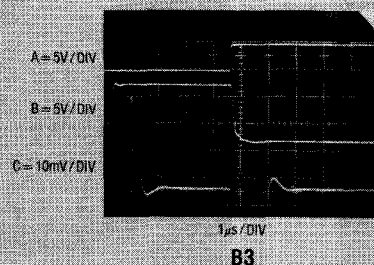
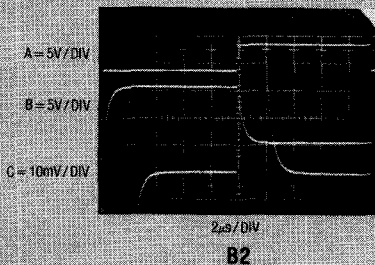
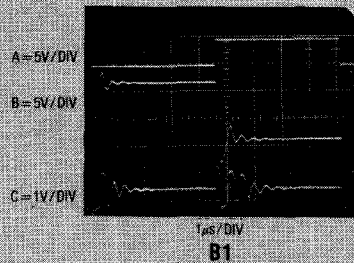
Figures A1-A6. The Overdrive Limit is Determined by Progressively Increasing Oscilloscope Gain and Watching for Waveform Aberrations

BOX SECTION B

Amplifier Compensation

To get the best possible settling time from any amplifier, the feedback capacitor, C_F , should be carefully chosen. C_F 's purpose is to roll off amplifier gain at the frequency which permits best dynamic response. The optimum value for C_F will depend on the feedback resistor's value and the characteristics of the source. One of the most common sources is also one of the most difficult. Digital-to-analog converters' current outputs must often be converted to a voltage. Although an op amp can easily do this, care is required to obtain good dynamic performance. A fast DAC can settle to 0.01% in 200ns but its output also includes a parasitic capacitance term, making the amplifier's job more difficult. Normally, the DAC's current output is unloaded directly into the amplifier's summing junction, placing the parasitic capacitance from ground to the amplifier's input. The capacitance introduces feedback phase shift at high frequencies, forcing the amplifier to "hunt" and ring about the final value before settling. Different DACs have different values of output capacitance. CMOS DACs have the highest output

capacitance and it varies with code. Bipolar DACs typically have 20pF–30pF of capacitance, stable over all codes. Because of their output capacitance, DACs furnish an instructive example in amplifier compensation. In practice, the Schottky bridge which feeds the AUT in the settle circuit is replaced with the DAC to be used. Depending on DAC input coding, it may be necessary to use inverters in the DAC input lines to maintain circuit nulling action. Figure B1 shows the response of an industry standard DAC-80 type and an LT1023 op amp which is optimized for inverting applications. Trace A is the input, while Traces B and C are the amplifier and settle outputs, respectively. In this example no compensation capacitor is used and the amplifier rings badly before settling. In B2, an 82pF unit stops the ringing and settling time goes down to 4 μ s. The overdamped response means that C_F dominates the capacitance at the AUT's input and stability is assured. If fastest response is desired, C_F must be reduced. B3 shows critically damped behavior obtained with a 22pF unit. The settling time of 2 μ s is the best obtainable for this DAC-amplifier combination.



Figures B1–B3. Effects of Different Feedback Capacitors on a DAC–Op Amp Combination

Designing Linear Circuits for 5V Single Supply Operation

Jim Williams

In predominantly digital systems it is often necessary to include linear circuit functions. Traditionally, separate power supplies have been used to run the linear components (see Box, "Linear Power Supplies—Past, Present, and Future").

Recently, there has been increasing interest in powering linear circuits directly from the 5V logic rail. The logic rail is a difficult place for analog components to function. The high amplitude broadband current and voltage noise generated by logic clocking makes analog circuit operation difficult. (See Box, "Using Logic Supplies for Linear Functions".)

Generally speaking, analog circuitry which must achieve very high performance levels should be driven from dedicated supplies. The difficulties encountered in maintaining the lowest possible levels of noise and drift in an analog system are challenging enough without contending with a digitally corrupted power supply.

Many analog applications, however, can be successfully implemented using the logic supply. Combining components intended to provide high performance from the log-

ic rail with good design can give excellent results (see Box, "High Performance, Single Supply Analog Building Blocks"). The examples which follow show this in a variety of precision measurement and control circuits which function from a 5V supply.

Linearized RTD Signal Conditioner

Figure 1 shows a circuit which provides complete, linearized signal conditioning for a platinum RTD. One side of the RTD sensor is grounded, often desirable for noise considerations. The Q1-Q2 current source is referenced to A1's output. A1's operating point is primarily fixed by the 2.5V LT1009 voltage reference. The RTD's constant current forces the voltage across it to vary with its resistance, which has a nearly linear positive temperature coefficient. The non-linearity causes several degrees of error over the circuit's 0°C–400°C operating range. A2 amplifies R_p's output, while simultaneously supplying non-linearity correction. The correction is implemented by feeding a portion of A2's output back to A1's input via the 10k-250k divider. This causes the Q1-Q2 current source

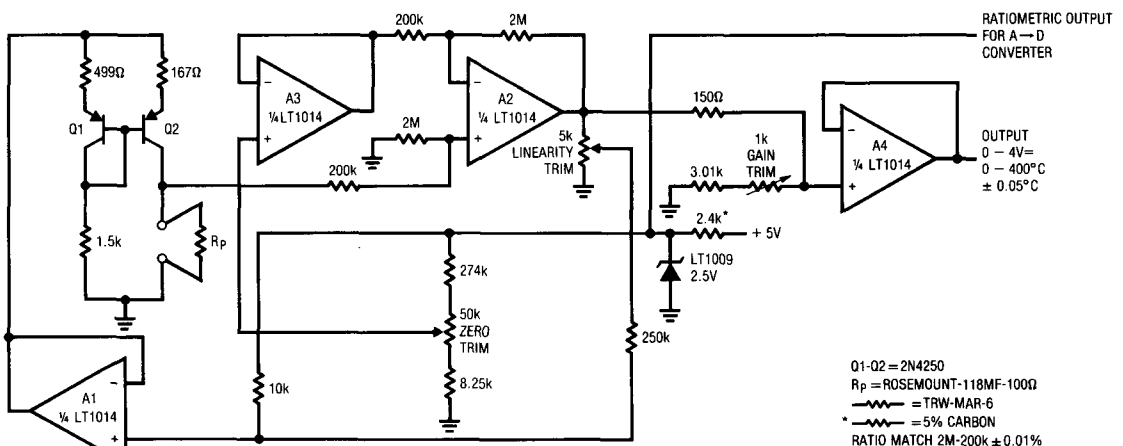


Figure 1. Linearized Platinum RTD Signal Conditioner

Application Note 11

output to shift with R_P 's operating point, compensating sensor non-linearity to within $\pm 0.05^\circ\text{C}$. A3, also referenced to the LT1004, voltage sums an offsetting signal at A2's negative input, allowing 0°C to equal 0V at A2's output. The resistive divider in A4's input line sets circuit gain, and the circuit's output is taken at A4.

To calibrate this circuit, substitute a precision decade box (e.g., General Radio 1432K) for R_P . Set the box to 0°C value (100.00Ω) and adjust the zero trim for a 0.0V output. Next, set the decade box for a 140°C output (154.26Ω) and adjust the gain trim for a 1.400V output reading. Finally, set the box to 400°C (249.0Ω) and trim the linearity adjustment for a 4.000V output. Repeat this sequence until all three points are fixed. Total error over the entire range will be within $\pm 0.05^\circ\text{C}$. The resistance values given are for a nominal 100.00Ω (0°C) sensor. Sensors deviating from this nominal value can be used by factoring in the deviation from 100.00Ω . This deviation, which is manufacturer-specified for each individual sensor, is an offset term due to winding tolerances during fabrication of the RTD. The gain slope of the platinum is primarily fixed by the purity of the material and is a very small error term.

Linearized Output Methane Detector

Figure 2 is another 5V-powered transducer circuit. Like the platinum RTD example, this circuit linearizes the transducer's output, but it performs a more complex mathematical operation. The circuit's frequency output is directly proportional to the methane concentration detected by the transducer specified. Figure 3 shows that the transducers output varies as;

$$\approx \frac{1}{\sqrt{\text{Concentration}}}$$

The circuit linearizes this function and its frequency output is also plotted.

The sensor's resistance vs methane concentration is converted to a voltage by A1. The LT1034 serves as a reference. A1's output feeds A2. The exponential relationship between V_{BE} and collector current in transistors is

utilized to generate a current in Q3's collector proportional to the square of A2's input current. This operation compensates the sensor's square root term. Q3's collector current sets the operating point of the A3-A4 oscillator. A3, an integrator, generates a positive going linear ramp (Trace A, Figure 4). The ramp is compared with Q3's current at A4's summing point (Trace B). A4 is configured as a current summing comparator. The feedback diode-bound network minimizes delay due to output slew time. When the ramp forces the summing point positive, A4's output (Trace C) swings negative. CMOS inverter A (Trace D) goes high, turning on the CD4016 switch to reset the A3 integrator. Simultaneously, inverter B goes low (Trace E), supplying AC positive feedback to A4's "+" input (Trace F). When the positive feedback decays, A4's output goes high, A3 begins to integrate, and the entire cycle repeats. Q3's collector current determines how long A3's ramp runs before A4 resets it. The ramp time is directly proportional to Q3's collector current, meaning that oscillation frequency is inversely ($1/X$) related to the current. The overall circuit transfer function is;

$$\frac{1}{X^2}$$

This linearizes the sensor's output. In practice, the sensor's response slightly deviates from the equation shown, actually being;

$$\frac{1}{\sqrt{1.9 \text{ Concentration}}}$$

The reset time constants at A4's input introduce enough oscillator "dead time" to partially compensate for the deviation. The dead time's frequency retarding characteristic effects the oscillator's high frequency range, providing a first order correction. The overall linearization achieved is within the sensor's manufacturing tolerances. The slight "bump" in the circuit's response curve is due to the mismatch between the sensors term and the circuits X^2 function.

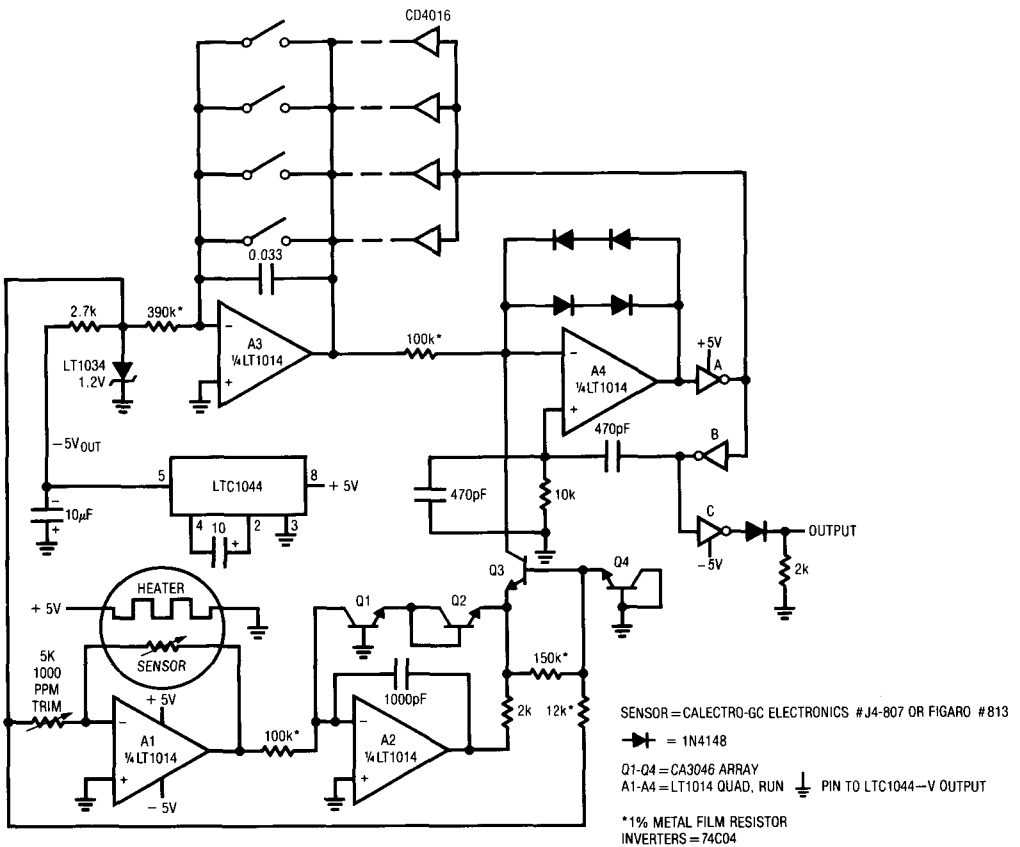


Figure 2. Linearized Methane Transducer Signal Conditioner

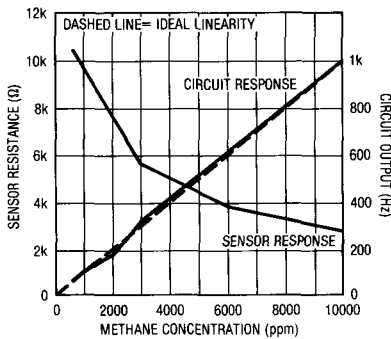


Figure 3. Transducer vs Circuit Response

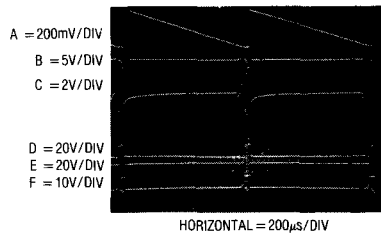


Figure 4. Linearized Methane Detector Waveforms

Application Note 11

The dead time correction in the oscillator smoothes this error out above 4000ppm. The LTC1044 voltage converter generates a negative supply directly from the 5V rail. This approach provides necessary negative circuit potentials while maintaining compatibility with 5V-supply-only operation. The sensor's heater is powered directly from the 5V rail, as specified by the manufacturer. To calibrate the circuit, place the sensor in a 1000ppm methane environment and adjust the 5k trim for a 100Hz output. Accuracy from 500ppm to 10,000ppm is limited by the sensor's 10% specification.

Cold Junction Compensated Thermocouple Signal Conditioner

Figure 5 shows a 5V powered, complete thermocouple signal conditioner. Cold junction compensation is included, and the circuit allows one leg of the thermocouple to be grounded, desirable for noise considerations. The LTC1043 combines the cold junction network differential output with the grounded thermocouple's signal at the LTC1052. The LTC1052 provides stable, low drift gain. To enable swing all the way to ground, the LTC1043's other switch section generates a small negative potential. This allows the LTC1052 output stage to run Class A for small outputs, permitting swing to 0V. The table gives proper values for R1 for various thermocouples. Output scaling may be set by R_F/R_I to whatever slope is desirable. Cold junction compensation holds within $\pm 1^\circ\text{C}$ over 0°C – 60°C .

5V Powered Precision Instrumentation Amplifier

Many transducer outputs require a true differential input "instrumentation" type amplifier. Transducers with single ended outputs do not, in theory, require a differential input amplifier but common-mode noise often exceeds the signal of interest. For these reasons, transducer systems often employ these type amplifiers.

No commercially manufactured instrumentation amplifier will function from a 5V supply and achieving good precision in a design is difficult. The circuits in Figure 6 meet these requirements. They also feature input protection, filtering capability and a shield driving output.

In Figure 6A, A1, A2 and A3 accomplish the differential-input-to-single-ended-output conversion, with R_G setting gain. The LT1014's high open loop gain permits accurate circuit gain. Offset and drift performance allows use with low level transducers such as thermocouples and strain gauges. The $100\text{k}\Omega$ - $1\mu\text{F}$ combination filters noise and 60Hz pickup; the amplifier is never exposed to high frequency common-mode noise. The transistor-diode clamps combine with the $100\text{k}\Omega$ resistors to prevent high voltage spikes or faults (common in industrial environments) from damaging the amplifiers. A4 is used as a shield driver to reduce the effects of input cable capacitance. It drives the shield at the input common-mode voltage, which is derived from the input amplifier's output. Performance characteristics are summarized in the table.

Figure 6B achieves greater DC precision at the expense of bandwidth. Here, the LTC1043 switched capacitor building block alternately commutates a $1\mu\text{F}$ capacitor between the circuit input and the LTC1052's input. This stage, accomplishing a differential-to-single-end transition, allows the chopper stabilized LTC1052 to take a ground referred measurement. The LTC1043's other switch stage generates a small negative potential, allowing the LTC1052 output to swing all the way to 0V. DC precision is excellent, surpassing all monolithic $\pm 15\text{V}$ instrumentation amps, although bandwidth is limited to 10Hz. The LTC1043's switching action, set at about 400Hz by the $0.01\mu\text{F}$ value, forms a low pass filter. This permits extremely high rejection of noise, allowing the CMRR to remain above 120dB at 20kHz. Overall performance is summarized in the table.

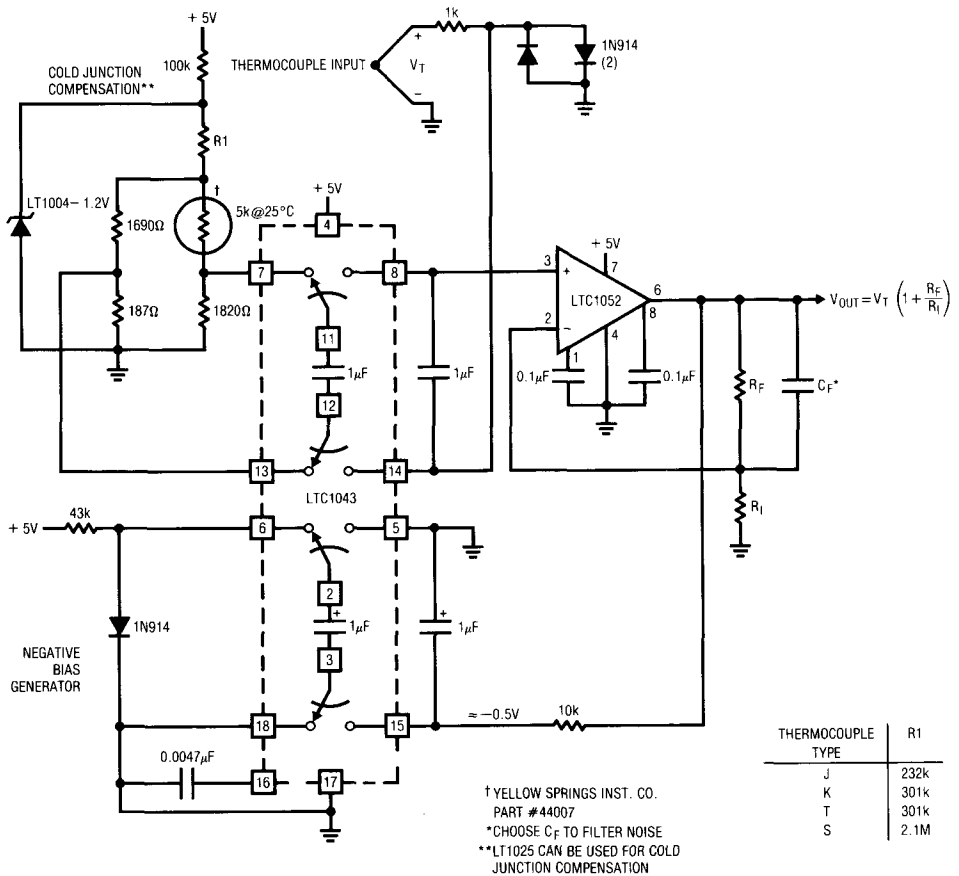


Figure 5. Cold Junction Compensated Thermocouple Signal Conditioner

Application Note 11

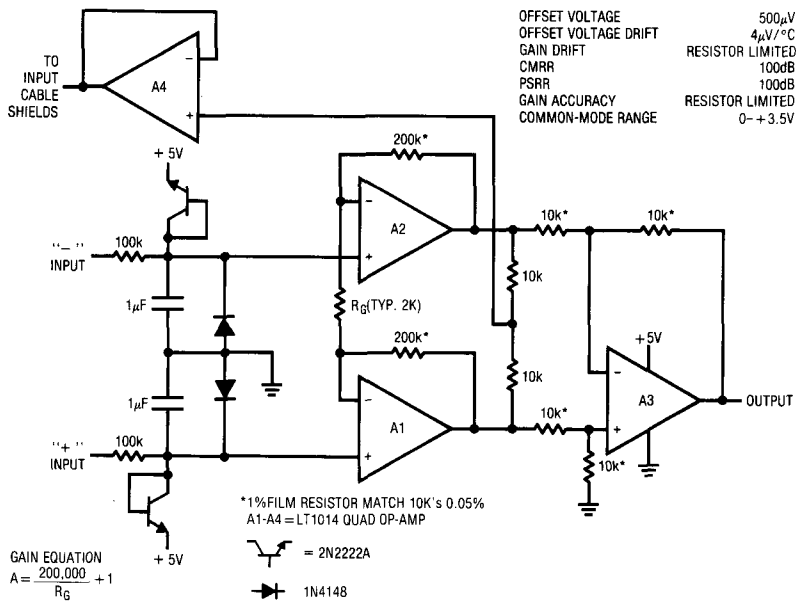


Figure 6A. Precision Instrumentation Amplifier

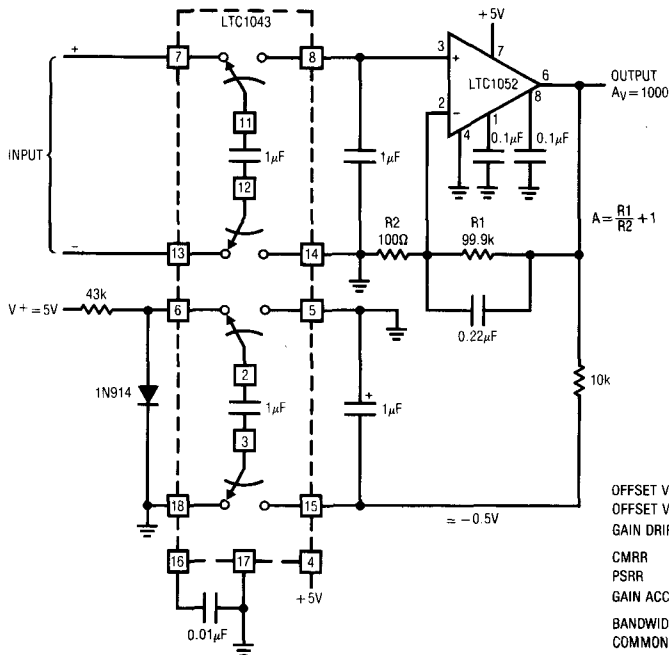


Figure 6B. Ultra Precision Instrumentation Amplifier

5V Powered Strain Gauge Signal Conditioner

Figure 7 shows an unusual approach to signal conditioning the bridge output of a strain gauge pressure transducer. The 5V circuit needs only two amplifiers and provides an auxiliary ratio output for a monitoring A-D converter. The design functions by converting the bridge's differential output into a ground referred single ended signal which is then amplified. This approach eliminates common-mode errors by eliminating the bridge's common-mode output component. Additionally, the number of precision resistors required is minimized and no matching is required.

A1 biases the LTC1044 positive-to-negative converter. The LTC1044's output pulls the bridge's output negative, causing A1's input to balance at 0V. This local loop permits a single-ended amplifier (A2) to extract the bridge's output signal. The 100k-0.33μF RC filter's noise and A2's gain is set to provide the desired output scale factor. Because bridge drive is derived from the LT1034 reference, A2's output is not affected by supply shifts. The LT1034's output is

available for ratio operation. To calibrate this circuit, apply or electrically simulate 0psi and trim the zero adjustment for 0V output. Next, apply or electrically simulate 350psi and trim gain for 3.500V out. Repeat these adjustments until both points are fixed.

"Tachless" Motor Speed Controller

Figure 8 shows a way to servo control the speed of a DC motor. This circuit is particularly applicable to digitally controlled systems in robotic and X-Y positioning applications. By functioning from the 5V logic supply it eliminates additional motor drive supplies. The "tachless" feedback saves additional space and cost. The circuit senses the motor's back EMF to determine its speed. The difference between the speed and a setpoint is used to close a sampled loop around the motor. Because no commercially available sample-and-hold circuit will run from a 5V supply, special techniques are required.

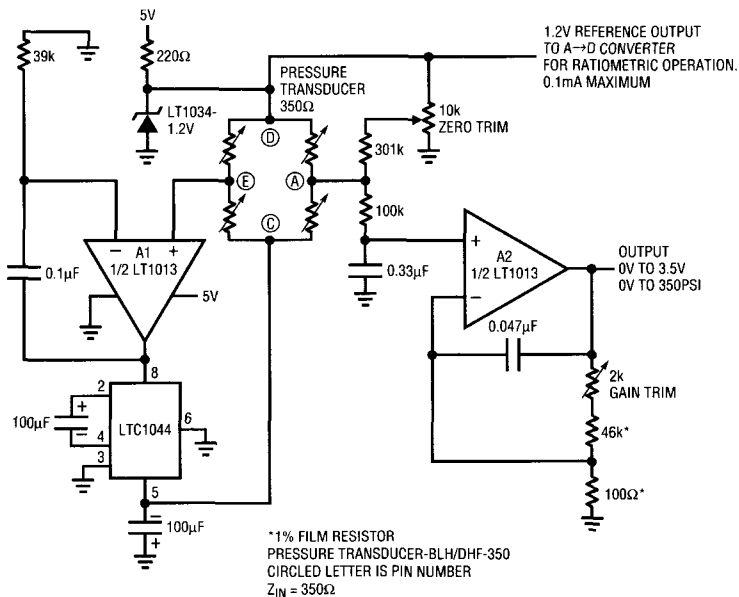


Figure 7. Strain Gauge Signal Conditioner

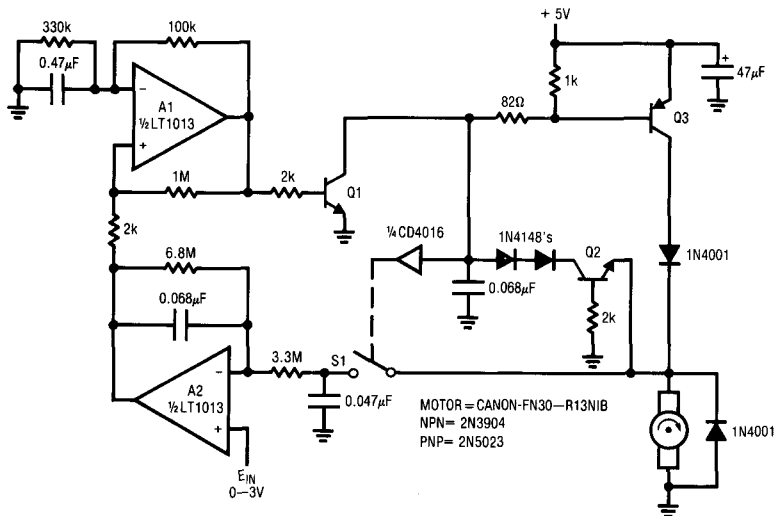


Figure 8. "Tachless" Motor Speed Controller

A1 generates a pulse train (Trace A, Figure 9). When A1's output is high, Q1 is biased and Q3 drives the motor's ungrounded terminal (Trace B). When A1 goes low, Q3 turns off and the motor's back EMF appears after the inductive flyback ceases. During this period, S1's input (Trace C) is turned on, and the 0.047 capacitor acquires the back EMF's value. A2 compares this value with the setpoint and the amplified difference (Trace D) changes A1's duty cycle, controlling motor speed. A2 has the desirable characteristic of assuming unity gain in the absence of a feedback signal. Start-up or input overdrive cannot force servo lock-up due to loss of sampling action. The loop is self-restoring and will establish control when abnormal conditions cease.

Drive to S1's control input must be carefully controlled for proper operation. Q2 prevents the switch from closing until the negative going flyback interval is over and the 0.068µF capacitor slows the switches turn-on edge. These measures ensure clean back EMF acquisition in the 0.047µF unit. Q2's collector line diodes compensate the motor's clamp diode drop, preventing destructive negative voltages at S1. The circuit controls from 20rpm to full speed with good transient response under all shaft loads. The gain and roll-off terms in A2's feedback loop are optimal for the motor listed, and should be reestablished for other types.

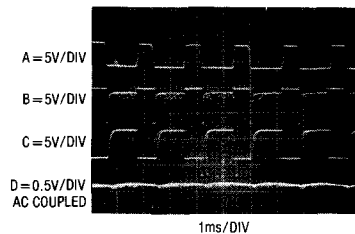


Figure 9. Motor Speed Controller Waveforms

4-20mA Current Loop Transmitter

Transmission of industry standard 4-20mA current loop signals to valves and other actuators is a common requirement. Resistive line losses and actuator impedances require current transmitters to be able to force a compliance voltage of at least 20V. Because of this, 5V powered systems usually cannot meet current loop transmitter requirements, but Figure 10 shows a way to do this. This 5V powered circuit utilizes a servo controlled DC-DC converter to generate the compliance voltage necessary for loop current requirements. It will drive 4-20mA into loads as high as 2200Ω (44V compliance) and is inherently short circuit protected. The circuit's input is applied to A2, whose output biases A1's "+" input via the offsetting network. A1's output goes high, biasing Q4 to turn on Q3. Q3's collector drives the T1-Q1-Q2 DC-DC converter, which is clocked by the RC-gate oscillator. T1 furnishes voltage

step-up and the rectified and filtered secondary current flows through the 100Ω resistor and the load. A1's negative input measures the voltage across the 100Ω resistor, completing a current control loop around T1. The 0.33μF capacitor furnishes stable loop roll-off and the 100pF unit suppresses local oscillation at Q4. Within the compliance limit, A1 maintains constant output current, regardless of load impedance shifts or supply changes. To calibrate this circuit, short the output, apply 0V to the input and adjust the "4mA trim" for 0.3996V across the 100Ω resistor. Next, shift the input to 4.000V and trim the 20mA adjustment for 1.998V across the 100Ω resistor. Repeat this procedure until both points are fixed. The gain trim network shunting the 100Ω resistor necessitates the odd voltage trim target values, but output current swings between 4.000mA and 20.00mA.

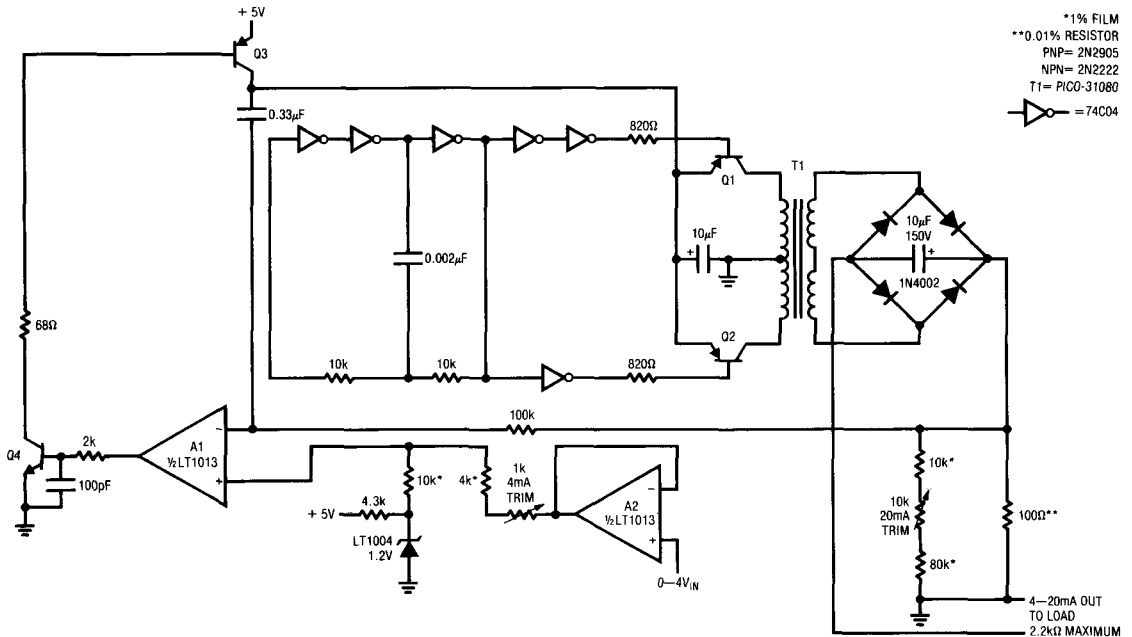


Figure 10. 4-20mA Current Loop Transmitter

Application Note 11

Figure 11 details modifications which permit the circuit's output current to galvanically float. This is often useful in industrial situations where the output lines may be exposed to common-mode voltages or high voltage fault conditions. The transformer's primary current, which theoretically reflects current delivered by the secondary, is sensed across a shunt and fed back via A2. In practice,

current control precision is limited by non-ideal transformer behavior to about 1%. Common-mode voltage is limited by T1's 300V breakdown.

Fully Isolated Limit Comparator

Figure 12's 5V powered circuit performs a fully isolated limit comparison on low level signals. It produces a digital

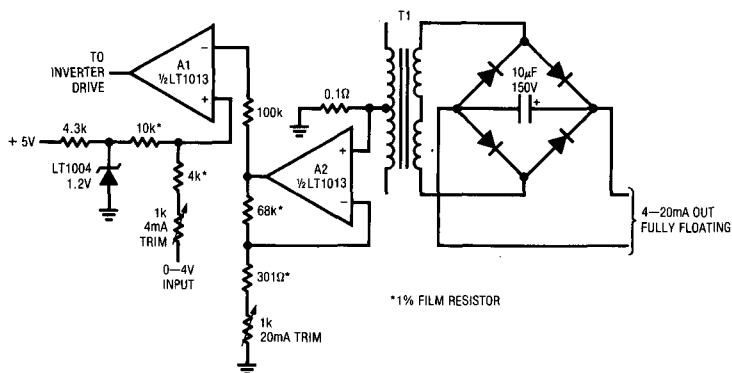


Figure 11. Floating Output Option for Current Loop Transmitter

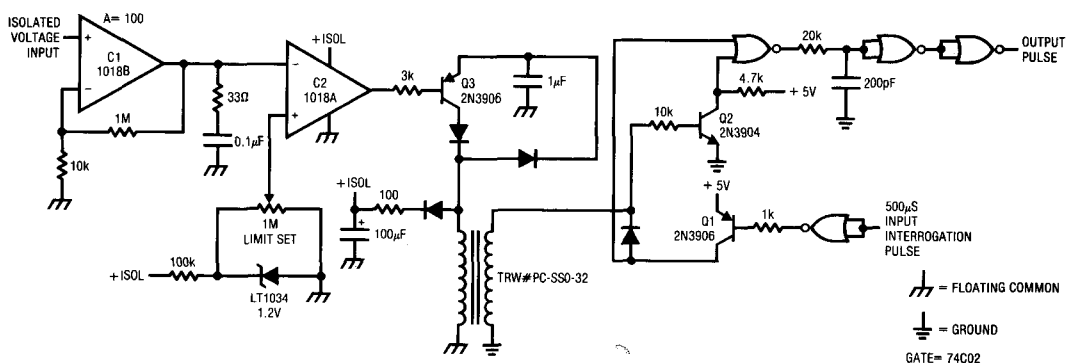


Figure 12. Fully Isolated Limit Comparator with Gain of 100.

output indicating if the input is above or below a preset limit. This circuit is ideal for process control applications where transducers operate at high common-mode voltages or where large ground loops exist. An uncommitted gain-of-100 amplifier allows thermocouples and other low level sources to be used with the circuit. The circuit functions by echoing an interrogation pulse if the input is above a preset level. If the input is below this level, no echo pulse occurs. A transformer is used to allow a two-way, galvanically isolated signal path and the energy contained in the interrogation pulse powers the circuit's floating elements. Figure 13 shows operating waveforms for the "above limit" case. When an input interrogation pulse is applied, Q1's collector drives the transformer primary (Figure 13, Trace A). Energy is transferred to the transformer's secondary and stored in the $100\mu\text{F}$ capacitor. The charge in the capacitor powers the isolated circuitry (" + ISOL" potential indicated in Figure 12). If low

power dual comparator C2's output is low, Q3 biases and drives current into the transformer secondary (Trace B). This is reflected in the transformer's primary (Trace C). Q2 and the associated gate circuitry form a demodulator which produces an output pulse (Trace D). If C2's output had been high (below limit set), the transformer would have received no secondary drive and there would be no output pulse. The demodulator is designed so that nothing appears on the output line unless the circuit is above the preset limit.

Comparator C1's output damper network allows it to function as an op amp for low level signals. This circuit easily extracts millivolt signals buried in high common-mode voltage or ground noise and delivers its limit decision to the output. The maximum common-mode voltage is limited by the transformer's 500V breakdown.

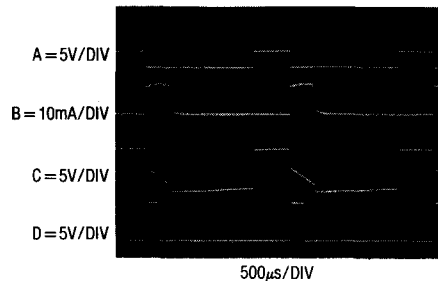


Figure 13. Isolated Limit Comparator Waveforms

Application Note 11

Fully Isolated 10 Bit A-D Converter

Figure 14's 5V powered circuit is a complete 10 bit A-D converter which is fully floating from system ground. It is ideal for performing 10 bit A-D conversions in the face of the high common-mode noise characteristics of predom-

inantly digital systems. It is also useful in industrial environments, where noise and high common-mode voltages are present in transducer fed systems.

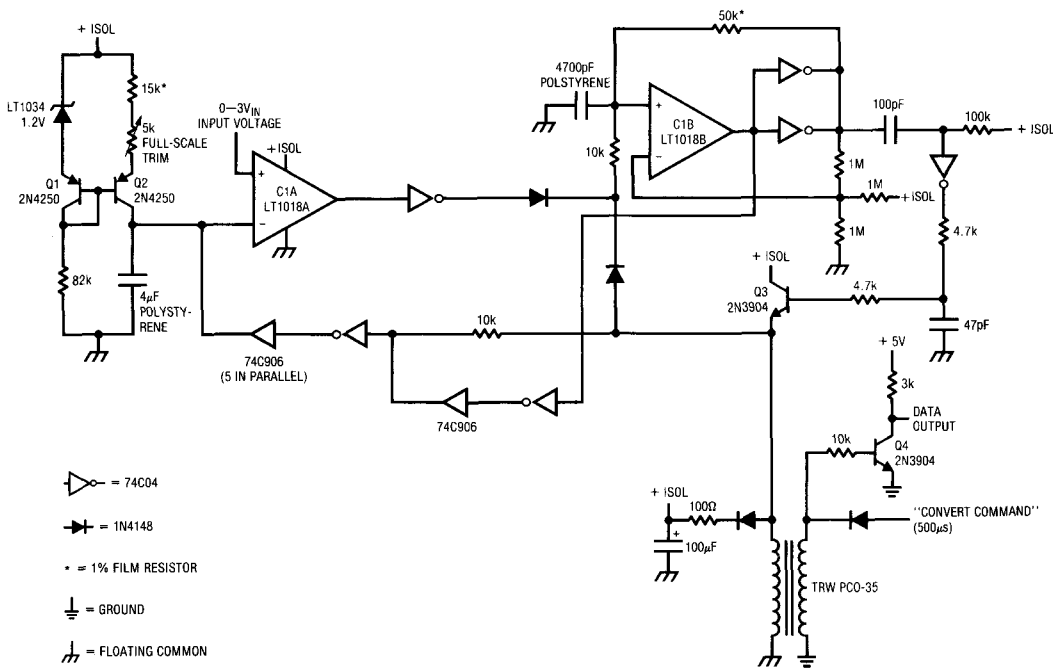


Figure 14. Fully Isolated A-D Converter

Circuit operation is initiated by applying a pulse to the “convert command” input (Trace A, Figure 15). This pulse appears at the transformer secondary and charges the 100 μ F capacitor. This potential is used to supply power to the floating A–D conversion circuitry. The transformer’s secondary pulse biases the inverter-open drain buffer combination to discharge the 4 μ F capacitor (Trace B). The secondary pulse also biases a diode to stop the C1B 3kHz oscillator output (Trace D). Concurrently, C1A goes high, forcing the inverter in its output line low (Trace C). When the convert command pulse ceases, the Q1-Q2 current source charges the 4 μ F capacitor with a linear ramp. The C1B oscillator now runs. When the ramp crosses the input voltage’s value, C1A’s output switches and its output line inverter (Trace C) goes high, cutting off the oscillator. The number of oscillator pulses occurring during this interval

is proportional to the input voltage value. These pulses are differentiated and fed to Q3, which drives the transformer. The differentiation causes narrow spikes to be fed to the transformer, easing power drain on the 100 μ F energy storage capacitor. Q3’s RC base delay and the inverter-buffer combination at C1B’s output prevent Q3’s emitter pulses from triggering a ramp reset. The waveforms appearing at the transformer’s input do not reflect the circuit’s complex operation, and easily interface to a digital system. Figure 16, Trace A shows the “convert command” pulse. Trace B is the transformer primary. The differentiated oscillator pulses coming from the transformer secondary appear as small amplitude spikes. In this case, a small voltage is being converted and the number of pulses is small. Trace C, the “data output”, is taken at Q4’s collector, and the pulses are TTL compatible.

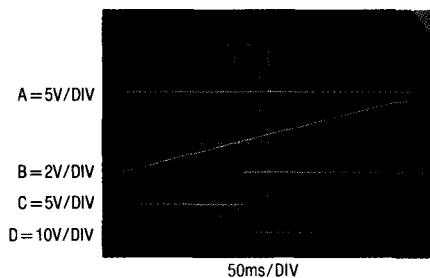


Figure 15. A–D Waveforms—Isolated Section

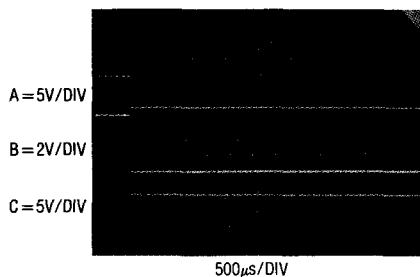


Figure 16. Detail of A–D Waveforms—Grounded Section

Application Note 11

Several subtle factors contribute to the 10 bit performance of this circuit. The 4700pF and 4 μ F polystyrene capacitors are both -120ppm/ $^{\circ}$ C gain terms. Because of this, their temperature drift's ratio and overall circuit gain drift is about 25ppm/ $^{\circ}$ C. The 5 parallel 74C906 open drain buffers provide an effective 0V reset for the 4 μ F capacitor, minimizing reset offset errors. Parallel inverters in C1B's output line reduce saturation caused errors, aiding oscillator stability with shifts in supply and temperature. Finally,

the diode path at Q3's emitter averts a ± 1 count uncertainty error by synchronizing the oscillator to the conversion sequence. The 5k potentiometer in the current source trims calibration to equal 1024 counts out for 3.000V input. The transformer used allows the converter to function at common-mode levels up to 175V. The circuit requires 330ms to complete a 10 bit conversion and drifts less than 1 LSB over 25 $^{\circ}$ C \pm 25 $^{\circ}$.

High Performance Single Supply Analog Building Blocks

Two new components provide the basic building blocks needed for high performance 5V single supply circuits. The LT1014 quad op amp, also available as the LT1013 dual, features DC specifications nearly as good as the best ± 15 V op amps. The LT1017/LT1018 series dual com-

parators combine low power and high DC precision with speed adequate for most applications. To ease single supply operation, both units' common-mode range includes ground, and the op amp's output swings nearly to ground.

LT1014 Basic Features

EOS—70 μ V
EOS Δ TC—2 μ V/ $^{\circ}$ C
I_{bias}—15nA
Gain—1.0 $\times 10^6$
Supply I—310 μ A
Noise—0.1Hz-10Hz-0.55 μ Vp-p
Common-Mode Range—Ground to (V⁺) - 1.5V
Supply Range—3.4V-40V
Output Swing No load (V⁺) - 0.6V
(V⁻) + 0.015V
600 Ω load (V⁺) - 1.0V
(V⁻) + 0.005V

LT1017/LT1018 Basic Features

EOS—500 μ V
EOS Δ TC—5 μ V/ $^{\circ}$ C
I_{bias}—15nA
Gain—1 million
Supply I—LT1017—30 μ A, LT1018—110 μ A
Response Time—6 μ s (LT1018)
Common-Mode Range—V⁻ to (V⁺) - 0.9V
Supply Range—1.1V-40V
Output Current—65mA pull down—60 μ A pull up
Output Stage can pull down loads above V_S

Linear Power Supplies—Past, Present, and Future

The amplitude of linear circuitry's power supplies has been determined by the available technology used for linear functions.

Probably the first standard linear supply was $\pm 300\text{V}$, used in analog computers. The operating characteristics of vacuum tubes necessitated high voltages. Additionally, because analog computers (from which operational amplifiers descended) were mathematical machines, bipolar supplies were desirable for computational purposes. With the arrival of solid state linear components in the early 1960's, new supply voltages were necessary and desirable. $\pm 15\text{V}$ was adapted because of transistor breakdown limits, as well as the availability of low voltage references (zener and avalanche diodes). Power and size advantages afforded by the new supply standard were also obviously attractive. It is significant that while the supply drop decreased available dynamic range of operation by over 20dB, the usable signal processing range did not decrease. This was due to the lower noise and drift of the solid state components.

The arrival of monolithic linear circuits in the late 1960's and subsequent design refinements expanded the available territory at the lower end of the signal processing range.

Currently available precision linear components and technology shifts are causing reevaluation of the power supply issue. In particular, several trends argue for linear functions to be able to operate from the low voltage digital rail. The increasing digital content of systems makes 5V compatible linear components attractive. Cost and space considerations in these systems often make separate linear supplies undesirable. This situation is not universal, and never will be, but is increasingly common.

A move to lower voltages for digital circuits, which must occur, underscores the need for low voltage, high performance linear ICs. Drops in digital supply value will be forced by increasing density requirements, which will lower IC breakdown limits.

Lower power consumption in systems goes along with supply voltage and density issues. Increasingly complex

systems are being put into smaller physical spaces, necessitating attention to dissipation. In many instances, portable operation is desirable, so circuitry must be directly compatible with battery potentials, as well as lower power. Linear components must not give up performance to function in this low voltage, digitally driven environment. Demands for precision remain high, and low voltage linear circuits, despite their narrowed dynamic operating range, must meet these requirements. This is not easy, considering that a 12 bit $\pm 15\text{V}$ system typically has a 2.5mV/LSB error budget. At 5V, this number shrinks to 1mV. To deal with this, design techniques developed for $\pm 15\text{V}$ components are being used in new, low voltage ICs and new approaches will also be employed.

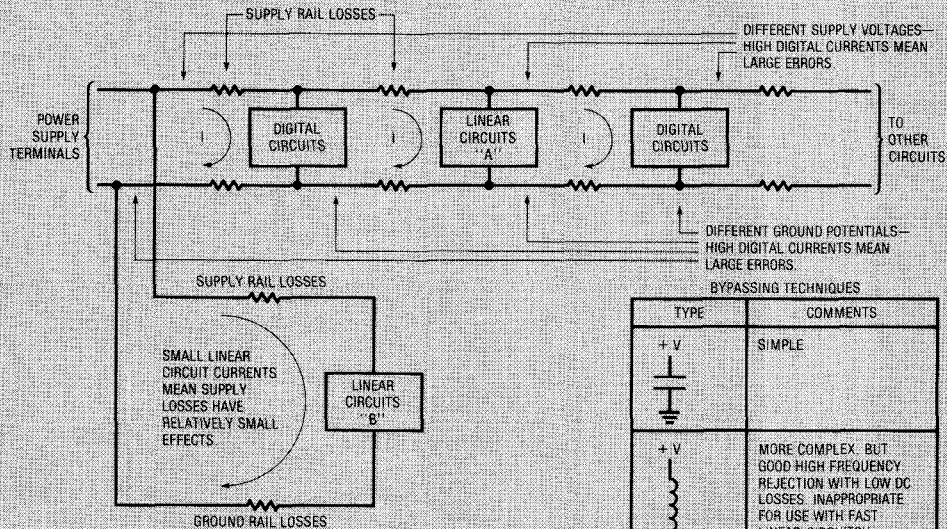
Using Logic Supplies for Linear Functions

The fast clocking and transient high currents characteristic of digital systems make logic supplies an unfriendly place for linear components to operate. A key to achieving good results is considering power bus routing as an integral part of the signal processing chain. The figure shows that supply rail impedances will cause both DC and AC errors at various points in a system. This is true of any power distribution scheme, but is especially troublesome in digitally oriented systems, where fast current spiking and clock harmonics are present. Circuitry located at position "A" will see appreciable positive rail noise and ground potential will be corrupted by fast, relatively high currents returning through conductor impedances. Supply bypassing can reduce positive rail noise, but ground potential uncertainty can cause unacceptable errors. Locating linear circuits as shown in "B" reduces both positive and ground rail problems by eliminating the digitally derived currents. The linear devices lower operating currents allow lower errors due to supply distribution impedances. Appropriate bypassing techniques are also shown. LC filters can be substantially more effective than simple capacitors, especially in cases where it is not practical to route the positive rail directly from the supply. RC filtering forces voltage drop across the resistor, but is often acceptable due to the linear components low power requirements.

Application Note 11

In many cases it is not possible to arrange a "clean" supply for the linear components. In such circumstances it may be possible to synchronize noise sensitive linear circuit operations to occur between system clock pulses. This approach utilizes the synchronous nature of most digital systems and the fact that supply bus disturbances are often minimized between clock pulses.

Probably the most effective technique for dealing with digital supply noise is to galvanically isolate the linear circuits from the supply. The most obvious way to do this is provision of separate power supplies for the linear circuits, but this is often unacceptable. Instead, transformer and optical isolation circuit techniques allow logic rail driven, galvanically isolated circuits (see Figures 11, 12 and 14).



BYPASSING TECHNIQUES

TYPE	COMMENTS
	SIMPLE
	MORE COMPLEX BUT GOOD HIGH FREQUENCY REJECTION WITH LOW DC LOSSES. INAPPROPRIATE FOR USE WITH FAST LINEAR CIRCUITRY.
	RC FILTER EFFECTIVE FOR HIGH FREQUENCY REJECTION BUT HAS DC LOSSES. LOW CURRENT LINEAR CIRCUITS CAN ALLOW THIS APPROACH. DO NOT USE WITH FAST LINEAR.

Circuit Techniques for Clock Sources

Jim Williams

Almost all digital or communication systems require some form of clock source. Generating accurate and stable clock signals is often a difficult design problem.

Quartz crystals are the basis for most clock sources. The combination of high Q, stability vs time and temperature, and wide available frequency range make crystals a price-performance bargain. Unfortunately, relatively little information has appeared on circuitry for crystals and engineers often view crystal circuitry as a black art, best left to a few skilled practitioners (see box, "About Quartz Crystals").

In fact, the highest performance crystal clock circuitry does demand a variety of complex considerations and subtle implementation techniques. Most applications, however, don't require this level of attention and are relatively easy to serve. Figure 1 shows five (5) forms of simple crystal clocks. Types A through D are commonly referred to as gate oscillators. Although these types are popular, they are often associated with tempermental operation, spurious modes or outright failure to oscillate. The primary reason for this is the inability to reliably identify the analog characteristics of the gates used as gain elements. It is not uncommon in circuits of this type for gates from different manufacturers to produce markedly different circuit operation. In other cases, the circuit works, but is influenced by the status of other gates in the same package. Other circuits seem to prefer certain gate locations within the package. In consideration of these difficulties, gate oscillators are generally not the best possible choice in a production design; nevertheless, they offer low discrete component count, are used in a variety of situations, and bear mention. Figure 1A shows a CMOS Schmitt trigger biased into its linear region. The capacitor adds phase shift and the circuit oscillates at the crystal resonant frequency. Figure 1B shows a similar version for higher frequencies. The gate gives inverting gain, with the capacitors providing additional phase shift to produce oscillation. In Figure 1C, a TTL gate is used to allow the 10MHz operating frequency. The low input resistance of TTL elements does not allow the high value, single resistor biasing method. The R-C-R network shown is a replace-

ment for this function. Figure 1D is a version using two gates. Such circuits are particularly vulnerable to spurious operation but are attractive from a component count standpoint. The two linearly biased gates provide 360 degrees of phase shift with the feedback path coming through the crystal. The capacitor simply blocks DC in the gain path. Figure 1E shows a circuit based on discrete components. Contrasted against the other circuits, it provides a good example of the design flexibility and certainty available with components specified in the linear domain. This circuit will oscillate over a wide range of crystal frequencies, typically 2MHz to 20MHz.

The 2.2k and 33k resistors and the diodes compose a pseudo current source which supplies base drive.

At 25°C the base current is:

$$\frac{1.2V - 1V_{BE}}{33k} = 18\mu A$$

To saturate the transistor, which would stop the oscillator, requires V_{CE} to go to near zero. The collector current necessary to do this is:

$$I_C(\text{sat.}) = \frac{5V}{1k} \text{ (delete } V_{CE} \text{ sat.)}$$

$$= 5mA$$

with 18 μ A of base drive a beta of:

$$\frac{5mA}{18\mu A} = 278$$

is required.

At 1mA the DC beta spread of 2N3904's is 70 to \approx 210.

The transistor should not saturate...even at supply voltages below 3.0V.

In similar fashion, the effects of temperature may also be determined.

V_{BE} vs temperature over 25°C – 70°C is:

$$- 2.2mV/^{\circ}C \times 45^{\circ} = - 99mV.$$

Application Note 12

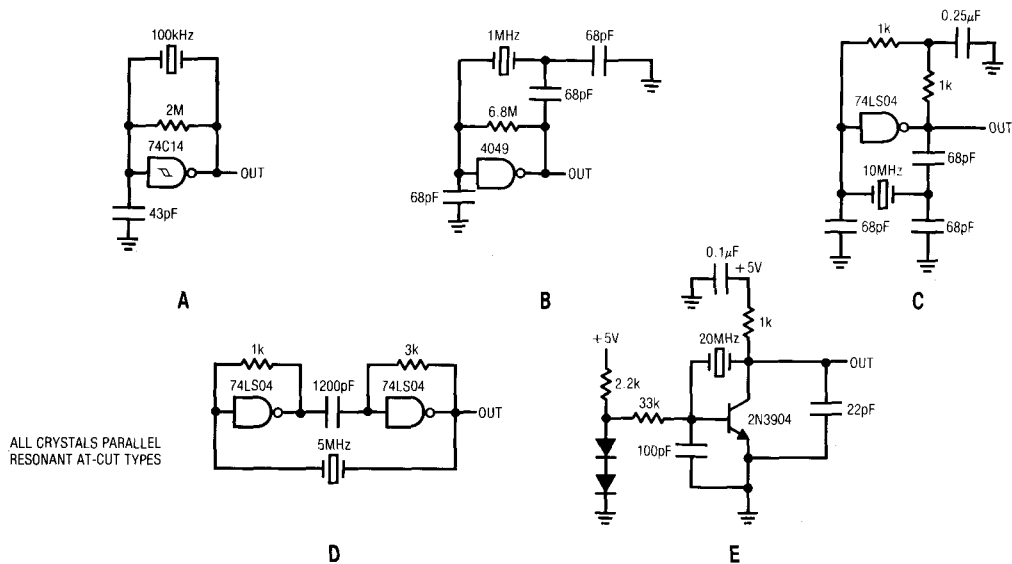


Figure 1. Typical Gate Oscillators and the Preferred Discrete Unit

The compliance voltage of the current source will move:

$$2 \times -2.2\text{mV}/^\circ\text{C} \times 45^\circ\text{C} = -198\text{mV}.$$

Hence, a first order compensation occurs:

$$-198\text{mV} - 99\text{mV} = -99\text{mV total shift}.$$

This remaining -99mV over temperature causes a shift in base current:

$$25^\circ\text{C current} = \frac{0.6\text{V}}{33\text{k}} = 18\mu\text{A}$$

$$70^\circ\text{C current} = \frac{0.5\text{V}}{33\text{k}} = 15\mu\text{A}$$

$$18\mu\text{A} - 15\mu\text{A} = 3\mu\text{A}.$$

This $3\mu\text{A}$ shift (about 16%) provides a compensation for transistor h_{FE} shift with temperature, which moves about 20% from 25°C to 70°C . Thus the circuit's behavior over temperature is quite predictable. The resistor, diode and V_{BE} tolerances mean that only first order compensations for V_{BE} and h_{FE} over temperature are appropriate.

Figure 2 shows another approach. This circuit uses a standard RC-comparator multivibrator circuit with the

crystal connected directly across the timing capacitor. Because the free running frequency of the circuit is close to the crystal's resonance, the crystal "steals" energy from the RC, forcing it to run at the crystal's frequency. The crystal activity is readily apparent in Trace A of Figure 3, which is the LT1011's "-" input. Trace B is the LT1011's output. In circuits of this type, it is important to ensure that enough current is available to quickly start the crystal resonating while, simultaneously, maintaining an RC time constant of appropriate frequency. Typically, the free running frequency should be set 5% to 10% above crystal resonance with a resistor feedback value calculated to allow about $100\mu\text{A}$ into the capacitor-crystal network. This type of circuit is not recommended for use above a few hundred kHz because of comparator delays.

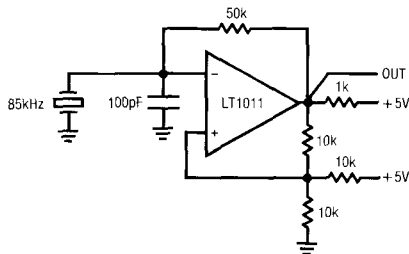


Figure 2. Crystal Stabilized Relaxation Oscillator

Figures 4A and 4B use another comparator based approach. In Figure 4A, the LT1016 comparator is set up with DC negative feedback. The 2k resistors set the common-mode level at the device's positive input. Without the crystal, the circuit may be considered as a very wideband (50GHz GBW) unity gain follower biased at 2.5V. With the crystal inserted, positive feedback occurs and oscillation commences. Figure 4A is useful with AT-cut fundamental mode crystals up to 10MHz. Figure 4B is similar, but supports oscillation frequencies to 25MHz. Above 10MHz, AT-cut crystals operate in overtone mode. Because of this,

oscillation can occur at multiples of the desired frequency. The damper network rolls off gain at high frequency, insuring proper operation.

All of the preceding circuits will typically provide temperature coefficients of 1ppm/°C with long term (1 year) stability of 5-10ppm. Higher stability is achievable with more attention to circuit design and control of temperature. Figure 5 shows a Pierce class circuit with fine frequency trimming provided by the paralleled fixed and variable capacitors. The transistor provides 180° of phase shift

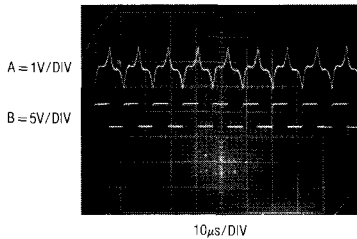


Figure 3. Figure 2's Waveforms

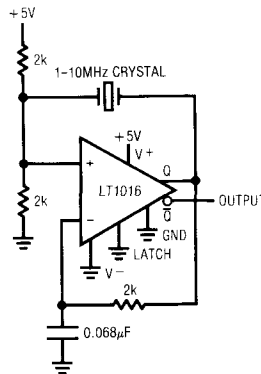


Figure 4A. 1-10MHz Crystal Oscillator

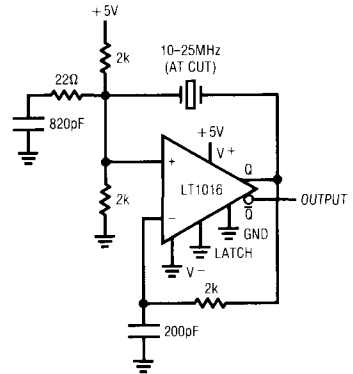
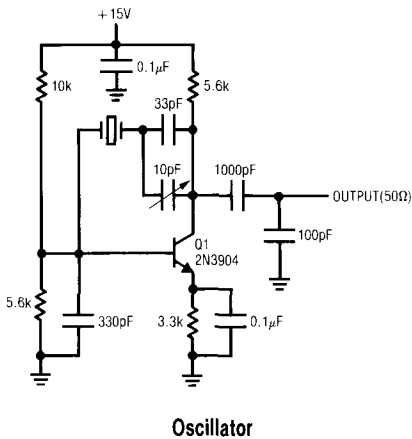
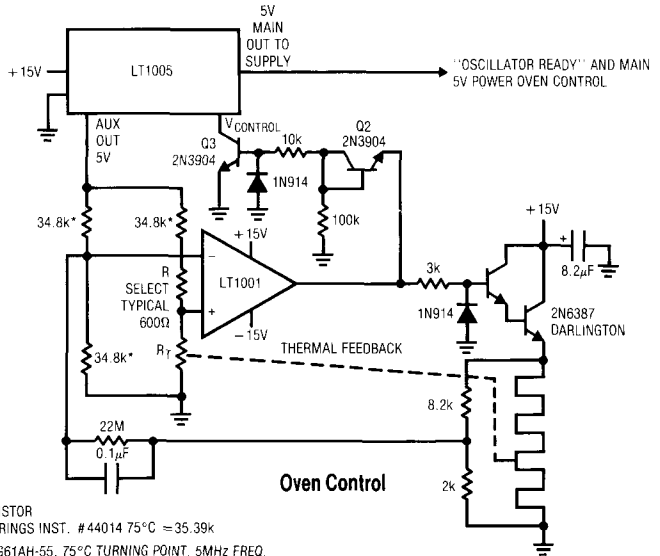


Figure 4B. 10-25MHz Crystal Oscillator



Oscillator



Oven Control

*TRW MAR-6 RESISTOR
 R_T = YELLOW SPRINGS INST. # 44014 75°C ≈ 35.39k
 = BLILEY # BG61AH-55, 75°C TURNING POINT, 5MHz FREQ.

Figure 5. Ovenized Oscillator

Application Note 12

with the loop components adding another 180° , resulting in oscillation. The LT1005 voltage regulator and the LT1001 op amp are used in a precision temperature servo to control crystal temperature. The LT1001 extracts the differential bridge signal and drives the Darlington stage to power the heater, which is monitored by the thermistor. In practice, the sensor is tightly coupled to the heater. The RC feedback values should be optimized for the thermal characteristics of the oven. In this case, the oven was constructed of aluminum tube stock 3" long \times 1" wide \times 1/8" thick. The heater windings were distributed around the cylinder and the assembly placed within a small insulating dewar flask. This allows 75°C setpoint (the zero TC or "turnover" temperature of the crystal specified) control of 0.05°C over 0°C - 70°C . The LT1005 regulator sources bridge drive from its auxiliary output and also keeps system power off until the crystal's temperature (hence, its frequency) is stabilized. When power is applied the negative TC thermistor is high in value, causing the LT1001 to saturate positive. This turns on zener-connected Q2, biasing Q3. Q3's collector current pulls the regulator's control pin low, disabling its output. When the oven arrives at its control point, the LT1001's output comes out of saturation and servo controls the oven at a point well below Q2's zener value. This turns off Q3, enabling the regulator to source power to whatever system the clock is associated

with. For the crystal and circuit values specified, this clock will drift less than 1×10^{-9} over 0°C - 70°C with a time drift of $1 \text{ part } 10^{-9} \text{ week}$.

The oven approach to removing temperature effects of crystal clock frequency is the most effective and in wide use. Ovens do, however, require substantial power and warm-up time. In some situations, this is unacceptable. Another approach to offsetting temperature effects is to measure ambient temperature and insert a scaled compensation factor into the crystal clock's frequency trimming network. This open loop correction technique relies on matching the clock frequency vs temperature characteristic, which is quite repeatable. Figure 6 shows a temperature compensated crystal oscillator (TXCO) which uses a first order linear fit to correct for temperature. The oscillator is a Colpitts type, with a capacitive tapped tank network. The LT319A picks off the output and the RC network at the LT319A's "—" input provides a signal adaptive trip threshold. The LT1005 regulator's auxiliary output buffers supply variations and the main regulator output control pin allows the system to be shut down without removing power from the oscillator, aiding overall stability. The ambient temperature is sensed by the linear thermistor network in A1's feedback loop with A2 used for scaling and offsetting. A2's voltage output expresses the ambient

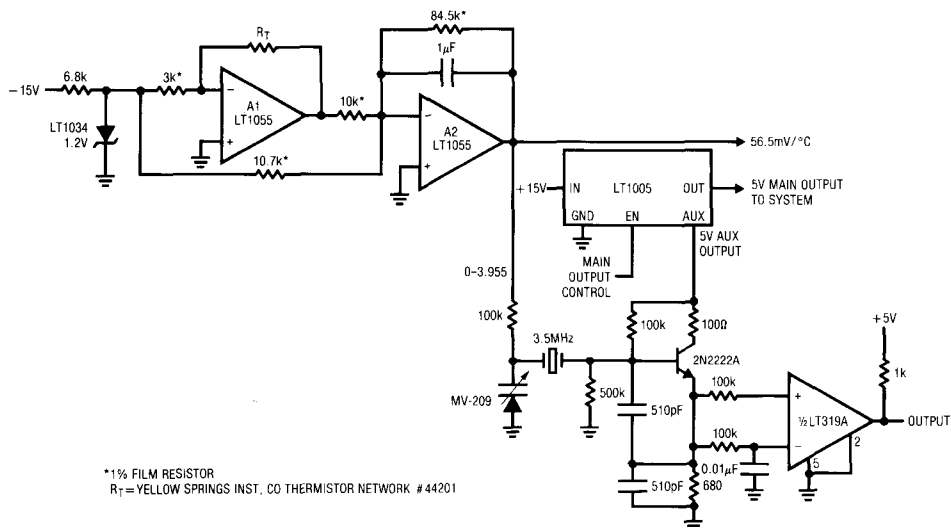


Figure 6. Temperature Compensated Crystal Oscillator (TXCO)

temperature information required to compensate the clock. The correction is implemented by biasing the varactor diode (a varactor diode's capacitance varies with reverse bias) which is in series with the crystal. The varactor's shift in capacitance is used to pull the crystal's frequency in a complementary fashion to the circuit's temperature error. If the thermistor is maintained isothermally with the circuit, compensation is very effective. Figure 7 shows the results. The -40ppm frequency shift over $0^\circ\text{C}-70^\circ\text{C}$ is corrected to within 2ppm . Better compensation is achievable by including 2nd and 3rd order terms in the temperature to voltage conversion to more accurately complement the non-linear frequency drift characteristic.

Figure 8 is another voltage-varactor tuned circuit but is configured to allow frequency shift instead of opposing it. This voltage controlled crystal oscillator (VXCO) has a

clean 20MHz sine wave output (Figure 9) suitable for communications applications. The curve of Figure 10 shows a 7kHz shift from 20MHz over the 10V tuning range. The 25pF trimmer sets the 20MHz zero bias frequency. In many applications, such as phase-locking and narrow bandwidth FM secure communications, the non-linear response is irrelevant. Improved linearity will require conditioning the tuning voltage or the varactor network's response. In circuits of this type it is important to remember that the limit on pulling frequency is set by the crystal's Q , which is high. Achieving wide dynamic "pull" range without stopping the oscillator or forcing it into abnormal modes is difficult. Typical circuits, such as this one, offer pull ranges of several hundred ppm. Larger shifts (e.g., $2000-3000\text{ppm}$) are possible without losing crystal lock, although clock output frequency stability suffers somewhat.

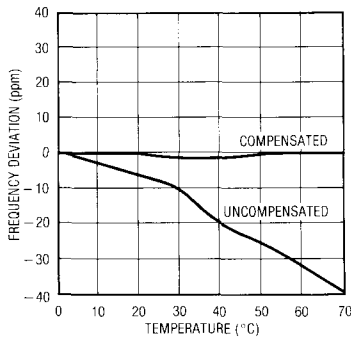


Figure 7. TXCO Drift Performance

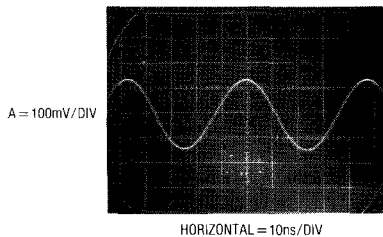


Figure 9. Figure 8's Output

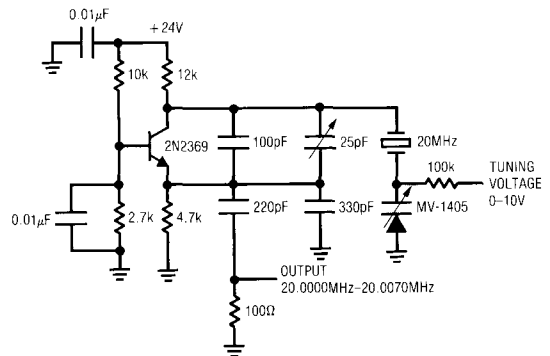


Figure 8. Voltage Controlled Crystal Oscillator (VXCO)

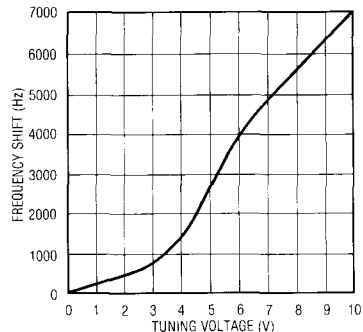


Figure 10. Figure 8's Tuning Characteristics

Application Note 12

Non-Crystal Clock Circuits

Although crystal based circuits are universally applied, they cannot serve all clock requirements. As an example, many systems require a reliable 60Hz line synchronous clock. Zero crossing detectors or simple voltage level detectors are often employed, but have poor noise rejection characteristics. The key to achieving a good line clock under adverse conditions is to design a circuit which takes advantage of the narrow bandwidth of the 60Hz fundamental. Approaches utilizing wide gain-bandwidth, even if hysteresis is applied, invite trouble with noise. Figure 11 shows a line synchronous clock which will not lose lock under noisy line conditions. The basic RC multivibrator is tuned to free run near 60Hz, but the AC-line-derived synchronizing input forces the oscillator to lock to the line. The circuit derives its noise rejection from the integrator characteristics of the RC network. As Figure 12 shows, noise and fast spiking on the 60Hz input (Trace A, Figure 12) has little effect on the capacitor's charging characteristics (Trace B, Figure 12) and the circuit's output (Trace C, Figure 12) is stable.

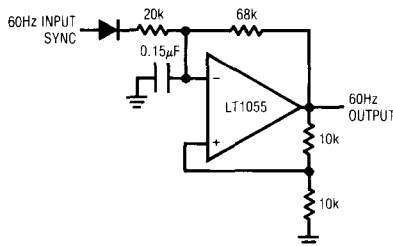


Figure 11. Synchronized Oscillator

Figure 13 is another synchronous clock circuit. In this instance, the circuit output locks at a higher frequency than the synchronizing input. Circuit operation is the time domain equivalent of a reset stabilized DC amplifier. The LT1055 and its associated components form a stable oscillator. The LM329 diode bridge and compensating diodes provide a stable bipolar charging source for the RC located at the amplifier's negative input. The synchronizing pulse (Trace A, Figure 14) is level shifted by the LT1011 comparator to drive the FET. When the synchronizing pulse appears, the FET turns on, grounding the capacitor (Trace B, Figure 14). This interrupts normal oscillator action, but only for a small fraction of a cycle. When the sync pulse falls, the capacitor's charge cycle, which has been reset to 0V, starts again. This resetting action forces the frequency of the RC charging to be synchronous and stabilized by the sync pulse. The only evidence of this operation at the output is an occasional, slightly enlarged pulse width (Trace C, Figure 14), which is caused by the synchronizing interval. The sync adjust potentiometer should

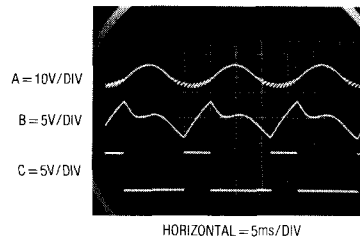


Figure 12. Figure 11's Waveforms

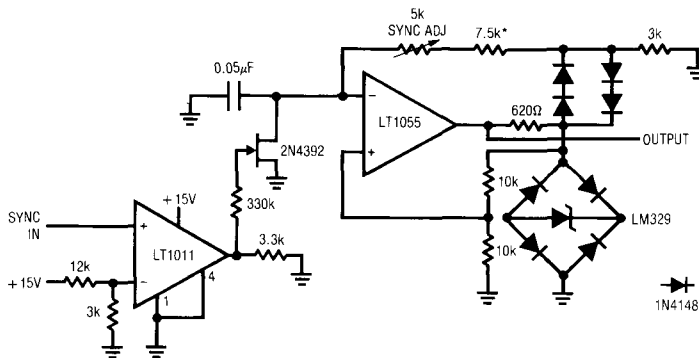


Figure 13. Reset Stabilized Oscillator

be trimmed so the sync pulse appears when the capacitor is near 0V. This minimizes output waveform width deviation and allows maximum protection against losing lock due to RC drift over time and temperature. The maximum practical output frequency to sync frequency ratio is about 50 x.

Pure RC oscillators are a final form of clock circuit. Although this class of circuit cannot achieve the stability of a synchronized or crystal based approach, it offers simplicity, economy and direct low frequency output. As such they are used in baud rate generators and other low frequency applications. The key to designing a stable RC oscillator is to make output frequency insensitive to drift in as many circuit elements as possible. Figure 15 shows an RC clock circuit which depends primarily on the RC elements for stability. All other components contribute very low order error terms, even for substantial shifts. In addition, the RC components have been chosen for opposing temperature coefficients, further aiding stability. The circuit is a standard comparator-multivibrator with parallel CMOS inverters interposed between the comparator output and the feedback resistors. This replaces the relatively large and unstable bipolar V_{CE} saturation losses of the

LT1011 output with the superior ON characteristics of MOS. Not only are the MOS switching losses to the rails low and resistive, but they tend to cancel. The paralleling of inverters further reduces errors to insignificant levels. With this arrangement, the charge and discharge time constant of the capacitor is almost totally immune from supply and temperature shifts. The 10k Ω units need not be precision types, because shifts in them will cancel. In addition, the effect of the comparator's DC input errors is also negated because of the symmetrical nature of the oscillator. This leaves only the RC network as a significant error term. The nominal $-120\text{ppm}/^\circ\text{C}$ temperature coefficient of the polystyrene capacitor is partially offset by the opposing positive temperature coefficient designed into the specified resistor. In practice, only a first order compensation is achievable because of the uncertainty of the capacitor's exact TC. For the test circuit, $0^\circ\text{C}-70^\circ\text{C}$ temperature excursion showed a $15\text{ppm}/^\circ\text{C}$ TC with a power supply rejection factor of less than $20\text{ppm}/\text{V}$. In contrast, a clock constructed from the popular 555 timer, using the compensating RC network, showed $95\text{ppm}/^\circ\text{C}$ and $1050\text{ppm}/\text{V}$ of supply shift. Because of comparator propagation delays, circuits of this type are less stable above a 5kHz-10kHz operating frequency.

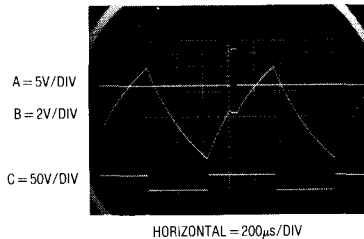
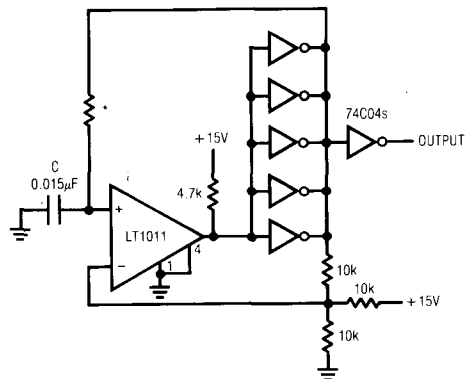


Figure 14. Figure 13's Waveforms

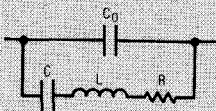


*TRW TYPE MTR-5/ $+120\text{ppm}/^\circ\text{C}$
 $C = 0.015\mu\text{F} = \text{POLYSTYRENE} -120\text{ppm}/^\circ\text{C} \pm 30\text{ppm WESCO TYPE 32-P}$

Figure 15. Stable RC Oscillator

About Quartz Crystals

The frequency stability and repeatability of quartz crystals represent one of nature's best bargains for the circuit designer. The equivalent circuit of a crystal looks like a series-parallel combination of elements.



Typical Values:

$$R = 100\Omega$$

$$L = 500\mu\text{H}$$

$$C = 0.01\text{pF}$$

$$C_0 = 5\text{pF}$$

$$Q = 50,000$$

C_0 is the static capacitance produced by the contact wires, crystal electrodes and the crystal holder. The RLC term is called the motional arm. C is the mechanical mass. R includes all electrical losses in the crystal and L is the reactive component of the quartz. Different angles of cut from the mother crystal produce different electrical characteristics in individual crystals. Cuts can be optimized for temperature coefficient, frequency range and other parameters. The basic "AT" cut used in most crystals in the 1MHz-150MHz range is a good compromise between temperature coefficient, frequency range, ease of manufacture and other considerations. Other factors affecting

resonator performance include the method of lead attachment, package sealing method and internal environment (e.g., vacuum, partial pressure, etc.). Some circuit considerations when using crystals include:

Load Capacitance—The reactance the crystal must present to the circuit. Some circuits use the crystal in the parallel resonant mode (e.g., the crystal looks inductive). Other circuits are specified as series resonant and the crystal appears resistive. In this mode, the circuit's load capacitance, including all parasitics, must be specified. A typical number is around 30pF.

Resistance—The impedance the crystal presents when it is resonating.

Drive Level—How much power may be dissipated in the crystal and still maintain all specifications. 10mW is typical. Excessive levels can fracture the crystal.

Temperature Coefficient/Turning Point—The tempco of the crystal is usually specified near the "turning point." This is the temperature at which the crystal tempco is zero. Typically the tempco will be below 1ppm/°C over the operating range and the turning point around 75°C, although different cuts can considerably alter these numbers.

Frequency Tolerance—The deviation from ideal frequency when used under specified circuit conditions at a defined temperature. Tolerances vary from 50ppm to less than 1ppm.

High Speed Comparator Techniques

Jim Williams

INTRODUCTION

Comparators may be the most underrated and underutilized monolithic linear component. This is unfortunate because comparators are one of the most flexible and universally applicable components available. In large measure the lack of recognition is due to the IC op amp, whose versatility allows it to dominate the analog design world. Comparators are frequently perceived as devices which crudely express analog signals in digital form—a 1-bit A-D converter. Strictly speaking, this viewpoint is correct. It is also wastefully constrictive in its outlook. Comparators don't "just compare" in the same way that op amps don't "just amplify".

Comparators, in particular high speed comparators, can be used to implement linear circuit functions which are as sophisticated as any op amp-based circuit. Judiciously combining a fast comparator with op amps is a key to achieving high performance results. In general, op amp-based circuits capitalize on their ability to close a feedback loop with precision. Ideally, such loops are maintained continuously over time. Conversely, comparator circuits are often based on speed and have a discontinuous output over time. While each approach has its merits, a fusion of both yields the best circuits.

This effort's initial sections are devoted to familiarizing the reader with the realities and difficulties of high speed comparator circuit work. The mechanics and subtleties of

achieving precision circuit operation at DC and low frequency have been well documented. Relatively little has appeared which discusses, in practical terms, how to get fast circuitry to work. In developing such circuits, even the most veteran designers sometimes feel that nature is conspiring against them. In some measure this is true. Like all engineering endeavors, high speed circuits can only work if negotiated compromises with nature are arranged. Ignorance of, or contempt for, physical law is a direct route to frustration. In this regard, much of the text and appendices are directed at developing awareness of and respect for circuit parasitics and fundamental limitations. This approach is maintained in the applications section, where the notion of "negotiated compromises" is expressed in terms of resistor values and compensation techniques. Many of the application circuits use the LT1016's speed to improve on a standard circuit. Some utilize the speed to implement a traditional function in a non-traditional way, with attendant advantages. A (very) few operate at or near the state-of-the-art for a given circuit type, regardless of approach. Substantial effort has been expended in developing these examples and documenting their operation. The resultant level of detail is justified in the hope that it will be catalytic. The circuits should stimulate new ideas to suit particular needs, while demonstrating the LT1016's capabilities in an instructive manner.

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THE LT1016 — AN OVERVIEW

A new ultra high speed comparator, the LT1016, features TTL-compatible complementary outputs and 10ns response time. Other capabilities include a latch pin and good DC input characteristics (see Figure 1). The LT1016's outputs directly drive all TTL families, including the new higher speed ASTTL and FAST parts. Additionally, TTL outputs make the device easier to use in linear circuit applications where ECL output levels are often inconvenient.

A substantial amount of design effort has made the LT1016 relatively easy to use. It is much less prone to oscillation and other vagaries than some slower comparators, even with slow input signals. In particular, the LT1016 is stable in its linear region, a feature no other high speed comparator has. Additionally, output stage switching does not appreciably change power supply current, further enhancing stability. These features make the application of the 200GHz gain-bandwidth LT1016 considerably easier than other fast comparators. Unfortunately, laws of physics dictate that the circuit environment the LT1016 works in must be properly prepared. The performance limits of high speed circuitry

are often determined by parasitics such as stray capacitance, ground impedance, and layout. Some of these considerations are present in digital systems where designers are comfortable describing bit patterns and memory access times in terms of nanoseconds. The LT1016 can be used in such fast digital systems and Figure 2 shows just how fast the device is. The simple test circuit allows us to see that the LT1016's (Trace B) response to the pulse generator (Trace A) is faster than a TTL inverter (Trace C)! In fact, the inverter's output never gets to a TTL "0" level. Linear circuits operating with this kind of speed make many engineers justifiably wary. Nanosecond domain linear circuits are widely associated with oscillations, mysterious shifts in circuit characteristics, unintended modes of operation and outright failure to function.

Other common problems include different measurement results using various pieces of test equipment, inability to make measurement connections to the circuit without inducing spurious responses and dissimilar operation between two "identical" circuits. If the components used

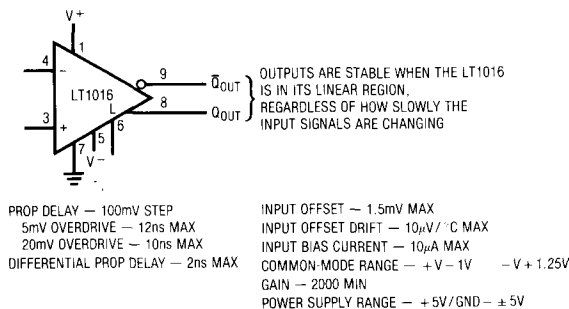


Figure 1. The LT1016 at a Glance

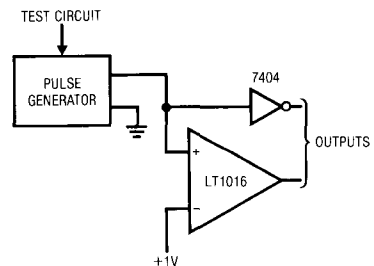
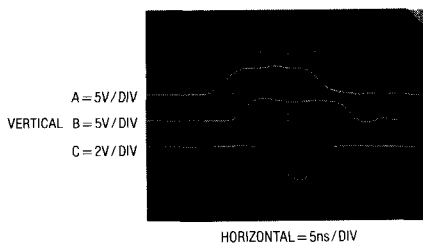


Figure 2. LT1016 vs a TTL Gate

Application Note 13

in the circuit are good and the design is sound, all of the above problems can usually be traced to failure to provide a proper circuit "environment." To learn how to do this requires studying the causes of the aforementioned difficulties.

The Rogue's Gallery of High Speed Comparator Problems

By far the most common error involves power supply bypassing. Bypassing is necessary to maintain low supply impedance. DC resistance and inductance in supply wires and PC traces can quickly build up to unacceptable levels. This allows the supply line to move as internal current levels of the devices connected to it change. This will almost always cause unruly operation. In addition, several devices connected to an unbypassed supply can "communicate" through the finite supply impedances, causing erratic modes. Bypass capacitors furnish a simple way to eliminate this problem by providing a local reservoir of energy at the device. The bypass capacitor acts like an electrical flywheel to keep supply impedance low at high frequencies. The choice of what type of capacitors to use for bypassing is a critical issue and should be approached carefully (see Appendix A, "About Bypass Capacitors"). An unbypassed LT1016 is shown responding to a pulse input in Figure 3. The power supply the LT1016 sees at its terminals has high impedance at high frequency. This impedance forms a voltage divider with the LT1016, allowing the supply to move as internal conditions in the comparator change. This causes local

feedback and oscillation occurs. Although the LT1016 responds to the input pulse, its output is a blur of 100MHz oscillation. *Always use bypass capacitors.*

In Figure 4 the LT1016's supplies are bypassed, but it still oscillates. In this case, the bypass units are either too far from the device or are lossy capacitors. *Use capacitors with good high frequency characteristics and mount them as close as possible to the LT1016. An inch of wire between the capacitor and the LT1016 can cause problems.*

In Figure 5 the device is properly bypassed but a new problem pops up. This photo shows both outputs of the comparator. Trace A appears normal, but Trace B shows an excursion of almost 8V — quite a trick for a device running from a +5V supply. This is a commonly reported problem in high speed circuits and can be quite confusing. It is not due to suspension of natural law, but is traceable to a grossly miscompensated or improperly selected oscilloscope probe. *Use probes which match your oscilloscope's input characteristics and compensate them properly* (for a discussion on probes, see Appendix B, "About Probes and Scopes"). Figure 6 shows another probe-induced problem. Here, the amplitude seems correct but the 10ns response time LT1016 appears to have 50ns edges! In this case, the probe used is too heavily compensated or slow for the oscilloscope. Never use 1X or "straight" probes. Their bandwidth is 20MHz or less and capacitive loading is high. *Check probe bandwidth to ensure it is adequate for the measurement. Similarly, use an oscilloscope with adequate bandwidth.*

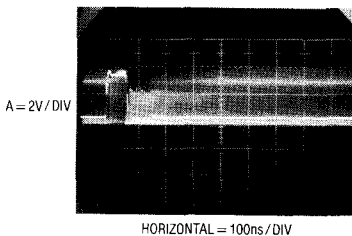


Figure 3. Unbypassed LT1016 Response

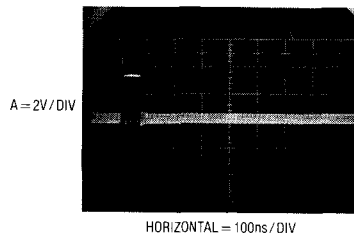


Figure 4. LT1016 Response with Poor Bypassing

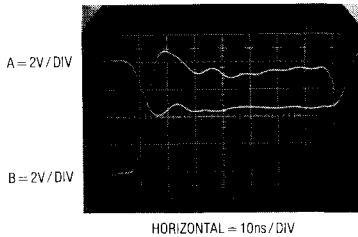


Figure 5. Improper Probe Compensation Causes Seemingly Unexplainable Amplitude Error

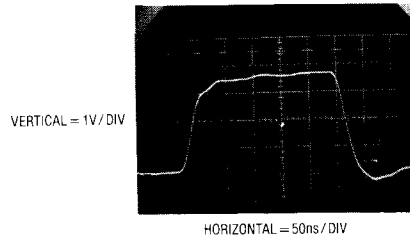


Figure 6. Overcompensated or Slow Probes Make Edges Look Too Slow

In Figure 7 the probes are properly selected and applied but the LT1016's output rings and distorts badly. In this case, the probe ground lead is too long. For general purpose work most probes come with ground leads about 6 inches long. At low frequencies this is fine. At high speed, the long ground lead looks inductive, causing the ringing shown. High quality probes are always supplied with some short ground straps to deal with this problem. Some come with very short spring clips which fix directly to the probe tip to facilitate a low impedance ground connection. For fast work, the ground connection to the probe should not exceed 1 inch in length. *Keep the probe ground connection as short as possible.*

The difficulty in Figure 8 is delay and inadequate amplitude (Trace B). A small delay on the leading edge is followed by a large delay before the falling edge begins.

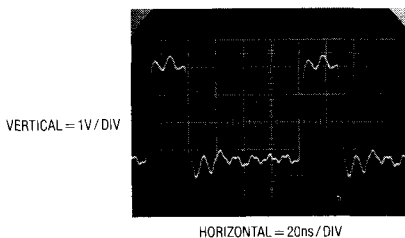


Figure 7. Typical Results Due to Poor Probe Grounding

Additionally, a lengthy, tailing response stretches 70ns before finally settling out. The amplitude only rises to 1.5V. A common oversight is responsible for these conditions.

A FET probe monitors the LT1016 output in this example. The probe's common-mode input range has been exceeded, causing it to overload and clip the output badly. The small delay on the rising edge is characteristic of active probes and is legitimate. During the time the output is high, the probe is driven deeply into saturation. When the output falls, the probe's overload recovery is lengthy and uneven, causing the delay and tailing.

Know your FET probe. Account for the delay of its active circuitry. Avoid saturation effects due to common-mode input limitations (typically $\pm 1V$). Use 10X and 100X attenuator heads when required.

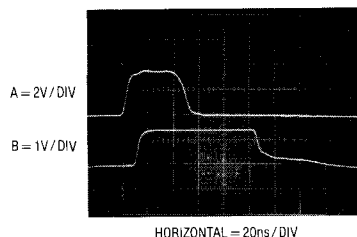


Figure 8. Overdriven FET Probe Causes Delayed, Tailing Response

Application Note 13

Figure 9 shows the LT1016's output (Trace B) oscillating near 40MHz as it responds to an input (Trace A). Note that the input signal shows artifacts of the oscillation. This example is caused by improper grounding of the comparator. In this case, the LT1016's ground pin connection is 1 inch long. The ground lead of the LT1016 must be as short as possible and connected directly to a low impedance ground point. Any substantial impedance in the LT1016's ground path will generate effects like this. The reason for this is related to the necessity of bypassing the power supplies. The inductance created by a long device ground lead permits mixing of ground currents, causing undesired effects in the device. The solution here is simple. *Keep the LT1016's ground pin connection as short (typically 1/4 inch) as possible and run it directly to a low impedance ground. Do not use sockets.*

Figure 10 addresses the issue of the "low impedance ground," referred to previously. In this example, the output is clean except for chattering around the edges. This photograph was generated by running the LT1016 without a "ground plane." A ground plane is formed by using

a continuous conductive plane over the surface of the circuit board (the theory behind ground planes is discussed in Appendix C). The only breaks in this plane are for the circuit's necessary current paths. The ground plane serves two functions. Because it is flat (AC currents travel along the surface of a conductor) and covers the entire area of the board, it provides a way to access a low inductance ground from anywhere on the board. Also, it minimizes the effects of stray capacitance in the circuit by referring them to ground. This breaks up potential unintended and harmful feedback paths. *Always use a ground plane with the LT1016.*

"Fuzz" on the edges is the difficulty in Figure 11. This condition appears similar to Figure 10, but the oscillation is more stubborn and persists well after the output has gone low. This condition is due to stray capacitive feedback from the outputs to the inputs. A 3k Ω input source impedance and 3pF of stray feedback allowed this oscillation. The solution for this condition is not too difficult. *Keep source impedances as low as possible, preferably 1k Ω or less. Route output and input pins and components away from each other.*

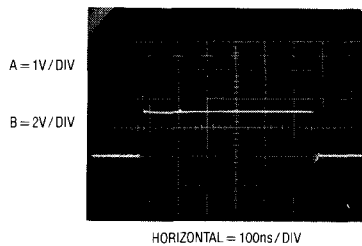


Figure 9. Excessive LT1016 Ground Path Resistance Causes Oscillation

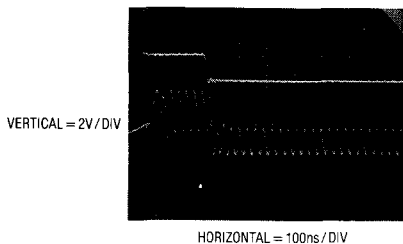


Figure 10. Transition Instabilities Due to No Ground Plane

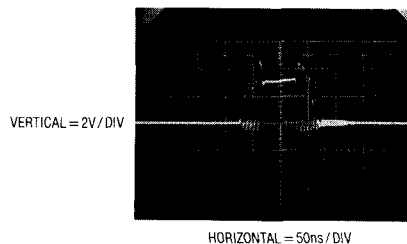


Figure 11. 3pF Stray Capacitive Feedback with 3k Ω Source Can Cause Oscillation

The opposite of stray-caused oscillations appears in Figure 12. Here, the output response (Trace B) badly lags the input (Trace A). This is due to some combination of high source impedance and stray capacitance to ground at the input. The resulting RC forces a lagged response at the input and output delay occurs. An RC combination of $2k\Omega$ source resistance and $10pF$ to ground gives a $20ns$ time constant — significantly longer than the LT1016's response time. *Keep source impedances low and minimize stray input capacitance to ground.*

Figure 13 shows another capacitance-related problem. Here the output does not oscillate, but the transitions are discontinuous and relatively slow. The villain of this situation is a large output load capacitance. This could be caused by cable driving, excessive output lead length or the input characteristics of the circuit being driven. In most situations this is undesirable and may be eliminated by buffering heavy capacitive loads. In a few circumstances it may not affect overall circuit operation and is tolerable. *Consider the comparator's output load characteristics and their potential effect on the circuit. If necessary, buffer the load.*

Another output-caused fault is shown in Figure 14. The output transitions are initially correct but end in a ringing condition. The key to the solution here is the ringing. What is happening is caused by an output lead which is too long. The output lead looks like an unterminated transmission line at high frequencies and reflections occur. This accounts for the abrupt reversal of direction on the leading edge and the ringing. If the comparator is driving TTL this may be acceptable, but other loads may not tolerate it. In this instance, the direction reversal on the leading edge might cause trouble in a fast TTL load. *Keep output lead lengths short. If they get much longer than a few inches, terminate with a resistor (typically 250Ω – 400Ω).*

A final malady is presented in Figure 15. These waveforms are reminiscent of the input RC-induced delay of Figure 12. The output waveform initially responds to the input's leading edge, but then returns to zero before going high again. When it does go high, it slews slowly. Additional odd characteristics include pronounced overshoot and pulse top aberration. The fall time is also slow and well delayed from the input. This is certainly strange

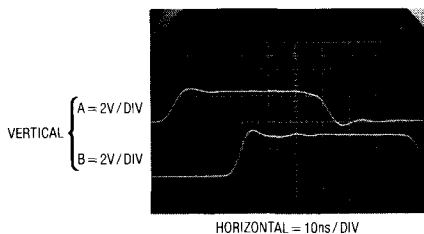


Figure 12. Stray 5pF Capacitance from Input to Ground Causes Delay

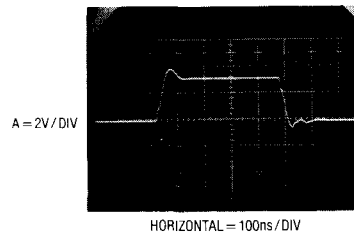


Figure 13. Excessive Load Capacitance Forces Edge Distortion

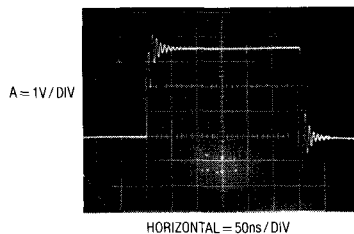


Figure 14. Lengthy, Unterminated Output Lines Ring from Reflections

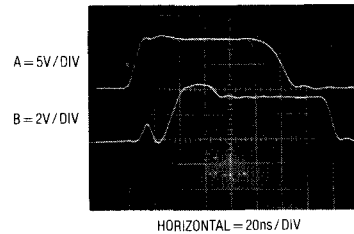


Figure 15. Input Common-Mode Overdrive Generates Odd Outputs

Application Note 13

behavior from a TTL output. What is going on here? The input pulse is responsible for all these anomalies. Its 10V amplitude is well outside the +5V powered LT1016's common-mode input range. Internal input clamps prevent this pulse from damaging the LT1016, but an overdrive of this magnitude results in poor response. *Keep input signals inside the LT1016's common-mode range at all times.*

Oscilloscopes

A few of the examples illustrated dealt with probe-caused problems. Although it should be obvious, it is worth mentioning that the choice of oscilloscope employed is crucial. Be certain of the characteristic of the probe-oscilloscope combination you are using. Rise time, bandwidth, resistive and capacitive loading, delay, overdrive recovery and other limitations must be kept in mind. High speed linear circuitry demands a great deal from test equipment and countless hours can be saved if the characteristics of the instruments used are well known (see Appendix C, "Measuring Equipment Response"). In fact, it is possible to use seemingly inadequate equipment to get good results if the equipment's limitations are well known and respected. All of the applications which follow involve rise times and delays well above the

100MHz–200MHz region, but 90% of the development work was done with a 50MHz oscilloscope. Familiarity with equipment and thoughtful measurement technique permit useful measurements seemingly beyond instrument specifications. A 50MHz oscilloscope cannot track a 5ns rise time pulse, but it can measure a 2ns delay between two such events. Using such techniques, it is often possible to deduce the desired information. There are situations where no amount of cleverness will work and the right equipment, e.g., a faster oscilloscope, must be used.

In general, use equipment you trust and measurement techniques you understand. Keep asking questions and don't be satisfied until everything you see on the oscilloscope is accounted for and makes sense.

The LT1016, combined with the precautionary notes listed above, permits fast linear circuit functions which are difficult or impossible using other approaches. Many of the applications presented represent the state-of-the-art for a particular circuit function. Some show new and improved ways to implement standard functions by utilizing the LT1016's speed. All have been carefully (and painfully) worked out and should serve as good idea sources for potential users of the device.

APPLICATIONS SECTION

1Hz–10MHz V→F Converter

The LT1016 and the LT1012 low drift amplifier combine to form a high speed V→F converter in Figure 16. A variety of circuit techniques is used to achieve a 1Hz to 10MHz output. Overrange to 12 MHz ($V_{IN} = 12V$) is provided. This circuit has a wider dynamic range (140dB, or 7 decades) than any commercially available unit. The 10MHz full-scale frequency is 10 times faster than currently available monolithic V→Fs. The theory of operation is based on the identity $Q = CV$.

Each time the circuit produces an output pulse, it feeds back a fixed quantity of charge (Q) to a summing node (Σ). The circuit's input furnishes a comparison current at the summing node. The difference signal at the node is integrated in a monitoring amplifier's feedback capacitor.

The amplifier controls the circuit's output pulse generator, completing a feedback loop around the integrating amplifier. To maintain the summing node at zero, the pulse generator runs at a frequency which permits enough charge pumping to offset the input signal. Thus, the output frequency will be linearly related to the input voltage. A1 is the integrating amplifier.

For low bias, high speed operation, a pair of discrete FETs directly drives A1's output stages, replacing A1's monolithic input circuitry. A1's input stage is turned off by connecting the input pins to the negative 15V rail. The FET gates become the "+" and "-" inputs of the amplifier. $0.2\mu V/^\circ C$ offset drift performance is obtained by stabilizing the A1-FET combination with A2, a precision op amp. A2 measures the DC value of the negative

input, compares it to ground, and forces the positive input to maintain offset balance in the A1-FET combination. Note that A2 is configured as an integrator and cannot see high frequency signals. It functions only at DC and low frequency. The A1-FET combination is arranged as an integrator with a 100pF feedback capacitor. When a positive voltage is applied to the input, A1's output integrates in a negative direction (Trace A, Figure 17). Dur-

ing this period, C1's inverting output is low. A very high speed level shifter, Q1-Q2 (see Appendix D, "About Level Shifters"), inverts this output and drives the zener reference bridge. The bridge's positive output is used to charge the 33pF capacitor. The 1.2V diode string provides cancellation and temperature compensation for the diode drops in the bridge so that the 33pF unit charges to $V_Z + V_{BE} Q3$.

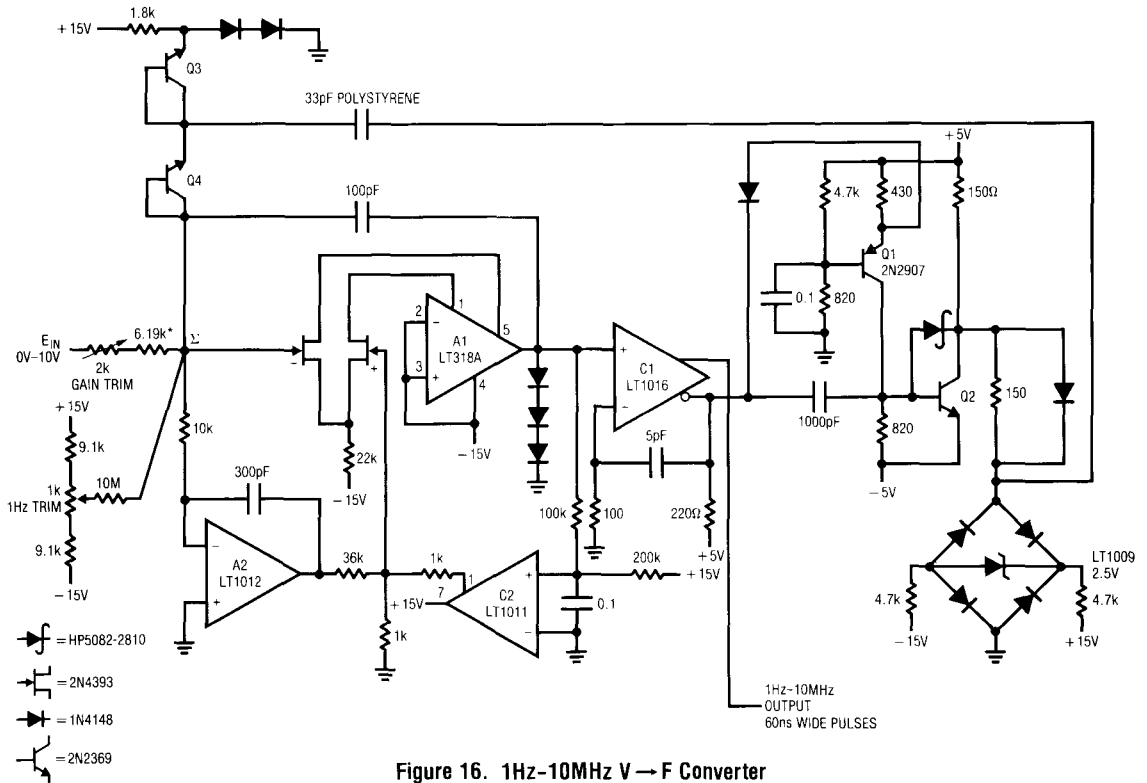


Figure 16. 1Hz-10MHz V → F Converter

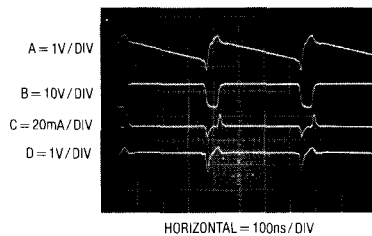


Figure 17. 10MHz V → Fs Operating Waveforms

Application Note 13

When A1's output crosses zero, C1's inverting output goes high and Q2's (Trace B) collector goes to $-5V$. This causes the 33pF unit to dispense charge into the summing node via Q4's V_{BE} . The amount of charge dispensed is a direct function of the voltage that the 33pF unit was charged to ($Q = CV$). Q4's V_{BE} compensates the Q3 V_{BE} term in the capacitor's charge equation. The current which flows through the 33pF unit (Trace C) reflects this charge pumping action. The removal of current from A1's summing junction (Trace D) causes the junction to be driven very quickly negative. The initial negative-going 20ns transient at A1's output is due to amplifier delay. The input signal feeds directly through the feedback capacitor and appears at the output. When the amplifier finally responds, its output (Trace A) slew limits as it attempts to regain control of the summing node. The amount of time Q2's collector (Trace B) remains at $-5V$ depends on how long it takes A1 to recover and the 5pF-100 Ω hysteresis network at C1. This 60ns interval is long enough for the 33pF unit to fully discharge. After this, C1 changes state and Q2's collector swings positive. The capacitor is recharged and the entire cycle repeats. The frequency at which this oscillation occurs is directly related to the voltage-input-derived current into the summing junction. Any input current will require a corresponding oscillation frequency to hold the summing point at an average value of 0V.

Maintaining this relationship at megahertz frequencies places severe restrictions on circuit timing. The key to achieving 10MHz full-scale operating frequency is the ability to transmit information around the loop as quickly as possible. The discharge-reset sequence is particularly critical and is detailed in Figure 18. Trace A is the A1 integrator output. Its ramp output crosses 0V at the first left vertical graticule division. A few nanoseconds later, C1's inverting output begins to rise (Trace B), driving the Q1-Q2 level shifter output negative (Trace C). Q2's collector begins to head negative about 12ns after A1's output crosses 0V. 4ns later, the summing point (Trace D) begins to go negative as current is pulled from it through the 33pF capacitor. At 25ns, C1's inverting output is fully up, Q2's collector is at $-5V$, and the summing point has been pulled to its negative extreme. Now, A1 begins to take control. Its output (Trace A) slews rapidly in the

positive direction, restoring the summing point. At 60ns, A1 is in control of the summing node and the integration ramp begins again.

Start-up and overdrive conditions could force A1's output to go to the negative rail and stay there. The AC-coupled nature of the charge dispensing loop can preclude normal operation and the circuit may latch. C2 provides a "watchdog" function for this condition. If A1's output tries to go too far below zero, C2 switches, forcing the "+" input FET gate positive. This causes A1's output to slew positive, initiating normal circuit action. The diode chain at C1's input prevents common-mode overdrive at the LT1016. To trim this circuit, ground the input and adjust the 1k pot for 1Hz output. Next, apply 10.000V and set the 2k Ω unit for 10.000MHz output. The transfer linearity of the circuit is 0.06%. Full-scale drift is typically 50ppm/ $^{\circ}C$ and zero point error about 0.2 μV / $^{\circ}C$ (0.2Hz/ $^{\circ}C$).

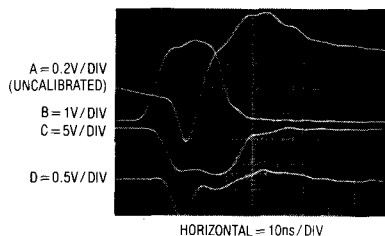


Figure 18. Detail of 60ns Reset Sequence (Whoosh!)

Quartz-Stabilized 1Hz-30MHz V \rightarrow F Converter

Figure 16's upper limit on operating frequency is imposed by delays in the active elements in the LT1016's feedback path. Higher speed is possible by minimizing these delays. Figure 19 shows a way to do this while retaining good drift and linearity characteristics. The circuit's untrimmed 150dB dynamic range is 1000 times greater than commercially available V \rightarrow F converters, whether monolithic, hybrid, or modular.

The technique employed allows the LT1016 to roar along at a 30MHz full-scale output frequency, substantially faster than any commercially available V \rightarrow F. The actual V \rightarrow F conversion is performed by the circuit shown inside the dashed lines. This circuit functions similarly to Figure 16.

The level shift and zener bridge are eliminated. Q1 charges the 200pF capacitor, which is unloaded by the Q2-Q3 buffer. When the LT1016's negative input rises above its positive input, its output goes low, pulling charge out of the capacitor via Q4, which serves as a low leakage diode. The 2.7pF capacitor provides positive feedback. If the left end of the 100k input resistor is driven from a voltage source, the LT1016 oscillates over a 1Hz to 30MHz range. Although this simple circuit is fast, its linearity is poor and drift exceeds 5000ppm/°C.

The remaining components in Figure 19 form a quartz-locked sampled-data loop to correct these terms without sacrificing speed. The loop works by counting the number of pulses at the LT1016's output during a fixed interval and converting this information to a voltage. The voltage is compared to the circuit's input by an amplifier which drives the LT1016 V→F circuit. This closed loop technique relies on the stability of the time interval and the digital-to-voltage conversion to achieve circuit stability. Frequent updating of the loop ensures long term stability. Figure 20 shows how the circuit functions.

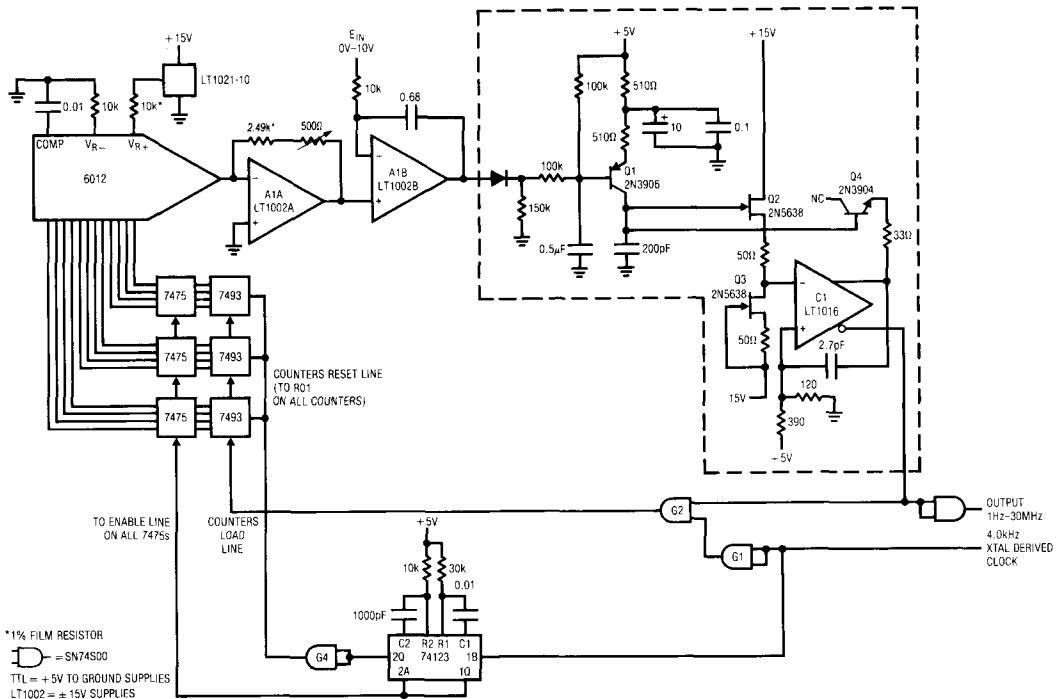


Figure 19. 30MHz V → F Utilizes Sampled Loop for High Stability and Linearity

Application Note 13

Waveforms A, B and C are the LT1016's negative input, output and positive input, respectively. Their similarity to Figure 17 (Traces A, B and C) reflects the two circuits' commonality of operation. Trace D shows the quartz-crystal-derived 4kHz clock. During the clock's low portion, the LT1016's gated output appears at G2's output (Trace E). This data is loaded into counters which drive a 12-bit DAC via the 7475 latches. When the clock goes high, one section of the 74123 one-shot generates a pulse (Trace F), allowing the latches to acquire the counter's data. After this pulse goes low, the one-shot's second half pulses (Trace G) the counter's reset line. At the clock's next falling edge the entire cycle repeats. The DAC and its associated output amplifier (A1A) provide a voltage representation of the digital word at the 7475 outputs. This voltage is compared to the circuit's input by A1B, whose output drives the LT1016-based $V \rightarrow F$. Any drift or nonlinearity in the $V \rightarrow F$ will be corrected by the feedback action of this stabilizing loop. The $10k-0.68\mu F$ time constant at A1B provides loop compensation.

Although it is not obvious, the frequency setting resolution is much greater than the 12-bit quantization limit of the DAC. This is because the DAC's output dithering around the LSB is integrated to a pure DC level by loop time constants. Once the DAC has settled within an LSB, its output acts like a 4kHz clocked pulse width modulator. The slow loop time constants integrate the width-modulated information to DC, affording smooth, continuous frequency setting capability. The practical limit on resolution is due to the LT1016 oscillator's short term jitter and is about 25ppm of reading.

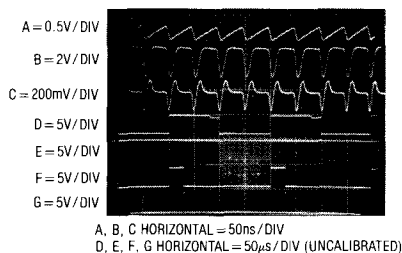


Figure 20. Waveforms for Figure 19. Sampled Data Loop (Traces D-G) Stabilizes Basic $V \rightarrow F$ (Traces A-C)

Although this approach allows higher speeds than Figure 16, there are some trade-offs. The loop's sampled nature, combined with its long time constants, limit settling time to about 100ms. Thus, although its output is faster than Figure 16's, it cannot track quickly varying inputs. Circuit linearity is DAC limited to 0.025% with full-scale drift of 50ppm/°C. Zero point drift of 1Hz/°C is due to A1B's $0.3\mu V / ^\circ C$ offset drift.

1Hz-1MHz Voltage-Controlled Sine Wave Oscillator

Both $V \rightarrow F$ converters described have pulse outputs. Many applications such as audio, shaker table driving, and automatic test equipment require voltage-controlled oscillators (VCO) with a sine wave output. The circuit of Figure 21 meets this need, spanning a 1Hz-1MHz range (120dB, or 6 decades) for a 0V to 10V input. It is over 10 times faster than previously published circuits, while maintaining 0.25% frequency linearity and 0.40% distortion specifications.

To understand the circuit, assume Q5 is on and its collector (Trace A, Figure 22) is at $-15V$, cutting off Q1. The positive input voltage is inverted by A3, which biases the summing node of integrator A1 through the 3.6k resistor and the self-biased FETs. A current, $-I$, is pulled from the summing point. A2, a precision op amp, DC stabilizes A1. A1's output (Trace B, Figure 22) integrates positive until C1's input (Trace C) crosses 0V. When this happens, C1's inverting output goes negative, the Q4-Q5 level shifter turns off, and Q5's collector goes to $+15V$. This allows Q1 to come on. The resistors in Q1's path are scaled to produce a current, $+2I$, exactly twice the absolute magnitude of the current, $-I$, being removed from the summing node. As a result, the net current into the junction becomes $+I$ and A1 integrates negatively at the same rate its positive excursion took.

When A1 integrates far enough in the negative direction, C1's '+' input crosses zero and its outputs reverse. This switches the Q4-Q5 level shifter's state, Q1 goes off and the entire cycle repeats. The result is a triangle waveform at A1's output. The frequency of this triangle is dependent on the circuit's input voltage and varies from 1Hz to 1MHz with a 0V-10V input.

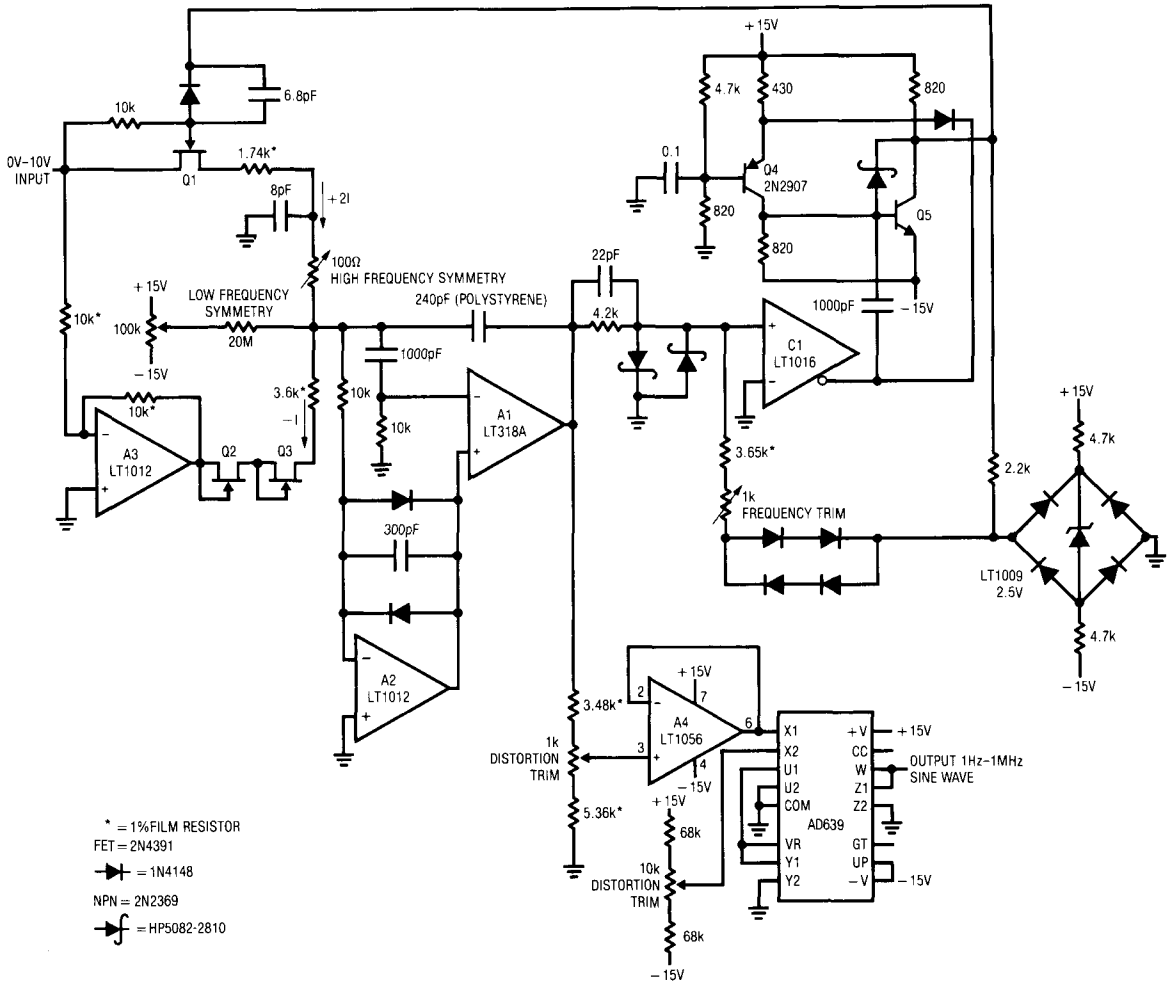


Figure 21. 1Hz-1MHz Sine Wave Output VCO

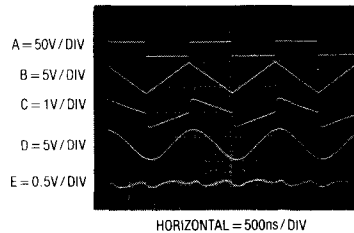


Figure 22. Sine Wave VCO Waveforms

Application Note 13

The LT1009 diode bridge and the series-parallel diodes provide a stable bipolar reference which always opposes the sign of A1's output ramp. The Schottky diodes bound C1's "+" input, assuring it clean recovery from overdrive.

The AD639 trigonometric function generator, biased via A4, converts A1's triangle output into a sine wave (Trace D).

The AD639 must be supplied with a triangle wave which does not vary in amplitude or output distortion will result. At higher frequencies, delays in the A1 integrator switching loop result in late turn on and turn off of Q1. If these delays are not minimized, triangle amplitude will increase with frequency, causing distortion level to also increase with frequency. The total delay generated by the LT1016, the Q4-Q5 level shifter, and Q1 is 14ns. This small delay, combined with the 22pF feedforward network at the LT1016's input, keeps distortion to just 0.40% over the entire 1MHz range. At 100kHz, distortion is typically inside 0.2%. The effects of gate-source charge transfer, which happens whenever Q1 switches, are minimized by the 8pF unit in Q1's source line. Without this capacitor, a sharp spike would occur at the triangle peaks, increasing distortion. The Q2-Q3 FETs compensate the temperature-dependent on-resistance of Q1, keeping the $+2I / -1$ relationship constant with temperature.

To adjust this circuit, put in 10.00V and trim the 100 Ω pot for a symmetrical triangle output at A1. Next, put in 100 μ V and trim the 100k pot for triangle symmetry. Then, put in 10.00V again and trim the 1k "frequency trim" adjustment for a 1MHz output frequency. Finally, adjust the "distortion trim" potentiometers for minimum distortion as measured on a distortion analyzer (Trace E). Slight readjustment of the other potentiometers may be required to get lowest possible distortion.

200ns-0.01% Sample-and-Hold Circuit

Figure 23's circuit uses the LT1016's high speed to improve upon a standard circuit function. The 200ns acquisition time is well beyond monolithic sample-and-hold capabilities and is matched only by hybrid and modular units selling in the \$200 range. Other specifications exceed the best commercial unit's performance. This circuit also gets around many of the problems associated

with standard sample-and-hold approaches, including FET switch errors and amplifier settling time. To achieve this, the LT1016's high speed is used in a circuit which completely abandons traditional sample-and-hold methods. When the sample-and-hold command line (Trace A, Figure 24) is high, Q2 conducts current, biasing Q3 on and forcing the 1000pF capacitor (Trace B) to discharge toward Q4's emitter potential. Q4's emitter, in turn, sits at a potential slightly below Q3's collector voltage. Q5 and the LT1009, biased from the input voltage, drive Q4. Concurrently, the TTL gate at the LT1016 grounds the latch pin (enabling the comparator) and the comparator's inverting output (Trace C) goes high. When the sample-and-hold command line (Trace A) falls, Q2 and Q3 go off and the Q1 current source charges the 1000pF unit (Trace B) with a fast linear ramp. This capacitor is buffered by Q7, a current sink loaded source follower. When Q7's output reaches the circuit's input value, the LT1016's inverting output (Trace C) switches low. The Q1 current source cuts off in about 2ns and capacitor charging ceases. The LT1016's low state also means the NOR gate's output is high, latching the comparator's output. This prevents input line noise or a change in signal from affecting the stored value in the 1000pF hold capacitor.

Ideally, Q7's output now sits at exactly the sampled value of the input voltage. In practice, a slight error exists because of the LT1016's delay and the turn-off time of Q1 (total 12ns). Because of these delays, the capacitor is able to charge to a higher voltage than the input before current stops. This error term is compensated by removing a small quantity of charge from the 1000pF capacitor when the LT1016's inverting output goes low. The charge is removed through the 8pF-1k Ω potentiometer network. Because the charging ramp's slope is fixed, the error term is constant and the compensation works over the circuit's ± 3 V input common-mode range. The lower four traces are expanded to show detail of the compensation and the circuit's critical ramp turn-off sequence. When the LT1016 goes off (Trace D), the ramp is seen to slightly overshoot its final value (Trace E).

The 1k Ω -8pF combination pulls enough charge (Trace F) out of the 1000pF hold capacitor to bring it back to the correct value. Trace G is the $\overline{\text{NOW}}$ line. It falls low 2 gate delays after the LT1016 inverting output goes low. When

this line goes low, the circuit's sampled output has settled from the correction transient and is valid data. The total time from the falling of the sample-and-hold line to the $\overline{\text{NOW}}$ output going low will always be inside 200ns.

The circuit's 200ns acquisition time is due to the high slew rate of the charging ramp and the action of Q4, Q5 and the LT1009. These components form a wideband

tracking amplifier whose output is always a fixed amount below the input. Q7's current source load (Q6) ensures that its V_{GS} does not change. Thus, Q3 will always reset the capacitor a small, relatively constant amount below any circuit input. In this way, the ramp does not have to run very long before it crosses the input value, and acquisition time versus input voltage is constant. In

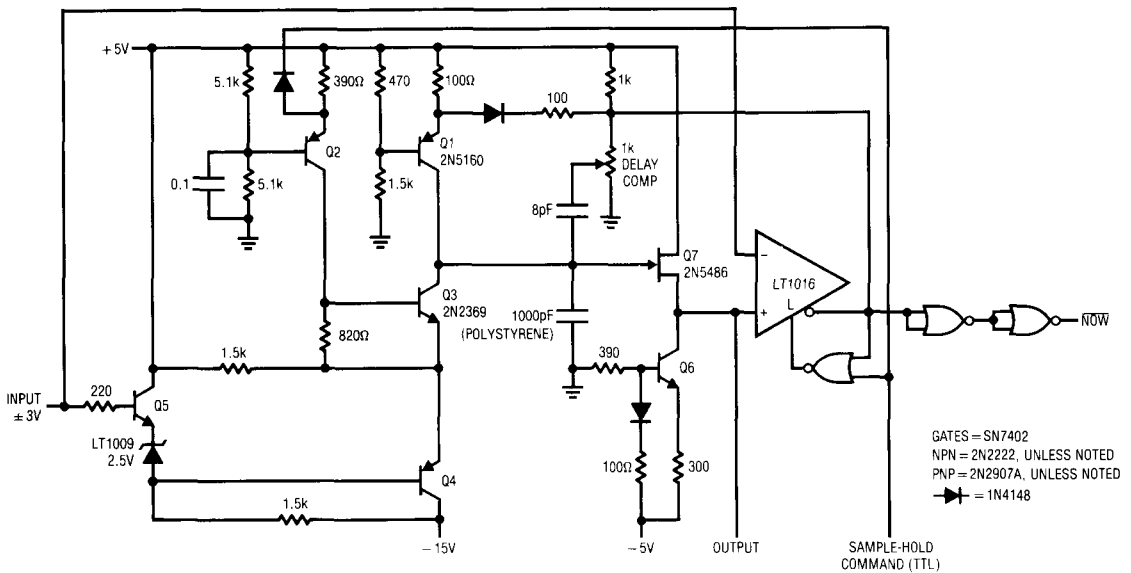


Figure 23. 200ns Sample-and-Hold

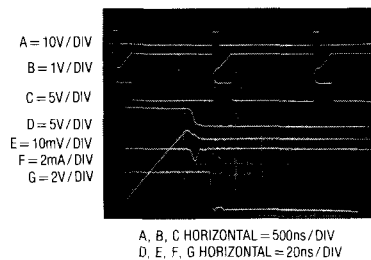


Figure 24. Fast Sample-and-Hold Waveforms.
Traces A-C Show Ramp-Compare Action.
Traces D-G Detail Delay Compensation

Application Note 13

Figure 25 the circuit is shown sampling a bipolar triangle wave. Trace A is the input and Trace B is the circuit output. Trace C is an expansion of Trace B (the "smearing" of the sampled pedestals in Trace C is due to the repetitive asynchronous sampling of the triangle). The action of the tracking amplifier is readily apparent. It always resets the ramp to the same point below the input voltage, regardless of the common-mode level. To calibrate the circuit, ground the input, repetitively pulse the sample-and-hold command line, and adjust the 1kΩ pot for 0V output.

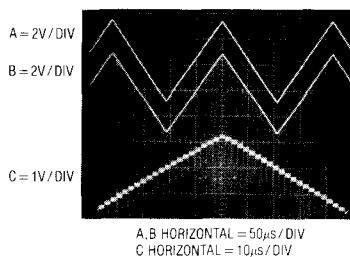


Figure 25. Fast Sample-and-Hold Tracking a Triangle Wave. Trace C is Expanded to Show the Ramping of the Circuit's Output.

Important specifications for this circuit include:

Acquisition Time	< 200ns
Common-Mode Input Range	± 3V
Drop	1µV/µs
Hold Step	2mV
Hold Settling Time	15ns
Feedthrough Rejection	>> 100dB

Fast Track-and-Hold Circuit

The track-and-hold circuit shown in Figure 26 is generically related to the sample-and-hold circuit of Figure 23.

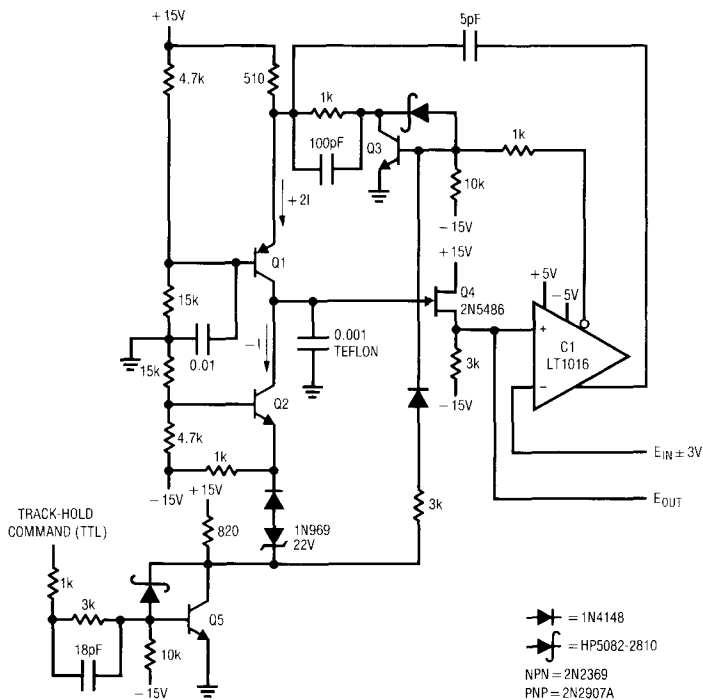


Figure 26. Comparator-Based Track-and-Hold

It also forsakes standard techniques in favor of an approach based on the LT1016's speed. This circuit's main blocks are a switched current source (Q1-Q3), a current sink (Q2), a FET follower (Q4), and the LT1016. To understand the circuit, assume the voltage stored in the 0.001 μ F hold capacitor is below the input potential and the track-and-hold command line (Trace A, Figure 27) is at a TTL "1" (track mode). Under these conditions Q5 is on and C1's output is positive. C1's inverting output is low and Q3 is off, allowing the Q1 current source to charge the hold capacitor. The Q2 current sink is also operating, but at $\frac{1}{2}$ the current density of Q1. The hold capacitor charges positively. When Q4's source (Trace B, Figure 27) ramps to the input voltage's value, C1's outputs reverse state. Q3 comes on, quickly turning off the Q1 current source. The 5pF feedforward capacitor speeds up Q1's turnoff by bypassing Q3. With Q1 off, Q2's sink current discharges the hold capacitor. This causes C1's output to change state and oscillation commences (Trace B, Figure 27). This controlled, 10mV-25MHz oscillation centers itself around the input voltage's value. When the track-and-hold line (Trace A) goes low, Q5 ceases conducting, Q1 and Q2 immediately go off, oscillations cease and the circuit's output sits within ± 5 mV of the input value at the time of turn-off. This 5mV uncertainty, caused by the nature of the circuit's operation, limits accuracy to 8 bits.

Figure 28 shows what happens when a square wave is fed into the circuit. Trace A is the input. Trace B is the output. Trace C is the track-and-hold command line and Trace D is the LT1016's output. Note that the controlled oscillation stops cleanly when the track-and-hold line goes low. If the source-sink transistors were run at

higher currents, the circuit's output would slew much faster to keep up with the input's transitions. The oscillation's error band would also proportionately enlarge. The 25MHz update rate allows this circuit to track a relatively slow signal very closely with settling time under 10ns when switched into hold.

10ns Sample-and-Hold

Figure 29 shows a 10ns acquisition time sample-and-hold which can be used with repetitive signals only. Here, the LT1016 (C1) drives a differential integrator's (A1) input. Feedback from the integrator back to the LT1016 closes a loop around the circuit. Figure 30 shows what happens when a 1MHz sine wave (Trace A, Figure 30) is applied to the input. C2 generates a zero crossing signal (Trace B) and one-shot "A" (Trace C) provides an adjustable width. One-shot B's Q output produces a 30ns pulse (Trace D) which is fed into a logic network with the \bar{Q} signal. The two inverter delays in Q's path give its associated gate a shorter duration output (Trace F) than \bar{Q} 's gate (Trace E). The last gate subtracts these two signals and generates a 10ns spike. This is inverted (Trace G) and fed to C1's latch pin. Each time the latch is enabled the comparator responds to the condition of the summing junction at its "+" input. If summing error is positive, A1 pulls current. If the error is negative, A1 sources current to the junction. After a number of input cycles, A1's output settles at a DC value which is the same as the level sampled during the time the latch is enabled. The "delay adjust" allows the 10ns sampling "window" to be positioned anywhere on the input sine wave.

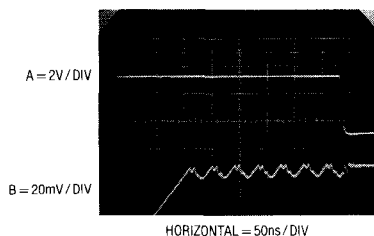


Figure 27. Track-and-Hold Circuit Acquiring an Input

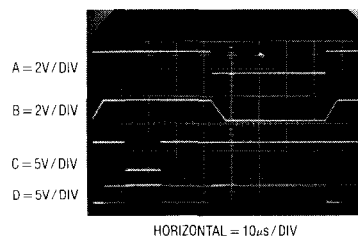


Figure 28. Track-and-Hold Responding to a Square Wave Input

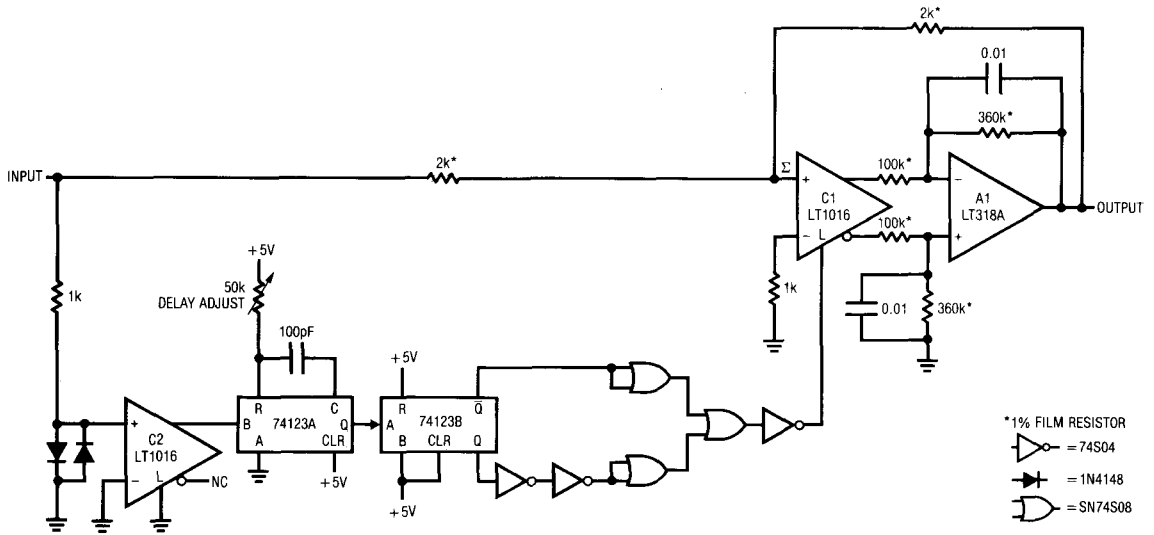


Figure 29. 10ns Sample-and-Hold for Repetitive Signals

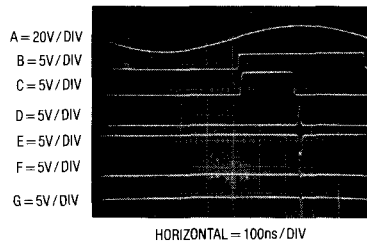


Figure 30. Waveforms for 10ns Sample-and-Hold. 10ns Sampling Window (Trace G) May be Positioned Anywhere on Input (Trace A)

5 μ s, 12-Bit A-D Converter

The LT1016's high speed is used to implement a fast 12-bit A-D converter in Figure 31. The circuit is a modified form of the standard successive approximation approach and is faster than most commercial SAR 12-bit units. In this arrangement the 2504 successive approximation register (SAR), A1 and C1 test each bit, beginning with the MSB, and produce a digital word representing V_{IN} 's value. To get faster conversion time, the clock (C2) is sped up after the third MSB is converted. This takes advantage of

the segmented DAC used, which has significantly faster settling time for the lower 9 bits.

A1 provides preamplification for C1 while adding only 7ns delay. The preamplification allows clean response to 1/2 LSB (1.22mV) overdrives at A1's input. Figure 32 shows the converter at work. To aid in observing operation, A1 has been eliminated and the DAC-input node drives the LT1016 "+" input directly. A1 should be employed in normal use.

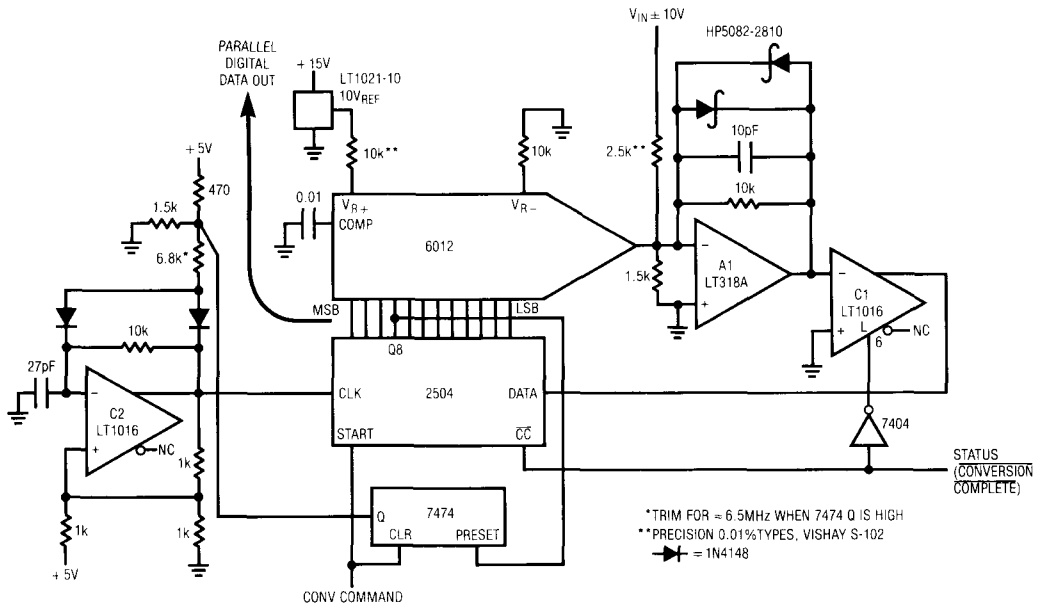


Figure 31. 5µs, 12-bit SAR Converter. Clock is Sped up after the Third Bit, Shortening Overall Conversion Time

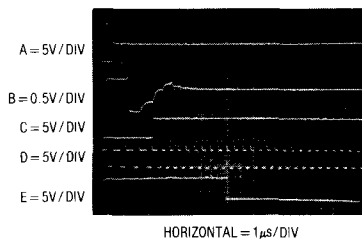


Figure 32. Fast SAR Converter Waveforms. Note Clock (Trace D) Speed-Up after 3rd Bit Conversion

The conversion begins when the "convert command" line (Trace A, Figure 32) drops low. When this happens the SAR begins to test each bit. The DAC output (Trace B), fed to the Schottky-clamped C1 input, sequentially converges toward final value. After the third MSB has been established, the 7474 Q line goes high (Trace C), forcing the 2.1MHz clock to shift to 3.2MHz (Trace D). This speeds up conversion of the remaining 9 bits, minimizing overall A-D time. When conversion is complete, the status line (Trace E) drops low and C1's latch is set by the TTL inverter, preventing the comparator from responding

to input noise or shifts. The next convert command reinitiates the entire cycle. Note that on the lowest order bits C1 must accurately respond to small signals without sacrificing speed. The high gain-bandwidth required makes this application one of the most difficult for a comparator. This circuit's 5µs conversion time is fast for a 12-bit A-D. Faster conversion time is possible, although the design becomes more complex. A "stretched" version of this circuit, with 1.8µs conversion time, appears in AN17, "Considerations for Successive Approximation A-D Converters".

Application Note 13

Inexpensive, Fast 10-Bit Serial Output A-D

Figure 33 shows a simple way to build a fast, inexpensive 10-bit A-D converter. This circuit is especially useful where a large number of converters is required and all of them can be serviced by one clock. The design consists of a current source, an integrating capacitor, a comparator and some gates.

Every time a pulse is applied to the convert command input (Trace A, Figure 34), Q1 resets the 1000pF capacitor to 0V (Trace B). This resetting action takes 200ns — the minimum acceptable convert command pulse width. On the falling edge of the convert command pulse, the capacitor begins to charge linearly. In precisely 10 μ s, it charges to 2.5V (over range to 3.0V is provided). Normally, Q1 would not be able to reset the capacitor to zero due to its V_{CE} saturation voltage. This effect is compensated by Q4. This device switches in inverting mode,

resulting in a reset within 1mV of ground. Q1 absorbs most of the capacitor's charge and Q4 completes the discharge.

The 10 μ s ramp is applied to the LT1016's positive input. The LT1016 compares the ramp to E_x , the unknown, at its negative input. For a 0V–2.5V range, E_x is applied to the 2.5k Ω resistor. For a 0V–10V range, the 2.5k Ω resistor is grounded and E_x is applied to the 7.5k Ω resistor. The 2.0k resistor at the positive input provides balanced source impedance for C1. The output of the LT1016 is a pulse (Trace C) whose width is directly dependent on the value of E_x . This pulse width is used to gate a 100MHz clock. The 74AS00 gate achieves this function and also gates out the portion of the LT1016 output pulse due to the convert command pulse. Thus, the 100MHz clock pulse bursts that appear at the output

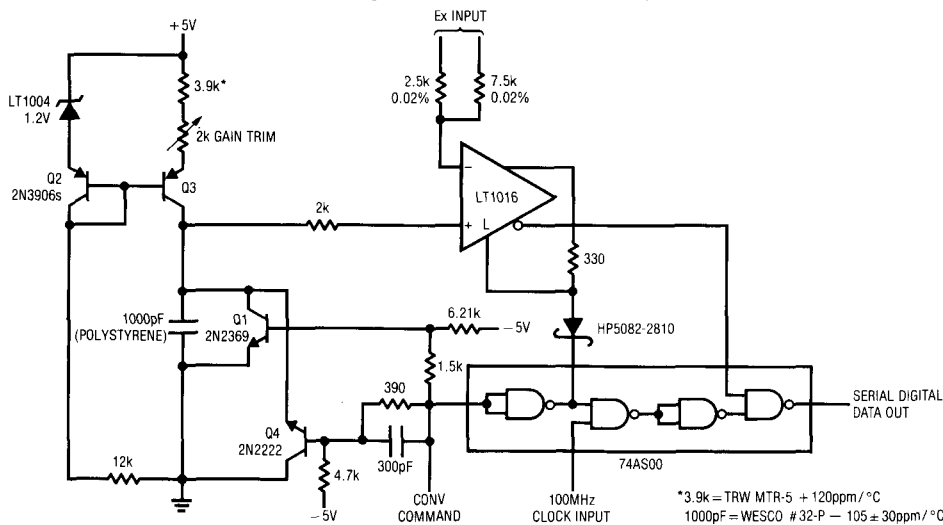


Figure 33. Simple, Fast 10-Bit A → D

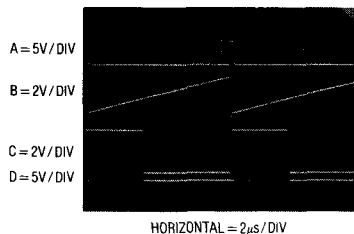


Figure 34. Waveforms for 10-Bit A → D

(Trace D) are proportional to Ex. For a 0V–10V input, 1024 pulses appear at full-scale, 512 at 5.00V, etc. The resistor-diode network at the LT1016's latch pin ensures clean comparator transitions by locking the LT1016 outputs after the conversion is completed. This latch is broken by the next convert command pulse.

The current source scaling resistor and ramp capacitor specified provide good temperature compensation because of their opposing thermal coefficients. The circuit will typically hold ± 1 LSB accuracy over 0°C–70°C with an additional ± 1 LSB uncertainty due to the asynchronous relationship between the clock and the conversion sequence.

Figure 35 details the most critical part of the converter's operation, the reset phase. Trace A is the convert command. Trace B is the capacitor (greatly magnified) resetting to zero. The comparator output appears in Trace C and Trace D is the gated serial output. Observe that the output pulses do not appear until the capacitor has started to ramp (just past mid-screen), even though the comparator is high.

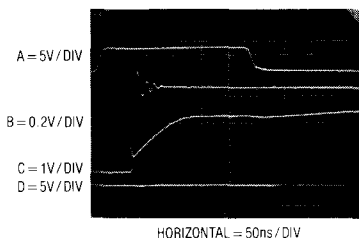


Figure 35. Figure 33's Reset Sequence. Q1–Q4 Combination Gives Quick, Low Offset Zero Reset

2.5MHz Precision Rectifier/AC Voltmeter

Most precision rectifier circuits rely on operational amplifiers to correct for diode drops. Although this scheme works well, bandwidth limitations usually restrict these circuits to operation below 100kHz. Figure 36 shows the LT1016 in an open-loop, synchronous rectifier configuration which has high accuracy out to 2.5MHz. An input

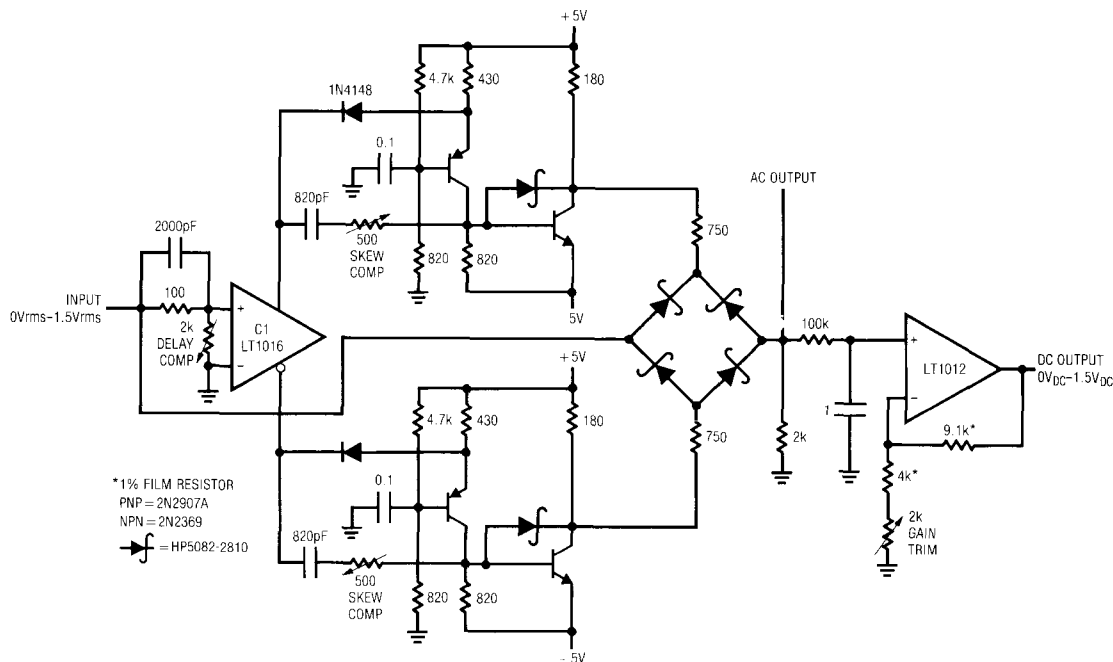


Figure 36. Fast, Synchronous Rectifier-Based AC-DC Converter

Application Note 13

1MHz sine wave (Trace A, Figure 37) is zero cross detected by C1. Both of C1's outputs drive identical level shifters with fast (delay = 2ns–3ns), $\pm 5V$ outputs. These outputs bias a Schottky switching bridge (Traces B and C are the switched corners of the bridge). The input signal is fed to the left-midsection of the bridge. Because C1 drives the bridge synchronously with the input signal, a half-wave rectified sine appears at the AC output (Trace D). The DC RMS value appears at the DC output. The Schottky bridge gives fast switching and eliminates the charge pump-through that a FET switch would contribute. This is evident in Trace E, which is an expanded version of Trace D. The waveform is clean with the exception of very small disturbances where bridge switching occurs. To calibrate this circuit, apply a 1MHz–2MHz 1Vp-p. Sine wave and adjust the delay compensation so bridge switching occurs when the sine crosses zero. This adjustment corrects for the small delays through the LT1016 and the level shifters. Next, adjust the skew compensation potentiometers for minimum aberrations in the AC output signal. These trims slightly shift the phase of the rising output edge of their respective level shifter. This allows skew in the complementary bridge drive signals to be kept within 1ns–2ns, minimizing output disturbances when switching occurs. A 100mV sine input will produce a clean output with a DC output accuracy of better than 0.25%.

10MHz Fiber Optic Receiver

Reception of high data rate fiber optic data is not easy. The high speed data and uncertain intensity of the light level

can cause erroneous results unless the receiver is carefully designed. The fiber optic receiver shown in Figure 38 will accurately condition a wide range of light inputs at up to 10MHz data rates. Its digital output features an adaptive threshold trigger which accommodates varying signal intensities due to component aging and other causes. An analog output is also available to monitor the detector output. The optical signal is detected by the PIN photodiode and amplified by a broadband fed-back stage, Q1–Q3. A second, similar, stage gives further amplification. The output of this stage (Q5's collector) biases a 2-way peak detector (Q6–Q7). The maximum peak is stored in Q6's emitter capacitor, while the minimum excursion is retained in Q7's emitter capacitor. The DC value of Q5's output signal's mid-point appears at the junction of the 500pF capacitor and the 22Meg units. This point will always sit midway between the signal's excursions, regardless of absolute amplitude. This signal-adaptive voltage is buffered by the low bias LT1012 to set the trigger voltage at the LT1016's positive input. The LT1016's negative input is biased directly from Q5's collector. Figure 39 shows the results using the test circuit indicated in Figure 38. The pulse generator's output is Trace A, while Q5's collector (analog output monitor) appears in Trace B. The LT1016 output is Trace C. The wideband amplifier responds within 5ns and rises in 25ns. Note that the LT1016's output transitions line up with the mid-point of Trace B, in accordance with the adaptive trigger's operation.

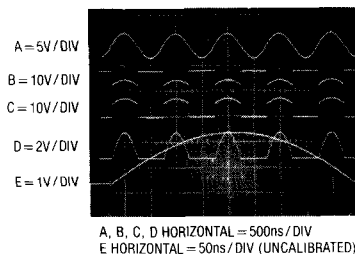


Figure 37. Fast AC-DC Converter Operating at 1MHz. Clean Switching is Due to LT1016's Speed and Compensations for Delay and Switching Skew

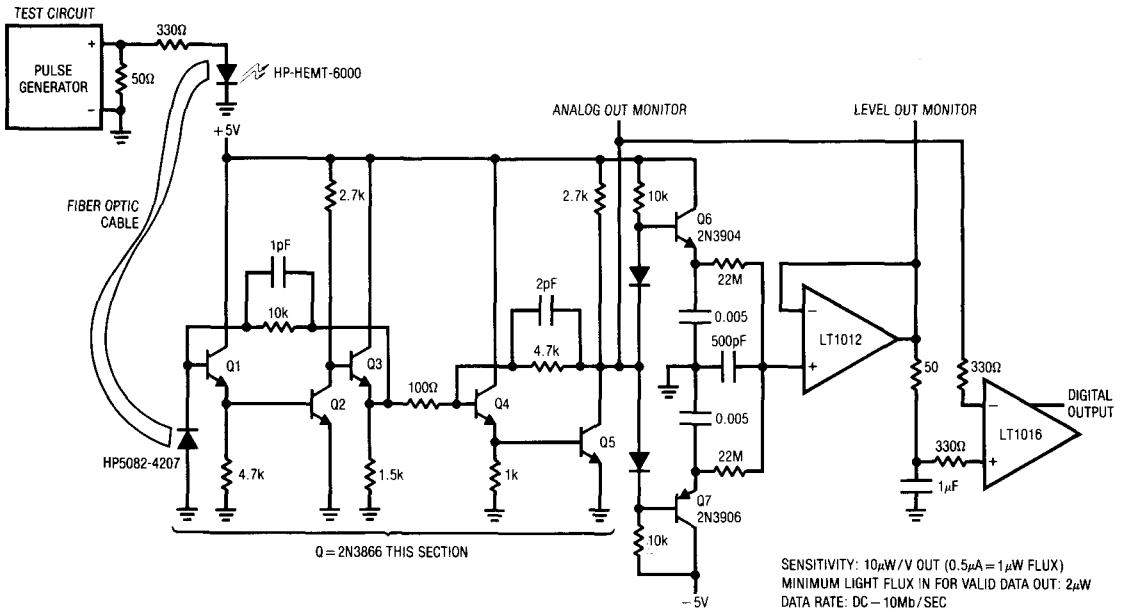


Figure 38. Fast Fiber Optic Receiver is Immune to Shifts in Operating Point

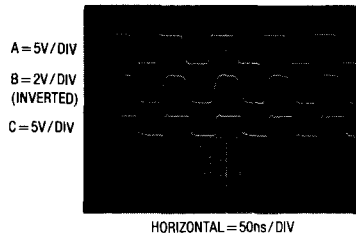


Figure 39. Fiber Optic Receiver Waveforms

12ns Circuit Breaker

Figure 40 shows a simple circuit which will turn off current in a load 12ns after it exceeds a preset value. This circuit has been used to protect integrated circuits during developmental probing and is also useful for protecting expensive loads during trimming and calibration. It is 3 times faster and less complex than previously published circuits. Under normal conditions the voltage across the 10Ω shunt is smaller than the potential at the LT1016's negative input. This keeps Q1 off and Q2 receives bias, driving the load. When an overload occurs (in this case via a test circuit, whose output is Trace A, Figure 41),

the current through the 10Ω sense resistor begins to increase (Trace B, Figure 41). When this current exceeds the preset value, the LT1016's outputs (non-inverting output shown in Trace C) reverse. This provides ideal turn-on drive for Q1 and it cuts off Q2 (Q2 emitter is Trace D) in 5ns. The delay from the onset of excessive load current to complete shutdown is just 13ns. Once the circuit has triggered, the LT1016 is held in its latched state by feedback from the non-inverting output. When the load fault has been cleared the pushbutton can be used to reset the circuit.

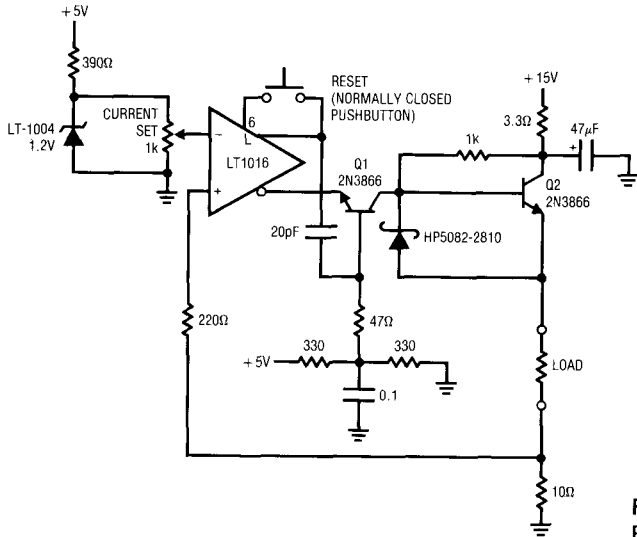


Figure 40. 12ns Circuit Breaker

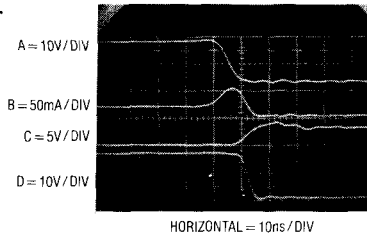
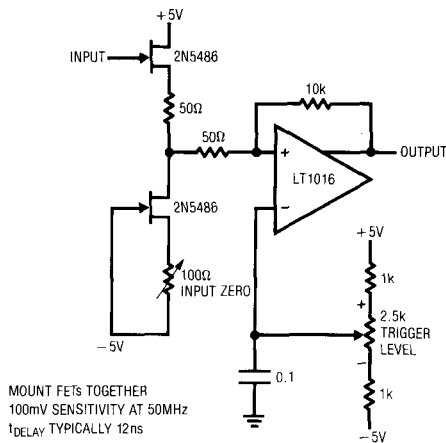


Figure 41. Operating Waveforms for the 12ns Circuit Breaker. Circuit Output (Trace D) Starts to Shut Down 12ns after Output Current (Trace B) Begins to Rise

50MHz Trigger

Counters and other instruments require a trigger circuit. Designing a fast, stable trigger is not easy, and often entails a considerable amount of discrete circuitry. Figure 42 shows a simple trigger with 100mV sensitivity at 50MHz. The FETs comprise a simple high speed buffer and the LT1016 compares the buffer's output to the potential at the "trigger level" potentiometer, which may be either

polarity. The 10k resistor provides hysteresis, eliminating "chattering" caused by noisy input signals. Figure 43 shows the trigger's response (Trace B) to a 50MHz sine wave (Trace A). To calibrate this circuit, ground the input and adjust the "input zero" control for 0V at Q2's drain terminal.



MOUNT FETs TOGETHER
100mV SENSITIVITY AT 50MHz
† DELAY TYPICALLY 12ns

Figure 42. 50MHz Trigger

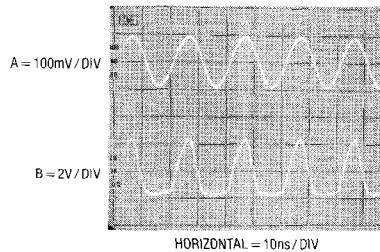


Figure 43. Trigger Responding to a 50MHz Sine Input

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APPENDIX A

About Bypass Capacitors

Bypass capacitors are used to maintain low power supply impedance at the point of load. Parasitic resistance and inductance in supply lines mean that the power supply impedance can be quite high. As frequency goes up, the inductive parasitic becomes particularly troublesome. Even if these parasitic terms did not exist, or if local regulation is used, bypassing is still necessary because no power supply or regulator has zero output impedance at 100MHz. What type of bypass capacitor to use is determined by the application, frequency domain of the circuit, cost, board space and many other considerations. Some useful generalizations can be made.

All capacitors contain parasitic terms, some of which appear in Figure A1. In bypass applications, leakage and dielectric absorption are second order terms but series R and L are not. These latter terms limit the capacitor's ability to damp transients and maintain low supply impedance. Bypass capacitors must often be large values

so they can absorb long transients, necessitating electrolytic types which have large series R and L.

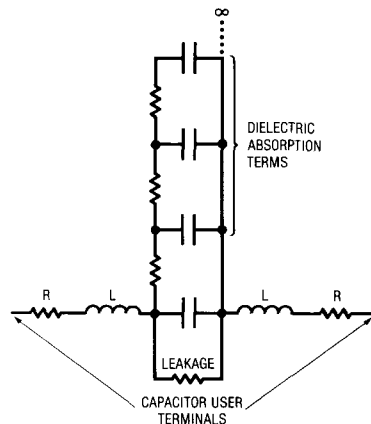


Figure A1. Parasitic Terms of a Capacitor

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Different types of electrolytics and electrolytic-non-polar combinations have markedly different characteristics. Which type(s) to use is a matter of passionate debate in some circles and the test circuit (Figure A2) and accompanying photos are useful. The photos show the response of 5 bypassing methods to the transient generated by the test circuit. Figure A3 shows an unbypassed line which sags and ripples badly at large amplitudes. Figure A4 uses an aluminum 10 μ F electrolytic to considerably cut the dis-

turbance, but there is still plenty of potential trouble. A tantalum 10 μ F unit offers cleaner response in A5 and the 10 μ F aluminum combined with a 0.01 μ F ceramic type is even better in A6. Combining electrolytics with non-polarized capacitors is a popular way to get good response but beware of picking the wrong duo. The right (wrong) combination of supply line parasitics and paralleled dissimilar capacitors can produce a resonant, ringing response, as in A7. Caveat!

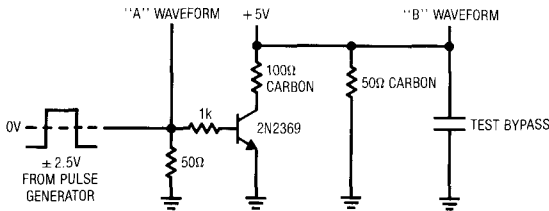


Figure A2. Bypass Capacitor Test Circuit

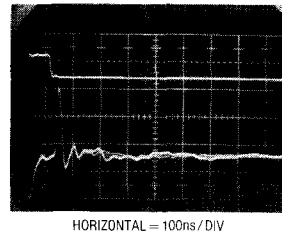


Figure A3. Response of Unbypassed Line

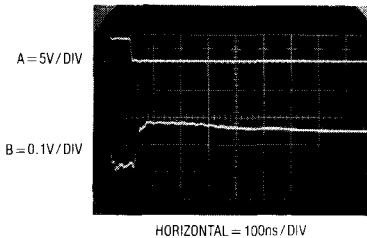


Figure A4. Response of 10 μ F Aluminum Capacitor

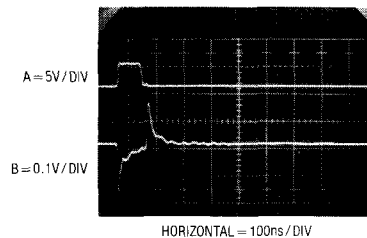


Figure A5. Response of 10 μ F Tantalum Capacitor

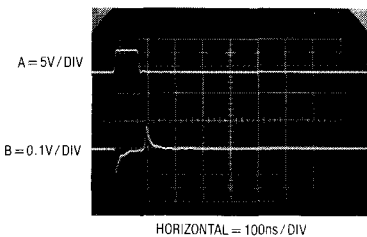


Figure A6. Response of 10 μ F Aluminum Paralleled by 0.01 μ F Ceramic

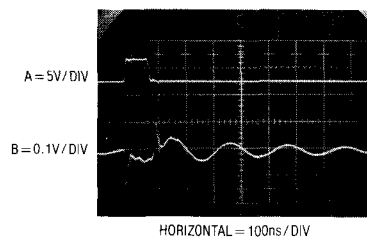


Figure A7. Some Paralleled Combinations can Ring. Try before Specifying!

APPENDIX B

About Probes and Oscilloscopes

The oscilloscope-probe combination used in high speed work is the most important equipment decision the designer must make. Ideally, the oscilloscope should have at least 150MHz bandwidth for work with the LT1016, but slower instruments are acceptable if their limitations are well understood. Be aware of your scope's behavior with respect to input impedance, noise, over-drive recovery, sweep nonlinearity, triggering, channel-to-channel feedthrough and other characteristics.

Probes are the most overlooked cause of oscilloscope mismeasurement. All probes have some effect on the point they are measuring. The most obvious is input resistance, but input capacitance usually dominates in a high speed measurement. Much time can be lost chasing circuit events which are actually due to improperly selected or applied probes. An 8pF probe looking at a 1k Ω source impedance will form an 8ns lag — close to the LT1016's response time! Low impedance probes, designed for 50 Ω inputs, (with 500 Ω to 1k Ω resistance) usually have input capacitance of 1pF or 2pF. They are a very good choice if you can stand the low resistance. FET probes maintain high input resistance and keep capacitance at the 1pF level but have substantially more delay than passive probes. FET probes also have limitations on input common-mode range which must be adhered to or serious measurement errors will result. Contrary to popular belief, FET probes *do not* have extremely high input resistance — some types are as low as 100k Ω .

Current probes are useful and convenient. The passive transformer-based types are fast and have less delay than the Hall effect-based versions. The Hall types, however, respond at DC and low frequency and the transformer types typically roll off around 100Hz to 1kHz. Both types have saturation limitations which, when exceeded, cause odd results on the CRT which will confuse the unwary.

When using different probes remember that they all have different delay times, meaning that apparent timing errors will occur on the CRT. Know what the individual probe delays are and account for them in interpreting the CRT display.

By far the greatest source of error in probe use is grounding. Poor probe grounding can cause ripples and discontinuities in the waveform observed. In some cases the choice and placement of a probe's ground strap will affect waveforms on another channel. In the worst case, connecting the probe's ground wire will virtually disable the circuit being measured. The cause of these problems is due to parasitic inductance in the probe's ground connection. In most oscilloscope measurements this is not a problem, but at nanosecond speeds it becomes critical. Fast probes are always supplied with a variety of spring clips and accessories designed to aid in making the lowest possible inductive connection to ground. Most of these attachments assume a ground plane is in use, which it should be. Always try to make the shortest possible connection to ground — anything longer than 1 inch may cause trouble.

The simple network of Figure B1 shows just how easy it is for poorly chosen or used probes to cause bad results. A 9pF input capacitance probe with a 4 inch long ground-strap monitors the output (Trace B, Figure B2). Although the input (Trace A) is clean, the output contains ringing. Using the same probe with a ¼ inch spring tip ground connection accessory seemingly cleans up everything (Figure B3). However, substituting a 1pF FET probe (Figure B4) reveals a 50% output amplitude error in measurement B3! The FET probe's low input capacitance allows a more accurate version of circuit action. The FET probe does, however, contribute its own form of error. Note that the probe's response is tardy by 5ns due to delay in its active circuitry. Hence, separate measurements with each probe are required to determine amplitude and timing parameters of the output.

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A final form of probe is the human finger. Probing the circuit with a finger can accentuate desired or undesired effects, giving clues that may be useful. The finger can be used to introduce stray capacitance to a suspected circuit node while observing results on the CRT. Two fingers, lightly moistened, can be used to provide an experimental resistance path. Some high speed engineers are particularly adept at these techniques and can estimate the capacitive and resistive effects created with surprising accuracy.

Examples of the probes discussed, along with different forms of grounding implements, are shown in Figure B5.

Probes A, B, E, and F are standard types equipped with various forms of low impedance grounding attachments.

The conventional ground lead used on G is more convenient to work with but will cause ringing and other effects at high frequencies, rendering it useless. H has a very short ground lead. This is better, but can still cause trouble at high speeds. D is a FET probe. The active circuitry in the probe and a very short ground connector ensure low parasitic capacitance and inductance. C is a separated FET probe attenuator head. Such heads allow the probe to be used at higher voltage levels (e.g., $\pm 10V$ or $\pm 100V$). The miniature coaxial connector shown can be mounted on the circuit board and the probe mated with it. This technique provides the lowest possible parasitic inductance in the ground path and is especially recommended.

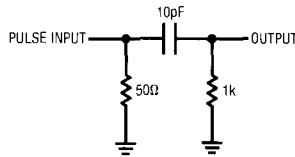


Figure B1. Probe Test Circuit

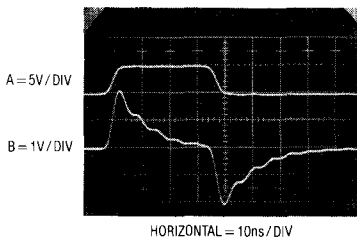


Figure B2. Test Circuit Output with 9pF Probe and 4 Inch Ground Strap

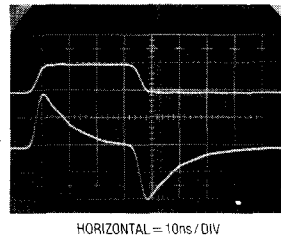


Figure B3. Test Circuit Output with 9pF Probe and 0.25 Inch Ground Strap

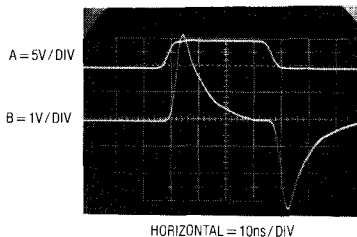


Figure B4. Test Circuit Output with FET Probe

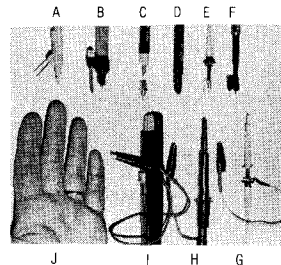


Figure B5. Various Probe-Ground Strap Configurations

I is a current probe. A ground connection is not usually required. However, at high speeds the ground connection may result in a cleaner CRT presentation. Because no current flows in the ground lead of these probes, a long strap is usually permissible. J is typical of the finger probes described in the text. Note the ground strap on the third finger.

The low inductance ground connectors shown are available from probe manufacturers and are always supplied with good quality, high frequency probes. Because most oscilloscope measurements do not require them, they invariably become lost. There is no substitute for these devices when they are needed, so it is prudent to take care of them. This is especially applicable to the ground strap on the finger probe.

APPENDIX C

About Ground Planes

Many times in high frequency circuit layout the term "ground plane" is used, most often as a mystical and ill-defined cure to spurious circuit operation. In fact, there is little mystery to the usefulness and operation of ground planes, and like many phenomena, their fundamental operational principle is surprisingly simple.

Ground planes are primarily useful for minimizing circuit inductance. They do this by utilizing basic magnetic theory. Current flowing in a wire produces an associated magnetic field. The field's strength is proportional to the current and inversely related to the distance from the conductor. Thus, we can visualize a wire carrying current (Figure C1) surrounded by radii of magnetic field. The unbounded field becomes smaller with distance. A wire's inductance is defined as the energy stored in the field set up by the wire's current. To compute the wire's inductance requires integrating the field over the wire's length

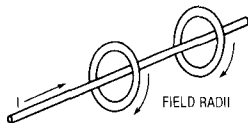


Figure C1. Single Wire Case

and the total radial area of the field. This implies integrating on the radius from $R = R_w$ to infinity, a very large number. However, consider the case where we have two wires in space carrying the same current in either direction (Figure C2). The fields produced cancel.

In this case, the inductance is much smaller than in the sample wire case and can be made arbitrarily small by reducing the distance between the two wires. This reduction of inductance between current carrying conductors is the underlying reason for ground planes. In a normal circuit, the path current takes from the signal source, through its conductor and back to ground includes a large loop area. This produces a large inductance for this conductor which can cause ringing due to LRC effects. It is worth noting that 10nH at 100MHz has an impedance of 6Ω . At 10mA a 60mV drop results.

A ground plane provides a return path directly under the signal carrying conductor through which return current can flow. The conductor's small physical separation means the inductance is low. Return current has a direct path to ground, regardless of the number of branches associated with the conductor. Currents will always flow through the return path of lowest impedance. In a properly designed ground plane this path is directly under the signal conductor. In a practical circuit it is desirable to "ground plane" one whole side of the PC card (usually the component side for wave solder considerations) and run the signal conductors on the other side. This will give a low inductance path for all the return currents.

Aside from minimizing parasitic inductance, ground planes have additional benefits. Their flat surface minimizes resistive losses due to AC "skin effect" (AC currents travel along a conductor's surface). Additionally, they aid the circuit's high frequency stability by referring stray capacitances to ground.

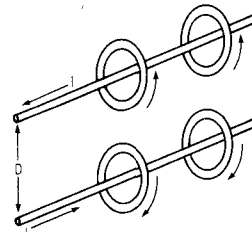


Figure C2. Two Wire Case

Application Note 13

Some practical hints for ground planes are:

1. Ground plane as much area as possible on the component side of the board, especially under traces that operate at high frequency.
2. Mount components that conduct substantial fast rise currents (termination resistors, ICs, transistors, decoupling capacitors) as close to the board as possible.
3. Where common ground potential is important (i.e., at comparator inputs), try to single point the critical components into the ground plane to avoid voltage drops.

For example, in Figure C3's common A/D circuit, good practice would dictate that grounds 2, 3, 4 and 6 be as close to single point as possible.

Fast, large currents must flow through R1, R2, D1 and D2 during the DAC settle time. Therefore, D1, D2, R1 and R2 should be mounted close to the ground plane to minimize their inductance. R3 and C1 don't carry any current, so their inductance is less important; they could be vertically inserted to save space and to allow point 4 to be single point common with 2, 3 and 6. In critical circuits the designer must often trade off the beneficial effects of lowered inductance versus the loss of single point ground.

4. Keep trace length short. Inductance varies directly with length and no ground plane will achieve perfect cancellation.

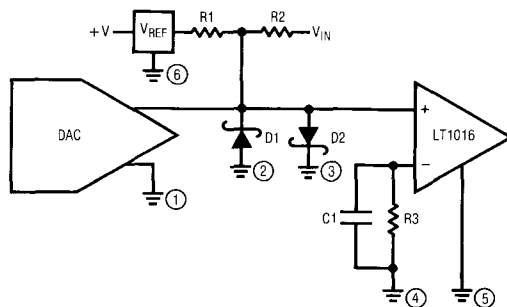


Figure C3. Typical Grounding Scheme

APPENDIX D

Measuring Equipment Response

The 10ns response time of the LT1016 and the circuitry it is used in will challenge the best test equipment. Many of the measurements made utilize equipment near the limit of its capabilities. It is a good idea to verify parameters such as probe and scope rise time and differences in

delays between probes and even oscilloscope channels. To do this, a source of very fast, clean pulses is necessary. The circuit shown in Figure D1 uses a tunnel diode to generate a pulse with a rise time well under 1ns.

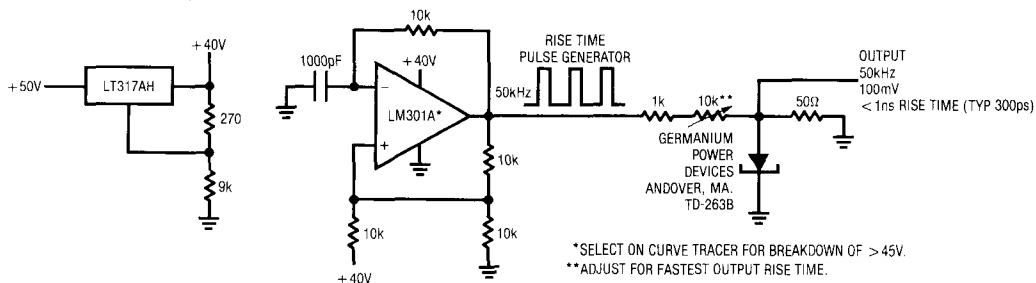


Figure D1. Tunnel Diode-Based 1ns Rise Time Pulse Generator

Figure C2 shows that the pulse is also very clean, with no attendant ringing or noise. In this photo the pulse is used to check a probe-scope combination with a specified 1.4ns rise time. The display shows that the equipment is being properly used and is in specification. Using the

tunnel diode generator to perform tests such as this can save countless hours pursuing "circuit problems," which in reality are caused by misapplied or out of spec equipment.

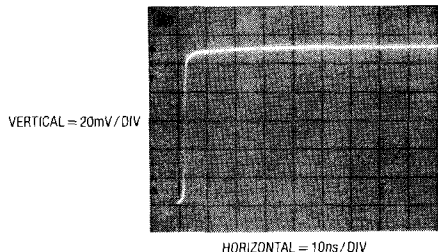


Figure D2. Figure D1's Output Monitored on a 275MHz Oscilloscope

APPENDIX E

About Level Shifts

The TTL output of the LT1016 will interface with many circuits directly. Many applications, however, require some form of level shifting of the output swing. With LT1016-based circuits this is not trivial because it is desirable to maintain very low delay in the level shifting stage. When designing level shifters, keep in mind that the TTL output of the LT1016 is a sink-source pair (Figure E1) with good ability to drive capacitance (such as feedforward capacitors).

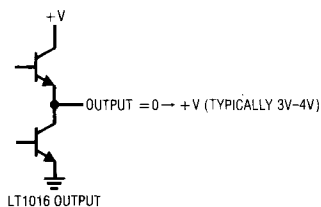


Figure E1

Figure E2 shows a non-inverting voltage gain stage with a 15V output. When the LT1016 switches, the base-emitter voltages at the 2N2369 reverse, causing it to switch very quickly. The 2N3866 emitter-follower gives a low impedance output and the Schottky diode aids current sink capability.

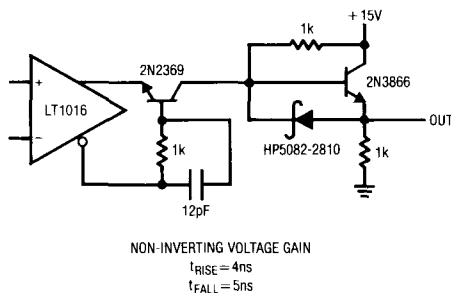


Figure E2

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Figure E3 is a very versatile stage. It features a bipolar swing which may be programmed by varying the output transistor's supplies. This 3ns delay stage is ideal for driving FET switch gates. Q1, a gated current source, switches the Baker-clamped output transistor, Q2. The heavy feedforward capacitor from the LT1016 is the key to low delay, providing Q2's base with nearly ideal drive. This capacitor loads the LT1016's output transition (Trace A, Figure E5), but Q2's switching is clean (Trace B, Figure E5) with 3ns delay on the rise and fall of the pulse.

Figure E4 is similar to E2 except that a sink transistor has replaced the Schottky diode. The two emitter-followers drive a power MOSFET which switches 1A at 15V. Most of the 7ns–9ns delay in this stage occurs in the MOSFET and the 2N2369.

When designing level shifters, remember to use transistors with fast switching times and high f_T 's. To get the kind of results shown, switching times in the ns range and f_T 's approaching 1GHz are required.

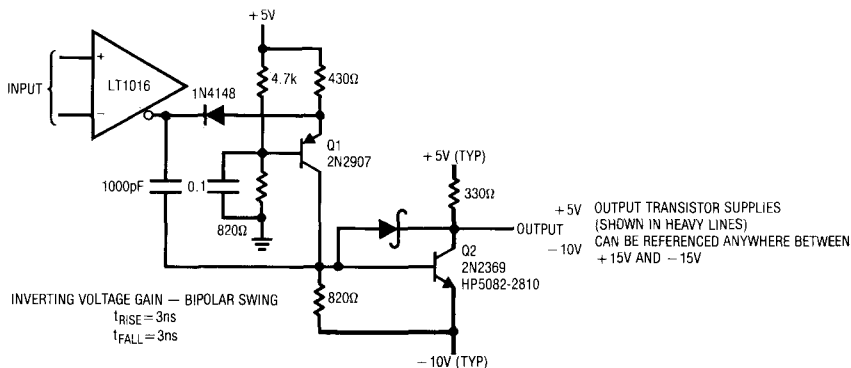


Figure E3

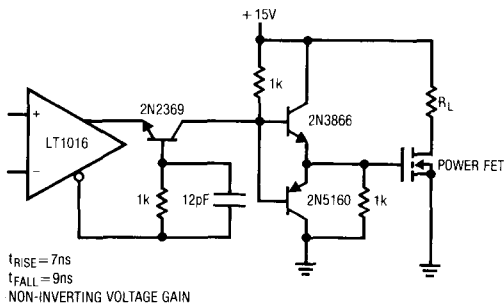


Figure E4

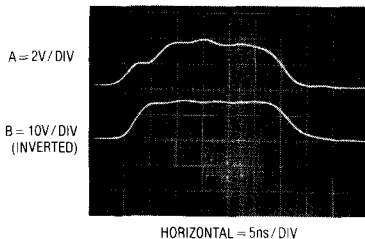


Figure E5. Figure E3's Waveforms

Designs for High Performance Voltage-to-Frequency Converters

Jim Williams

Monolithic, modular and hybrid technologies have been used to implement voltage-to-frequency converters. A number of types are commercially available and overall performance is adequate to meet many requirements. In many cases, however, very high performance or special characteristics are required and available units will not work. In these instances $V \rightarrow F$ circuits specifically optimized for the desired parameter(s) are required. This application note presents examples of circuits which offer substantially improved performance over commercially available $V \rightarrow F$ s. Various approaches (see Box Section, "V \rightarrow F Design Techniques") permit improvements in speed, dynamic range, stability and linearity. Other circuits feature low voltage operation, sine wave output and deliberate nonlinear transfer functions.

Ultra-High Speed 1Hz-100MHz $V \rightarrow F$ Converter

Figure 1's circuit uses a variety of circuit methods to achieve wider dynamic range and higher speed than any commercial $V \rightarrow F$. Rocketing along at 100MHz full-scale (10% overrange to 110MHz is provided), it leaves all other $V \rightarrow F$ s far behind. The circuit's 160dB dynamic range (8 decades) allows continuous operation down to 1Hz. Additional specifications include 0.06% linearity, 25ppm/ $^{\circ}$ C gain temperature coefficient, 50nV/ $^{\circ}$ C (0.5Hz/ $^{\circ}$ C) zero shift and a 0V to 10V input range.

In this circuit an LTC1052 chopper-stabilized amplifier servo-biases a crude but wide range $V \rightarrow F$ converter. The $V \rightarrow F$ output drives a charge pump. The averaged difference between the charge pump's output and the circuit's input biases the servo amplifier, closing a control loop around the wide range $V \rightarrow F$. The circuit's wide dynamic range and high speed are derived from the basic $V \rightarrow F$'s characteristics. The chopper-stabilized amplifier and charge pump stabilize the circuit's operating point, contributing high linearity and low drift. The LTC1052's 50nV/ $^{\circ}$ C offset drift allows the circuit's 100nV/Hz gain slope, permitting operation down to 1Hz.

The positive input voltage causes A1, the servo amplifier, to swing positive. The 2N3904 current sink pulls current (Trace A, Figure 2) from the varactor diode, serving as an integrating capacitor. A3 unloads the varactor and biases a trigger made up of the ECL gate and its associated components. This circuit, similar to those employed in oscilloscope triggering applications, features voltage threshold hysteresis and 1ns response time. When A3 ramps to the trigger's lower trip point, its outputs reverse state. The inverting output, operating as an unterminated emitter-follower, deposits a fast positive current spike (Trace B) into the varactor diode integrator. The trigger-gate's complementary output goes low (Trace C), clocking the ECL ± 16 counter. This counter's output (Trace D), level shifted by the differential pair of 2N5160s, feeds the 4013 flip-flop. The 4013's square wave drive (Trace E) to the LTC1043 provides charge pump action. The switch-capacitor pairs in the LTC1043 run out of phase and charge is pumped (Trace F) from A1's positive input on each edge of the LTC1043's square wave input. The amount of charge delivered per cycle is primarily dependent on the LT1009 voltage reference and the 100pF value of the capacitors ($Q = CV$). The slight difference between the charge delivered on the clock's rising and falling edge is due to capacitor tolerances and does not influence circuit operation. The charge pump's overall accuracy is determined by the stability of the LT1009 and the capacitors and the low charge injection of the LTC1043. The ECL counter and the flip-flop divide the trigger's output by 32, setting the LTC1043's maximum switching frequency at about 3MHz (100MHz \div 32); within its specified operating range. The 0.22 μ F capacitor integrates the pumping action to DC. The averaged difference between the positive input-derived current and the charge pump-feedback signal is amplified by A1, which servo-controls the circuit's operating point. The compensation capacitor at A1 provides stable loop compensation. Nonlinearity and drift in the basic $V \rightarrow F$ circuit are compensated by A1's servo action, resulting in the high linearity and low drift previously noted.

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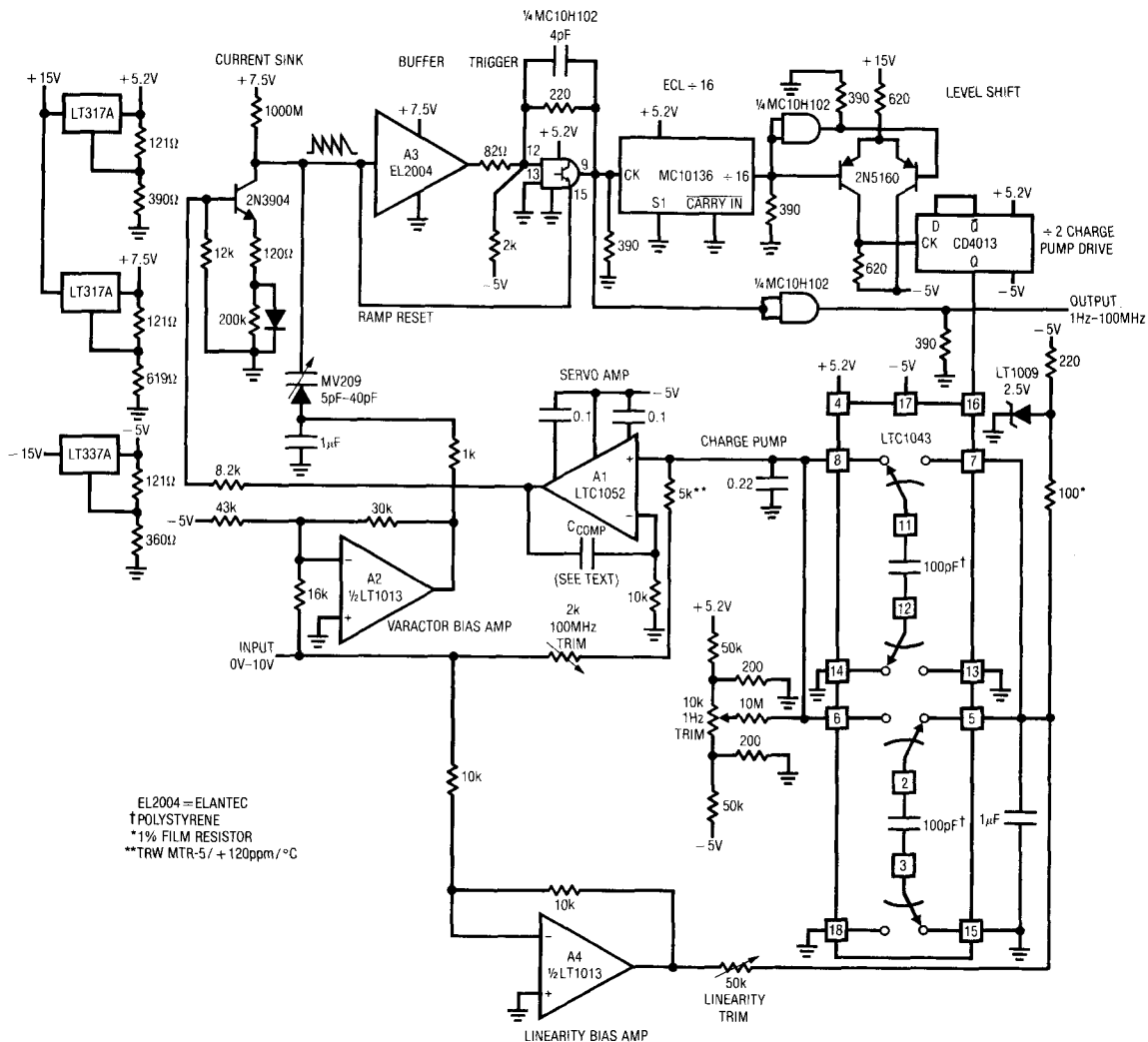


Figure 1. 1Hz → 100MHz Voltage-to-Frequency Converter (King Kong V → F)

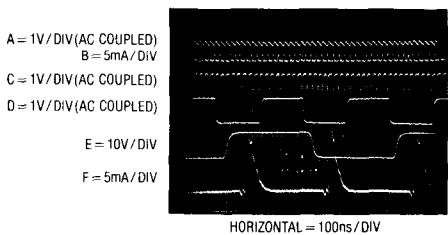


Figure 2. 1Hz → 100MHz V → F Waveforms

Some special techniques are required for this circuit to achieve its specifications. A2, driven from the input voltage, provides DC bias for the varactor diode-integrating capacitor. This DC bias causes the varactor's capacitance to vary inversely with input, helping the circuit achieve its 8-decade dynamic range. The $1\mu\text{F}$ capacitor, in series with the varactor, gives the relatively large ramp currents a low impedance path to ground. The 1000Ω resistor in the current sink sources enough current to swamp the effects of all leakages from the 2N3904 collector. This ensures that current must always be sunk from the varactor-integrator to sustain oscillation, even at the very lowest frequencies.

The 200k-diode combination in the 2N3904's emitter reduces low frequency jitter. It does this by reducing current sink noise at low frequencies by increasing emitter resistance at low base bias voltages.

The 2k pull-down resistor at the trigger input ensures clean, quick transitions at low ramp slew rates, aiding low frequency jitter performance.

The 5k input resistor specified has a temperature coefficient which opposes that of the polystyrene capacitors in the charge pump. This reduces the effect of their tempco, lowering overall circuit gain drift.

A4 supplies a small, input-related current to the charge pump's voltage reference, correcting nonlinear terms due to residual charge imbalance in the LTC1043. The input-derived correction is effective because the effect of this imbalance varies directly with frequency.

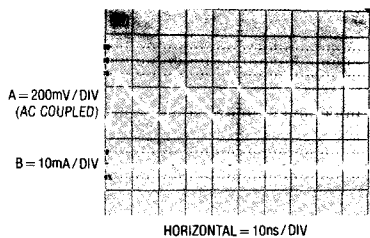


Figure 3. Ramp and Reset Current Detail at 50MHz

The 100MHz full-scale frequency sets stringent restrictions on oscillator cycle time. At this frequency only 10ns is available for a complete ramp-and-reset sequence. The ultimate limitation on speed in the circuit is the time required to reset the varactor-integrator. Figure 3 shows high speed details. The combination of a small amplitude ramp and fast ECL switching yields the necessary high speed operation. Trace A is the ramp and Trace B is the reset current from the ECL gate's open emitter. Note that reset occurs in 3.5ns, with little aberration or overshoot.

Figure 4 plots output frequency jitter as a function of frequency. At 100MHz, jitter is 0.01%, falling to about 0.002% at 1MHz. In this range the jitter is dominated by noise in the current source and ECL inputs. Below this, jitter slowly rises as operating frequency approaches the servo amplifier's roll-off. At 1kHz (10ppm of full-scale) jitter is still below 1%, with about 10% jitter at 1Hz (0.01ppm) for $C_{COMP} = 1\mu\text{F}$. With $C_{COMP} = 0.1\mu\text{F}$, jitter increases below 1kHz and operation below 10Hz is not possible due to loop instability and A1's noise floor. The trade-off is loop settling time. With the larger compensation capacitor the loop settles in 600ms. The $0.1\mu\text{F}$ value permits 60ms settling.

To calibrate this circuit, apply 10.000V and trim the 100MHz adjustment for 100.00MHz at the output. If a fast enough counter is not available, the ± 32 signal at pin 16 of the LTC1043 will read 3.1250MHz. Next, ground the input, install $C_{COMP} = 1\mu\text{F}$ and adjust the "1Hz trim" until the circuit oscillates at 1Hz. Finally, set the "linearity trim" for 50.00MHz for a 5.000V input. Repeat these adjustments until all three points are fixed.

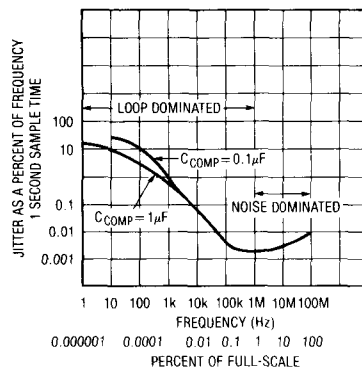


Figure 4. Jitter vs Output Frequency

Application Note 14

Fast Response 1Hz-2.5MHz V → F Converter

Figure 5's circuit is not nearly as fast as Figure 1's, but its 2.5MHz output settles from a full-scale input step in only 3μs. This makes the circuit a good candidate for FM applications or any area where fast response to input movement is required. Linearity is 0.05% with a 50ppm/°C gain tempco. A chopper-stabilized correction network holds zero point error to 0.025Hz/°C. This circuit, a high speed charge-dispensing type (see Box Section) also uses

charge feedback. The charge feedback scheme used is a highly modified, high speed variant of the approach originally described by R. A. Pease (see References). A servo amplifier is not used, permitting fast response to input steps. Instead, the charge is fed back directly to the oscillator, which can respond immediately. Although this approach permits fast response, it also requires attention to parasitics to achieve high linearity and low drift.

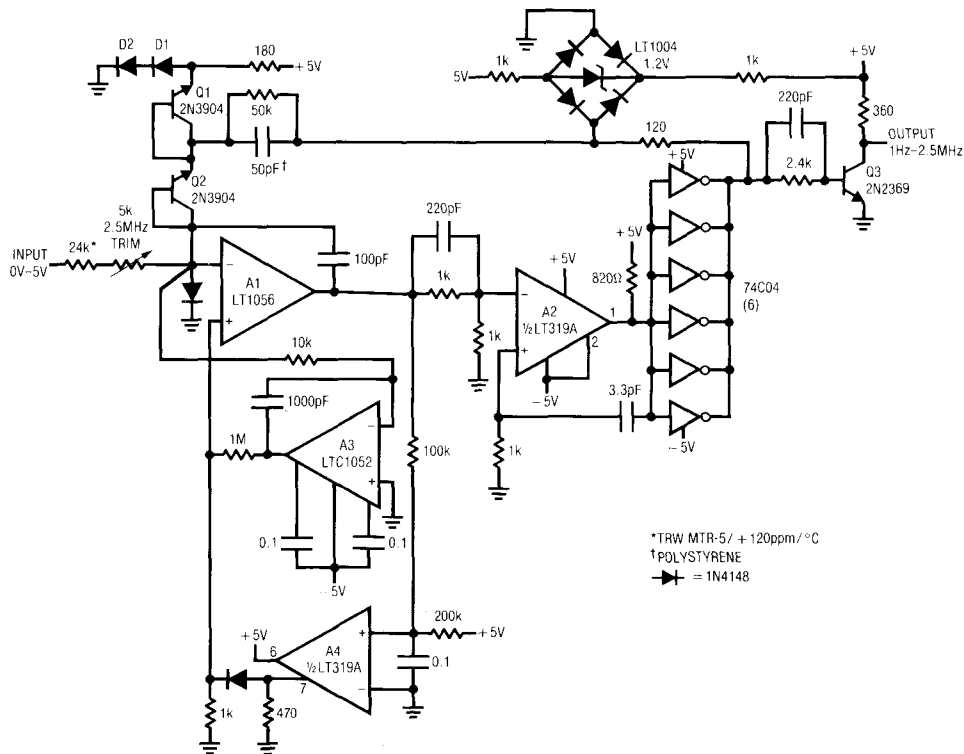


Figure 5. 1Hz → 2.5MHz Fast Response V → F

When an input voltage is applied, A1 integrates in a negative direction (Trace A, Figure 6). When its output crosses zero, A2's output switches, causing the paralleled inverters to go low (Trace B). The feedforward network in A2's negative input aids response. This causes the LT1004-diode bridge to bound at $-2.4V (-V_Z \text{ LT1004}) + (-2V_{FWD})$. Local positive feedback at A2's positive input (Trace C) reinforces this action. During this interval, charge is pulled (Trace D) from A1's summing junction via the 50pF-50k combination, forcing A1's output to move quickly positive. This causes the A2-inverter combination to switch positive (Trace B), bounding the LT1004-diode bridge at $+2.4V$. Now the 50pF capacitor receives charge, while A1 again integrates negative, and the entire cycle repeats. The frequency of this action is a linear function of the input voltage.

D1 and D2 compensate the diodes in the bridge. Diode-connected Q1 compensates steering diode Q2. (The diode-connected transistors provide lower leakage from the summing junction than conventional diodes.) A3, a chopper-stabilized op amp, offset stabilizes A1, eliminating the necessity for zero trimming.

A4 guards against circuit latch-up, which can occur due to the AC-coupled feedback loop. If the circuit latches, A1's output goes to the negative rail and stays there. This causes A4's output (A4 is used in emitter-follower output mode) to go high. A1's output now heads positive, initiating normal circuit behavior. The diode at A1's negative in-

put ensures that the start-up loop will dominate over any input condition.

The 50k resistor across the 50pF charge-dispersing capacitor improves linearity by permitting complete discharge on each cycle, despite junction tailing effects in Q2. The input resistor specified has a temperature coefficient opposite that of the capacitor's, enhancing circuit gain tempo.

Figure 7 shows circuit step response. Trace A is the input, while Trace B is the output. Frequency shift is quick and clean, with no evidence of poor dynamics or time constants.

To trim the circuit, apply 5.000V and adjust the 5k potentiometer for a 2.500MHz output. A3's low offset eliminates the requirement for a zero trim. The circuit maintains 0.05% linearity with 50ppm/°C drift from 1Hz to 2.5MHz. A TTL-compatible output is available at Q3's collector (Trace E). A 10MHz full scale circuit of this type appears in AN13.

High Stability Quartz Stabilized V → F Converter

The gain temperature coefficient of the previous circuits is affected by drift in the charge pumping capacitors. Although compensation schemes were employed in both cases to minimize the effect of this drift, another approach is required to get significantly lower gain drift.

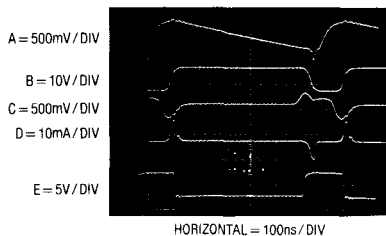


Figure 6. Fast Response V → F Waveforms

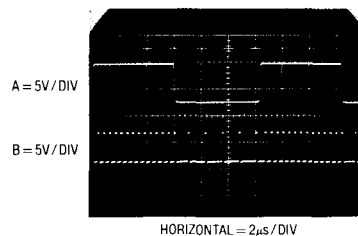


Figure 7. Step Response of 2.5MHz V → F

Application Note 14

Figure 8's circuit reduces gain TC to 5ppm/°C by replacing the capacitor with a quartz-stabilized clock.

In charge pump-based circuits the feedback is based on $Q = CV$. In a quartz-stabilized circuit the feedback is based on $Q = IT$, where I is a stable current source and T is an interval of time derived from the clock.

Figure 9 details Figure 8's waveforms of operation. A positive input voltage causes A1 to integrate in the negative direction (Trace A, Figure 9). The flip-flop's Q1 output (Trace B) changes state at the first positive-going clock edge after A1's output has crossed the D input's switching

threshold. The 50kHz clock (Trace C) comes from the flip-flop's other half, which is driven by A2, a quartz-stabilized relaxation oscillator. The flip-flop's Q1 output controls the gating of a precision current sink composed of A3, the LM199 voltage reference, a FET and the LTC1043 switch. When A1 is integrating negative, the Q1 output is high and the LTC1043 directs the current sink's output to ground via pins 11 and 7. When A1's output crosses the D input's switching threshold, Q1 goes low at the first positive clock edge. LTC1043 pins 11 and 8 close and a precise, quickly rising current flows out of A1's summing point (Trace D).

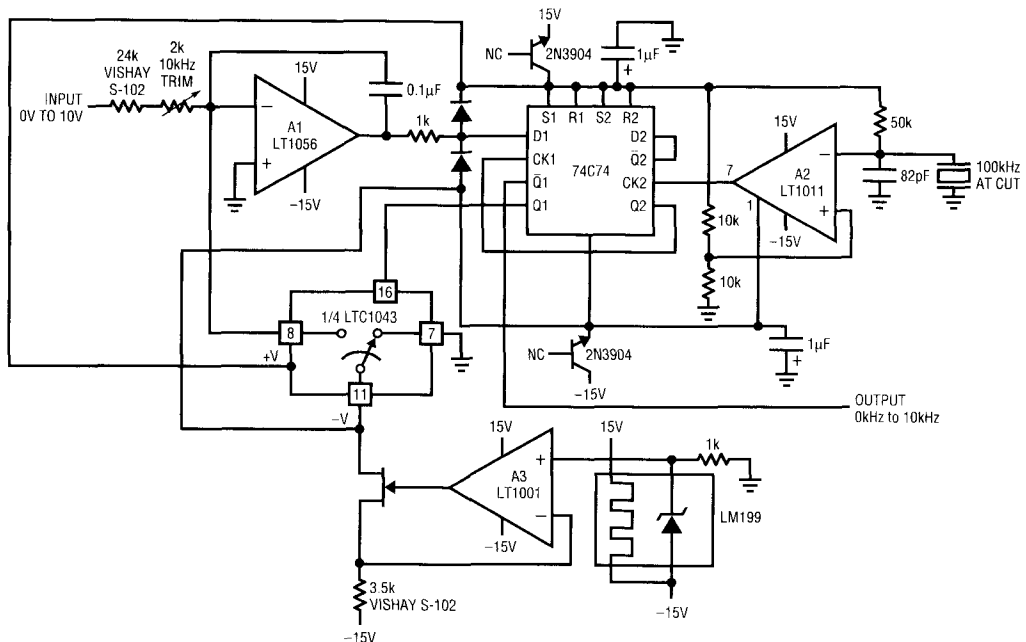


Figure 8. Quartz-Stabilized V → F

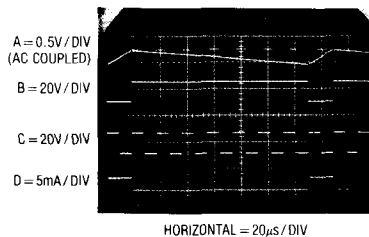


Figure 9. Waveforms for Quartz-Stabilized V → F

This current, scaled to be greater than the maximum signal-derived input current, causes A1's output to reverse direction. At the first positive clock pulse after A1's output crosses the D input's trip point, switching again occurs and the entire process repeats. The repetition frequency depends on the input-derived current, hence the frequency of oscillation is directly related to the input voltage. The circuit's output may be taken from the flip-flop's Q1 or $\bar{Q}1$ outputs. Because this circuit replaces the capacitor with a quartz-locked clock, temperature drift is low, typically 5ppm/°C. The quartz crystal contributes about 0.5ppm/°C, with the remaining drift a function of the current source components, switching time variations and the input resistor.

The reverse-biased 2N3904s serve as zener diodes, providing about 15V across the CMOS flip-flop. The diodes at the D1 input prevent transient overdrive from A1 during circuit start-up.

A $V \rightarrow F$ of this type is usually restricted to relatively low full-scale frequencies, e.g., 10kHz-100kHz, because of speed limitations in accurately switching the current sink.

Additionally, short term frequency jitter may occur because of the uncertain timing relationship between A1's output switching the flip-flop and the clock phase. This is normally not a problem because the circuit's output is usually read over many cycles, e.g., 0.1 to 1 second.

As shown circuit linearity is 0.005%, gain temperature coefficient is 5ppm/°C and full-scale frequency is 10kHz. The LT1056's low input offset reduces zero point error to 0.005Hz/°C. To trim this circuit, apply exactly 10V in and adjust the 2k potentiometer for 10.000kHz output.

Ultra-Linear $V \rightarrow F$ Converter

Figure 10 shows a $V \rightarrow F$ circuit optimized for very high linearity. Although it may be used in a "stand-alone" mode it is specifically intended for processor-driven applications which require 17-bit accuracy, such as weighing scales. This $V \rightarrow F$ has a resolution of 1ppm, with linearity inside 7ppm (0.0007%). When combined with a processor-driven gain/zero calibration loop it has negligible zero and gain drift. To further ease interface with processor-based systems, the circuit functions from a single 5V power supply.

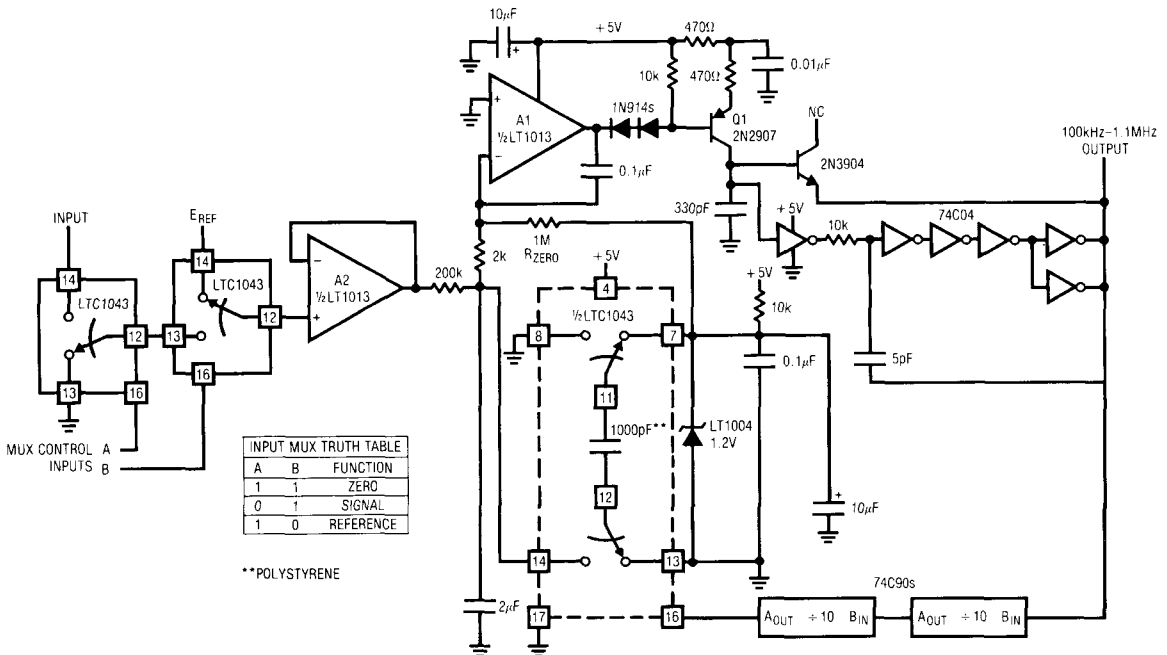


Figure 10. Ultra-Linear $V \rightarrow F$

Application Note 14

The circuit is conceptually similar to the 100MHz $V \rightarrow F$ of Figure 1. A1 servo-controls a crude $V \rightarrow F$ converter composed of Q1, in this case a current source, and the 74C04 gates. The $V \rightarrow F$'s output is divided digitally and drives a charge pump whose output closes a loop back at A1. In Figure 1's case, the crude $V \rightarrow F$'s output was divided down to permit the LTC1043 to function; it cannot operate at 100MHz toggle rates. Here, the divider's purpose is to lower the toggle frequency, allowing the charge pump to achieve much higher precision than with direct feedback.

Before discussing processor-driven operation it is necessary to understand basic circuit operation. To do this, delete A2 and R_{ZERO} . Assume a positive voltage is applied to the left end of the 200k resistor which was previously connected to A2. This forces A1's output to move negatively, turning on Q1. A1's collector (Trace A, Figure 11) ramps the 330pF capacitor positively. When this ramp crosses the 74C04 inverter's threshold, its output moves toward ground, causing the entire chain to switch. AC positive feedback from the paralleled outputs enhances switching. The output inverter's signal (Trace B), the circuit's output, also drives the ± 100 counter chain. The counter's output (Trace C) clocks the LTC1043 which is configured to pump negative charge (Trace D) into the 200k-2k-2 μ F junction. The 2 μ F capacitor integrates the discrete charge events to DC, closing a loop around A1. Thus, A1 biases Q1 at whatever point is required to maintain its inputs at balance. This forces the crude $V \rightarrow F$'s output frequency to be a direct function of the

input voltage over a 0-1MHz output range. The relatively low LTC1043 clock frequency furnished by the dividers permits 0.0007% $V \rightarrow F$ linearity.

For processor-driven auto-zero/gain loop operation, the input multiplexer and R_{ZERO} must be added. With the multiplexer set to the "zero" function (see Truth Table), A2's input is grounded and the 200k resistor receives no drive. A1 receives bias via R_{ZERO} , however, and the circuit oscillates around 100kHz. After the processor has read this frequency it shifts the multiplexer to the "signal" function. Here, A2's output is a buffered version of the signal input. The circuit's output frequency is now determined by this input and the current through R_{ZERO} . Typical outputs will range from 100kHz to 1MHz. After reading this frequency the processor selects the "reference" multiplexer state and determines the frequency produced. The reference voltage must be greater than the largest signal input. It may be either a stable potential or one ratiometrically related to the signal input, as is the case in many transducer-based systems. Typically, it will produce a 1.1MHz output. Once this measurement sequence is completed the processor has enough information to determine the value of the signal input by mathematical manipulation. Additionally, because the multiplexing sequence occurs relatively quickly, drifts in the $V \rightarrow F$ are cancelled. No precision components are required, although the polystyrene capacitor is needed for high linearity. The circuit's 7ppm linearity and 1ppm resolution will suit almost all applications, although processor techniques could be used to obtain even better linearity.

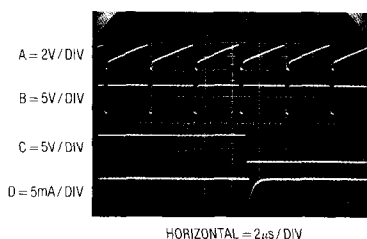


Figure 11. Ultra-Linear $V \rightarrow F$ Waveforms

Single Cell V → F Converter

High speed and precision are not the only areas where special V → F circuits are needed. Figure 12 shows a circuit which runs from a single 1.5V cell with only 125 μ A current drain. The circuit uses an LT1017 dual micropower comparator in a servo-controlled charge pump configuration. The input is applied to C1, which is compensated by the 10 μ F and 1 μ F capacitors to act as an op amp. C1's output drives the 110k-0.02 μ F RC, causing the capacitor to ramp (Trace A, Figure 13).

During the ramp, C2's output is high, turning off Q1 and biasing Q2 on. The potential across the Q3-Q4 V_{BE} voltage reference (Trace B) is zero. The 0.01 μ F capacitor receives no charge. When the ramp equals the potential at C2's positive input, switching occurs. C2's output goes low, and the 0.02 μ F unit discharges. AC positive feedback (Trace C) "hangs up" C2 long enough for a ramp reset of about 80mV. Concurrently, Q1 comes on and Q2 goes off. The Q3-Q4 reference comes on (Trace B) and charges the 0.01 μ F capacitor via Q6.

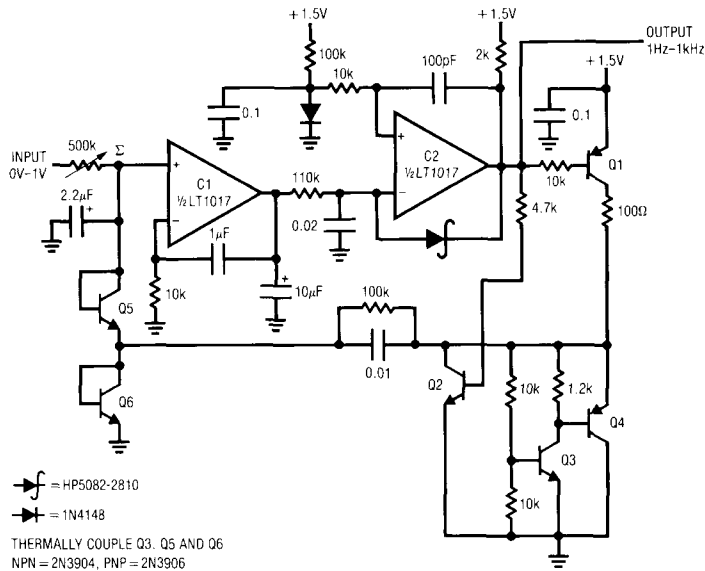


Figure 12. Single Cell V → F

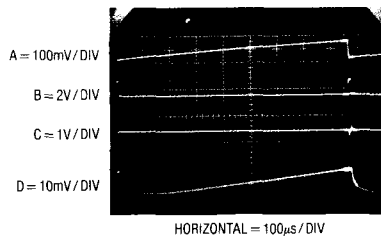


Figure 13. Single Cell V → F Waveforms

Application Note 14

When the positive feedback at C2 ceases, its output returns high, cutting off Q1 and biasing Q2. Now, the 0.01 μ F capacitor discharges, forcing current to flow from C1's 2.2 μ F summing point capacitor (Trace D) via Q5 and Q2. C1 servo-controls this oscillator to whatever frequency is required to maintain C1's summing point near zero. Since the current into C1's input is a linear function of the input voltage, oscillator frequency is also linear. The 1 μ F-10k combination at C1 provides loop stability. The 100k resistor across the 0.01 μ F capacitor influences its discharge characteristic, aiding overall circuit linearity.

The temperature coefficient of the 1.2V Q3-Q4 reference is largely compensated by the junction tempcos of Q5 and

Q6, giving the circuit a 250ppm/ $^{\circ}$ C gain drift. Battery discharge introduces less than 1% error over 1000 hours operation.

Sine Wave Output V \rightarrow F Converter

Almost all V \rightarrow F converters have a pulse or square wave output. Many applications such as audio, filter testing and automatic test equipment require a sine wave output. The circuit of Figure 14 meets this need, spanning a 1Hz to 100kHz range (100dB or 5 decades) for a 0V to 10V input. It is significantly faster than previously published circuits while maintaining 0.1% frequency linearity and 0.2% distortion specifications.

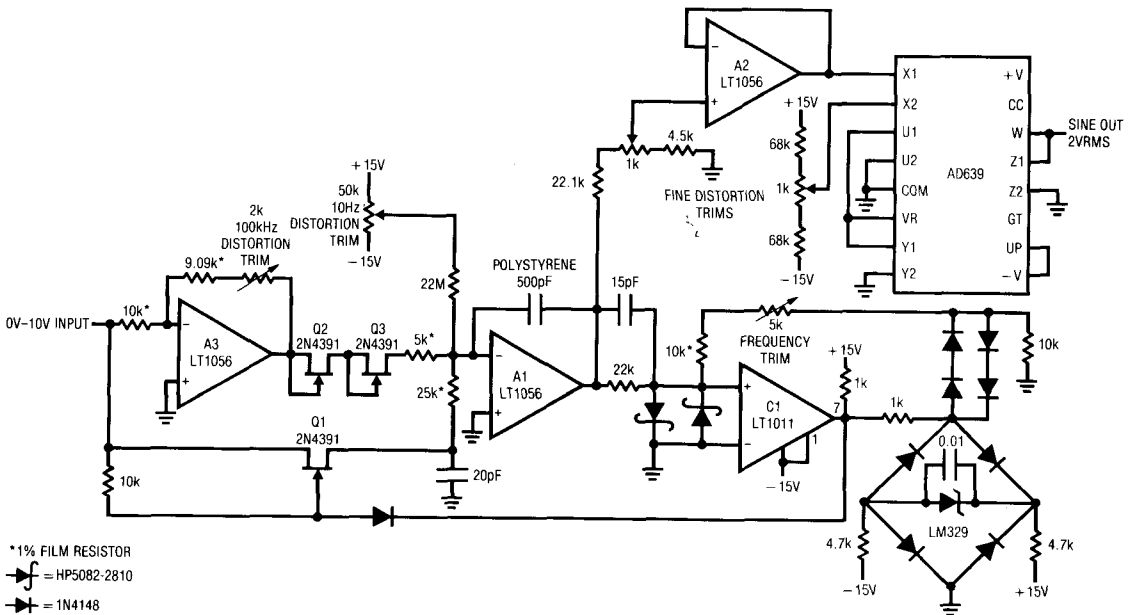


Figure 14. Sine Wave Output 1Hz \rightarrow 100kHz V \rightarrow F (VCO)

To understand the circuit, assume C1 is low, cutting off Q1. The positive input voltage is inverted by A3, which biases the summing node of integrator A1 through the 5k resistor and the self-biased FETs. A current, $-I$, is pulled from the summing point. A1's output (Trace A, Figure 15) integrates positive until C1's input crosses 0V. When this happens, C1's output goes positive (Trace B), allowing Q1 to come on. The resistor in Q1's path is scaled to produce a current, $+2I$, exactly twice the absolute magnitude of the current, $-I$, being removed from the summing node. As a result, the net current into the junction becomes $+I$ and A1 integrates negatively at the same rate its positive excursion took. When A1 integrates far enough in the negative direction, C1's positive input crosses zero and it again switches. This turns Q1 off and the entire cycle repeats. The result is a triangle waveform at A1's output. The frequency of this triangle is dependent on the circuit's input voltage and varies from 1Hz to 100kHz with a 0V-10V input. The LM329 diode bridge and the series-parallel diodes provide a stable bipolar reference which always opposes the sign of A1's output ramp. The Schottky diodes bound C1's positive input, assuring it clean recovery from overdrive. The AD639 trigonometric function generator, biased via A2, converts A1's triangle output into a sine wave (Trace C). The AD639 must be supplied with a triangle wave which does not vary in amplitude or output distortion will result. At high frequencies, delays in the A1 integrator switching loop result in late turn on and turn off of Q1. If the effects of the delays are not minimized,

triangle amplitude will increase with frequency, causing distortion level to also increase with frequency. The 15pF feedforward network at C1's input compensates the delay, keeping distortion to just 0.2% over the entire 100kHz range. At 10kHz, distortion is inside 0.07%. The effects of gate-source charge transfer, which happens whenever Q1 switches, are minimized by the 20pF unit in Q1's source line. Without this capacitor, a sharp spike would occur at the triangle peaks, increasing distortion. The Q2-Q3 FETs compensate the temperature-dependent on-resistance of Q1, keeping the $+2I - I$ relationship constant with temperature. Circuit gain TC is 150ppm and zero point drift is 0.1Hz/°C.

This circuit features extremely fast response to input changes, something most sine wave circuits cannot do. Figure 16 shows what happens when the input switches between two levels (Trace A). The circuit's output (Trace B) shifts frequency immediately, with no glitching or poor dynamics.

To adjust this circuit, put in 10.00V and trim the 2k pot for a symmetrical triangle output at A1. Next, put in 100 μ V and trim the 50k pot for triangle symmetry. Then, put in 10.00V again and trim the 5k "frequency trim" adjustment for a 100.0kHz output frequency. Finally, adjust the "distortion trim" potentiometers for minimum distortion as measured on a distortion analyzer (Trace D). Slight readjustment of the other potentiometers may be required to get lowest possible distortion.

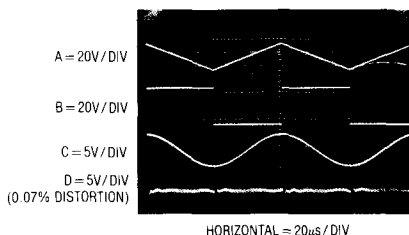


Figure 15. Sine Wave Output V — F Converter Waveforms

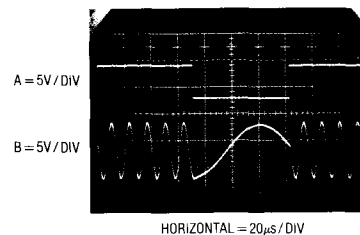


Figure 16. Sine Wave Output V — F Input Step Response

Application Note 14

1/X Transfer Function $V \rightarrow F$ Converters

Another dimension in $V \rightarrow F$ design is converters which have a deliberate nonlinear transfer function. Such converters are useful in linearizing outputs from transducers such as gas sensors and flow meters. Figure 17's circuit converts input voltages of 0V to 10V to an output frequency of 1kHz to 2Hz with a 0.05% accurate 1/X conformity.

A1 integrates current from the LT1009 2.5V reference. A1's negative output ramp (Trace A, Figure 18) is compared at C1 to the input voltage via a current summing network. When C1's input goes negative, its output (Trace B) falls, triggering the flip-flop (Trace C) Q output high. This turns on Q1, resetting the ramp. When the ramp reset gets very

near ground, C2 triggers low (Trace D), resetting the Q output low. This turns off Q1, allowing the ramp to begin again and the entire cycle repeats. Waveforms E, F, G and H are expanded versions of A through D, respectively, and show detail of the ramp resetting sequence.

In most $V \rightarrow F$ converters the input signal controls the integrator slope. Here the integrator runs at a fixed slope. The length of time the integrator requires to cross the input voltage is inversely proportional to the input's amplitude and loop oscillation is related by 1/X to the input. The ramp reset time is a first order error term because it is lost in the integration. At low frequencies the

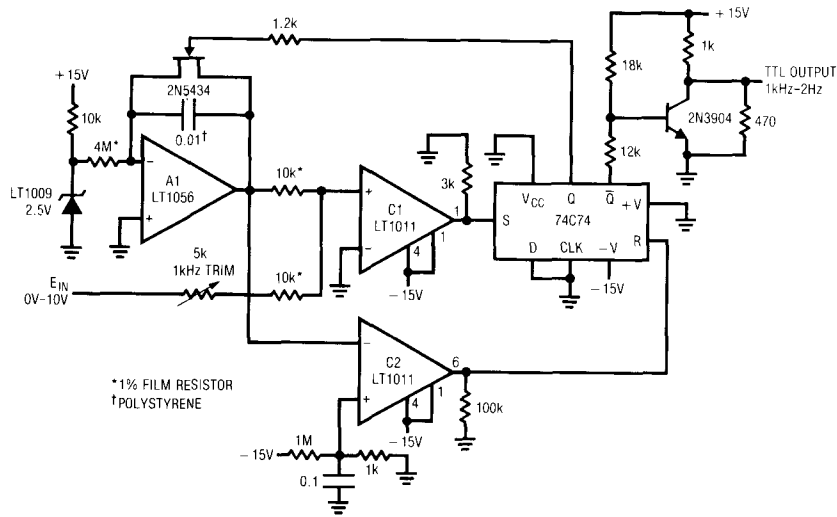


Figure 17. $\frac{1}{E_{IN}} \rightarrow$ Frequency Converter

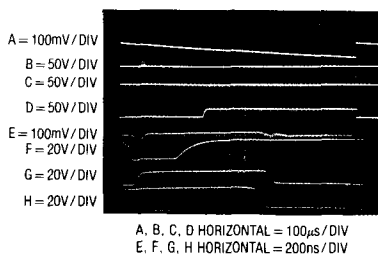
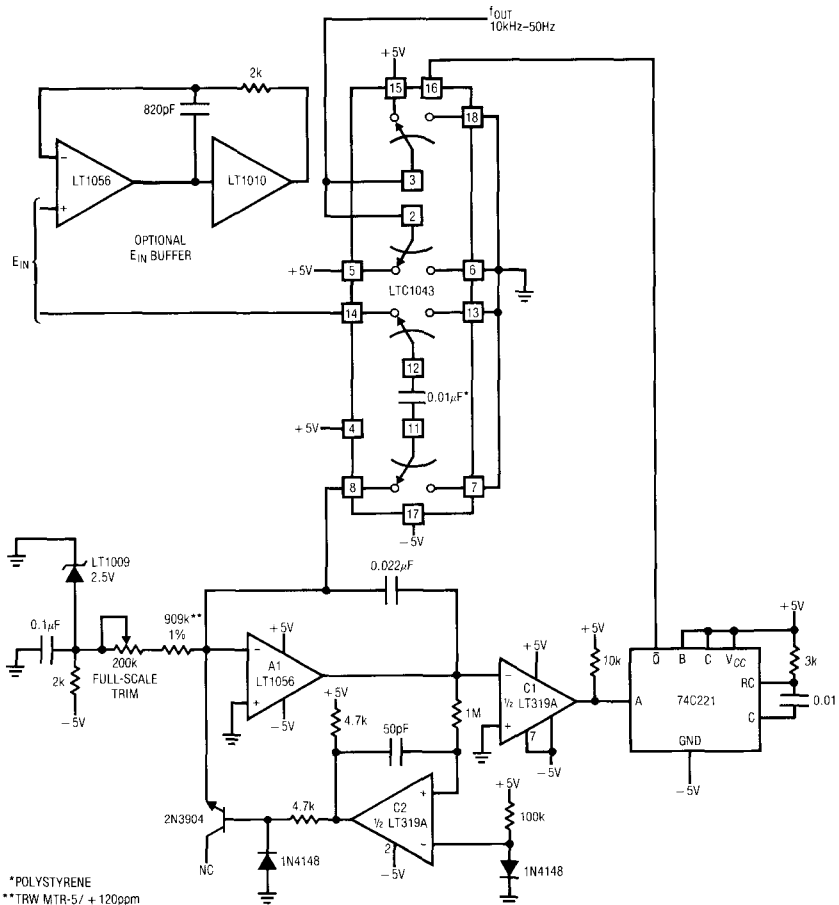


Figure 18. $\frac{1}{E_{IN}} \rightarrow$ Frequency Converter Waveforms

ramp reset time is a small term, even though reset takes longer (because the ramp had to run to a higher amplitude to cross the input). At higher frequencies, even though it is shorter, the reset period becomes significant because its "dead time" is a substantial percentage of the oscillation frequency. The 2 comparator-flip-flop reset scheme reduces this error by adaptively controlling and minimizing the ramp reset time, regardless of peak ramp amplitude. A simple fixed AC feedback scheme would not do this because its time constant would have to be long enough to reset the ramp from large peak amplitudes (e.g., at low frequency). Even with this reset arrangement, the circuit's

0.05% 1/X conformity can only be achieved by limiting maximum frequency to about 1kHz. It is worth noting that this circuit has almost ten times the accuracy of analog multipliers and other analog 1/X computing techniques. Circuit drift is about 150ppm/°C. To trim the circuit, put in 50mV and adjust the 5k potentiometer for 1kHz output.

Figure 19's 1/X V → F, developed by R. Essaff, provides better performance, although it is somewhat more complex. This charge pump class design gives 0.005% 1/X conformity, 50ppm/°C drift and 10kHz-50Hz outputs for 0V to 5V in.



* POLYSTYRENE
 ** TRW MTR-5/ + 120ppm

Figure 19. Charge Pump $\frac{1}{E_{IN}} \rightarrow$ Frequency Converter

Application Note 14

A1 and its associated components form an integrator which ramps positive (Trace A, Figure 20). When A1's output crosses zero, C1 goes negative (Trace B), triggering the one-shot. The one-shot output (Trace C) toggles the LTC1043 switch, transferring charge from E_{IN} to A1's summing point via the $0.01\mu\text{F}$ capacitor (Trace D). This forces A1's output negative by an amount related to the charge transferred. When charge transfer ceases, A1 again ramps positively. The depth of A1's negative excursion is directly proportional to E_{IN} , hence loop oscillation frequency is inversely ($1/X$) related to E_{IN} .

The circuit's output is taken from the paralleled LTC1043 switch sections.

Because this circuit relies on charge feedback, integrator reset time does not influence accuracy. The loop runs at whatever frequency is required to maintain A1's summing point at zero.

If A1's output ever overruns 0V, the oscillator loop will latch. This condition is detected by C2, which goes high, driving current into A1's summing point via the low

leakage 2N3904 BE junction. A1's output is forced negative, and normal circuit operation commences.

This circuit's primary disadvantage is that the input signal must be capable of supplying substantial current each time the LTC1043 commutates the $0.01\mu\text{F}$ capacitor to A1's summing point. The current required varies directly with input voltage, with 25mA drawn at $E_{IN}=5\text{V}$. The optional input buffer shown will provide the necessary drive, although input voltage range must fall within the buffer's common-mode limits.

To calibrate this circuit, apply exactly 5V and trim the $200\text{k}\Omega$ potentiometer for 50Hz output.

E^X Transfer Function $V \rightarrow F$ Converter

Figure 21's $V \rightarrow F$ circuit responds exponentially to its input voltage. It is ideally suited to electronic music synthesizers and, as shown, has a 1V in/octave of frequency out scale factor. Exponential conformity is within 0.13% over a 10Hz–20kHz range and drift is 150ppm/°C. The circuit has a pulse output and also provides a ramp output for applications which require substantial power at the fundamental frequency.

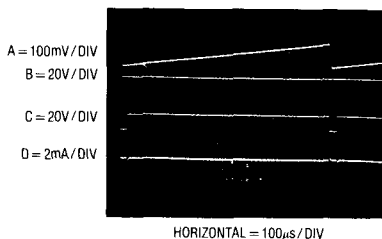


Figure 20. Charge Pump-Based $\frac{1}{E_{IN}}$ \rightarrow Frequency Converter Waveforms

A1's $1\mu\text{F}$ input capacitor integrates current from Q4's emitter, forming a ramp at A1's input (Trace A, Figure 22). When the ramp crosses zero, A1's output flips (Trace B, Figure 22), causing the LTC1043 to change states. The $0.0012\mu\text{F}$ capacitor, charged to the LT1021's 10V potential, is switched to pull current from A1's summing point (Trace C). The 30pF capacitor provides A1's positive input with positive AC feedback (Trace D), insuring enough time for a complete discharge of the $0.0012\mu\text{F}$ unit. This action

forces A1's input ramp to go in a negative direction, resetting it toward zero. When the positive AC feedback around A1 decays, the cycle repeats. Q5 and its associated components form a start-up loop, insuring proper circuit start sequence. Start-up conditions or input overdrive could force A1's output to go to the negative rail and stay there. If this occurs, Q5 comes on, pulling A1's negative input toward -15V and initializing normal circuit operation.

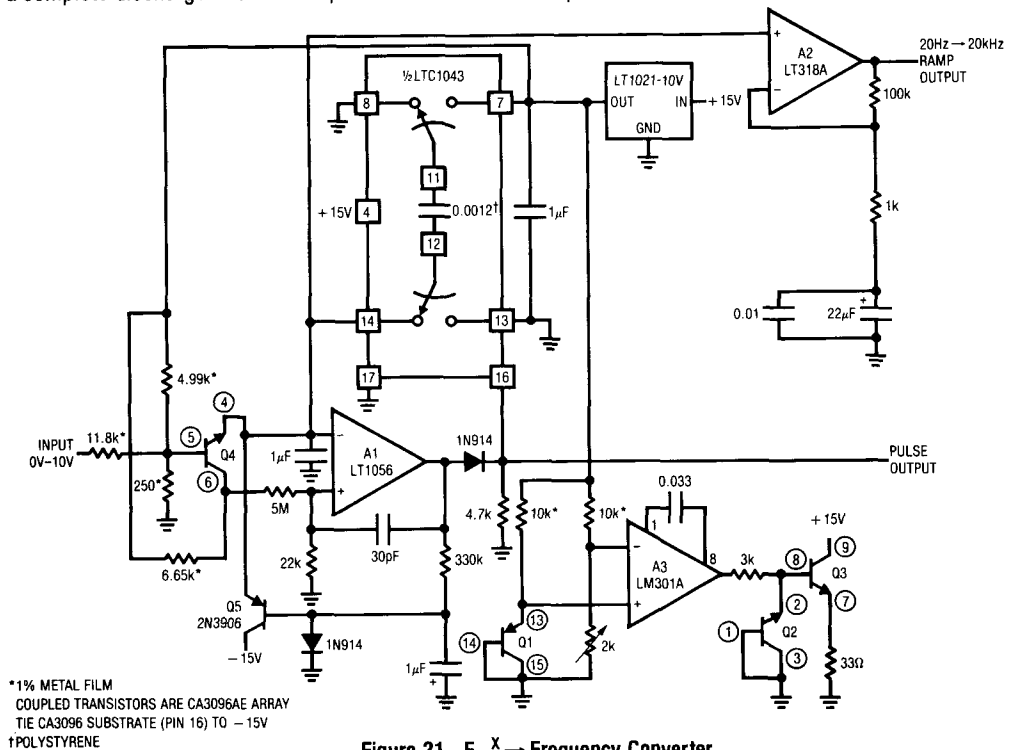


Figure 21. $E_{IN}^X \rightarrow$ Frequency Converter

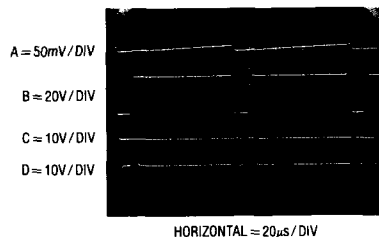


Figure 22. $E_{IN}^X \rightarrow$ Frequency Converter Waveforms

Application Note 14

The oscillation frequency of this charge pump class current-to-frequency converter is linearly related to Q4's emitter current. Q4's emitter current, in turn, is exponentially related to its V_{BE} , which is determined by the resistors connected to it and the input voltage. This is in accordance with the well-known relationship between collector current and V_{BE} in transistors. Normally Q4's operating point would be quite sensitive to temperature, but it is part of an array which is temperature-stabilized by the A3 configuration. Q1, also part of the array, senses temperature. A3 compares Q1's V_{BE} with a bridge potential and drives array transistor Q3 to close a thermal control loop. This stabilizes the array, preventing ambient temperature shifts from influencing Q4's operation. Q2, serving as a clamp, ensures against loop lock-up conditions and prevents Q3 from ever becoming reverse biased.

With the thermal loop controlling Q4, the circuit's exponential behavior is stable and repeatable. The $5M\Omega$ value from Q4's collector to A1's positive input introduces a slight shift in A1's operating point at high frequencies (e.g., high Q4 collector currents). This compensates Q4's bulk emitter resistance term, maintaining good exponential performance up to 20kHz. The 4.99k resistor sets the 0V input frequency at about 10Hz, while the 250Ω value establishes circuit k factor, nominally 1V/octave output, as shown.

To use this circuit, adjust the 2k potentiometer so that A3's negative input is 100mV below its positive input with Q3's base grounded. Next, unground Q3's base and the circuit is ready for use.

$$\frac{R1}{R2} = \frac{V1}{V2} \rightarrow \text{Frequency Converter}$$

Figure 23's circuit produces an output frequency proportional to the ratio of the voltages across two externally supplied resistors. This circuit has wide application in transducer signal conditioning. Both R1 and R2 are ground-referred, preferable for noise considerations. In this case, R1 is a Platinum resistance sensor, with R2 being set at the sensor's 0°C value. The grounded end of R2 allows fine trimming with decade boxes without excessive noise problems. R1's grounded side allows it to be located at the end of a cable run, with similar noise rejection properties.

The 6012 DAC serves as a simple source of two identical currents. The DAC's MSB is set high and all other bits are low. This sets the DAC's output currents equal. With constant, equal, currents through them, R1 and R2 produce a differential voltage which is sampled by the LTC1043 switch-capacitor configuration. The LTC1043's internal clock continuously switches the 3900pF capacitor across the R1-R2 pair and then dumps the charge into A1's summing point. The quantity of charge delivered per cycle is a direct function of the voltage difference across R1 and R2 ($Q = CV$). A1's output ramps (Trace A, Figure 24) negative. The ramp is compared to A2's output at C1. A2's DC output is a function of the 330pF charge pump capacitor at the LTC1043, A2's feedback resistor and the LTC1043 clock frequency. Because A1 and A2 are receiving charge at the same rate, LTC1043 oscillator drift affects each equally and does not contribute error.

When A1's ramp crosses A2's output value, C1 goes high (Trace B), turning on the FET. AC positive feedback to C1's positive input (Trace C) ensures a complete discharge for A1's feedback capacitor. When the feedback ceases, the cycle repeats. The oscillation frequency is a linear function of the R1-R2 ratio.

The two polystyrene capacitors at the LTC1043 provide temperature coefficient cancellation. A2's specified feedback resistor compensates A1's polystyrene feedback capacitor. Overall circuit tempco is about 35ppm/°C. As shown, a 0°C–100°C excursion at the R1 sensor gives a 0kHz–1kHz output with an accuracy, limited by the sensor, of 0.35°. This is well outside the dead time error produced by A1's reset time and the circuit contributes no appreciable measurement error. In practice, slight trimming of R2's value may be required to compensate for individual R1 tolerances at 0°. The 5k potentiometer trims for 1kHz out at a 100°C R1 temperature. This circuit may be used with any resistive based transducer. For negative tempco devices, reverse the positions of R1 and R2.

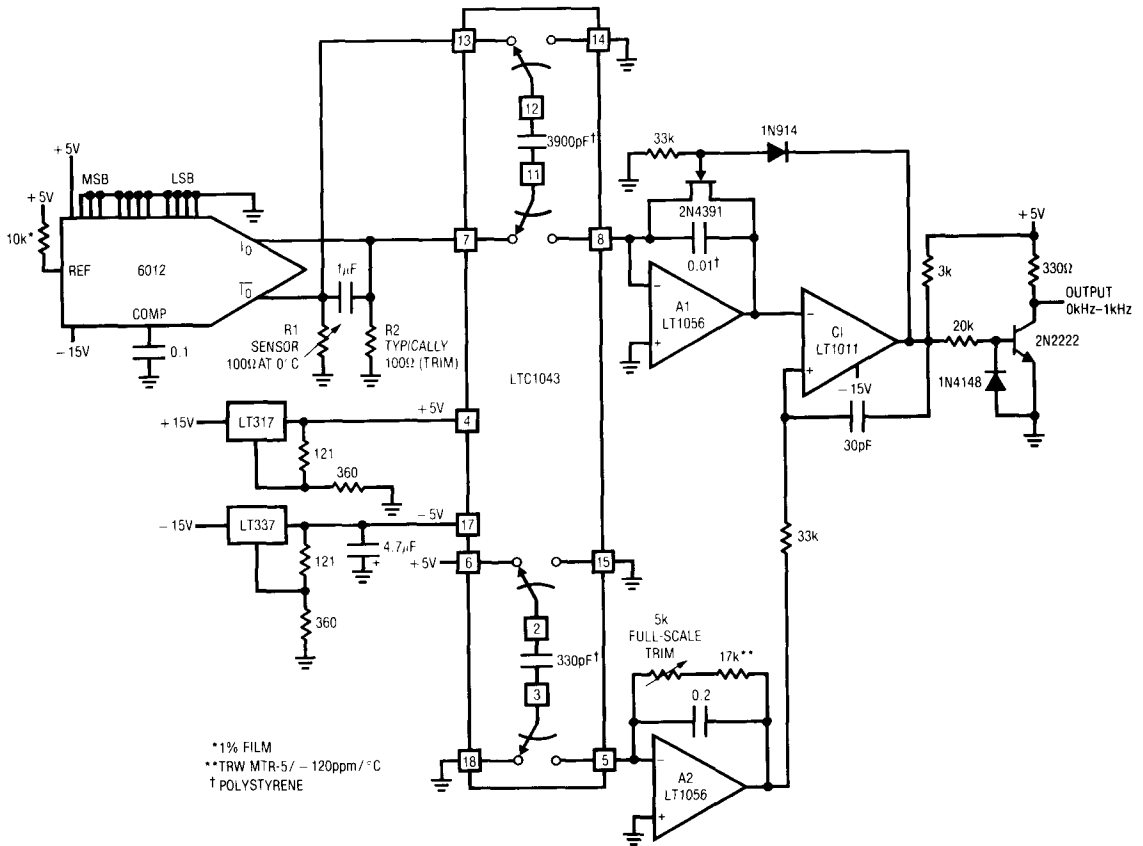


Figure 23. $\frac{R1}{R2} = \frac{V1}{V2}$ → Frequency Converter

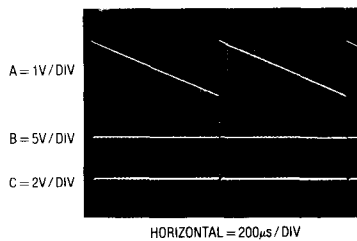


Figure 24. $\frac{R1}{R2} = \frac{V1}{V2}$ → Frequency Converter Waveforms

Application Note 14

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5. Gilbert B., "A Versatile Monolithic Voltage-to-Frequency Converter," *IEEE J. Solid State Circuits*, Volume SC-11, pages 852-864, December 1976.
6. Williams, J., "Applications Considerations and Circuits for a New Chopper Stabilized Op Amp," 1Hz-30MHz $V \rightarrow F$, pages 14-15, Linear Technology Corporation, Application Note 9.

BOX SECTION

V \rightarrow F Techniques

There are many ways to convert a voltage to a frequency. The best approach in an application varies with desired precision, speed, response time, dynamic range and other considerations. Figure B1 shows one of the most obvious. The input drives an integrator. The integrator's ramp slope varies with the input-derived current. When the ramp crosses V_{REF} , the comparator turns on the switch, discharging the capacitor and reinitializing the cycle. The frequency of this action directly relates to input voltage. With careful design, one op amp can serve as both integrator and comparator, providing circuit economy.

A serious drawback to this approach is the capacitor's discharge-reset time. This time, "lost" in the integration, results in significant linearity error as operating frequency

approaches it. For example, a $1\mu s$ reset interval introduces 0.1% error at 1kHz, rising to 1% at 10kHz. Also, variations in reset time contribute additional errors. Because of this, circuit operation is restricted to relatively low frequencies if good linearity and stability are required. Although various compensation methods can reduce these errors, performance is still limited.

Figure B2 gets around B1's problems by enclosing the integrator in a charge-dispensing loop. In this approach C1 charges to V_{REF} during the integrator's ramping time. When the comparator trips, C1 is discharged into A1's summing point, forcing its output high. After C1's discharge, A1 begins to ramp and the cycle repeats.

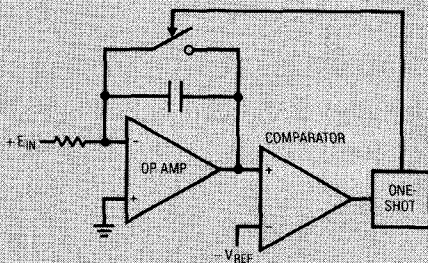


Figure B1. Ramp-Comparator V \rightarrow F

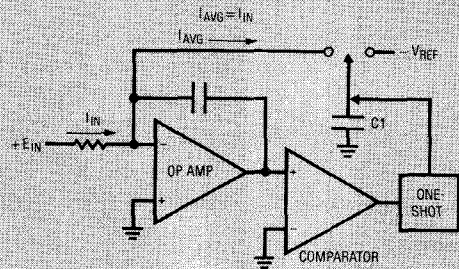


Figure B2. Charge Pump V \rightarrow F

Because the loop acts to force the average summing currents to zero, integrator time constant and reset time do not affect frequency. This approach yields high linearity (typically 0.01%) up to high frequencies. With attention to design, converters of this type can be constructed with a single op amp.

Figure B3 is conceptually similar, except that it uses feedback current instead of charge to maintain the op amp's summing point. Each time the op amp's output trips the comparator, the current sink pulls current from the summing point. Current is pulled from the summing point for the timing reference's duration, forcing the integrator positive. At the end of the current sink's period, the

integrators output again heads negative. The frequency of this action is input-related.

Figure B4 uses DC loop correction. This arrangement offers all the advantages of charge and current balancing except that response time is slower. Additionally, it can achieve exceptionally high linearity (0.001%), output speeds exceeding 100MHz and very wide dynamic range (160dB). The DC amplifier controls a relatively crude $V \rightarrow F$. This $V \rightarrow F$ is designed for high speed and wide dynamic range at the expense of linearity and thermal stability. The circuit's output switches a charge pump whose output, integrated to DC, is compared to the input voltage.

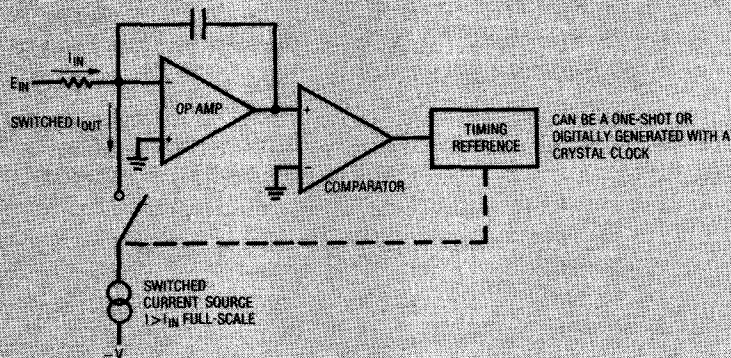


Figure B3. Current Balance $V \rightarrow F$

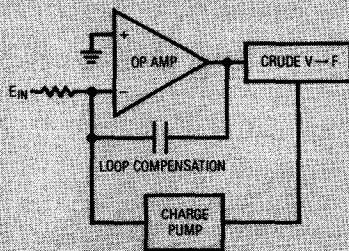


Figure B4. Loop-Charge Pump $V \rightarrow F$

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The DC amplifier forces $V \rightarrow F$ operating frequency to be a direct function of input voltage. The DC amplifier's frequency compensation capacitor, required because of loop delays, limits loop response time. Figure B5 is similar, except that the charge pump is replaced by digital counters, a quartz time base and a DAC. Although it is not immediately obvious, this circuit's resolution is not restricted by the DAC's quantizing limitations. The loop

forces the DAC's LSB to oscillate around the ideal value. These oscillations are integrated to DC in the loop compensation capacitor. Hence, the circuit will track input shifts much smaller than a DAC LSB. Typically, a 12-bit DAC (4096 steps) will yield 1 part in 50,000 resolution. Circuit linearity, however, is set by the DAC's specification. An example of this approach appears in AN-13, "High Speed Comparator Techniques".

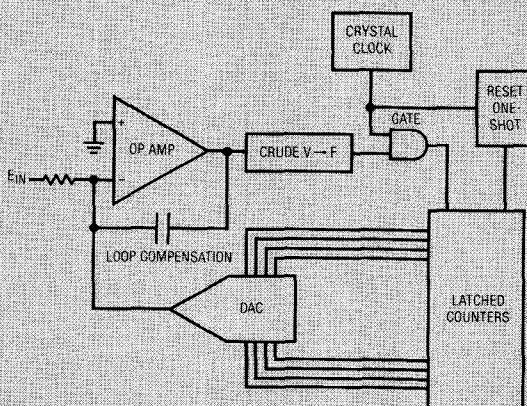


Figure B5. Loop-DAC $V \rightarrow F$

Circuitry for Single Cell Operation

Jim Williams

Portable, battery powered operation of electronic apparatus has become increasingly desirable. Medical, remote data acquisition, power monitoring and other applications are good candidates for battery operation. In some circumstances, due to space, power or reliability considerations, it is preferable to operate the circuitry from a single 1.5V cell. Unfortunately, a 1.5V supply eliminates almost all linear ICs as design candidates. In fact, the LM10 op amp-reference and the LT1017/LT1018 comparators are the only IC gain blocks fully specified for 1.5V operation. Further complications are presented by the 600mV drop of silicon transistors and diodes. This limitation consumes a substantial portion of available supply range, making circuit design difficult. Additionally, any circuit designed for 1.5V operation must function at end-of-life battery voltage, typically 1.3V. (See Box Section, "Components For 1.5V Operation.")

These restrictions are painful, especially if complex linear circuit functions such as data converters and sample-holds are needed. Despite the problems, designing such circuits is possible by combining considerable attention to component characteristics with unusual circuit methods.

10kHz V-F Converter

Figure 1, an example of this approach, is a complete 1.5V powered 10kHz V-F converter. A 0-1V input produces a 25Hz to 10kHz output, with a transfer linearity of 0.35%. Gain drift is 250ppm/°C and current consumption about 205 μ A.

To understand circuit operation, assume C1's positive input is slightly below its negative input (C2's output is low).

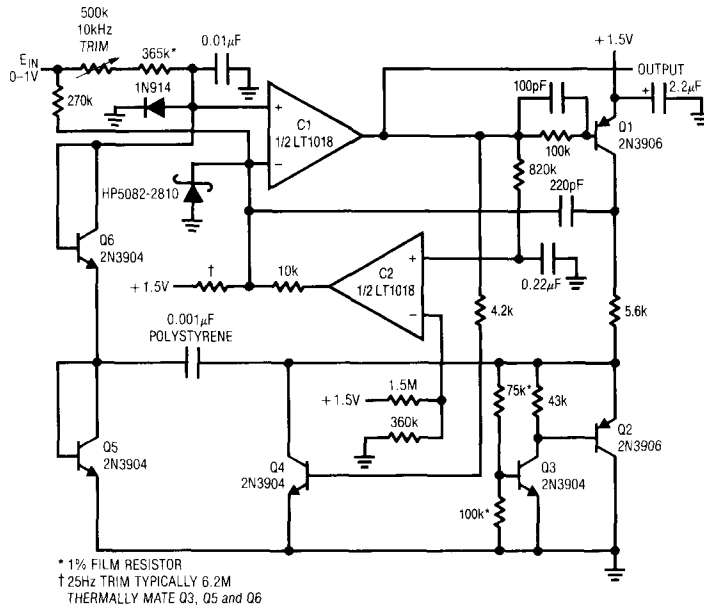


Figure 1. 10kHz V-F Converter

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The input voltage causes a positive going ramp at C1's positive input (Trace A, Figure 2). C1's output (Trace B) is low, biasing Q1 on. Q1's collector current drives the Q2-Q3 combination, forcing Q2's emitter (Trace C) to clamp at 1V. The 0.001 μ F capacitor charges to ground (0.001 μ F unit's current waveform is Trace D) via Q5. When the ramp at C1's positive input goes high enough, C1's output goes high, cutting off Q1, Q2 and Q3. Q4 conducts, pulling current from C1's positive input capacitor via Q6. This current removal resets C1's positive input ramp to a potential slightly below ground, forcing C1's output low. The 100pF capacitor at Q1's collector furnishes AC positive feedback, ensuring that C1's output remains positive long enough for a complete discharge of the 0.001 μ F capacitor.

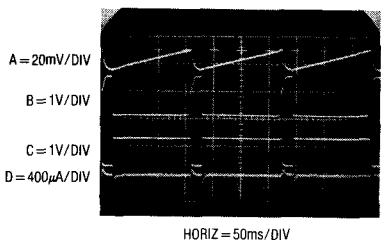


Figure 2. V-F Operating Waveforms

The Schottky diode prevents C1's input from being driven outside its negative common-mode limit. This action cuts off Q4, Q1-Q3 come on and the entire cycle repeats. The oscillation frequency directly depends on the input voltage-derived current. The temperature coefficient of the Q2-Q3 1V clamp is largely compensated by the junction tempcos of Q5 and Q6, minimizing overall temperature

drift. The 270k Ω resistor path provides an input voltage derived trip point for C1, enhancing circuit linearity performance. This resistor should be selected to achieve the quoted linearity.

Circuit start-up or overdrive can cause the circuit's AC-coupled feedback loop to latch. If this occurs, C1's output goes high. C2 detects this, via the 820k-0.22 μ F lag, and also goes high, lifting C1's negative input towards +1.5V. Because C1's positive input is diode clamped at 600mV, its output switches low, initiating normal circuit behavior.

To calibrate this circuit, select the 100k value for $V_{CLAMP} = 1V$. Next, apply 2.5mV at the input and select the resistor value indicated at C1's input for a 25Hz output. Then, put in exactly 1V and trim the 500k Ω potentiometer for 10kHz output.

10 Bit A-D Converter

Figure 3 is another data converter circuit. This integrating A-D converter has a 60ms conversion time, consumes 460 μ A from its 1.5V supply and maintains 10 bit accuracy over a 15°C to 35°C temperature range.

A pulse applied to the convert command line (Trace A, Figure 4) causes Q3, operating in inverted mode, to discharge the 1 μ F capacitor (Trace B). Simultaneously, Q4 is biased through the 10k-diode path, forcing its collector (Trace D) low. Q3's inverted mode switching results in a capacitor discharge within 1mV of ground. When the convert command falls low, Q3 goes off, Q4's collector lifts, and the LT1004 stabilized Q1-Q2 current source charges the 1 μ F unit with a linear ramp. During the time the ramps value is below the input voltage, C1A's output is low (Trace C). This

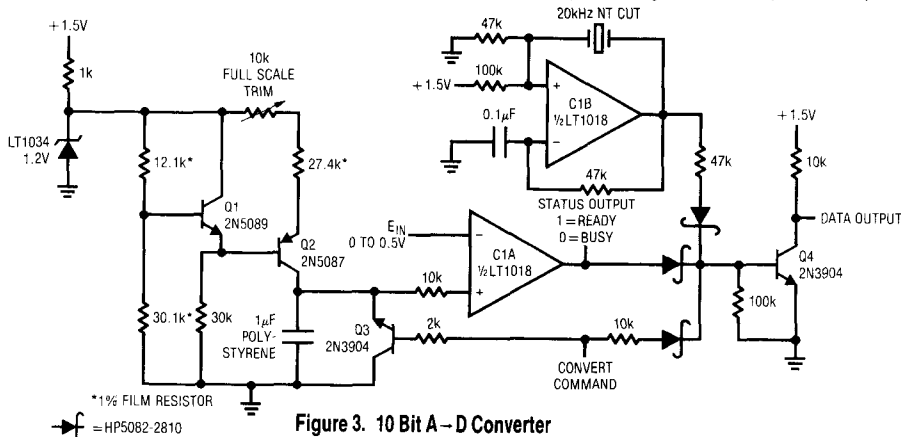


Figure 3. 10 Bit A-D Converter

allows pulses from C1B, a quartz stabilized oscillator, to modulate Q4. Output data appears at Q4's collector (Trace D). When the ramp crosses the input voltages value C1A's output goes high, biasing Q4 and output data ceases. The number of pulses appearing at the output is directly proportional to the input voltage. To calibrate this circuit apply 0.5000V to the input and trim the 10k potentiometer for exactly 1000 pulses out each time the convert command line is pulsed. No zero trim is required, although Q3's inverted 1mV saturation voltage limits zero resolution to 2 LSBs.

Sample-Hold Amplifier

A logical companion to the A-D converter described is a sample-and-hold amplifier. A sample-and-hold is one of the most difficult circuits to design for 1.5V operation, primarily because FET switches with low enough pinch-off voltages are not available. Two methods are presented here. The first circuit gets around the switch problem with an ap-

proach that eliminates the switch. Although an unusual way to implement a sample-and-hold, it requires no special components or trimming, is easy to build and has a 4ms acquisition time to 0.1%. The second circuit, a more conventional design, requires specially selected and matched components and is more complex, but offers 125 μ s (0.1%) acquisition time—a 30 \times improvement over the other design.

When a sample command (Figure 5, Trace A) is applied to the circuit of Figure 6, Q1, operating in inverting mode, discharges the 1 μ F capacitor (Trace C). When the sample command falls, Q1 goes off and C1A's internal output pull-up current source (Trace B) charges the capacitor via Q2, connected as a low leakage diode. The capacitor's charging ramp is followed by the LM10, which biases C1B's positive input. When the ramp potential crosses the circuit's input voltage, applied to C1B's negative input, C1B's output goes high (Trace D).

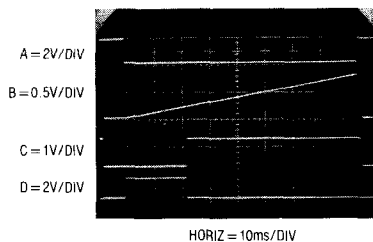


Figure 4. A-D Converter Waveforms

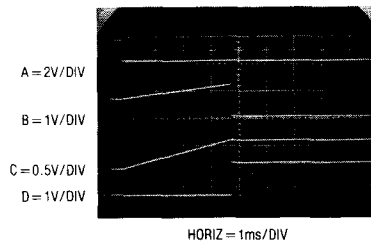


Figure 5. Sample-Hold Waveforms

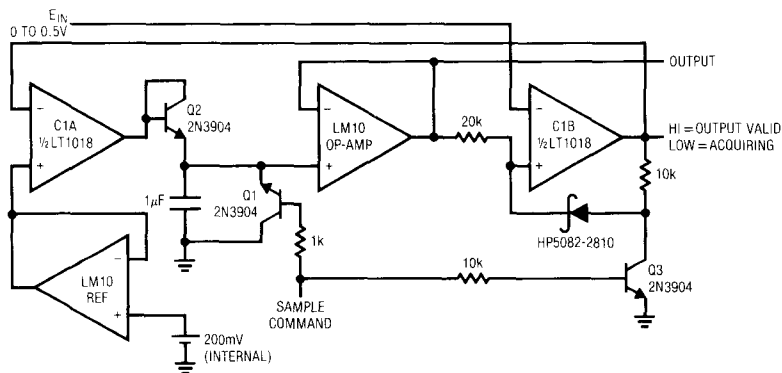


Figure 6. Sample-Hold Circuit

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This forces C1A's output low, and the $1\mu\text{F}$ capacitor stops charging. Under these conditions, the circuit is in the "hold" mode. The voltage the capacitor sits at is the same as the input voltage, and the circuit output is taken at the LM10. The $10\text{k}\Omega$ diode path at C1B provides a latch, preventing input voltage changes or noise from affecting the value stored in the $1\mu\text{F}$ capacitor. When the next sample command is received, Q3 breaks the latch and circuit action repeats.

Acquisition time is directly proportional to input value, with 4ms required for full-scale (0.5V). Although faster acquisition is possible, the delay in shutting off C1A's output will degrade accuracy. The circuit's primary advantages are elimination of the FET switch requirement and relative simplicity. Accuracy is 0.1% , droop rate specs at $10\mu\text{V}/\text{ms}$ and current consumption is $350\mu\text{A}$.

Fast Sample-Hold Amplifier

Figure 7, a more conventional approach to a sample-and-hold, is significantly faster, but also more complex and has special construction requirements. Q1 serves as the sample-and-hold switch, with Q6 and Q7 providing a level shift to drive the gate. To minimize power consumption, a 1500pF feed-forward path is used for fast gate switching without resorting to high operating currents in Q6 and Q7. C1A, a

simple squarewave oscillator, drives Q4. C1B inverts C1A's output and biases Q5. The transistors serve as synchronous switches and charge is pumped to the $2.2\mu\text{F}$ capacitor at Q5's collector, resulting in a negative potential there.

Q1's low pinch-off voltage is obtained at the expense of on-resistance. The typical R_{ON} of $1.5\text{--}2\text{k}\Omega$ means the circuit's hold capacitor must be small if fast acquisition is desired. This mandates a low bias current output amplifier, or droop rate will suffer. Q2, Q3 and A2 meet this need. Q2 and Q3 are set up as source followers, with the resistors used as level shifters to keep A2's inputs inside the LM10's common-mode range. A2's output diode ensures clean dynamic performance for voltages close to zero by setting the LM10's output bias point well above ground. The 180pF capacitor compensates the composite amplifier.

Several special considerations are required to use this circuit. Q1, an extremely low pinch-off device, must be further selected for a pinch-off below 500mV to enable proper turn-off. Also, any V_{GS} mismatch between Q2 and Q3 will contribute offset error, and these devices must be selected for V_{GS} matching within $500\mu\text{V}$. Additionally, the Q2-Q3 V_{GS} absolute value must be inside 500mV or A2 may encounter common-mode limitations for circuit inputs near full-scale.

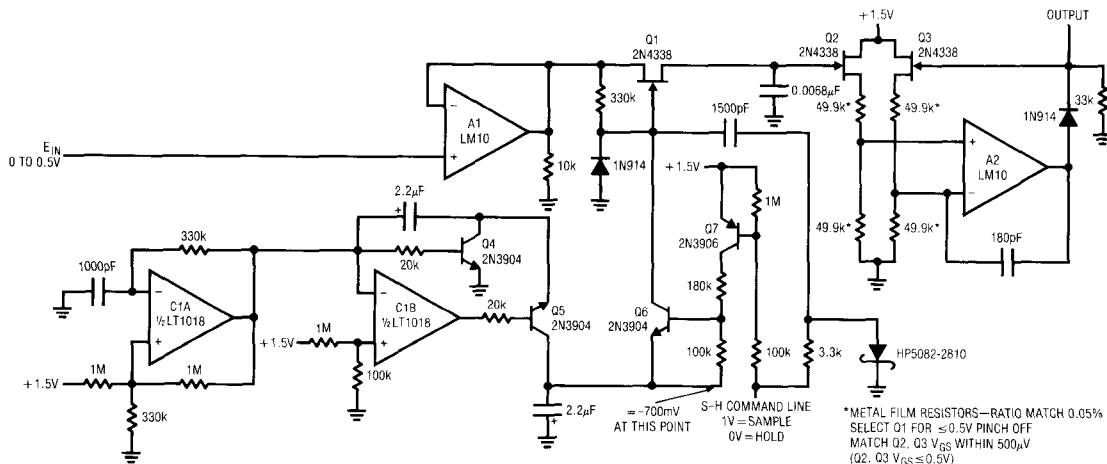


Figure 7. Fast Sample-and-Hold

Finally, mismatches in the resistor level shift contribute a gain error. To hold 0.1% circuit accuracy, the resistors should be ratio matched within 0.05%.

Once these special provisions have been attended to, the circuit delivers excellent specifications for a 1.5V powered sample-hold. Acquisition time is $125\mu\text{s}$ to 0.1% with a droop rate of $10\mu\text{V/ms}$. Current consumption is inside $700\mu\text{A}$.

Figure 8 shows the circuit acquiring a full-scale input. Trace A is the sample-hold command, while Trace B is the circuit's output. Trace C, an amplitude expanded version of B, shows acquisition detail. The input is acquired within $125\mu\text{s}$ and sample-to-hold offset is within a millivolt.

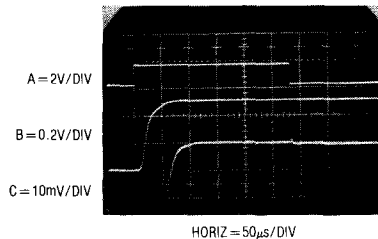


Figure 8. Fast Sample-Hold Waveforms

Temperature Compensated Crystal Clock

Many systems require a stable clock source and crystal oscillators which run from 1.5V are relatively easy to construct. However, if good stability over temperature is required, things become more difficult. Ovenizing the crystal is one approach, but power consumption is excessive. An alternate method provides open loop, frequency correcting bias to the oscillator. The bias value is determined by absolute temperature. In this fashion, the oscillator's thermal drift, which is repeatable, is corrected. The simplest way to do this is by slightly varying the crystal's resonance point with a variable shunt or series impedance. Varactor diodes, the capacitance of which varies with reverse voltage, are commonly employed for this purpose. Unfortunately, these diodes require volts of reverse bias to generate significant capacitance shift, making direct 1.5V powered operation impossible.

Figure 9's circuit accomplishes the temperature compensation function. The transistor and associated components form a Colpitts class oscillator which runs directly from the 1.5V supply. The varactor diode, in series with the crystal, tunes oscillator frequency as its DC bias varies. An ambient temperature dependent DC bias is generated by the remaining circuitry.

The thermistor network and the LM10 amplifier are arranged to produce a temperature dependent signal which corrects the thermal drift of the crystal type specified. Normally, the 1.5V powered LM10 could not provide the output levels required to bias the varactor. Here, however, a self-exciting switching up-converter (T1 and associated components) is included in the LM10's feedback loop. The LM10 drives the switching converter's input to generate whatever output voltage is required to close the loop. The thermistor-bridge network and amplifier feedback resistor values are scaled to produce appropriate temperature dependent varactor bias. The LM10's reference portion stabilizes the temperature network against 1.5V supply variations. The 100pF positive feedback forces the LM10's output into switched mode operation, conserving power.

Figure 10 plots compensated versus uncompensated oscillator drift. The compensation improves drift performance by more than a factor of ten. The residual aberrance in the compensated curve is due to the first-order linear correction used. Current consumption is inside $850\mu\text{A}$.

Voltage Boosted Output Amplifier

In many circumstances, it is desirable to have 1.5V powered circuitry interface to higher voltage systems. The most obvious example is 1.5V driven, remote data acquisition apparatus which feeds a line-powered data gathering point. Although the battery powered portion may locally process signals with 1.5V circuitry, it is useful to address the monitoring high level instrumentation at high voltage.

Figure 11's design borrows from the method used in Figure 9 to generate high voltage outputs. This 1.5V powered amplifier provides 0-10V outputs at up to $75\mu\text{A}$ capacity. The LM10 drives the self-exciting up-converter with whatever energy is required to close the feedback loop. In this case, the amplifier is set-up with a gain of 101, although other gains are easily realized. The sole restriction is that

Application Note 15

the 1.5V powered LM10's common-mode input range not be exceeded. The Schottky diode bypasses the up-converter for low voltage outputs, aiding output noise performance. Overlap between the up-converters turn-on threshold and the diode forward breakdown ensures clean

dynamic behavior at the transition point. To increase efficiency the $0.033\mu\text{F}$ capacitor provides AC positive feedback, forcing the LM10 output to pulse-width modulate the up-converter.

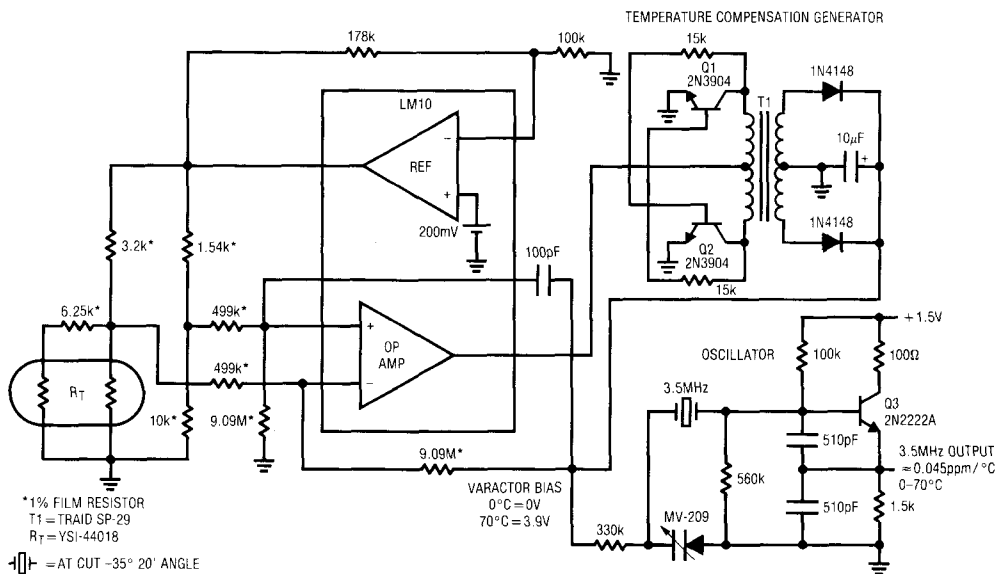


Figure 9. Temperature Compensated Crystal Oscillator

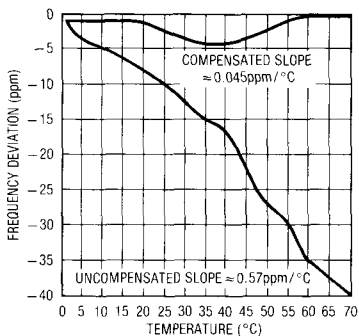


Figure 10. Compensated vs Uncompensated Oscillator Results

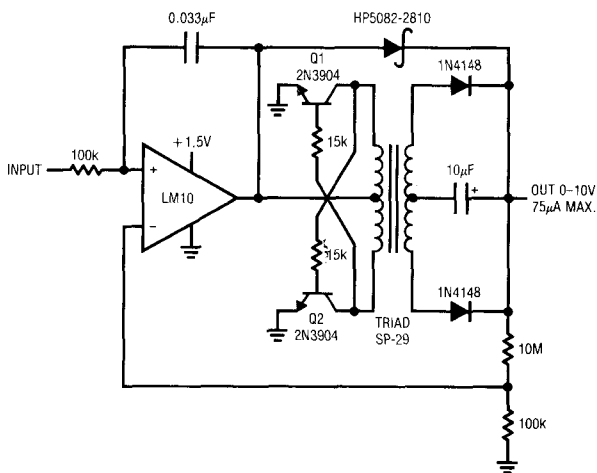


Figure 11. Voltage Boosted Output Op-Amp

Figure 12 details operation. The circuit's output (Trace A) decays until the LM10 switches (Trace B), starting the up-converter. The two transistors alternately drive the transformer (transistor collectors are Traces C and D) until the output voltage rises high enough to shut-off the LM10 output. This sequence repeats, with repetition rate dependent upon output voltage and loading conditions.

5V Output Switching Regulator

No commercially available logic, processor or memory family will operate from 1.5V. Many of the circuits described previously normally work in logic driven systems. Because of this, a way to permit use of standard logic functions from a 1.5V battery is necessary. The simplest

way to do this is a switching regulator specifically designed for 1.5V input operation. Figure 13's flyback configuration, a variant of a design by R. J. Widlar, gives a 5V output. C1A serves as an oscillator, providing a ramp (Trace A, Figure 14) at C1B's DC biased negative input. C1B compares a divided version of the output to a reference point derived from the LT1034. The ramp signal, summed with the reference point, causes C1B's output to width modulate (Trace B). During the time C1B is low, current builds in its output inductor (Trace C). When the ramp at C1B goes low enough, C1B's output goes high, and the inductor discharges into the 47 μ F capacitor. The diode from C1A's output to C1B's positive input supplies a pulse (Trace D) on each oscillator cycle, ensuring loop start up.

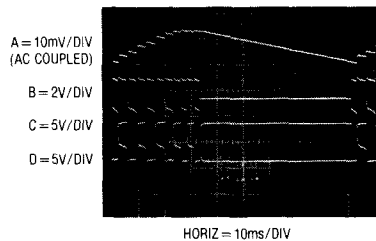


Figure 12. Boosted Op-Amp Waveforms

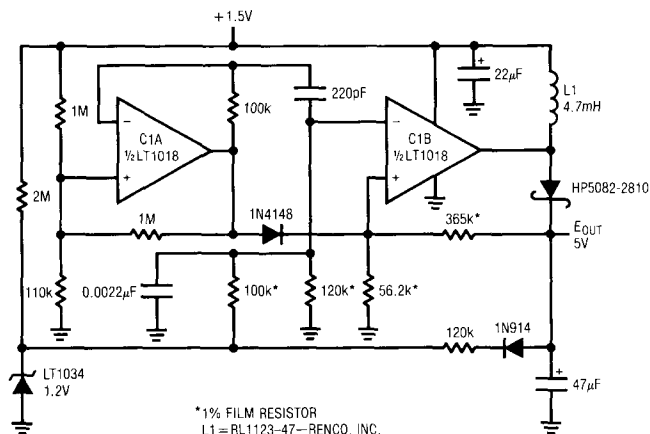


Figure 13. Flyback Regulator

Application Note 15

The 120kΩ diode path from the output bootstraps LT1034 bias, aiding overall regulation.

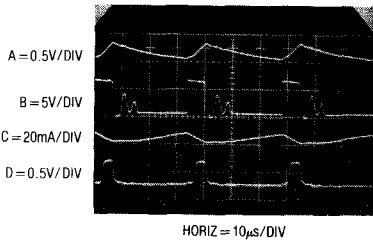


Figure 14. Flyback Regulator Waveforms

Figure 15 plots regulator efficiency. Small loads produce lowest efficiency because of fixed losses in the regulator, although 80% efficiency is achieved above 1500μA.

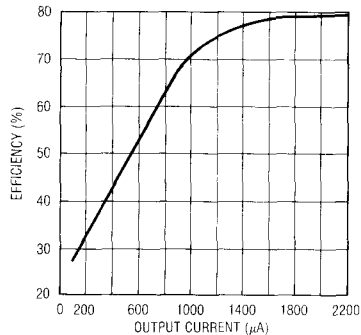


Figure 15. Flyback Regulator Efficiency

Components for 1.5V Operation

Almost all commercially available linear ICs are not capable of 1.5V operation. Two that are capable include the LM10 and LT1017/LT1018. The LM10 op amp-reference runs as low as 1.1V; the LT1017/LT1018 comparator goes down to 1.2V. The LM10 provides good DC input characteristics, although speed is limited to 0.1V/μs. The LT1017/LT1018 comparator series features microsecond range response time, high gain and good DC characteristics. Both devices feature low power consumption. The LT1004 and LT1034 voltage references feature 20μA operating currents and 1.2V operation.

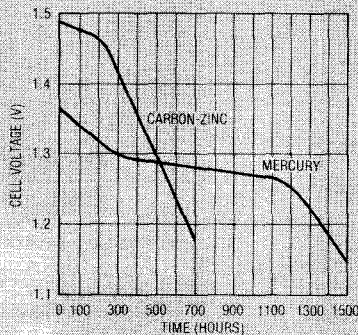
Standard PN junction diodes have a 600mV drop, a substantial percentage of available supply range. At currents below 10–20μA, this figure reduces to about 450mV. Schottky diodes typically exhibit only 300mV drop, although reverse leakage is higher than standard diodes. Germanium diodes are lowest, with 150–200mV drop, even at relatively high currents. Often, though, the significant reverse leakage of Germanium precludes its use.

Standard silicon transistors have a 600mV V_{BE} , although this figure comes down somewhat at very low base currents. The V_{CE} saturation of silicon transistors is well below 100mV at reasonable currents, and judicious device selection and use can reduce this figure below 25mV. Inverted mode operation allows V_{CE} saturation losses below

1mV, although beta is often below 0.1, necessitating substantial base drive. Germanium transistors have 2–3 times lower V_{BE} and V_{CE} losses, although speed, leakage and beta are generally not as good as silicon types.

Perhaps the most important component is the battery. Many types of cells are available, and the best choice varies with the application. Two common types are Carbon-Zinc and Mercury. Carbon-Zinc offers higher initial voltage, but Mercury units have a much flatter discharge curve (e.g., better supply regulation) if currents are controlled (see figure).

Typical Discharge Curves of Similar Size (AA) Mercury and Carbon Zinc Cells (1mA Load)



Unique IC Buffer Enhances Op Amp Designs, Tames Fast Amplifiers

Robert J. Widlar

abstract: *A unity gain IC power buffer that uses NPN output transistors while avoiding the usual problems of quasi-complementary designs is described. Free of parasitic oscillations and stable with large capacitive loads, the buffer has a 20MHz bandwidth, a 100V/ μ s slew and can drive $\pm 10V$ into a 75 Ω load. Standby current is 5mA. A number of applications using the buffer are detailed, and it is shown that a buffer has many uses beyond driving a heavy load.*

introduction

An output buffer can do much more than increase the output swing of an op amp. It can also eliminate ringing with large capacitive loads. Fast buffers can improve the performance of high speed followers, integrators and sample/hold circuits, while at the same time making them much easier to work with.

Interest in buffers has been low because a reasonably priced, high-performance, general purpose part has not been available. Ideally, a buffer should be fast, have no crossover distortion and drive a lot of current with large output swing. At the same time, the buffer should not eat much power, drive all capacitive loads without stability problems and cost about the same as the op amps it is used with. Naturally, current limiting and thermal overload protection would be nice.

These goals have been a dream for twenty years; but thanks to some new IC design techniques, they have finally been reached. A truly general purpose buffer has been made that is faster than most op amps but not hard to use in slow applications. It is manufactured using standard bipolar processing, and die size is 50 \times 82 mils.

The electrical characteristics of the buffer are summarized in table I. Offset voltage and bias current win no

medals; but the buffer will usually be driven from an op amp output and put within the feedback loop, virtually eliminating these terms as errors. Loaded voltage gain is mostly determined by the output resistance. Again, any error is much reduced with the buffer inside a feedback loop.

Unloaded, the output swings within a volt of the positive supply and almost to the negative rail. With $\pm 150mA$ loading, this saturation voltage increases by 2.2V. Except for output voltage swing, performance is little affected for a total supply voltage between 4V and 40V. This means that it can be powered by a single 5V logic supply or $\pm 20V$ op amp supplies.

Bandwidth and slew rate decrease somewhat with reduced load resistance. The values given in table I are for a 100 Ω in parallel with 100pF. The speed is quite impressive considering that quiescent current is but 5mA.

table I. Typical performance of the buffer at 25°C. Supply voltage range is 4V to 40V.

parameter	value
output offset voltage	70mV
input bias current	75 μ A
voltage gain	0.999
output resistance	7 Ω
positive saturation voltage	0.9V
negative saturation voltage	0.1V
output saturation resistance	15 Ω
peak output current	$\pm 300mA$
bandwidth	22MHz
slew rate	100V/ μ s
supply current	5mA

Application Note 16

design concept

The functional schematic in figure 1 describes the basic elements of the buffer design. The op amp drives the output sink transistor, Q30, such that the collector current of the output follower, Q29, never drops below the quiescent value (determined by I_1 and the area ratio of Q12 and Q28). As a result, the high frequency response is essentially that of a simple follower even when Q30 is supplying the load current. The internal feedback loop is isolated from the effects of capacitive loading by a small resistor in the output lead.

The scheme is not perfect in that the rate of rise of sink current is noticeably less than for source current. This can be mitigated by connecting a resistor between the bias terminal and V^+ , raising quiescent current. A feature of the final design is that the output resistance is largely independent of the follower current, giving low output resistance at low quiescent current. The output will swing to the negative rail, which is particularly useful with single-supply operation.

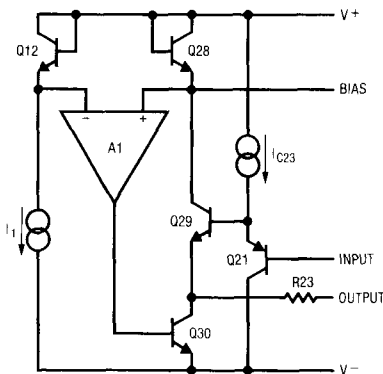


figure 1. In the buffer, main signal path is through followers Q21 and Q29. Op amp keeps Q29 turned on even when Q30 is supplying load current, so response is that of followers.

basic design

Figure 2 shows the essential details of the buffer design using the concept in figure 1 (for clarity, parts common to simplified and developed schematics use the same number). The op amp uses a common base pnp pair, Q10 and Q11, degenerated with R6 and R7 for an input stage. The differential output is converted to single-ended by a current mirror, Q13 and Q14; and this drives the output sink transistor, Q30, through a follower, Q19.

A clamp, Q15, is included to insure that the output sink transistor does not turn off completely. Its biasing circuitry, Q6 through Q9, is arranged such that the emitter current of Q15 is about equal to the base current of Q19 with no output load.

The control loop is stabilized with a feedforward capacitor, C1. Above 2MHz, feedback is predominantly through the capacitor. The break frequency is determined by C1 and R7 plus the emitter resistance of Q11. The loop is made stable for capacitive and resonant loading by R23, which limits the phase lag that can be induced at the emitter of Q29.

A resistor, R10, has been added to improve the negative slew response. With a large negative transient, Q29 will cut off. When this happens, R10 pulls stored charge from Q28 and provides enough voltage swing to get Q30 from its clamp level into conduction.

Start-up biasing is done with a collector FET, Q4. Once in operation, the collector current of Q6 is added to the drain current of Q4 to bias Q5. These currents plus the current through Q9 and Q10 flow through Q12 to set the output quiescent current (along with R10).

follower boost

The boost circuit in figure 3 reduces the buffer standby current by at least a factor of three while improving performance. It does this by increasing the effective current gain of Q29 so that the current source current, I_{C23} , can be drastically cut. Secondly, it can give under 0.5Ω follower output resistance at less than 3mA bias, something that normally takes over 40mA. Hard as it may be to believe, the boost does not degrade the high frequency response of the final design.

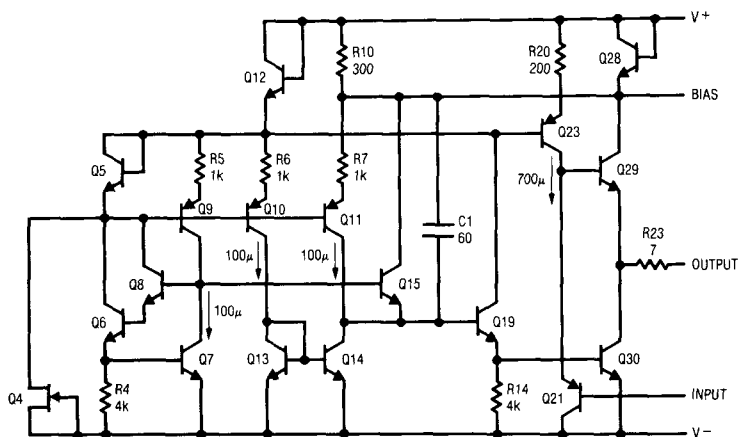


figure 2. Implementation of the buffer in figure 1. Simple op amp uses common base pnp input transistors (Q10 and Q11). Control loop is stabilized with feedforward capacitor (C1); and clamp (Q15) keeps Q30 from turning off entirely.

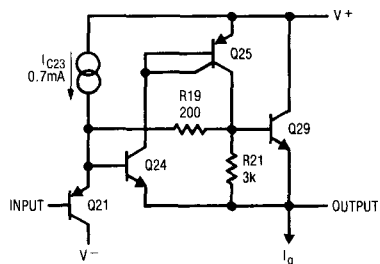


figure 3. This boost circuit raises effective current gain and transconductance of the output transistor, giving low standby current along with low output resistance.

If R19 is removed (opened), circuit operation becomes clearer. Output resistance is determined by Q24, with Q25 and Q29 providing current gain. If the current through R21 is larger than the base current of Q29, output resistance is proportionately reduced. Without R21, output resistance depends on Q29 bias, like a simple follower.

The purpose of R19 is to provide a direct ac path at high frequencies and kill *unnneeded* gain in the boost feedback loop. If R21 is properly selected, voltage change across R19 with loading is less than 40mV, so a small value causes no problems (increasing load does cause Q21 bias current to increase). The quiescent drop across R19 is set by sizing Q24, Q25 and Q29 geometries.

charge storage pnp

At high frequencies, a lateral pnp looks like a low impedance between the base and emitter because charge stored between the emitter and subcollector (the pnp base) has a capacitive effect. The input pnp, Q21, has been designed to have *more than 30 times* the stored charge of a standard lateral for a given emitter current. This stored charge couples in the input to slow internal stray capacitances and drive the output follower while the boost circuitry is coming into action.

Stored charge can be maximized in a lateral pnp by using large emitter area and wide base spacing. Dimensions of several mils are practical; diffusion lengths are in the order of 6 mils with good processing.

Application Note 16

A sketch of a charge storage pnp is shown in figure 4. With the dimensions shown, current gains of 10 can be obtained regularly. A sinker base contact is shown here because a low resistance from the base terminal to the area under the emitter is important.

The charge stored *under* the emitter is most effective in obtaining a fast charge transfer from base to emitter with minimum change of emitter base voltage. Using the notation in figure 4, this charge varies as

$$Q_E \propto \frac{WB_{AE}}{S_E}$$

$$\propto (X_C - X_E)X_E,$$

where S_E is the emitter periphery. With X_C fixed, it can be shown that Q_E is maximized for $X_E = 0.5X_C$.

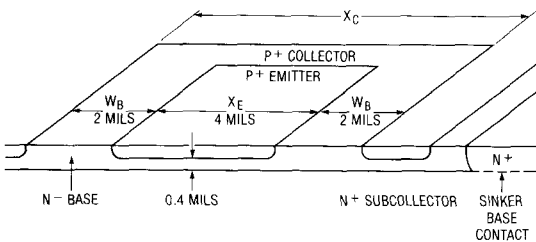


figure 4. Charge storage pnp is lateral structure with base and emitter dimensions of several mils. As above, current gains of 10 are practical.

isolation-base transistor

Transistors can be made by substituting an isolation diffusion for the normal base diffusion. Figure 5 shows the impurity profile of such a transistor. Base doping under the emitter is three orders of magnitude higher than standard transistors, and the base extends all the way to the subcollector. The measured current gains of 0.1 are not lower than might be expected.

The emitter-base voltage of an isolation-base transistor is about 120mV greater than a standard IC transistor when operating at the same emitter current. Production variations in V_{BE} are much less than standard npns, probably because net base doping is little affected by anything but the isolation doping.

As will be seen on the complete schematic, the isolation-base transistor is used as a bias diode for current sources because of its high V_{BE} . One (Q28) is also used in the collector of the output follower because the behavior at very high current densities is much better than a standard transistor.

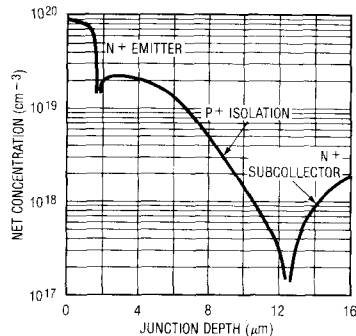


figure 5. Impurity profile of isolation-base transistor. In contrast, typical standard npn has peak base concentration of $5 \times 10^{16} \text{cm}^{-3}$ and base width of $1 \mu\text{m}$.

complete circuit

A complete schematic of the LT1010 buffer is given in figure 6. Component identification corresponds to the simplified schematics. All details discussed thus far have been integrated into the diagram.

Current limiting for the output follower is provided by Q22 and Q31, which serve to clamp the voltage into the follower boost circuitry when the voltage across R22 equals a diode drop.

Negative current limit is less conventional because putting a sense resistor in the emitter of Q30 will seriously degrade negative slew under load. Instead, the sense resistor, R17, is in the collector. When the drop across it turns on Q27, this transistor supplies current directly to the sink current control amplifier, limiting sink current.

Should the output terminal rise above V^+ because of some fault condition, Q27 can saturate, breaking the current limit loop. Should this happen, Q26 (a lateral collector near Q27 base) takes over to control current by removing sink drive through Q16. This reserve current limit oscillates, but in a controlled fashion.

Clamp diodes, from the output to each supply, should be used if the output can be driven beyond the supplies by a high-current source. Unlike most ICs, the LT1010 is designed so that ordinary junction diodes are effective even when the IC is much hotter than the external diodes.

Current limit is backed up by thermal overload protection. The thermal sensor is Q1, with its base biased near 400mV. When Q1 gets hot enough to pull base drive off Q2 (about 160°C), the collector of Q2 will rise, turning on Q16 and Q20. These two transistors then shut down the buffer. Including R2 generates hysteresis to control the frequency of thermal limit oscillation.

Base drive to Q20 is limited by R15, a pinched base resistor. The value of this resistor varies as transistor h_{FE} over temperature and in production, controlling the turn off current near 2mA. An emitter into the isolation wall capacitor, C2, keeps Q20 from turning on with fast signals on its collector.

In current limit or thermal limit, excessive input-output voltage might damage internal circuitry. To avoid this, back-to-back isolation zeners, Q32 and Q33, clamp the input to the output. They are effective as long as the input current is limited to about 40mA.

Other details include the negative saturation clamp, Q17 and Q18. This clamp allows the output to saturate within 100mV of the negative supply rail without increasing supply current while recovering cleanly from saturation. The base of Q17 is connected internally into Q30 to sense voltage on the internal collector side of the saturation resistance to insure optimum operation at high currents.

When sinking large currents, the base of Q19 loads the control amplifier. This unbalances the control loop and reduces the output follower bias current. To compensate for this, the base current of Q30 is routed to the bias diode, Q12, through Q19. A small resistor, R19, aids compensation. This action raises the bias to Q23 and is responsible for increasing the input pnp bias current with sink current.

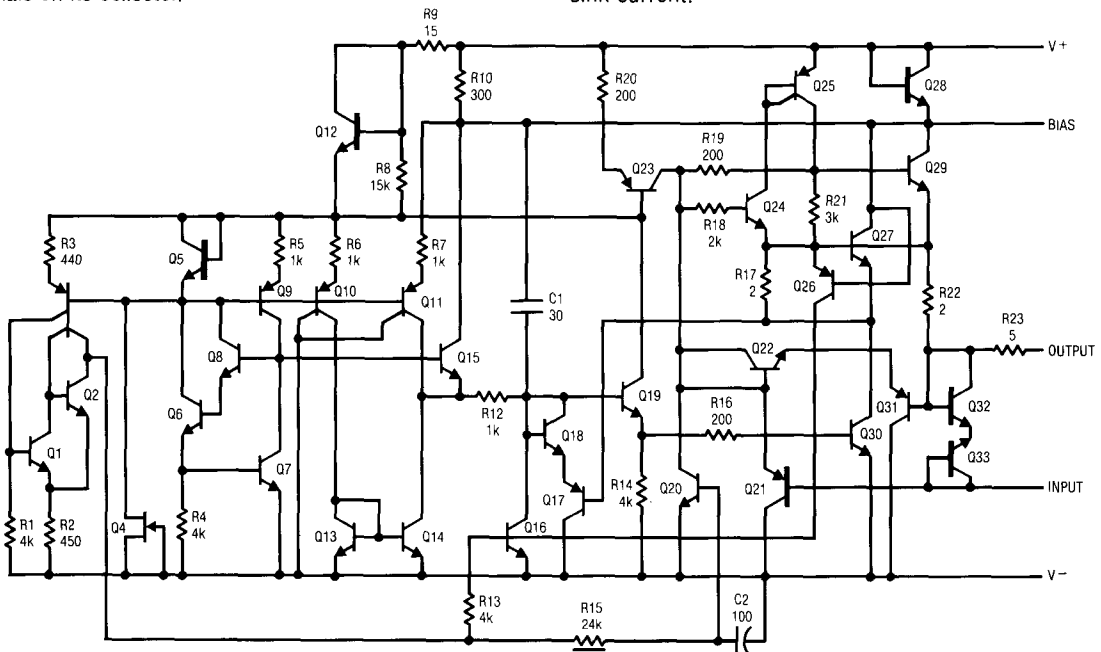


figure 6. Complete schematic of the LT1010 buffer. Component identification corresponds to simplified schematics. The isolation-base transistors are drawn with heavy base, as is the charge storage pnp. Follower drive boost has been included along with negative saturation clamp (Q17 and Q18) and protection circuitry.

Application Note 16

Final details of the design are that the collectors of Q10 and Q11 are segmented so that only a fraction of the emitter current is sent to the current mirror, with the rest dumped to V^- . This allows the transistors to be operated

at their f_T peak without requiring large C1. Lastly, R8 has been included to shape the temperature characteristics of output stage quiescent current.

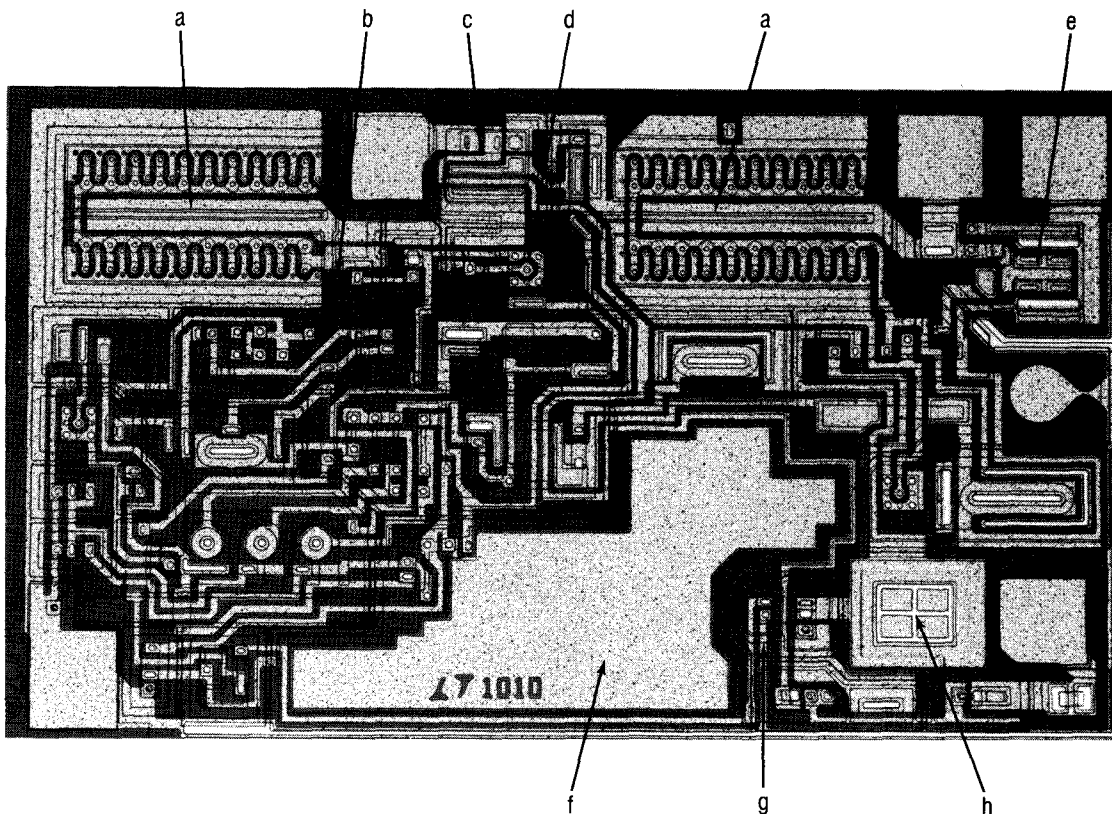


figure 7. Photomicrograph of the LT1010. Die size is 50 × 82 mils.

A photomicrograph of the LT1010 die is shown in figure 7. The features pointed out are identified below.

- a) Output transistors were designed to maximize high frequency performance, while obtaining some ballasting.
- b) Clamp pnp base (Q17) is connected by subcollector stripe to region furthest from Q30 collector contact to isolate saturation resistance.
- c) Output resistors are in floating tub so that IC tubs are not forward biased when junction diodes clamp output below V^- .
- d) A high f_T , 0.3 mil stripe, cross geometry is used for the sink transistor driver (Q19).
- e) Isolation-base transistor (Q28) carries the same 500mA peak current as the output transistor but is much smaller.
- f) MOS capacitor (C1) takes up considerable area.
- g) Capacitance formed by diffusing emitter into isolation wall takes advantage of unused area.
- h) Charge storage pnp.

buffer performance

Table I in the introduction summarizes the typical specifications of the LT1010 buffer. The IC is supplied in three standard power packages: the solid kovar base TO-5 (TO-39), the steel TO-3, and the plastic TO-220. The bias terminal is not available in the TO-39 package because it has only four leads, compared to five for the other packages.

The thermal resistance for one output transistor, excluding the package, is $20^{\circ}\text{C}/\text{W}$ because it was kept as small as possible to enhance speed. This explains the junction-to-case thermal resistance of $40^{\circ}\text{C}/\text{W}$ for the TO-39 package and $25^{\circ}\text{C}/\text{W}$ for the TO-3 and TO-220, again for one transistor. With ac loads, both transistors will be conducting; if the frequency is high enough, thermal resistance is reduced by $10^{\circ}\text{C}/\text{W}$.

The operating case temperature range for the LT1010 is -55°C to 125°C . The maximum junction temperature for the internal power transistors is 150°C . A commercial version, the LT1010C, is also available. It rated for 0°C to 100°C case temperature with a maximum junction temperature of 125°C .

The following curves describe the buffer performance in some detail. The fact that quiescent current boost (5mA–40mA) is not available on the TO-39 package should be noted.

bandwidth

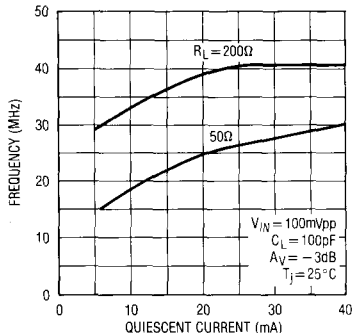


figure 8. The dependence of small signal bandwidth on load resistance and quiescent current boost is shown here. The 100pF capacitive load that is specified limits the bandwidth that can be obtained with boost and light loads.

phase delay

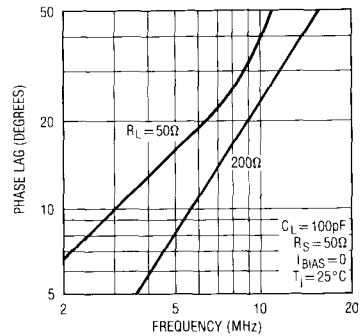


figure 9. The phase delay gives more useful information about high frequency performance than bandwidth. This is a plot of phase delay as a function of frequency with 50Ω and 100Ω loads. Capacitive loading is 100pF, and quiescent current is not boosted.

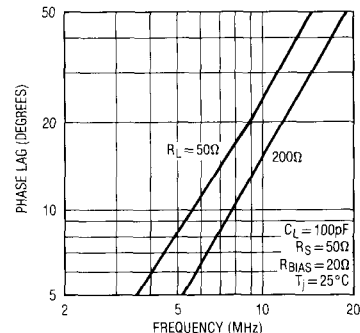


figure 10. This shows reduction in phase lag with quiescent current boosted to 40mA ($R_{BIAS} = 20\Omega$).

Application Note 16

step response

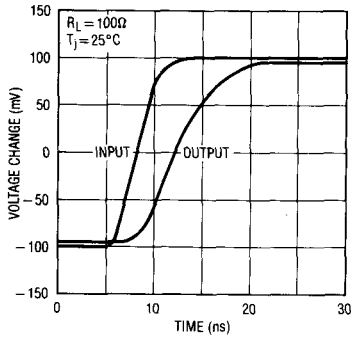


figure 11. The small signal step response with 100Ω load shows a 2ns output delay. This gives an excess phase delay of 15° at 20MHz, explaining why the -3dB bandwidth is greater than the frequency for 45° phase delay.

capacitive loading

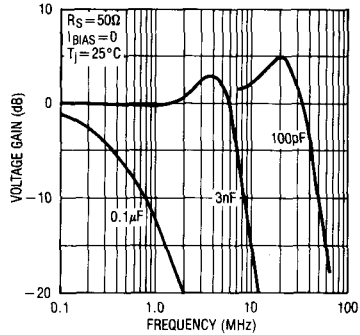


figure 13. These frequency response plots, with capacitive load only, show that nothing unusual happens as load capacitance is varied over a wide range. Minor peaking is reduced with quiescent current boost.

output impedance

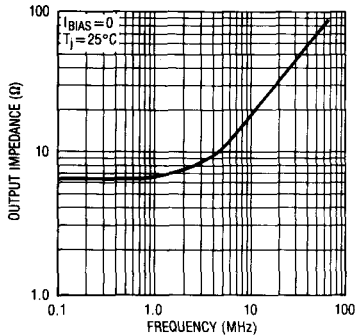


figure 12. The unloaded small signal output impedance stays down to 1MHz, indicating the frequency limit of the follower boost circuitry.

slew response

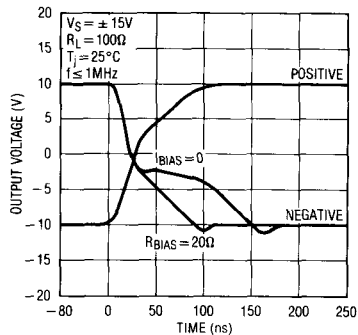


figure 14. The negative slew delay is reduced by using quiescent current boost (40mA). Positive slew is not affected by boost.

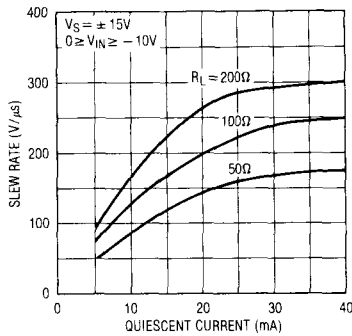


figure 15. The worst-case slew response, going from 0V to $-10V$, is plotted here. It is clear that substantial improvement can be made with quiescent current boost.

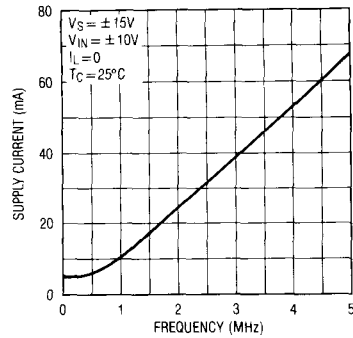


figure 17. The no load supply current increases above 1MHz under large signal conditions. This is a quiescent current boost caused by charging of internal capacitances. It does give very good power bandwidth even with load, although the excess dissipation may cause the IC to go into power limit.

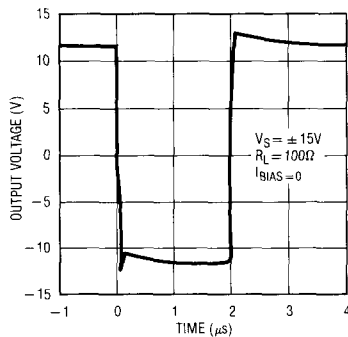


figure 16. This 500ns slew residue is caused by recovery of the follower boost circuitry. For positive outputs, the boost circuit is hit hard by the input through the charge storage pnp. For negative outputs, it is hit by the leading edge overshoot on the output. Recovery is from a positive boost overshoot in both cases.

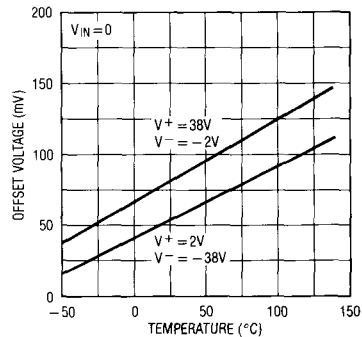


figure 18. The offset voltage is determined by matching between the output follower and the input pnp. The charge storage pnp on the input is run at high injection levels to maximize stored charge. Therefore, the high offset voltage drift shown here is no surprise. The offset voltage change with supply voltage shown in the figure is mostly positive supply sensitivity. Changing the negative supply by 35V shifts offset by 5mV.

Application Note 16

input bias current

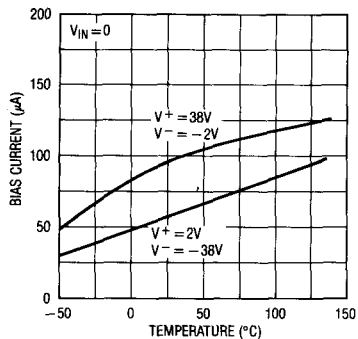


figure 19. The increase in bias current with temperature reflects the current gain characteristics of the charge storage pnp. Sensitivity of bias current to supply voltage is about three times greater on positive supply.

voltage gain

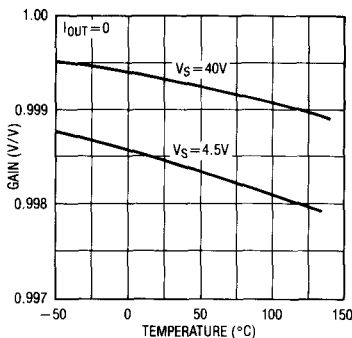


figure 21. The unloaded voltage gain is high enough to be ignored in most any application. In practice, gain will be determined by the load working against the output resistance.

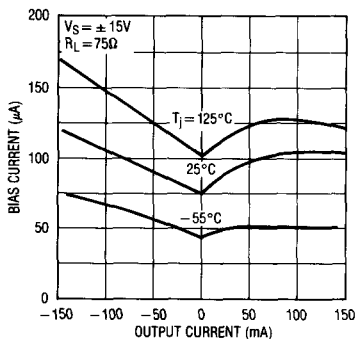


figure 20. The change in input bias current with load current is not excessive, but it shows that the follower is not designed for working with high source resistances. For positive output current, increase is caused by follower boost. For negative output, it results from sink transistor base current increasing bias to the input pnp current source.

output resistance

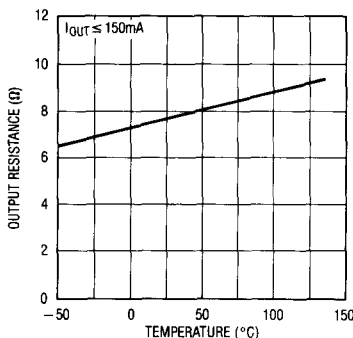


figure 22. The output resistance is essentially independent of dc output loading. The temperature sensitivity is shown here.

output noise voltage

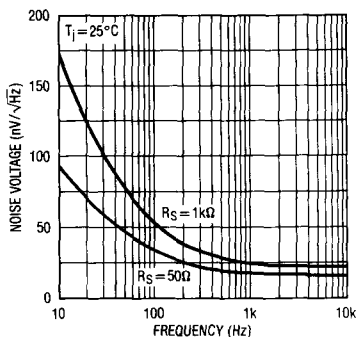


figure 23. The noise performance of a buffer is of small concern unless it is grossly bad. This plot shows that the buffer noise is low by comparison to the excess output noise of op amps.

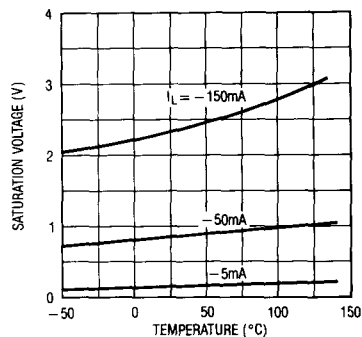


figure 25. This curve gives the negative saturation voltage. Unloaded saturation voltage is $<0.1\text{V}$, again increasing linearly with current. The saturation characteristics are negligibly affected by supply voltage and are used to determine output swing under load.

saturation voltage

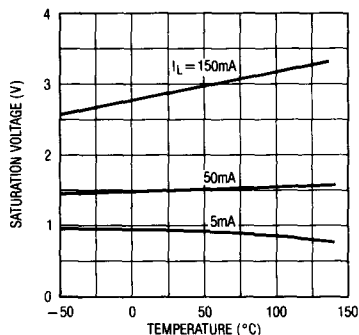


figure 24. The positive saturation voltage (referred to the positive supply) is plotted here as a function of temperature. Unloaded saturation voltage is 0.9V , with the saturation voltage increasing linearly with current to 150mA .

supply current

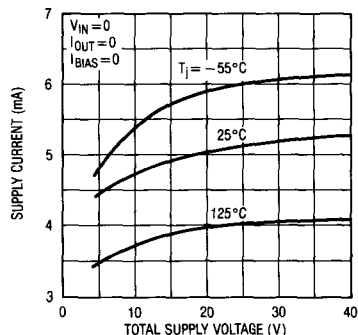


figure 26. Supply current is not greatly affected by supply voltage, as shown in this expanded-scale plot. This accounts for the 4V to 40V supply range with unchanged specifications.

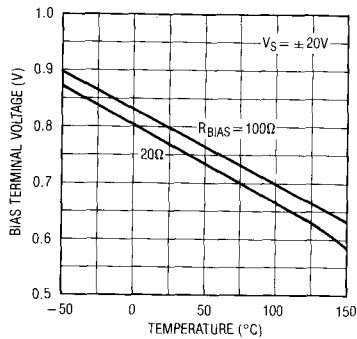


figure 27. The quiescent current boost is determined by the bias terminal voltage across an external resistor. This expanded-scale plot shows the change in bias terminal voltage with temperature. The voltage increases less than 20mV as the total supply voltage is raised from 4.5V to 40V.

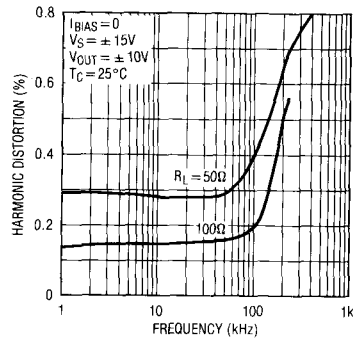


figure 29. Distortion is low to 100kHz, even without quiescent current boost. The influence of load resistance is indicated here.

total harmonic distortion

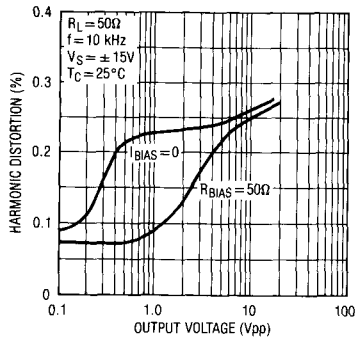


figure 28. The buffer distortion is not high, even when it is outside a feedback loop, as shown here. The reduced-distortion curve is for 20mA supply current.

maximum power

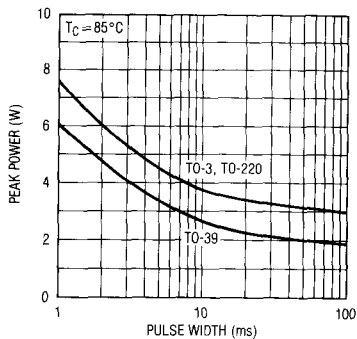


figure 30. These curves indicate the peak power capability of one output transistor for $T_C = 85^\circ\text{C}$. With ac loading, power is divided between the two output transistors. This can reduce thermal resistance to $30^\circ\text{C}/\text{W}$ for the TO-39 and $15^\circ\text{C}/\text{W}$ for the TO-3, as long as the frequency is high enough that the peak rating of neither transistor is exceeded.

short circuit characteristics

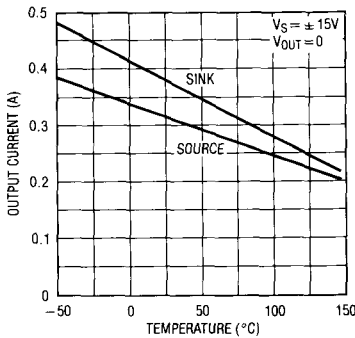


figure 31. The output short circuit current is plotted here as a function of temperature. Above 160°C it falls off sharply because of thermal limit. The peak output current is equal to the short circuit current; with capacitive loads greater than 1nF, current limiting can reduce slew rate.

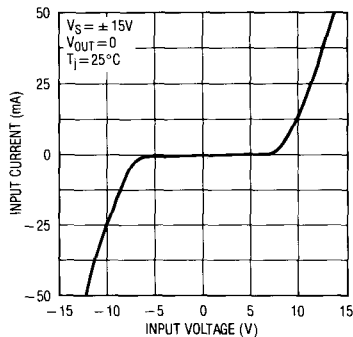


figure 32. The input characteristics, with the output shorted, are plotted here. The input is clamped to the output to protect internal circuitry. Therefore, it is necessary to externally limit input current. The output-current limit of IC op amps is adequate protection.

isolating capacitive loads

The buffered follower in figure 33a shows the recommended method of isolating capacitive loads. At lower frequencies, the buffer is within the feedback loop so that offset voltage and gain errors are negligible. At higher frequencies (above 80kHz here) op amp feedback is through C1 so that phase shift from the load capacitance acting against the buffer output impedance does not cause instability.

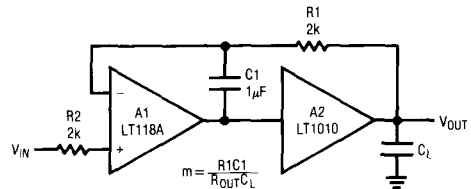
The initial step response is the same as if the buffer were outside the feedback loop; the gain error of the buffer is then corrected by the op amp with a time constant determined by R1C1. This is shown in figure 33b.

With small load capacitors, the bandwidth is determined by the slower of the two amplifiers. The op amp and the buffer in figure 33 give a bandwidth near 15MHz. This is reduced for capacitive loads greater than 1nF (determined by the output impedance of the buffer).

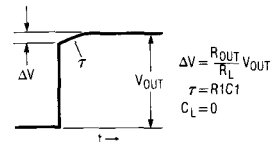
Feedback-loop stability with large capacitive loads is determined by the ratio of the feedback time constant (R1C1) to that of the buffer output resistance and load capacitance (R_{OUT}C_L). A stability factor, m, can be expressed as

$$m = \frac{R1C1}{R_{OUT}C_L}$$

where R_{OUT} is the buffer output resistance.



a. connection diagram



b. step response

figure 33. Capacitive loading on this buffered follower reduces bandwidth without causing ringing. Step response with no capacitive load has residue as shown here.

Application Note 16

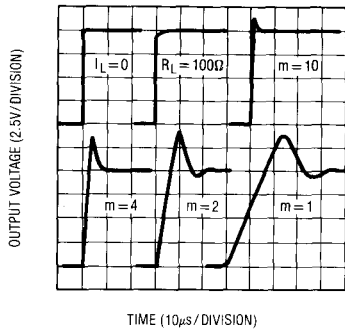


figure 34. Large signal step response ($\pm 5V$) of the buffered follower in figure 33 for indicated loads.

The measured large signal step response for the circuit in figure 33a is given in figure 34 for various loads. For $m \geq 4$ ($C_L \leq 0.068\mu F$) there is overshoot but no ringing. For $m < 1$ ($C_L > 0.33\mu F$) ringing becomes pronounced.

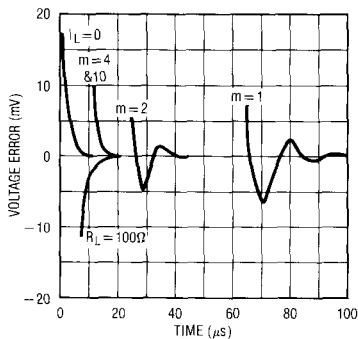


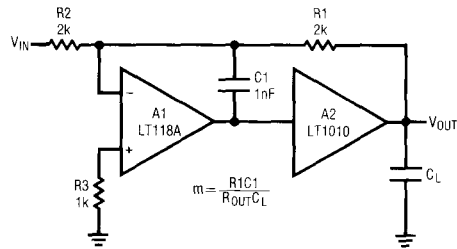
figure 35. Measured settling for output steps in figure 34. For capacitive loads less than $0.068\mu F$ ($m = 4$) settling is based on a $2\mu s$ time constant.

The settling time constant is determined by $R1C1$ for $m \geq 4$. Without capacitive loading, the initial error on the output step is smaller, so time to settle is less. The settling characteristics are shown in figure 35.

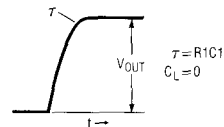
With $R1C1$ as shown in figure 33, any op amp with a bandwidth greater than $200kHz$ will give the same results on stability. Settling time, however, will be dominated by the slew rate limitations of slow op amps.

Certain op amps, like the LM118, have back-to-back protection diodes across the input terminals. With input rise times in excess of the op amp slew rate, $C1$ can be charged through these diodes, increasing settling time. Including $R2$ in series with the input takes care of the problem. Good supply bypass ($22\mu F$ solid tantalum) should be used because high peak currents are required to drive load capacitors and supply transients can feed into the op amp, increasing settling time.

The same load isolation technique is shown applied to an inverting amplifier in figure 36. The response differs in that the output rise time and bandwidth are limited by $R1C1$. This does reduce overshoot for $m \geq 4$, as shown in figure 37. For $m < 4$, response approaches that of the follower.



a. connection diagram



b. step response

figure 36. With an inverter, bandwidth and rise time are limited by $R1C_L$. For $m \geq 4$, capacitive loading has little effect on bandwidth.

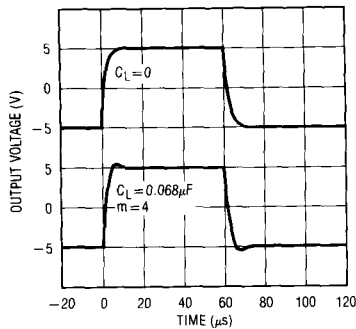
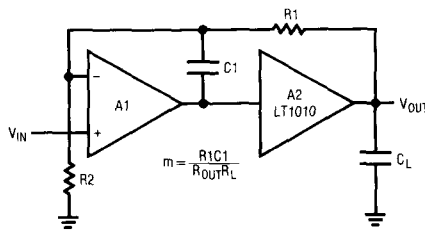


figure 37. Large signal pulse response of the inverter in figure 36.

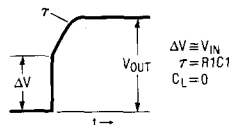
Although the small signal bandwidth is reduced by C_1 , considerable isolation can be obtained without reducing it below the power bandwidth. Often, bandwidth reduction is desirable to filter high frequency noise or unwanted signals.

An alternate method of isolating capacitive loads is to buffer an inverter output with the follower shown in figure 33.

Capacitive load isolation for non-inverting amplifiers is shown in figure 38, along with the step response for small C_L . Rise time of the initial step is reduced with increasing C_L , and response approaches that of the inverter.



a. connection diagram



b. step response

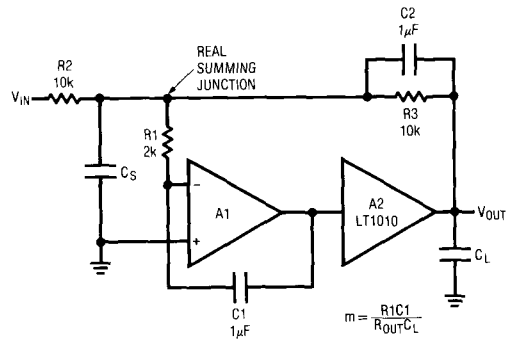
figure 38. With non-inverting amplifier, rise time of initial step decreases with increasing C_L . Stability requirements are the same as for follower and inverter.

integrators

A low pass amplifier can be formed just by using large C_1 with the inverter in figure 36, as long as the op amp is capable of supplying the required current to the summing junction and the increase in closed loop output impedance above the cutoff frequency is not a problem (it will never rise above the buffer output impedance).

If the integrating capacitor must be driven from the buffer output, the circuit in figure 39 can be used to provide capacitive load isolation. The method does introduce errors, as is shown in the figure.

The op amp does not respond instantly to an input step, and the input current is supplied by the buffer output. The resulting change in buffer output voltage is seen at the real summing junction and is corrected at an R_1C_1 time constant. As the output ramps, the voltage change across C_1 generates a current through R_1 , shifting the real summing junction off ground.

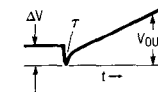


a. connection diagram

$$\Delta V = \left(\frac{R_1 C_1}{R_2 C_2} + \frac{R_{OUT}}{R_{IN}} \right) \Delta V_{IN}$$

$$\tau = R_1 C_1$$

$$C_L = 0$$



b. step response

figure 39. Capacitive load isolation for a low pass or integrating amplifier when integrating capacitor must go to buffer output. Response given is for negative input step.

Application Note 16

Figure 40 shows the voltage on the real summing junction for an input square wave. Both error terms are apparent in the top curve. With $C_L = 0.33\mu\text{F}$, response is reasonable. This suggests that $m = 1$ be used as a stability criterion for this type of circuit if the shift of real summing node voltage with output ramp is a problem. A capacitor can be used on the real summing junction to absorb current transients and reduce spiking, as shown in the lower curve.

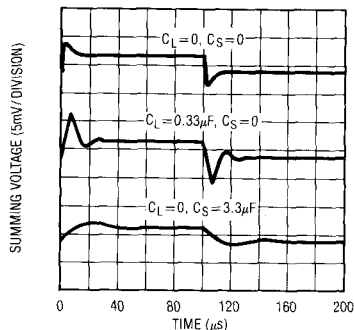


figure 40. Step response of the integrating amplifier in figure 39. The real summing junction voltage is shown for $\pm 0.5\text{mA}$ input change.

With large R_2 and $C_S = 0$, the output voltage of the integrator will be the response of an ideal integrator plus the voltage of the real summing junction. Large C_S will increase the high frequency loop gain so that this is no longer true.

impulse integrator

With certain sensors, like radiation detectors, the output is delivered in short, high-current bursts. Frequently, it is necessary to integrate these impulses to determine net charge. A complication with some solid-state sensors is that the peak voltage across them must be kept low to avoid error.

The circuit in figure 41 will integrate high current pulses while keeping the summing node under control. Although it increases noise gain, C_S is often required for stability and to absorb the leading edge of fast pulses. The buffer increases the peak current available to the summing node and improves stability by isolating C_f and C_S from the op amp output. Increased output drive capability is a bonus.

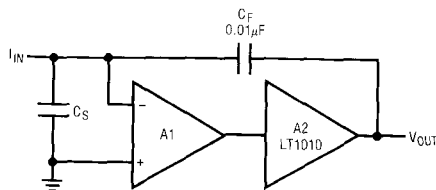


figure 41. Buffer increases current available to summing node. Input capacitor absorbs input impulses and raises loop gain.

The summing node response to a 100mA , 100ns input impulse is shown in figure 42 for three different cases. With $C_S = 0.33\mu\text{F}$, the LT118A will settle faster than the LF156 because of its higher gain-bandwidth product; but C_S cannot be made much smaller for $C_f = 0.01\mu\text{F}$. The LF156 works with $C_S = 0.02\mu\text{F}$ and settles even faster because it goes through unity gain at a frequency where the LT1010 is better able to handle $C_f = 0.01\mu\text{F}$ as a load capacitance. However, the smaller C_S does allow the summing node to get further off null during the input impulse.

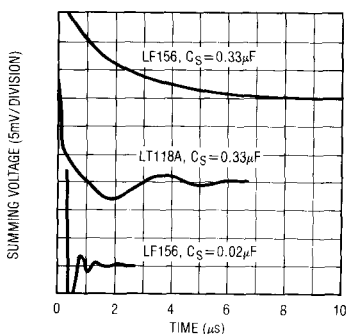


figure 42. Summing node voltage of impulse integrator in figure 41 with 100mA , 100ns input impulse and -10mA recovery.

parallel operation

Parallel operation provides reduced output impedance, more drive capability and increased frequency response under load. Any number of buffers can be directly paralleled as long as the increased dissipation in individual units caused by mismatches of output resistance and offset voltage is taken into account.

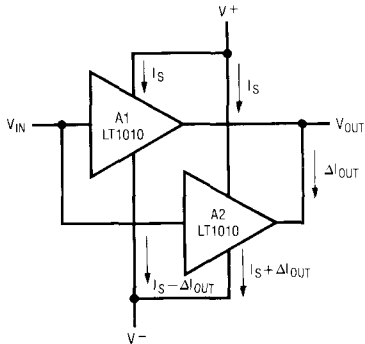


figure 43. When two buffers are paralleled, a current can flow between outputs, but total supply current is not greatly affected.

When the inputs and outputs of two buffers are connected together as shown in figure 43, a current, ΔI_{OUT} , flows between the outputs:

$$\Delta I_{OUT} = \frac{V_{OS1} - V_{OS2}}{R_{OUT1} + R_{OUT2}}$$

where V_{OS} and R_{OUT} are the offset voltage and output resistance of the respective buffers.

Normally, the negative supply current of one unit will increase and the other decrease, with the positive supply current staying the same. The worst-case ($V_{IN} \rightarrow V^+$) increase in standby dissipation can be assumed to be $\Delta I_{OUT} V_T$, where V_T is the total supply voltage.

Offset voltage is specified worst-case over a range of supply voltages, input voltage and temperature. It would be unrealistic to use these worst-case numbers above because paralleled units are operating under identical conditions. The offset voltage specified for $V_S = \pm 15V$, $V_{IN} = 0$ and $T_A = 25^\circ C$ will suffice for a worst-case condition.

Output load current will be divided based on the output resistance of the individual buffers. Therefore, the available output current will not quite be doubled unless output

resistances are matched. As for offset voltage above, the $25^\circ C$ limits should be used for worst-case calculations.

Parallel operation is not thermally unstable. Should one unit get hotter than its mates, its share of the output and its standby dissipation will decrease.

As a practical matter, parallel connection needs only some increased attention to heat sinking. In some applications, a few ohms equalization resistance in each output may be wise. Only the most demanding applications should require matching, and then just of output resistance at $25^\circ C$.

wideband amplifiers

Figure 44 shows the buffer inside the feedback loop of a wideband amplifier that is not unity gain stable. In this case, C1 is not used to isolate capacitive loads. Instead, it provides an optimum value of phase lead to correct for the buffer phase lag with a limited range of load capacitances.

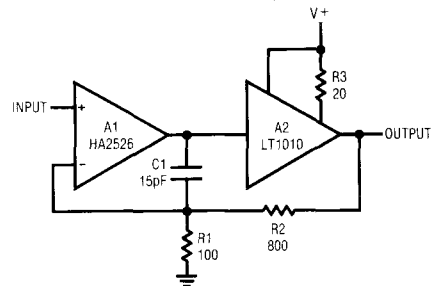


figure 44. Capacitive load isolation described earlier does not apply for amplifiers that are not unity gain stable. This 8MHz, $A_V = 9$ amplifier handles only 200pF load capacitance.

With the TO-3 and TO-220 packages, behavior can be improved by raising the quiescent current with a 20Ω resistor from the bias terminal to V^+ . Alternately, devices in the TO-39 package can be operated in parallel.

Putting the buffer outside the feedback loop, as shown in figure 45, will give capacitive load isolation, with large output capacitors only reducing bandwidth. Buffer offset, referred to the op amp input, is divided by the gain. If the load resistance is known, gain error is determined by the output resistance tolerance. Distortion is low.

Application Note 16

The 50Ω video line splitter in figure 46 puts feedback on one buffer, with others slaved. Offset and gain accuracy of slaves depends on their matching with master.

When driving long cables, including a resistor in series with the output should be considered. Although it reduces gain, it does isolate the feedback amplifier from the effects of unterminated lines which present a resonant load.

When working with wideband amplifiers, special attention should always be paid to supply bypassing, stray capacitance and keeping leads short. Direct grounding of test probes, rather than the usual ground clip lead, is absolutely necessary for reasonable results.

The LT1010 has slew limitations that are not obvious from standard specifications. Negative slew is subject to glitching, but this can be minimized with quiescent current boost. The appearance is always worse with fast rise signal generators than in practical applications.

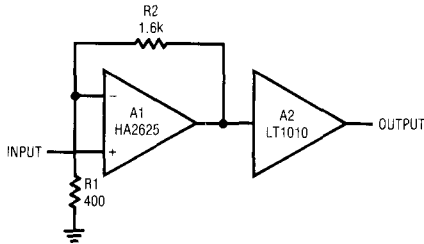


figure 45. Buffer outside feedback loop gives capacitive load isolation. Buffer offset is divided by amplifier gain, gain error is determined by output resistance tolerance and distortion is low.

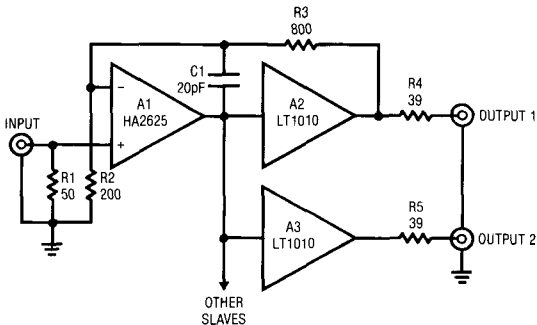


figure 46. This video line splitter has feedback on one buffer with others slaved. Offset and gain accuracy of slaves depends on matching with master.

track and hold

A 5MHz track and hold circuit is shown in figure 47. It has a power bandwidth of 400kHz with a $\pm 10V$ signal swing.

The buffered input-follower drives the hold capacitor, C4, through Q1, a low resistance ($< 5\Omega$) FET switch. The positive hold command is supplied by TTL logic with Q3 level shifting to the switch driver, Q2.

When the FET gate is driven to V^- for hold, it pulls charge that depends upon the input voltage and drain-gate capacitance out of the hold capacitor. A compensating charge is put into the hold capacitor through C3.

Below the FET pinch voltage, the gate capacitance increases sharply. Since the FET will always be pinched off in hold, the turn-off charge from this excess capacitance will be constant over the input voltage range.

Going into hold, the inverting amplifier, A4, makes the positive voltage step into C3 proportional to the negative step on the switch gate, plus a constant to account for the increased capacitance below pinch-off. The step into hold is made independent of the input level with R7 and adjusted to zero with R10 (initially setting up for $V_{IN} = \pm 5V$ avoids special problems at input voltage extremes). The circuit is brought into adjustment range for a particular design with an appropriate value for C3, although a couple hundred ohms in series with C3 may be advised for larger values to insure the stability of A4.

The positive input voltage range is determined by the common mode range of the op amps. However, if the output of A4 saturates, gate-capacitance compensation will be affected.

The input voltage must be above the negative supply by at least the pinch voltage of the FET to keep it off in hold. In addition, the negative supply must be sufficient to maintain current in D2; or gate-capacitance compensation will suffer. The voltage on the emitter of Q2 can be made more negative than the op amp supplies to extend the operating range.

Since internal dissipation can be quite high when driving fast signals into a capacitive load, using a buffer in a power package is recommended.* Raising buffer quiescent current to 40mA with R3 improves frequency response.

*Overheating of the buffer causes a sharp reduction in slew rate before thermal limit is activated.

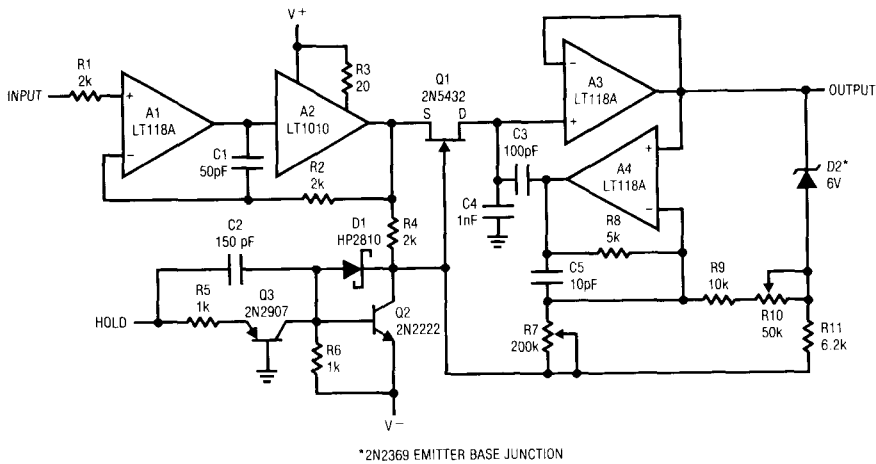


figure 47. A 5MHz track and hold. With buffer, bandwidth and slew rate is little affected by the hold capacitor. Compensation for gate capacitance of FET switch is included.

This circuit is equally useful as a fast acquisition sample and hold. A LF156 might be used for A3 to reduce drift in hold because its lower slew rate is not usually a problem in this application.

Using an LT118A and lower feedback resistors would give much lower output capacitance at the expense of output resistance.

bidirectional current sources

The voltage-to-current converter in figure 48 uses the standard op amp configuration. It has differential input, so either input can be grounded for the desired output sense. Output is bidirectional.

Maximum output resistance is obtained by trimming the resistors. High frequency output characteristics will depend on the bandwidth and slew rate of the op amp, as well as stray capacitance to the op amp inputs. This $\pm 150\text{mA}$ current source had a measured output resistance of $3\text{M}\Omega$ and 48nF equivalent output capacitance.

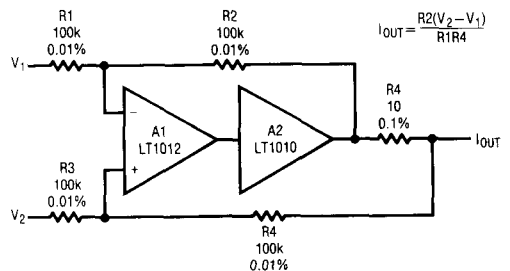


figure 48. This voltage/current converter requires excellent resistor matching or trimming to get high output resistance. Buffer increases output current and capacitive load stability with small R4.

Application Note 16

In figure 49, an instrumentation amplifier is used to eliminate the feedback resistors and any sensitivity to stray capacitances. The circuit had a measured output resistance of $6M\Omega$ and an equivalent output capacitance of $19nF$. Pins 7 and 8 of the LM163 are differential inputs, but they are loaded internally with $50k\Omega$ to V^- . Either input can be grounded to get the desired output sense. Because of the loading, the input should be driven from a low impedance source like an op amp.

Both circuits are stable for all capacitive loads.

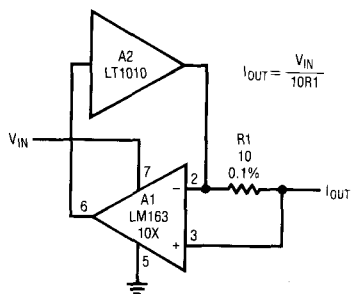


figure 49. Voltage/current converter using instrumentation amplifier does not require matched resistors.

voltage regulator

Even though it operates from a single supply, the circuit in figure 50 will regulate voltage down to $200mV$. It will also source or sink current.

The circuit's ability to handle capacitive loads is determined by $R3$ and $C1$. The values given are optimized for up to $1\mu F$ output capacitance, as might be required for an IC test supply.

The purpose of $C1$ is to lower the drive impedance to the buffer at high frequencies because the high frequency output impedance of the LM10 runs above $1k\Omega$. Without $C1$ there could be low level oscillation at certain capacitive loads.

It is important to connect pin 4 of the LM10 and the bottom of $R2$ to a common ground point to avoid poor regulation because of ground loop problems.

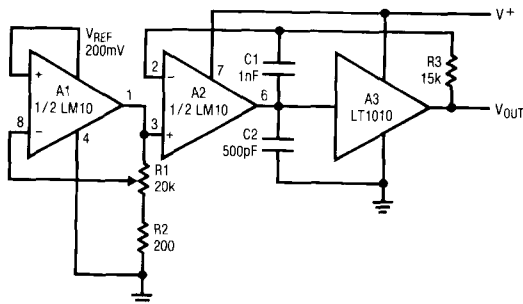


figure 50. This voltage regulator operates from a single supply yet is adjustable down to $200mV$ and can source or sink current.

voltage/current regulator

Figure 51 shows a fast power buffer that regulates the output voltage at V_V until the load current reaches a value programmed by V_I . For heavier loads it is a fast, precision current regulator.

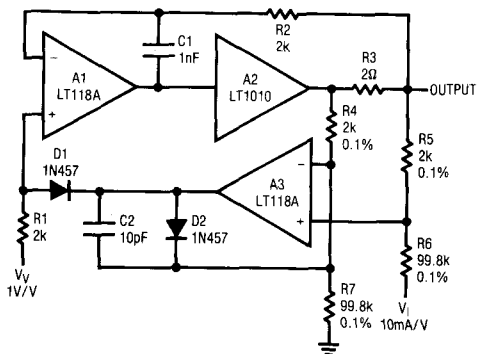


figure 51. This circuit is a power buffer with automatic transition into precision, programmable current limit. Fast, clean response into and out of current limit is a feature of the design.

With output current below the current limit, the current regulator is disconnected from the loop by $D1$, with $D2$ keeping its output out of saturation. This output clamp enables the current regulator to get control of the output current from the buffer current limit within a microsecond for an instantaneous short.

In the voltage regulation mode, A1 and A2 act as a fast voltage follower using the capacitive load isolation technique described earlier. Load transient recovery, as well as capacitive load stability, are determined by C1. Recovery from short circuit is clean.

Bidirectional current limit can be provided by adding another op amp connected as a complement to A3. Increased output current and less sensitivity to capacitive loading are obtained by paralleling buffers.

This circuit can be used to make an operational power supply with a bandwidth up to 10MHz that is well suited to IC testing. Output impedance is low without output capacitors and current limit is fast so that it will not damage sensitive circuits. The bandwidth and slew rate are reduced to 2MHz and $15V/\mu s^\dagger$ (without paralleling) by the $0.01\mu F$ required for supply bypass on many ICs. Large output capacitors can be accommodated by switching a larger capacitor across C1.

supply splitter

Dual supply op amps and comparators can be operated from a single supply by creating an artificial ground at half the supply voltage. The supply splitter shown in figure 52 can source or sink 150mA.

The output capacitor, C2, can be made as large as necessary to absorb current transients. An input capacitor is also used on the buffer to avoid high frequency instability that can be caused by high source impedance.

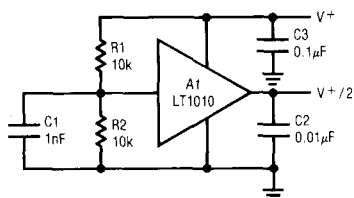


figure 52. Using the buffer to supply an artificial ground ($V^+/2$) to operate dual supply op amps and comparators from a single supply.

\dagger Slewing large capacitors causes high buffer dissipation.

overload clamping

The input of a summing amplifier is at virtual ground as long as it is in the active region. With overloads this is no longer true unless the feedback is kept active.

Figure 53 shows a chopper-stabilized current-to-voltage converter. It is capable of 10pA resolution, yet is able to keep the summing node under control with overload currents to $\pm 150mA$.

During normal operation, D3 and D4 are not conducting; and R1 absorbs any leakage current from the zener clamps, D6 and D7. In overload, current is supplied to the summing node through the zener clamps rather than the scaling resistor, R2. A capacitor on the input absorbs fast transients.

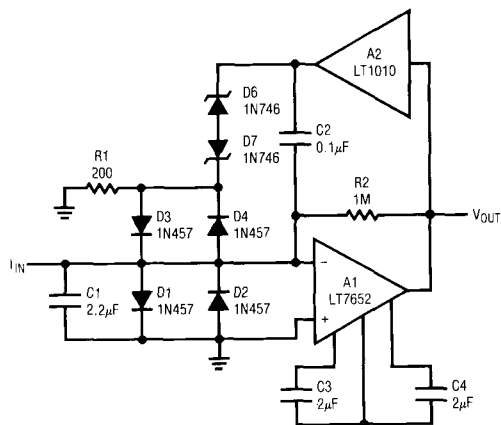


figure 53. Chopper-stabilized current/voltage converter has picoampere sensitivity, yet is capable of keeping summing node under control with 150mA input current.

Application Note 16

conclusions

A new class-B output stage has been described that is particularly well suited to IC designs. It is fast and avoids the parasitic oscillation problems of the quasi-complementary output. This has been combined with the charge storage transistor, a new diode structure and a novel boost circuit to make a general-purpose buffer that combines speed, large output drive and low standby current. The buffer has been well characterized and shows few disagreeable characteristics.

The applications section has demonstrated that buffers can be quite useful in everyday analog design. They also

make touchy wideband amplifiers easy to use. The availability of a low cost, high-performance IC buffer should be a stimulus to expanding upon these applications. Buffers no longer need to be considered an exotic component; they will become a standard analog design tool.

acknowledgement

Thanks are due to Felisa Velasco for special engineering assembly which was key to product development and to Guy Hoover for doing most of the experimental work presented here.

appendix

The following summarizes some design details that might otherwise be overlooked when first using the buffer. An equivalent circuit is given, and guaranteed electrical characteristics from the data sheet are listed for reference.

supply bypass

The buffer is no more sensitive to supply bypassing than slower op amps, as far as stability is concerned. The 0.1 μ F disc ceramic capacitors usually recommended for op amps are certainly adequate for low frequency work. As always, keeping the capacitor leads short and using a ground plane is prudent, especially when operating at high frequencies.

The buffer slew rate can be reduced by inadequate supply bypass. With output current changes much above 100mA/ μ S, using 10 μ F solid tantalum capacitors on both supplies is good practice, although bypassing from the positive to the negative supply may suffice.

When used in conjunction with an op amp and heavily loaded (resistive or capacitive), the buffer can couple into supply leads common to the op amp causing stability problems with the overall loop and extended settling time.

Adequate bypassing can usually be provided by 10 μ F solid tantalum capacitors. Alternately, smaller capacitors could be used with decoupling resistors. Sometimes the op amp has much better high frequency rejection on one supply, so bypass requirements are less on this supply.

power dissipation

In many applications, the LT1010 will require heat sinking. Thermal resistance, junction to still air is 150°C/W for the TO-39 package, 100°C/W for the TO-220 package and 60°C/W for the TO-3 package. Circulating air, a heat sink or mounting the package to a printed circuit board will reduce thermal resistance.

In dc circuits, buffer dissipation is easily computed. In ac circuits, signal waveshape and the nature of the load determine dissipation. Peak dissipation can be several times average with reactive loads. It is particularly important to determine dissipation when driving large load capacitance.

With ac loading, power is divided between the two output transistors. This reduces the effective thermal resistance, junction to case, to 30°C/W for the TO-39 package and 15°C/W for the TO-3 and TO-220 packages, as long as the peak rating of neither output transistor is exceeded. Figure 30 indicates the peak dissipation capabilities of one output transistor.

overload protection

The LT1010 has both instantaneous current limit and thermal overload protection. Foldback current limiting has not been used, enabling the buffer to drive complex loads without limiting. Because of this, it is capable of power dissipation in excess of its continuous ratings.

Normally, thermal overload protection will limit dissipation and prevent damage. However, with more than 30V across the conducting output transistor, thermal limiting is not quick enough to insure protection in current limit. The thermal protection is effective with 40V across the conducting output transistor as long as the load current is otherwise limited to 150mA.

drive impedance

When driving capacitive loads, the LT1010 likes to be driven from a low source impedance at high frequencies. Certain low power op amps (e.g., the LM10) are marginal in this respect. Some care may be required to avoid oscillations, especially at low temperatures.

Bypassing the buffer input with more than 200pF will solve the problem. Raising the operating current also works, but this cannot be done with the TO-39 package.

equivalent circuit

Below 1MHz, the LT1010 is quite accurately represented by the equivalent circuit shown in figure A for both small and large signal operation. The internal element, A1, is

an idealized buffer with the unloaded gain specified for the LT1010. Otherwise, it has zero offset voltage, bias current and output resistance. The output of A1 saturates to its supply terminals.

Loaded voltage gain can be determined from the unloaded gain, A_V , the output resistance, R_{OUT} , and the load resistance, R_L , using

$$A_{VL} = \frac{A_V R_L}{R_{OUT} + R_L}$$

Maximum positive output swing is given by

$$V_{OUT}^+ = \frac{(V^+ - V_{SOS}^+) R_L}{R_{SAT} + R_L}$$

where V_{SOS} is the unloaded output saturation voltage and R_{SAT} is the output saturation resistance.

The input swing required for this output is

$$V_{IN}^+ = V_{OUT}^+ \left(1 + \frac{R_{OUT}}{R_L} \right) - V_{OS} + \Delta V_{OS}$$

where ΔV_{OS} is the clipping allowed in making the saturation measurements (100mV).

The negative output swing and input drive requirements are determined similarly. The values given in figure A are typical; worst-case numbers are obtained from the data sheet reproduced on the back page.

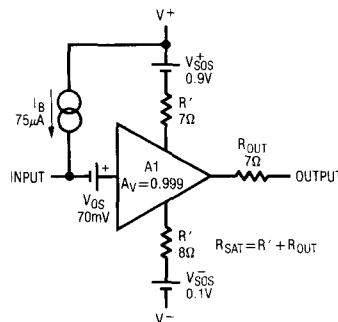


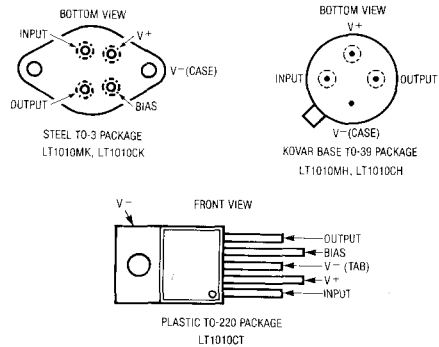
figure A. An idealized buffer, A1, as modified by this equivalent circuit describes the LT1010 at low frequencies.

Application Note 16

absolute maximum ratings

Total Supply Voltage	± 22V
Continuous Output Current	± 150mA
Continuous Power Dissipation (Note 1)	
LT1010MK	5.0W
LT1010CK	4.0W
LT1010CT	4.0W
LT1010MH	3.1W
LT1010CH	2.5W
Input Current (Note 2)	± 40mA
Operating Junction Temperature	
LT1010M	-55°C to 150°C
LT1010C	0°C to 125°C
Storage Temperature	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

connection diagrams



electrical characteristics

SYMBOL	PARAMETER	CONDITIONS (NOTE 3)	LT1010M		LT1010C		UNITS
			MIN	MAX	MIN	MAX	
V _{OS}	Output Offset Voltage	Note 3 V _S = ± 15V, V _{IN} = 0	20	110	0	150	mV
			-10	220	-20	220	mV
			40	90	20	100	mV
I _B	Input Bias Current	I _{OUT} = 0 I _{OUT} ≤ 150mA	0	150	0	250	μA
			0	250	0	500	μA
			0	300	0	800	μA
A _V	Large Signal Voltage Gain		0.995	1.00	0.995	1.00	V/V
R _{OUT}	Output Resistance	I _{OUT} = ± 1mA I _{OUT} = ± 150mA	6	9	5	10	Ω
			6	9	5	10	Ω
				12		12	Ω
	Slew Rate	V _S = ± 15V, V _{IN} = ± 10V V _{OUT} = ± 8V, R _L = 100Ω	75		75		V/μs
V _{SOS} ⁺	Positive Saturation Offset	Note 4, I _{OUT} = 0		1.0		1.0	V
				1.1		1.1	V
V _{SOS} ⁻	Negative Saturation Offset	Note 4, I _{OUT} = 0		0.2		0.2	V
				0.3		0.3	V
R _{SAT}	Saturation Resistance	Note 4, I _{OUT} = ± 150mA		18		22	Ω
				24		28	Ω
V _{BIAS}	Bias Terminal Voltage	Note 5, R _{BIAS} = 20Ω	750	810	700	840	mV
			560	925	560	880	mV
I _S	Supply Current	I _{OUT} = 0, I _{BIAS} = 0		8		9	mA
				9		10	mA

Note 1: For case temperatures above 25°C, dissipation must be derated based on a thermal resistance of 25°C/W with the K and T packages or 40°C/W with the H package. See applications information.

Note 2: In current limit or thermal limit, input current increases sharply with input-output differentials greater than 8V; so input current must be limited. Input current also rises rapidly for input voltages 8V above V⁺ or 0.5V below V⁻.

Note 3: Specifications apply for 4.5V ≤ V_S ≤ 40V, V⁻ + 0.5V ≤ V_{IN} ≤ V⁺ - 1.5V and I_{OUT} = 0, unless otherwise stated. Temperature range is -55°C ≤ T_J ≤ 150°C, T_C ≤ 125°C, for the LT1010M and 0°C ≤ T_J ≤ 125°C, T_C ≤ 100°C, for the LT1010C. The ● and **boldface type** on limits denote the specifications that apply over the full temperature range.

Note 4: The output saturation characteristics are measured with 100mV output clipping. See applications information for determining available output swing and input drive requirements for a given load.

Note 5: With the TO-3 and TO-220 packages, output stage quiescent current can be increased by connecting a resistor between the bias pin and V⁺. The increase is equal to the bias terminal voltage divided by this resistance.

Considerations for Successive Approximation A → D Converters

Jim Williams

The most popular A → D method employed today is the successive approximation register (SAR) converter (see Box, "The Successive Approximation Technique"). Numerous monolithic, hybrid and modular devices embodying the successive approximation technique are available, and monolithic devices are slowly gaining in performance. Nevertheless, hybrid and modular SAR types feature the best performance. In particular, at the 12-bit level, the fastest monolithic devices currently available require about 10 μ s to convert. Modular and hybrid units achieve

conversion speeds below 2 μ s, although they are quite expensive. Because of these factors, it is often desirable to build, rather than buy, a high speed 12-bit SAR converter. Even in cases where high speed is not required, lower cost may still mandate building the circuit instead of using a monolithic device.

Figure 1 shows a simple 12-bit, 12 μ s SAR converter. Understanding this circuit's performance limitations is useful in

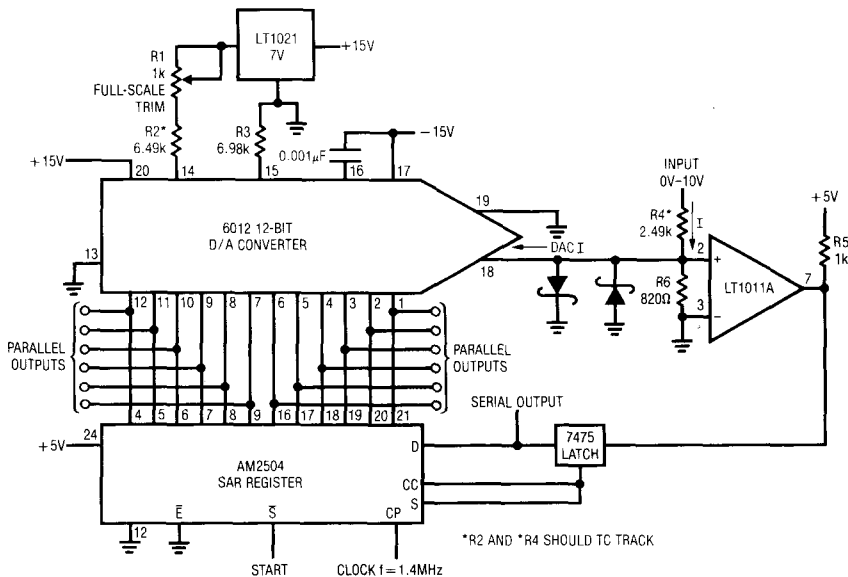


Figure 1. Basic 12-Bit, 12 μ s Successive Approximation A → D Converter

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designing faster converters. Figure 2 shows waveforms of operation. Trace A is the clock, which is applied to the 2504 IC successive approximation register (SAR), while Trace B is the start pulse. On the rising edge of the start pulse, the SAR-DAC combination begins to test each bit, beginning with the MSB. This action is reflected in conditions at the LT1011's positive input (Trace C). This waveform is seen to sequentially converge towards zero as the SAR, DAC and comparator servo the node. After the LSB has been converted the "conversion complete" (CC) line (Trace D) goes high, signaling the end of the sequence. The 7475 latch prevents the comparator from responding to input noise or shifts after the conversion is complete. It is reset at the next "conversion command". The major limitations on speed in this circuit are the DAC and the comparator. Most bipolar DACs require 150-200ns to settle for a worst-case (full-scale) step and the comparator's delay time must also be accounted for. The clamp diodes limit overdrive, aiding comparator response. Additionally, the 820 Ω resistor to ground shunts the DACs output capacitance, helping the comparator-DAC node settle more quickly. The shunt degrades the voltage per-LSB available to the comparator, but the LT1011's high gain makes up for this.

In general, this is a fairly typical 12-bit SAR converter with good speed and low cost. To get higher conversion speed requires more sophisticated circuitry.

Figure 3 shows a circuit which uses a clock modulation scheme to decrease conversion time. The A \rightarrow D is identical to Figure 1's circuit, but the clock terminal (CP) is driven by a 2 speed oscillator. Figure 4 shows operating details. A convert command pulse (Trace A) initiates the SAR routine. Simultaneously, the 7474 flip-flop's Q output is set high (Trace C), biasing Q1. This causes the 47pF capacitor to be paralleled with the 33pF unit. These capacitors are part of the timing network of C1, which is configured as an oscillator. C1's output pulses (Trace B) drive the SAR's clock terminal ("CP" in the schematic). After the third MSB has been converted, the flip-flop is reset (Trace C). Q1 goes off and the clock oscillator (Trace B) speeds up. The increase in clock speed results in less dwell time per bit at the DAC-comparator junction (Trace D), allowing faster total conversion time. Trace E, the conversion complete pulse ("CC"), drops low 7.5 μ s after the conversion started.

This clock modulation approach buys significantly improved speed, but does nothing to get around the comparator's contribution to delay. Minimizing comparator delay would seem to be as simple as using a faster device. At the 8 or even 10-bit level this usually works, but 12-bit performance raises problems. Replacing the LT1011, a 150ns device, with a 10ns LT1016 increases speed, but decreases available gain. The LT1011 has a minimum gain of

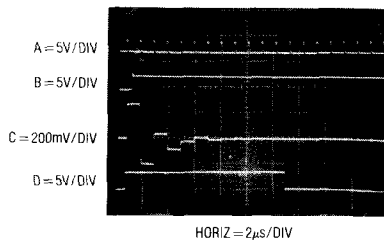


Figure 2. 12 μ s A \rightarrow D Waveforms

200,000. The LT1016's high speed sacrifices gain. Minimum gain for this device is 1400. For a 10V full-scale A → D, the LSB size is given by:

$$\frac{10V}{4096 \text{ steps}} = 2.44mV/LSB$$

To switch a full TTL output level with 1/2 LSB overdrive (1.22mV), the comparator must have a minimum gain of:

$$\frac{5V}{1.22mV} = 4,098.$$

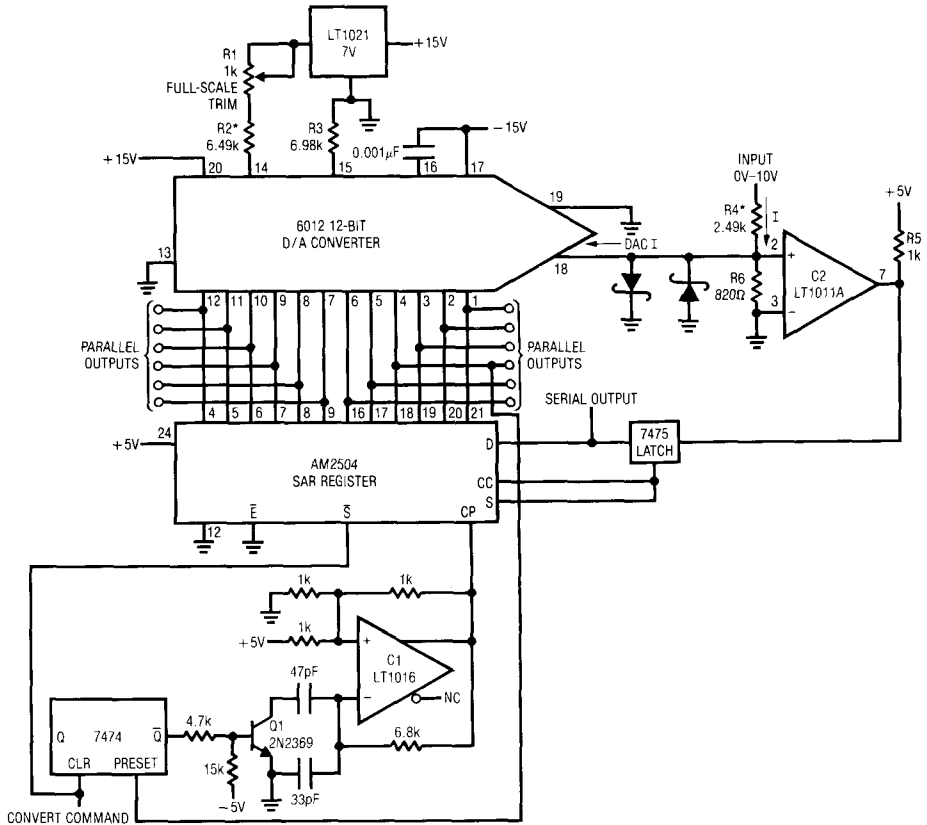


Figure 3. 7.5µs A-D Using a 2 Speed Clock

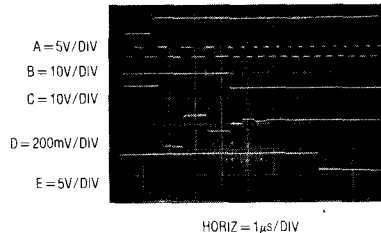


Figure 4. Figure 3's Waveforms

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This figure clearly means the comparator cannot do the job without some help. The input signal reduction caused by the shunt resistor at the DAC output worsens the problem. Finally, the comparator's speed degrades for such low level overdrives.

The solution to the aforementioned difficulties is to place a gain stage ahead of the comparator. While the gain stage adds some delay, it also increases gain, providing the needed overdrive to the comparator.

Figure 5 shows a simple pre-amplifier. This pre-amp-comparator combination gives adequate gain and an overall response time of 40-50ns. A1 is set up as a Schottky bounded amplifier. The bound diodes prevent A1 from saturating due to excessive summing point overdrive, aid-

ing response time. The 10pF capacitor, a typical value, compensates DAC output capacitance and is selected for best amplifier damping. The 10k feedback resistor, also typical, is chosen for best gain-bandwidth performance. Voltage gains of 4 to 10 are common. Figure 6 shows performance. Trace A, a test input pulse, causes A1's output (Trace B) to slew through zero (screen center horizontal line). When A1 crosses zero, C1's input biases negative and it responds (C1's output is Trace C) 10ns later with a TTL output.

A simple circuit like this results in faster comparisons. Substituted for the LT1011 in Figure 3's circuit, it permits conversion times in the 3-5 μ s range. Further reduction in conversion time is possible with a faster discrete preamplifier.

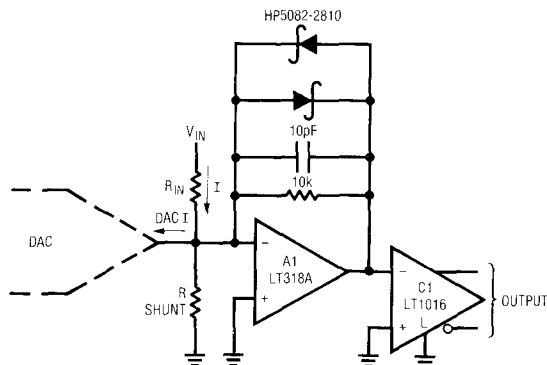


Figure 5. Simple Pre-Amplifier for the Comparator

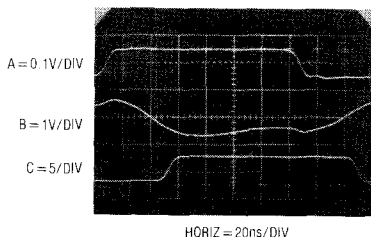


Figure 6. Pre-Amplified Comparator Waveforms

Figure 7 shows a very fast pre-amplifier built with GHz range transistors. This cascoded differential amplifier is placed ahead of C1, an LT1016. Q4 and Q5 provide bias current compensation for Q1's base current. Figure 8

shows results for a test input signal (Trace A). C1's output (Trace B) switches in 15-20ns. About 10ns of this delay is due to C1, with the pre-amplifier contributing the rest.

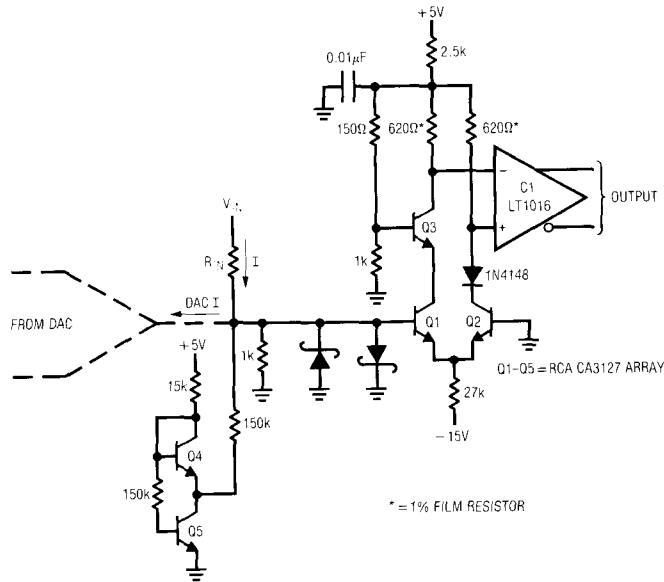


Figure 7. Fast Pre-Amplifier-Comparator

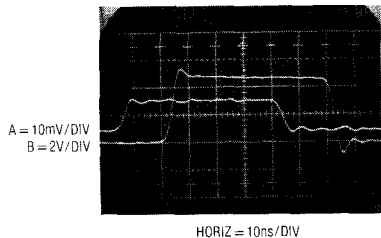


Figure 8. Fast Pre-Amp-Comparator Waveforms

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Figure 9 shows the discrete pre-amplifier used in a very fast 12-bit SAR converter. The design utilizes a variety of techniques to attain extremely high speed. Primary speed enhancing features include a closed loop clock control

method and active summing node clamping. The circuit achieves a full 12-bit conversion in 1.8 μ s, about the practical limit with off-the-shelf components.

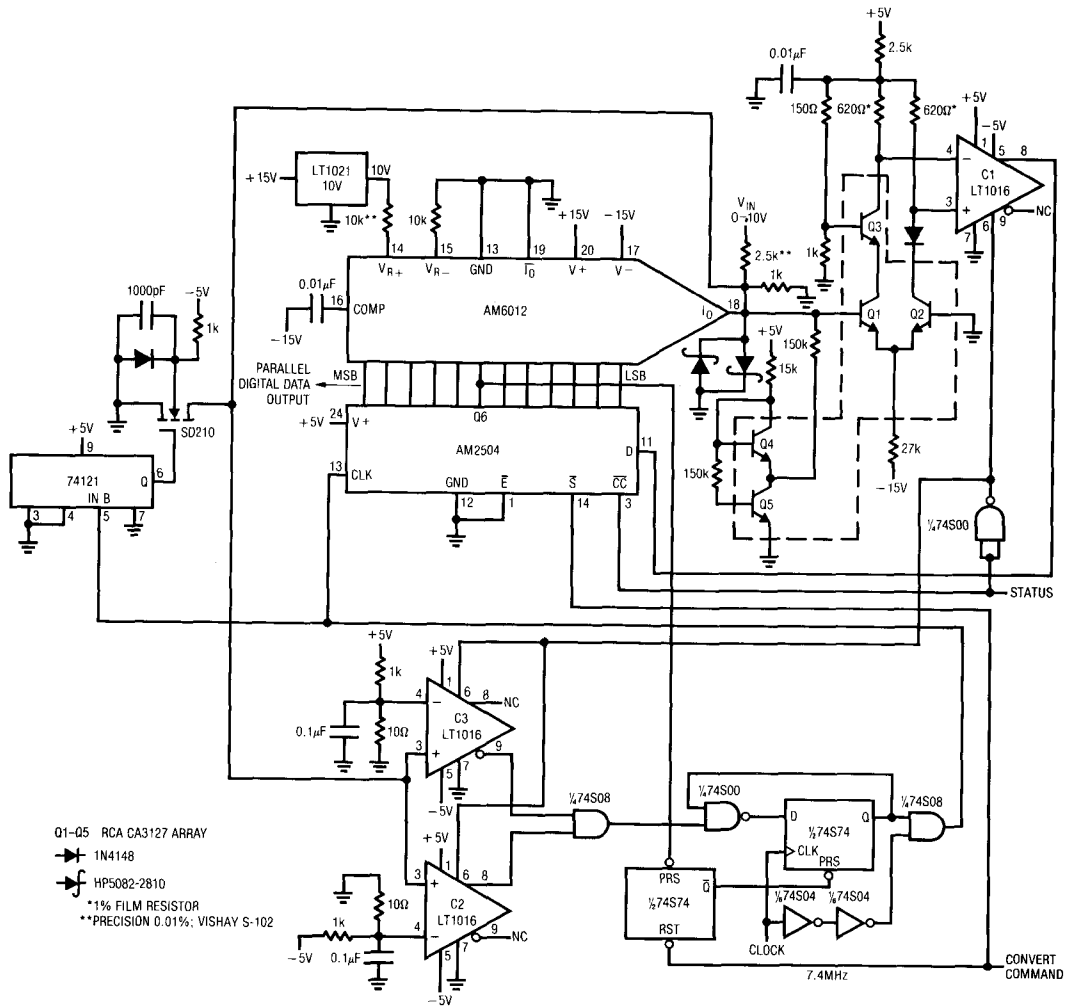


Figure 9. 12-Bit 1.8 μ s SAR A - D

The design is similar in concept to Figure 3, except that the fast pre-amplifier replaces the LT1011. Additionally, the clock speed change is implemented with the digital logic shown. Unlike before, the clock rate is accelerated after the fifth MSB is converted. During conversion of the upper four bits, the clock rate is controlled by a closed loop to maximize overall speed. The loop monitors conditions at the DAC-comparator summing node. If the node is outside $\pm 50\text{mV}$, the SAR is clocked at the maximum rate. For node responses inside $\pm 50\text{mV}$, the clock rate is retarded, giving adequate time for settling. The clock loop speeds conversion by not waiting for bits which aren't going to settle within $\pm 50\text{mV}$. C2 and C3 form a high speed window comparator which delivers summing node information in digital form to the clock logic.

Figure 10 shows the effects of the closed loop clocking scheme. Trace A is the convert command. Trace B is the gated output of the C2-C3 window comparator. Trace B's state controls the clock line, which is Trace C. Trace D is the summing point, and the dwell time-per-bit is controlled by the window comparator's decision. Beyond the fifth bit, the SAR's Q6 line instructs the clock logic to run at maximum speed. As described to this point, the circuit achieves a $1.9\mu\text{s}$ conversion time.

If the 74121 one-shot and associated circuitry are included, conversion time is reduced to $1.8\mu\text{s}$. These

components form an active clamp at the DAC-comparator summing node. Each time the SAR clock is pulsed (Trace A, Figure 11), the 74121 puts out a 30ns FET gate pulse (Trace B). The FET comes on, shunting the summing node (Trace C) to ground. The FET's low on resistance aids DAC settling by discharging the DACs 30pF output capacitance for 30ns. The summing node (Trace C) is reset to zero by this action at each SAR-directed step. When the one shot times out, the node settles to its final value. This active clamping results in about a 10ns-per-bit time savings.

This circuit's $1.8\mu\text{s}$ conversion time is very close to what is practically achievable for a 12-bit SAR A \rightarrow D converter. The special techniques used result in an effective DAC settling time of about 100ns per bit. Comparator-pre-amp delay is about 20ns per bit and SAR chip delays are in the 25ns per bit range. Adding these together gives; $(100\text{ns} + 20\text{ns} + 25\text{ns} \times 12 = 1.74\mu\text{s})$. The comparator and SAR delays, about 31% of the total, are not easily reduced. A discrete Schottky SAR design and a faster pre-amp can cut this figure somewhat, but the DAC settling time, 69% of the total, remains. The effective 100ns/bit DAC settling time compares favorably with published specifications for monolithic DACs, and is not readily reducible. Beyond this speed, other conversion methods are required.

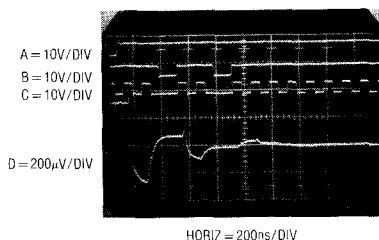


Figure 10. Figure 9's Waveforms

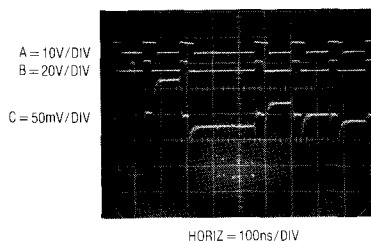


Figure 11. Figure 9's Waveforms Using Active Clamping

The Successive Approximation Technique

The successive approximation technique is probably as old as the first crude weighing scale ever constructed. It is most easily visualized when considering the operation of a beam balance. The unknown weight, in one pan, is determined by successive trials with standard weights placed in the other pan. Overweight-underweight decisions are made by the balance as standard weights (and combinations of them) are successively tried in a logical sequence which converges towards balancing the scale.

Successive approximation A → D converters start with the MSB and proceed toward the LSB as each under-over decision is made. The figure shows the summing node response (Trace A) as the DAC, instructed by the clock driven (Trace B) successive approximation register (SAR) logic, tries different bit weights. The comparator's decisions are also shown (Trace C). Note how the summing point sequentially converges towards zero, the analog of null in a beam balance.

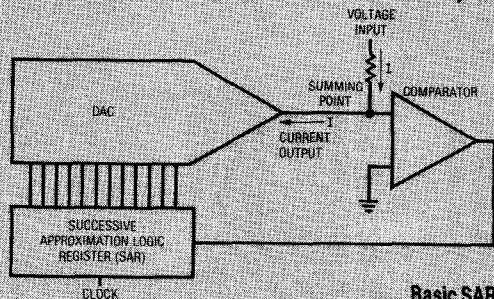
Digital to Analog Converters in SAR Applications

Selecting a DAC for use in an SAR-based A → D requires some thought. Most often, bipolar current mode DACs are employed because of their higher speed. CMOS DACs output capacitance, in the 100-150pF range, causes excessive summing node settling times. Monolithic bipolar types, in the 30pF region, settle more quickly. Voltage mode output DACs are almost never used because they are not necessary to achieve summing action and they are substantially slower than current output types.

Speed is often important, and since the DAC is the slowest part of the converter, it should be carefully considered. Settling time specifications for DACs are usually stated

for full-scale transitions. Smaller bit changes take less time, so some interpretation of the full-scale settling time number can be made when considering the DACs effective settling time-per-bit in an A → D application. Unfortunately, the complex dynamics of DAC internals prevent simple straight line calculations (e.g., 1 LSB will not settle in 1/12 the time of full-scale for a 12-bit unit). At moderate speeds, the simplest course is to allow the specified full-scale settling time for each bit decision. This conservative method will never get you into trouble, but almost certainly guarantees slower than necessary DAC performance. The best way to find out just how far you can push the DACs settling time specifications in an SAR application is to consult the manufacturer. Additionally, it is worthwhile to actually measure the settling time under conditions appropriate to the intended use (see LTC Application Note 10, "Methods for Measuring Op Amp Settling Time", for circuits readily adaptable to DAC settling time measurements). The wide variety of DACs and individual output termination requirements make obtainable results vary considerably. However, some guidelines on what to expect are possible. For example, the popular 565A type, specified at 250ns full-scale settling time into 0Ω, can achieve 110-150ns effective settling time-per-bit in SAR applications with careful design. It is also worth noting that the dynamics of DAC types can vary considerably between manufacturers of what is nominally the same part.

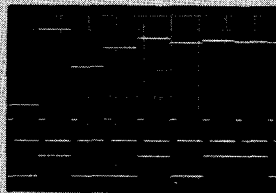
Speed is not the only concern. The DACs DC specifications translate directly into A → D error terms. Linearity, drift, accuracy and other DC terms contribute on a 1:1 basis to the A → D's error characteristics. One specification, monotonicity, can contribute a particularly nasty term. The effect of a non-monotonic DAC is an inability of the A → D to produce some output codes ("missing codes") under any input condition.



A = 0.1V/DIV

B = 5V/DIV

C = 5V/DIV



HORIZ = 20ns/DIV

Basic SAR Circuit and Waveforms

Power Gain Stages for Monolithic Amplifiers

Jim Williams

Most monolithic amplifiers cannot supply more than a few hundred milliwatts of output power. Standard IC processing techniques set device supply levels at 36V, limiting available output swing. Additionally, supplying currents beyond tens of milliamperes requires large output transistors and causes undesirable IC power dissipation.

Many applications, however, require greater output power than most monolithic amplifiers will deliver. When voltage or current gain (or both) is needed, a separate output stage is necessary. The power gain stage, sometimes called a "booster," is usually placed within the monolithic amplifier's feedback loop, preserving the IC's low drift and stable gain characteristics.

Because the output stage resides in the amplifier's feedback path, loop stability is a concern. The output stage's gain and AC characteristics must be considered if good dynamic performance is to be achieved. Overall circuit phase shift, frequency response and dynamic load handling capabilities are issues that cannot be ignored when designing a power gain stage for a monolithic amplifier. The output stage's added gain and phase shift can cause poor AC response or outright oscillation. Judicious application of frequency compensation methods is needed for good results (see box section, "The Oscillation Problem").

The type of circuitry used in an output stage varies with the application, which can be quite diverse. Current and voltage boosting are common requirements, although both are often simultaneously required. Voltage gain stages are usually associated with the need for high voltage power supplies, but output stages which inherently generate such high voltages are an alternative.

A simple, easily used current booster is a good place to begin a study of power gain stages.

150mA Output Stage

Figure 1A shows the LT1010 monolithic 150mA current booster placed within the feedback loop of a fast FET amplifier. At lower frequencies, the buffer is within the feedback loop so that its offset voltage and gain errors are negligible. At higher frequencies, feedback is through C_f , so that phase shift from the load capacitance acting against the buffer output resistance does not cause loop instability.

Small signal bandwidth is reduced by C_f , but considerable load isolation can be obtained without reducing it below the power bandwidth. Often a bandwidth reduction is desirable to filter high frequency noise or unwanted signals.

The LT1010 is particularly adept at driving large capacitive loads, such as cables.

The follower configuration (Figure 1B) is unique in that capacitive load isolation is obtained without a reduction in small signal bandwidth, although the output impedance of the buffer has a 10MHz bandwidth without capacitive loading, yet it is stable for all load capacitance to over 0.3 μ F.

Figure 1C shows LT1010's used in a bridge type differential output stage. This permits increased voltage swing across the load, although the load must float.

All of these circuits will deliver 150mA of output current. The LT1010 supplies short circuit and thermal overload protection. Slew limit is set by the op amp used.

High Current Booster

Figure 2 uses a discrete stage to get 3A output capacity. The configuration shown provides a clean, quick way to increase LT1010 output power. It is useful for high current loads, such as linear actuator coils in disk drives.

Application Note 18

The 33Ω resistors sense the LT1010's supply current, with the grounded 100Ω resistor supplying a load for the LT1010. The voltage drop across the 33Ω resistors biases Q1 and Q2. Another 100Ω value closes a local feedback loop, stabilizing the

output stage. Feedback to the LT1056 control amplifier is via the 10k value. Q3 and Q4, sensing across the 0.18Ω units, furnish current limiting at about 3.3A.

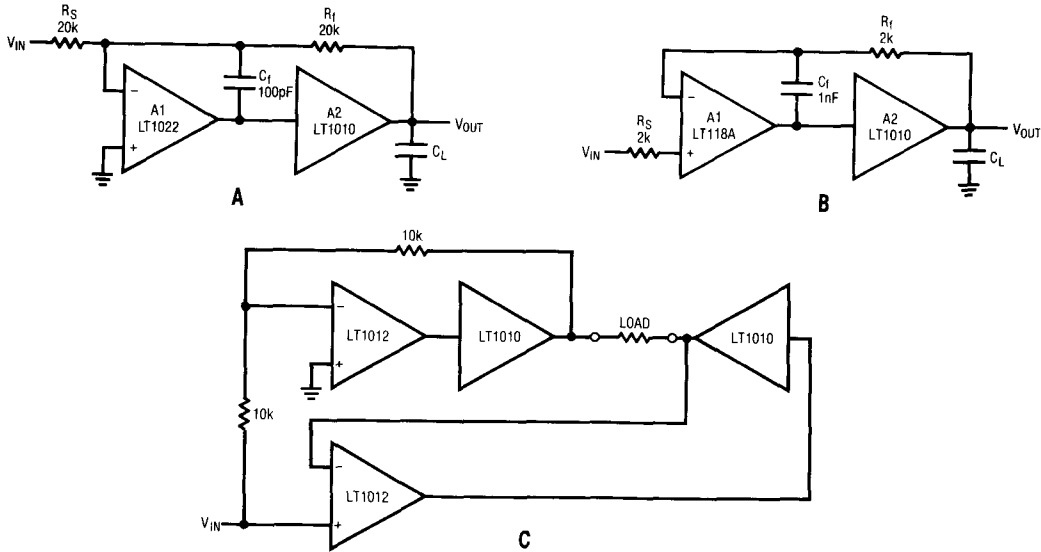
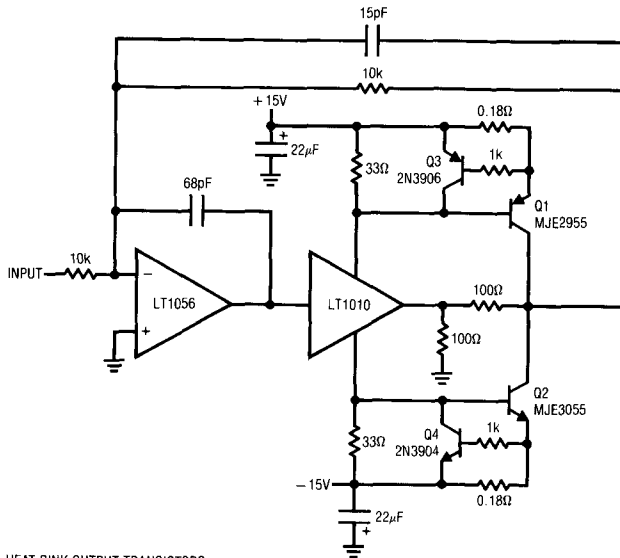


Figure 1. LT1010 Output Stages



HEAT SINK OUTPUT TRANSISTORS

Figure 2. LT1010 Based Output Stage

The output transistors have low F_t , and no special frequency compensation considerations are required. The LT1056 is rolled off by the 68pF capacitor for dynamic stability, and the 15pF feedback capacitor trims edge response. At full power ($\pm 10V$, 3A peaks), bandwidth is 100kHz and slew rate about $10V/\mu s$.

Ultra-Fast Fed—Forward Current Booster

The previous circuits place the output stage booster within the op amp's feedback loop. Although this ensures low drift and gain stability, the op amp's response limits speed. Figure 3 shows a very wideband current boost stage. The LT1012 corrects DC errors in the booster stage, and does not see high frequency signals. Fast signals are fed directly to the stage via Q5 and the 0.01 μF coupling capacitors. DC and low frequency signals drive the stage via the op amp's output. This parallel path approach allows very broadband performance without sacrificing the DC stability of the op amp. Thus, the LT1012's output is effectively current and speed boosted.

The output stage consists of current sources Q1 and Q2 driving the Q3-Q5 and Q4-Q7 complementary emitter followers. The transistors specified have F_t 's approaching 1GHz, resulting in a very fast stage. The diode network at the output steers drive away from the transistor bases when output current exceeds 250mA, providing fast short circuit protection. Net inversion in the stage means the feedback must return to the LT1012's positive input. The circuit's high frequency summing node is the junction of the 1k and 10k resistors at the LT1012. The 10k-39pF pair filters high frequencies, permitting accurate DC summation at the LT1012's positive input. The low frequency roll-off of the fast stage is matched to the high frequency characteristics of the LT1012 section, minimizing aberration in the circuit's AC response. The 8pF feedback capacitor is selected to optimize settling characteristics at the highest speeds.

This current boosted amplifier features a slew rate in excess of $1000V/\mu s$, a full power bandwidth of 7.5MHz and a 3dB point of 14MHz. Figure 4 shows the circuit driving a 10V pulse into a 50 Ω load. Trace A is the input and Trace B is the output.

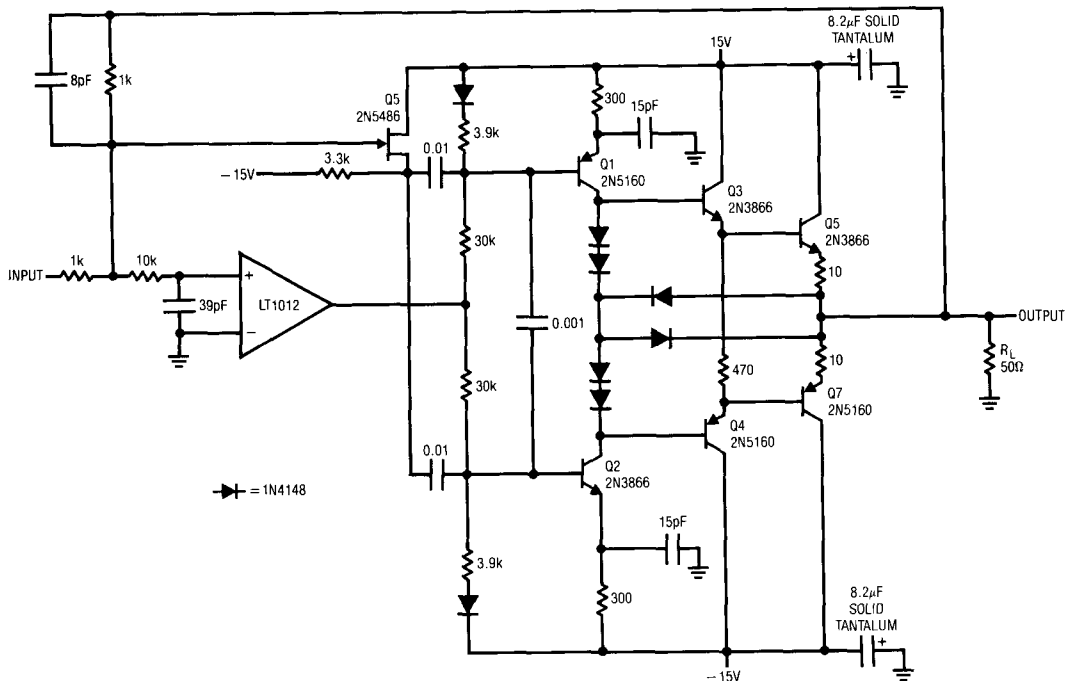


Figure 3. Fed-Forward Wideband Current Booster

Application Note 18

Slew and settling characteristics are quick and clean, with pulse fidelity approaching the quality of the input pulse generator. Note that this circuit relies on summing action, and cannot be used in the non-inverting mode.

useful in 5V powered analog systems, where improvements in available output swing are desirable to maximize signal processing range.

Simple Voltage Gain Stages

Voltage gain is another type of output stage. A form of voltage gain stage is one that allows output swing very near the supply rails. Figure 5A utilizes the resistive nature of the complementary outputs of a CMOS logic inverter to make such a stage. Although this is an unusual application for a logic inverter, it is a simple, inexpensive way to extend an amplifier's output swing to the supply rails. This circuit is particularly

The paralleled logic inverters are placed within the LT1013's feedback loop. The paralleling drops output resistance, aiding swing capability. The inversion in the loop requires the feedback connection to go to the amplifier's positive input. An RC damper eliminates oscillation in the inverter stage, which has high gain-bandwidth when running in its linear region. Local capacitive feedback at the amplifier gives loop compensation. The table provided shows that output swing is quite close to the positive rail, particularly at loads below several milliamperes.

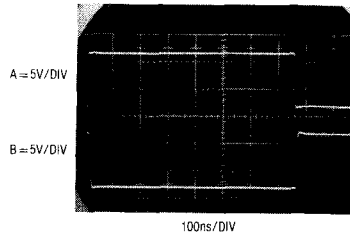


Figure 4. Figure 3's Response. Slew Rate Exceeds $1000\text{V}/\mu\text{s}$ at 10V Into 50Ω .

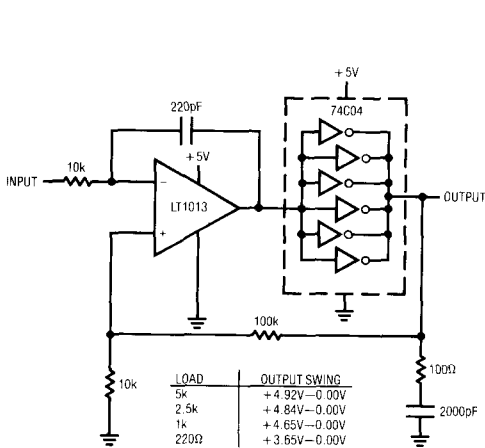


Figure 5A. CMOS Inverter Based Output Stage with Voltage Gain

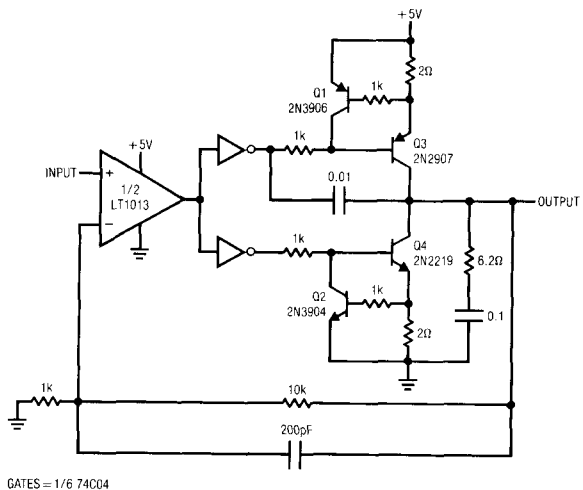


Figure 5B. Common Emitter Output Stage with Voltage Gain

Figure 5B is similar, except that the CMOS inverters drive bipolar transistors to reduce saturation losses, even at relatively high currents. Figure 6A shows Figure 5B's output saturation characteristics. Note the extremely low saturation limits below 25mA. Removing the current limit circuitry permits even better performance, particularly at high output currents.

Figure 6B shows waveforms of operation for circuit Figure 5A. The LT1013's output (Trace B) serves around the 74C04's switching threshold (about 1/2 supply voltage) as it

controls the circuit's output (Trace A). This allows the amplifier to operate well within its output swing range while controlling a circuit output with nearly rail-to-rail capability.

High-Current Rail-to-Rail Output Stage

Figure 7 is another rail-to-rail output stage, but features higher output current and voltage capability. The stage's voltage gain and low saturation losses allow it to swing nearly to the rails while simultaneously supplying current gain.

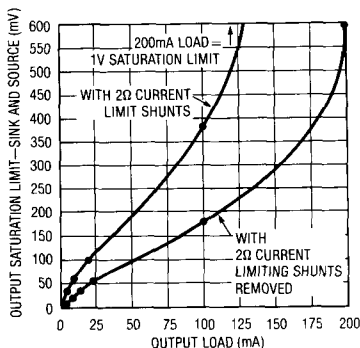


Figure 6A. Figure 5B's Saturation Characteristics

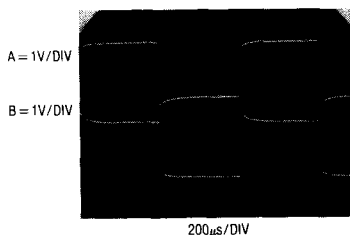


Figure 6B. Figure 5A's Waveforms

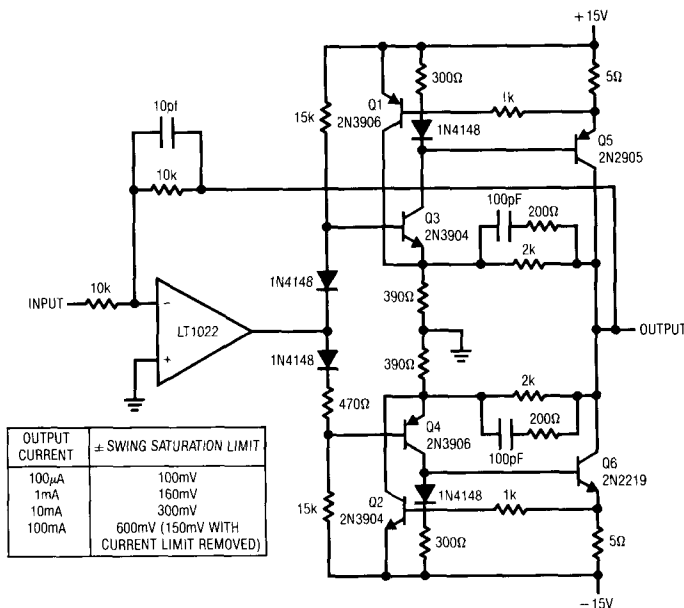


Figure 7. Complementary Closed Loop Common Emitter Stages Provide High Current and Good Saturation Performance

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Q3 and Q4, driven from the op-amp, provide complementary voltage gain to output transistors Q5-Q6. In most amplifiers, the output transistors run as emitter followers, furnishing current gain. Their V_{BE} drop, combined with voltage swing limitations of the driving stage, introduces the swing restrictions characteristic of such stages. Here, Q5 and Q6 run common emitter, providing additional voltage gain and eliminating V_{BE} drops as a concern. The voltage inversion of these devices combines with the drive stage inversion to yield overall non-inverting operation. Feedback is to the LT1022's negative input. The 2k-390 Ω local feedback loop associated with each side of the booster limits stage gain to about 5. This is necessary for stability. The gain bandwidth available through the Q3-Q5 and Q4-Q6 connections is quite high, and not readily controllable. The local feedback reduces the gain bandwidth, promoting stage stability. The 100pF-200 Ω damper across each 2k feedback resistor provides heavy gain attenuation at very high frequencies, eliminating parasitic local loop oscillations in the 50-100MHz range. Q1 and Q2, sensing across the 5 Ω shunts, furnish 125mA current limiting. Current flow above 125mA causes the appropriate transistor to come on, shutting off the Q3-Q4 driver stage.

Even with the feedback enforced gain-bandwidth limiting, the stage is quite fast. AC performance is close to the amplifier used to control the stage. Using the LT1022, full power bandwidth is 600kHz and slew rate exceeds 23V/ μ s under 100mA output loading. The chart in the figure shows output swing versus loading. Note that, at high current, output swing is primarily limited by the 5 Ω current sense resistors, which may be removed. Figure 8 shows response to a bipolar input pulse for 25mA loading. The output swings nearly to the rails, with clean dynamics and good speed.

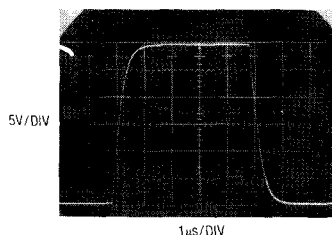
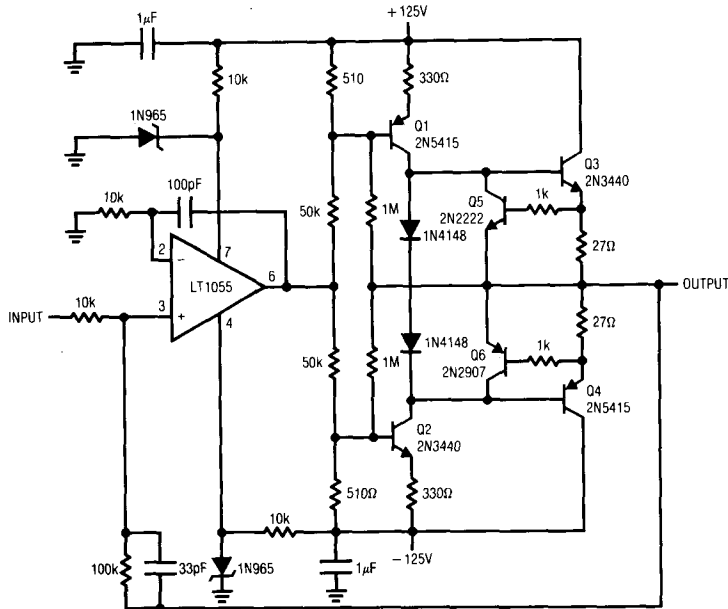


Figure 8. Figure 7 Drives $\pm 14.85V$ Into a 100mA Load

$\pm 120V$ Output Stage

Figure 9 is another voltage gain output stage. Instead of minimizing saturation losses, it provides high voltage outputs from a $\pm 15V$ powered amplifier. Q1 and Q2 furnish voltage gain, and feed the Q3-Q4 emitter follower outputs. $\pm 15V$ power for the LT1055 control amplifier is derived from the high voltage supplies via the zener diodes. Q5 and Q6 set current limit at 25mA by diverting output drive when voltages across the 27 Ω shunts become too high. The local 1M-50k feedback pairs set stage gain at 20, allowing $\pm 10V$ LT1055 drives to cause full $\pm 120V$ output swing. As in Figure 7, the local feedback reduces stage gain-bandwidth, making dynamic control easier. This stage is relatively simple to frequency compensate because only Q1 and Q2 contribute voltage gain. Additionally, the high voltage transistors have large junctions, resulting in low F_t 's, and no special high frequency roll-off precautions are needed. Because the stage inverts, feedback is returned to the LT1055's positive input. Frequency compensation is achieved by rolling off the LT1055 with the local 100pF-10k pair. The 33pF capacitor in the feedback peaks edge response and is not required for stability. Full power bandwidth is 15kHz with a slew limit of about 20V/ μ s. As shown, the circuit operates in inverting mode, although non-inverting operation is possible by exchanging the input and ground assignments at the LT1055's input. Under non-inverting conditions, the LT1055's input common-mode voltage limits must be observed, setting the minimum non-inverting gain at 11. If over-compensation is required, it is preferable to increase the 100pF value, instead of increasing the 33pF loop feedback capacitor. This prevents excessive high voltage energy from coupling to the LT1055's inputs during slew. If it is necessary to increase the feedback capacitor, the

summing point should be diode clamped to ground or to the $\pm 12V$ input pulse (Trace A). The output (Trace B) responds with a cleanly damped 240V peak-to-peak pulse.



HEAT SINK OUTPUT TRANSISTORS

Figure 9. $\pm 120V$ Output Stage. **DANGER! High Voltages Present. Use Caution.**

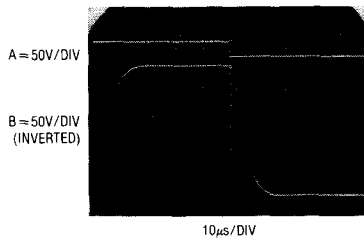


Figure 10. Figure 9 Swinging $\pm 120V$ Into 6k Ω . **DANGER! High Voltages Present. Use Caution.**

Application Note 18

Figure 11 is a similar stage, except that Figure 9's output transistors are replaced with vacuum tubes. Most of this stage is conceptually identical to Figure 9, but major changes are needed to get the vacuum tube output to swing negatively. Positive swing is readily achieved by simply replacing Figure 9's NPN emitter follower with a cathode follower (V1A). Negative outputs require PNP Q3 to drive a zener biased common cathode configuration. The transistor inverter is necessitated because our thermionic friends have no equivalent to PNP transistors. Zener biasing of V1B's cathode allows Q3's swing to cut off the tube, a depletion mode device.

Without correction, the DC biasing asymmetry caused by the Q3-V1B configuration will force the LT1055 to bias well away from zero. Tolerance stack-up could cause saturation limiting

in the LT1055's output, reducing overall available swing. This is avoided by skewing the stage's bias string with the potentiometer adjustment. To make this adjustment, ground the input and trim the potentiometer for 0V out at the LT1055.

Figure 11's full power bandwidth is 12kHz, with a slew rate of about $12V/\mu s$. Figure 12 shows response to a bipolar input (Trace A). The output responds cleanly, although the slew and settling characteristics reflect the stage's asymmetric gain-bandwidth. This stage's output is extremely rugged, due to the inherent forgiving nature of vacuum tubes. No special short circuit protection is needed, and the output will survive shorts to voltages many times the value of the $\pm 150V$ supplies.

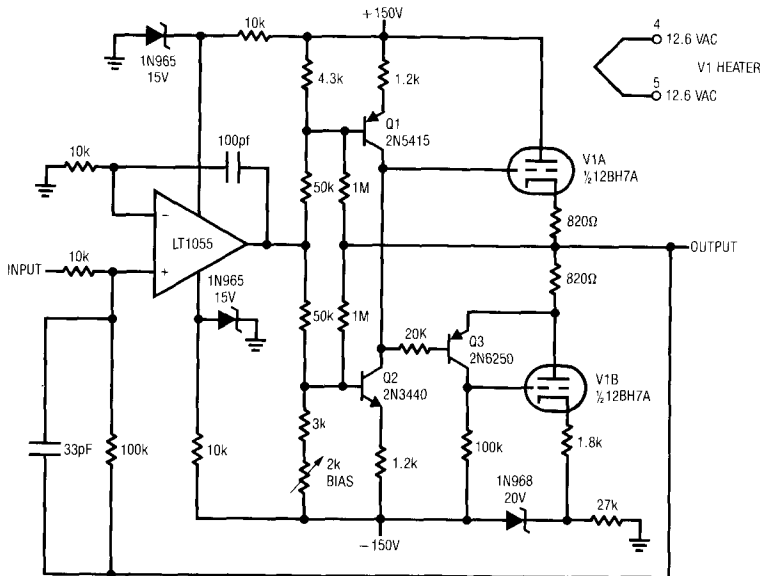


Figure 11. Rugged $\pm 120V$ Output Stage Employing Mr. De Forest's Descendants. **DANGER! High Voltages Present. Use Caution.**

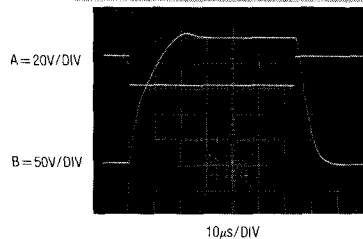


Figure 12. Figure 11's Response. Asymmetric Slew and Settling Are Due to Q3-V1B Connection. **DANGER! High Voltages Present. Use Caution.**

Unipolar Output, 1000V Gain Stage

Figure 13 shows a unipolar output gain stage which swings 1000V and supplies 15W. This boost stage has the highly desirable property of operating from a single, low voltage supply. It does not require a separate high voltage supply. Instead, the high voltage is directly generated by a switching converter which is an integral part of the gain stage.

A2's output drives Q3, forcing current into T1. T1's primary is chopped by MOSFET's Q1 and Q2, which receive complementary drive from the 74C04 based square wave oscillator. A1 supplies power to the oscillator. T1 provides voltage step-up. Its rectified and filtered output is the boost stage's output. Its rectified and filtered output is the boost stage's output.

The 1M-10k divider furnishes feedback to A2, closing a loop around it. The 0.01 μ F capacitor from Q3's emitter to A2's negative input gives loop stability and the 0.002 μ F unit trims step response damping. C1 is used for short circuit limiting. Current from Q1 and Q2 passes through the 0.1 Ω shunt. Abnormal output currents cause shunt voltage to rise, tripping C1's output low. This simultaneously removes drive from Q3, Q1 and Q2's gates and the oscillator, resulting in output shutdown. The 1k-1000pF filter ensures that C1 does not trip due to current spikes or noise during normal operation.

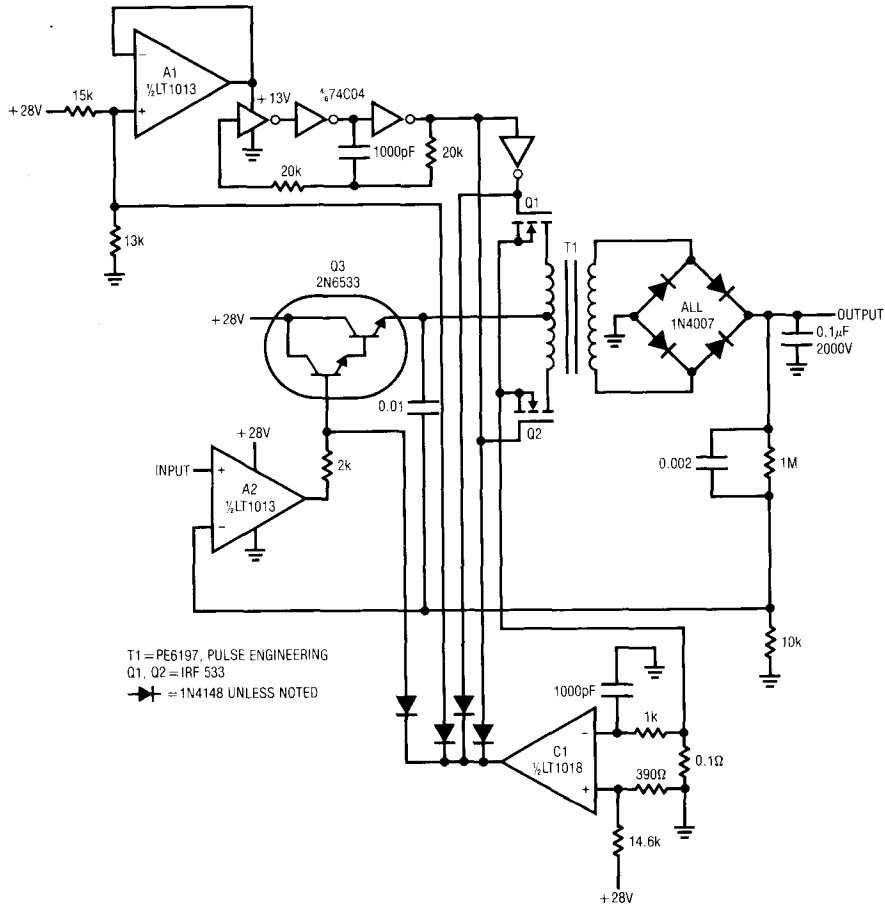


Figure 13. 15 Watt, 1000V Unipolar Output Stage. **DANGER! High Voltages Present. Use Caution.**

Application Note 18

A2 supplies whatever drive is required to close the loop, regardless of the output voltage called for. The low, resistive saturation losses of the VMOS FETs combined with A2's servo action allows controlled outputs all the way down to 0V.

Substituting higher power devices for Q1 and Q2 along with a larger transformer allows more output power, although dissipation in Q3 will become excessive. If higher power is desired, a switched mode stage should be substituted for Q3 to maintain efficiency.

The 0.1 μ F filter capacitor at the output limits full power bandwidth to about 60Hz. Figure 14 shows dynamic response at full load. Trace A, a 10V input, produces a 1000V output in Trace B. Note that slew is faster on the leading edge, because the stage cannot sink current. The falling edge slew rate is determined by the load resistance.

$\pm 15V$ Powered, Bipolar Output, Voltage Gain Stage

Figure 13's output is limited to unipolar operation because the step-up transformer cannot pass DC polarity information.

Obtaining bipolar output from a transformer based voltage booster requires some form of DC polarity restoration at the output. Figure 15's $\pm 15V$ powered circuit does this, using synchronous demodulation to preserve polarity in its $\pm 100V$ output. This booster features 150mA current output, 150Hz full power output and a slew rate of 0.1V/ μ s.

The high voltage output is generated in similar fashion to Figure 13's circuit. The 74C04 based oscillator furnishes complementary gate drive to VMOS devices Q1 and Q2, which chop Q3's output into T1, a step-up transformer. In this design, however, a synchronously switched absolute value amplifier is placed between servo amplifier A1 and Q3's drive point. Input signal polarity information, derived from A1's output, causes C1 to switch the LTC1043 section located at A2's

positive input. This circuitry is arranged so that A2's output is the positive absolute value of A1's input signal. A second, synchronously switched LTC1043 section gates oscillator pulses to the appropriate SCR trigger transformer at the output. For positive inputs LTC1043 pins 2 and 6 are connected, as well as pins 3 and 18. A2, acting as a unity gain follower, passes A1's output directly and drives Q3. Simultaneously, oscillator pulses are conducted through an inverter via LTC1043 pin 18. The inverter drives trigger transformer T2, turning Q4 on. Q4, biased from the full wave bridge's positive point, supplies positive polarity voltage to the output.

Negative inputs cause the LTC1043 switch positions to reverse. A2, functioning as an inverter, again supplies Q3 with positive voltage drive. The Schottky diode at A2 prevents the LTC1043 from seeing transient negative voltages. Oscillator pulses are directed to SCR Q5 via LTC1043 pin 15, its associated inverter and T3. This SCR connects the full wave bridge's negative point to the output. Both SCR cathodes are tied together to form the circuit's output. The 100k-10k divider supplies feedback to A1 in the conventional manner. The synchronous switching allows polarity information to be preserved in the stage's output, permitting full bipolar operation. Figure 16 shows waveforms for a sine wave input. Trace A is A1's input. Traces B and C are Q1 and Q2's drain waveforms. Traces D and E are the full wave bridge's negative and positive outputs, respectively. Trace F, the circuit output, is an amplified, reconstructed version of A1's input. Phase skewing between the SCR switching and the carrier borne signal causes some distortion at the zero crossover. The amount of skew is both load and signal frequency dependent, and is not readily compensated. Figure 17 shows distortion products (Trace B) at a 10Hz output (Trace A) at full load ($\pm 100V$ at 150mA peak). Residual high frequency carrier components are clearly present, and the zero point SCR switching causes the sharp peaks. RMS distortion measured 1% at 10Hz, rising to 6% at 100Hz.

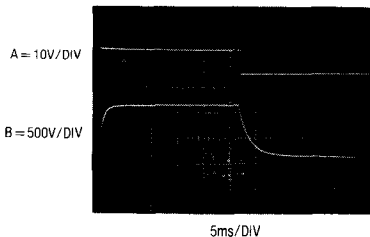


Figure 14. Figure 13's Pulse Response. **DANGER! High Voltages Present. Use Caution.**

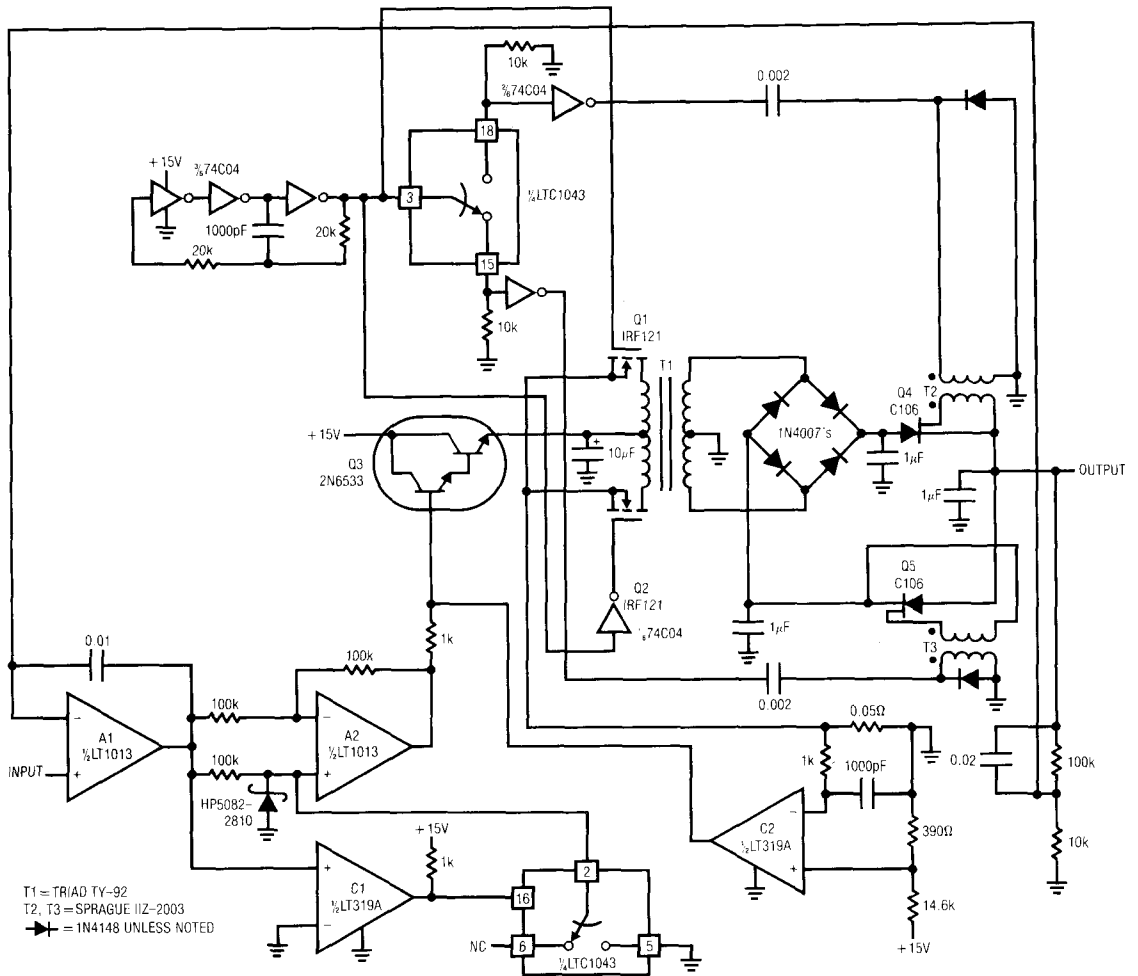


Figure 15. ±100V Output Stage Runs From ±15V Supply. DANGER! High Voltages Present. Use Caution.

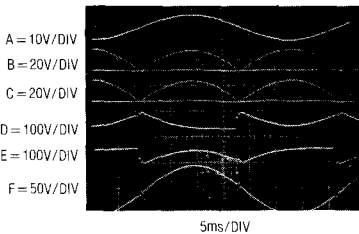


Figure 16. Figure 15's Operating Details. DANGER! High Voltages Present. Use Caution.

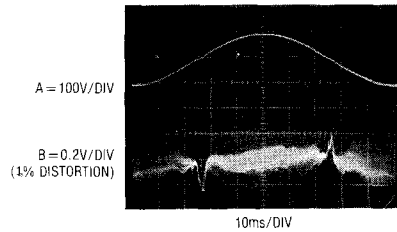


Figure 17. Crossover Residue Reflects Chopping and Zero Cross Switching. DANGER! High Voltages Present. Use Caution.

Application Note 18

C2 supplies current limiting in identical fashion to Figure 13's scheme. Frequency compensation is also similar. A $0.01\mu\text{F}$ capacitor at A1 gives loop stability, while the $0.02\mu\text{F}$ feedback unit sets damping.

Figure 18 summarizes the capabilities of the power gain stages presented, and should be useful in selecting an approach for a given application.

FIGURE	VOLTAGE GAIN	CURRENT GAIN	FULL POWER BANDWIDTH	COMMENTS
1A	No	Yes, 150mA output	600kHz	Simple, easy.
1B	No	Yes, 150mA output	1.5MHz	Simple, easy.
2	No	Yes, 3A	100kHz	
3	No	Yes, 200mA	7.5MHz	Feedforward technique gives high bandwidth > 1000V/ μs slew. Inverting operation only.
5A, 5B	Yes	No	Depends on op amp	Simple stages allow wide swing, almost to rails.
7	Yes	Yes, 125mA	600kHz	High current, nearly rail-to-rail swing capability.
9	Yes, $\pm 120\text{V}$	Yes, 25mA	15kHz	Good, general purpose high voltage stage.
11	Yes, $\pm 120\text{V}$	Yes, 25mA	12kHz	Almost indestructible output.
13	Yes, + 1000V	No	60Hz	High voltage output with no external high voltage supplies required. Limited bandwidth with assymetrical slewing. Positive outputs only.
15	Yes, $\pm 100\text{V}$	Yes, 150mA	150Hz	High voltage outputs with no external high voltage supplies. Limited bandwidth. Full bipolar output.

Figure 18. Summary of Circuit Characteristics

The Oscillation Problem (Frequency Compensation Without Tears)

All feedback systems have the propensity to oscillate. Basic theory tells us that gain and phase shift are required to build an oscillator. Unfortunately, feedback systems, such as operational amplifiers, have gain and phase shift. The close relationship between oscillators and feedback amplifiers requires careful attention when an op amp is designed. In particular, excessive input-to-output phase shift can cause the amplifier to oscillate when feedback is applied. Further, any time delay placed in the amplifier's feedback path introduces additional phase shift, increasing the likelihood of oscillation. This is why feedback loop enclosed power gain stages can cause oscillation.

A large body of complex mathematics is available which describes stability criteria, and can be used to predict stability characteristics of feedback amplifiers. For the most sophisticated applications, this approach is required to achieve optimum performance.

However, little has appeared which discusses, in practical terms, how to understand and address the issues of compensating feedback amplifiers. Specifically, a practical approach to stabilizing amplifier-power gain stage combinations is discussed here, although the considerations can be generalized to other feedback systems.

Oscillation problems in amplifier-power booster stage combinations fall into two broad categories; *local* and *loop* oscillations. *Local* oscillations can occur in the boost stage, but should not appear in the IC op amp, which presumably was debugged prior to sale. These oscillations are due to transistor parasitics, layout and circuit configuration caused instabilities. They are usually relatively high in frequency, typically in the 0.5MHz to 100MHz range. Usually, local booster stage oscillations do not cause loop disruption. The major loop continues to function, but contains artifacts of the local oscillation. Text Figure 7 furnishes an instructive example. The Q3-Q5 and Q4-Q6 pairs have high gain bandwidth. The intended resistive feedback loops allow them to oscillate in the 50-100MHz region without the 100pF-200nF network shunting the DC feedback. This network rolls off gain-bandwidth, preventing oscillation. It is worth noting that a ferrite bead in series with the 2k Ω resistor will give similar results. In this case, the bead raises the inductance of the wire, attenuating high frequencies.

The photo in Figure B1 shows text Figure 7 following a bipolar squarewave input with the local high frequency RC compensation networks removed. The resultant high frequency oscillation is typical of locally caused disturbances. Note that the major loop is functional, but the local oscillation corrupts the waveform.

Eliminating such local oscillations starts with device selection. Avoid high F_T transistors unless they are needed. When high frequency devices are in use, plan layout carefully. In very stubborn cases, it may be necessary to lightly bypass transistor junctions with small capacitors or RC networks. Circuits which use local feedback can sometimes require careful transistor selection and use. For example, transistors operating in a local loop may require different F_T 's to achieve

stability. Emitter followers are notorious sources of oscillation, and should never be directly driven from low impedance sources.

Text Figure 5 uses an RC damper network from the 74C04 inverters to ground to eliminate local oscillations. In that circuit the 74C04's are forced to run in their linear region. Although their DC gain is low, bandwidth is high. Very small parasitic feedback terms result in high frequency oscillations. The damper network provides a low impedance to ground at high frequency, breaking up the unwanted feedback path.

Loop oscillations are caused when the added gain stage supplies enough delay to force substantial phase shift. This causes the control amplifier to run too far out of phase with the gain stage. The control amplifier's gain combined with the added delay causes oscillation. Loop oscillations are usually relatively low in frequency, typically 10Hz-1MHz.

A good way to eliminate loop caused oscillations is to limit the gain-bandwidth of the control amplifier. If the booster stage has higher gain-bandwidth than the control amplifier, its phase delay is easily accommodated in the loop. When control amplifier gain-bandwidth dominates, oscillation is assured. Under these conditions, the control amplifier hopelessly tries to servo a feedback signal which consistently arrives "too late." The servo action takes the form of an electronic tail chase, with oscillation centered around the ideal servo point.

Frequency response roll-off of the control amplifier will almost always cure loop oscillations. In many situations it is preferable to "brute force" compensation using large capacitors in the major feedback loop. As a general rule, it is wise to stabilize the loop by rolling off control amplifier gain-bandwidth. The feedback capacitor serves to trim step response only and should not be relied on to stop outright oscillation.

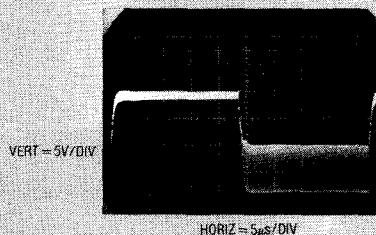


Figure B1. Typical Local Output Stage Oscillation

Application Note 18

Figures B2 and B3 illustrate these issues. The 600kHz gain-bandwidth LT1012 amplifier used with the LT1010 current buffer produces the output shown in Figure B2. The LT1010's 20MHz gain-bandwidth introduces negligible loop delay, and dynamics are clean. In this case, the LT1012's internal roll-off is well below that of the output stage, and stability is achieved with no external compensation components. Figure B3 uses a 15MHz LT318A as the control amplifier. The associated photo shows the results. Here, the control amplifier's roll-off, close to the output stages, causes problems. The phase shift through the LT1010 is now appreciable and oscillations occur. Stabilizing this circuit requires degenerating the LT318A's gain-bandwidth (see text Figure 1).

The fact that the slower op amp circuit doesn't oscillate is a key to understanding how to compensate booster loops. With the slow device, compensation is "free". The faster amplifier makes the AC characteristics of the output stage become significant and requires roll-off components for stability.

Text Figure 9's high voltage stage is an interesting case. The high voltage transistors are very slow devices, and the LT1055 amplifier has a much higher gain-bandwidth than the output stage. The LT1055 is locally compensated by the 10k-100pF network, giving it an integrator-like response. This compensation, combined with the damping provided by the 33pF feedback capacitor, gives good loop response. The procedure used to compensate this circuit is typical of what is done to stabilize boosted amplifier loops and is worth reviewing.

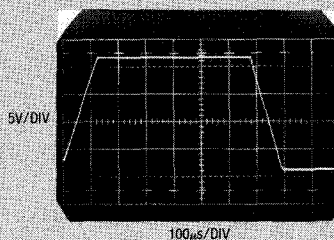


Figure B2. A Slow Control Amplifier Gives "Free" Loop Compensation

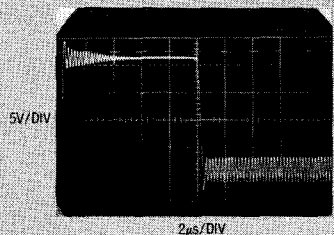
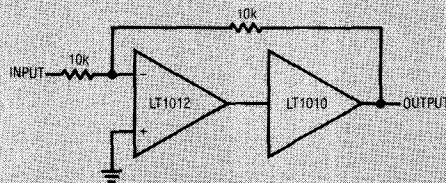
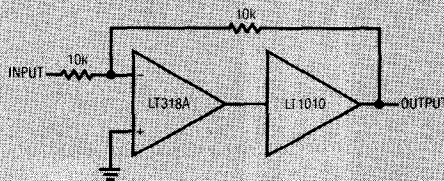


Figure B3. A Fast Control Amplifier Gives "Free" Loop Oscillation



With no compensation components installed, the circuit is turned on and oscillations are observed (photo, Figure B4). The relatively slow oscillation frequency suggests a loop oscillation problem. The LT1055 gain-bandwidth is degenerated with the RC components around the amplifier. The RC time constant is chosen to eliminate oscillations and give the best possible response (photo, Figure B5) with no loop feedback capacitor in place. Observe that the $1\mu\text{s}$ time constant selected offers significant attenuation at the oscillation frequency noted in the photo, Figure B4. Finally, the loop

feedback capacitor (33pF) is selected to give the optimum damping shown in text Figure 10.

When making tests like these, remember to investigate the effects of various loads and output operating voltages. Sometimes a compensation scheme which appears fine gives bad results for some output conditions. For this reason, check the completed circuit over as wide a variety of operating conditions as possible.

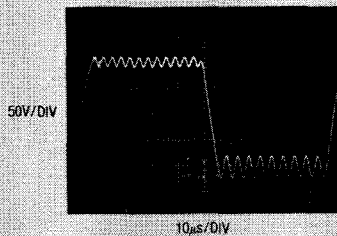


Figure B4. Oscillations After Slewing Suggest a Loop Problem

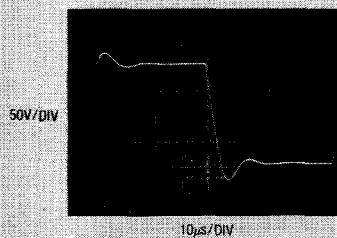


Figure B5. Control Amplifier Roll-Off Stabilizes B4's Problems

Application Note 18

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LT1070 Design Manual

Carl Nelson

INTRODUCTION

Three terminal monolithic linear voltage regulators appeared almost 20 years ago, and were almost immediately successful for a variety of reasons. In particular, there were relatively few engineers capable of designing a good linear voltage regulator. The new devices were also easy to use, and inexpensive. In currently popular parlance they were "expert systems", containing a good deal of their designer's knowledge in silicon form. Because of these advantages, the regulators quickly eclipsed discrete and earlier monolithic building blocks and dominated the market.

More recently, there has been increasing interest in switching-based regulators. Switching regulators, with their high efficiency and small size, are increasingly desirable as overall package sizes have shrunk. Unfortunately, switching regulators are also one of the most difficult linear circuits to design. Mysterious modes, sudden failures, peculiar regulation characteristics and just plain explosions are common occurrences during the design of a switching regulator.

Most switching regulator ICs are building blocks. Many discrete components are required, and substantial expertise is assumed on the part of the user. Some newer devices in-

clude the power switch on the die, but still require a significant amount of engineering to apply. Finally, there has been a notable lack of comprehensive and practical application literature support from manufacturers.

These considerations are reminiscent of the state of linear regulator design when the first three terminal monolithic regulators appeared. Given this historical lesson, the LT1070 five terminal switching regulator has been designed for ease of use and economy. It does not require the user to be well schooled in switching regulator design, and is versatile enough to be used in all the popular switching regulator configurations. To obtain maximum user benefit, a significant applications effort has been associated with this part. This note covers both ancillary tutorial material as well as direct operating considerations for the part. It is intended to be used "as required". For those in a mission-oriented hurry, much of the discussion can be ignored, and breadboards constructed with a high probability of success. The more academically inclined reader may choose to peruse the material more carefully. Either approach is valid, and the note is intended to satisfy both.

— Jim Williams

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PREFACE

Smaller Versions of the LT1070

Since this application note was written, several new versions of the LT1070 have been developed. The LT1071 and LT1072 are identical to the LT1070 except for switch current ratings, 2.5A and 1.25A, respectively. Designs which result in lower switch currents can take advantage of the cost savings of these smaller chips. Design equations for the LT1071 and LT1072 are identical to the LT1070 with the following exceptions:

Peak Switch Current (I_p)	= 5A	LT1070
	= 2.5A	LT1071
	= 1.25A	LT1072
Switch "On" Resistance (R)	$\approx 0.2\Omega$	LT1070
	$\approx 0.4\Omega$	LT1071
	$\approx 0.8\Omega$	LT1072
V_C Pin to Switch Current Transconductance	$\approx 8A/V$	LT1070
	$\approx 4A/V$	LT1071
	$\approx 2A/V$	LT1072

Also available in the 2nd quarter of 1989 will be 100kHz versions of the LT1070/71/72.

Inductance Calculations

Feedback from readers of AN19 shows that there is confusion about the use of ΔI to calculate inductance values. ΔI is the *change* in inductor or primary current during switch "on" time, and the suggested value is approximately 20% of the peak current rating of the LT1070 switch (5A), or in some cases, 20% of the average inductor current. This 20% rule-of-thumb is designed to give near maximum output power for a given switch current rating. If maximum output power is not needed, much smaller inductors/transformers may be used by allowing ΔI to increase. The design approach is to calculate peak inductor/switch current (I_p) using the formulas provided in AN19, with $L = \infty$.

Then compare this current to the peak switch current. The difference is the "room" allowable for ΔI ;

$$\Delta I_{MAX} = 2(I_{SWITCH(PEAK)} - I_p)$$

This formula assumes continuous mode operation. If ΔI , as calculated by this formula, exceeds I_p , it may be possible to go to discontinuous mode operation, with further reductions in inductance. Discontinuous mode requires higher switch currents and not all the AN19 topologies show design equations for this mode, but it should definitely be considered for very low output powers or where inductor/transformer size is critical. All topologies work well in discontinuous mode with the exception of fully isolated flyback. Drawbacks of discontinuous mode include higher output ripple and slightly lower efficiency.

Example 1: Negative buck converter with $V_{IN} = -24V$, $V_{OUT} = -5V$, $I_{OUT} = 1.5A$

$$I_p \text{ (equation 37)} = I_{OUT} + \frac{(V_{IN} - V_{OUT})(V_{OUT})}{2 \cdot V_{IN} \bullet f \bullet (L \approx \infty)} = I_{OUT} = 1.5A$$

$$\begin{aligned} \Delta I_{MAX} &= 2(I_{SW} - I_p) = 2(5 - 1.5) = 7A \text{ (1070)} \\ &= 2(2.5 - 1.5) = 2A \text{ (1071)} \\ &= 2(1.25 - 1.5) = \text{N.A. (1072)} \end{aligned}$$

The LT1072 is too small ($I_p > I_{SW}$), so select the LT1071, which yields a maximum ΔI of 2A. A conservative value of actual ΔI is selected at 1A. This allows room for efficiency losses and variations in component values. Using equation 37:

$$L = \frac{(V_{IN} - V_{OUT})(V_{OUT})}{V_{IN}(\Delta I) \bullet f} = \frac{(24 - 5)(5)}{(24)(1)(40k)} = 99\mu H$$

Example 2: Flyback converter with $V_{IN} = 6V$, $V_{OUT} = \pm 15V @ 35mA$, and $5V @ 0.2A$, $N = 0.4$ (primary to 5V secondary). For calculations, the entire output power of 2.05W is referred to the 5V secondary, yielding one value for $N(0.4)$, $V_{OUT}(5V)$, and $I_{OUT} = 0.41A$.

Using Equation 79:

$$I_P = \frac{I_{OUT}}{E} \left(\frac{V_{OUT}}{V_{IN}} + N \right) + \frac{(V_{IN})(V_{OUT})}{2 \cdot f \cdot (V_{OUT} + N V_{IN}) \cdot (L = \infty)} =$$

$$\frac{0.41A}{0.75} \left(\frac{5V}{6V} + 0.4 \right) = 0.674A$$

The LT1072 is large enough to handle this current, yielding;

$$\Delta I_{MAX} = 2(1.25A - 0.674A) = 1.15A$$

Using a conservative value of 0.7A for ΔI (note that this is 56% of the 1.25A Max LT1072 switch current, not 20%), and equation 77, yields:

$$L = \frac{(V_{IN})(V_{OUT})}{\Delta I \cdot f (V_{OUT} + N V_{IN})} = \frac{(6)(5)}{(0.7)(40k)(5 + 0.4 \cdot 6)} = 145\mu H$$

Protecting the Magnetics

A second problem for LT1070 designers has been protection of the magnetics under overload or short circuit conditions. Physical size restraints often require inductors or transformers which are not specified to handle the full current limit values of the LT1070. This problem can be handled in several ways.

1. Use an LT1071 or LT1072 if full load current requirements allow it.
2. Take advantage of the fact that the LT1070 current limit drops at higher temperatures. The worst-case current limit values shown on the old data sheets allow for both temperature extremes with one specification. New data sheets will specify a maximum of 10A for the LT1070, 5A for the LT1071, and 2.5A for the LT1072 at temperatures of 25°C or higher. Be aware that the temperature dependence of current limit has been improved considerably on the LT1070 since the original data sheet was printed. The old

value was greater than $-0.3\%/^{\circ}C$, while the new figure is under $-0.1\%/^{\circ}C$. The current limit graphs on the new data sheets reflect this improved characteristic.

3. Reconsider the necessity of limiting the inductor/transformer current to the manufacturers' specification. Maximum current ratings in many cases are determined by core saturation considerations. Allowing the core to saturate does *not* harm the core. Core or winding damage occurs only if temperatures rise so far that material properties are permanently altered. Core saturation used to be considered a "fatal" condition for conventional switches or diodes. The LT1070 limits current on an instantaneous cycle-by-cycle basis, preventing current "run away" even with grossly overdriven cores. The major consideration then is the heating effect of the winding current ($I^2 R$). Under short circuit conditions, winding currents in inductors are nearly constant at the current limit value of the LT1070. Transformer *secondary* winding currents are nearly constant at $1/N$ times the LT1070 current limit. This assumes that the core is not heavily saturated. If the core saturates significantly below the current limit values, RMS winding current will be significantly *lower* than the current limit. The best way to resolve this complex situation is to actually measure core/winding temperature with a thermocouple under overload conditions. The thermocouple should be "buried" as deeply as possible in the windings and/or core to reflect peak temperatures. The magnetic and electric fields generated by the switching may affect the thermocouple meter. If this occurs, simply check the temperature periodically by turning off power. Consult with the magnetics manufacturer to determine peak allowable temperatures, with permanent damage as the criteria, not performance specifications. The major failure mode is winding shorts caused by insulation melting. High temperature insulation is available from most manufacturers.

New Switch Current Specification

The LT1070 was specified at 5A peak switch current, for duty cycles of 50% or less. At higher duty cycles the peak current was limited to 4A. This abrupt change in specification at 50% duty cycle was bothersome because many designs operate near 50% duty cycle and require maximum possible output power. To solve this problem, switch current limit on new data sheets will be specified as a linearly decreasing function, from 5A at 50% duty cycle to 4A at 80% duty cycle. The LT1071 and LT1072 will also be specified this way.

High Supply Voltages

It has become apparent that many applications for the LT1070 have maximum input voltages which exceed 40V. The straightforward approach is to use the "HV" devices which are specified at 60V, but in some cases the standard part can be used at lower cost simply by dropping supply voltage with a zener diode as shown. The LT1070 supply pin (V_{IN}) requires only a few volts to operate, so in most cases the unregulated input voltage range is not compromised with this zener. Zener dissipation can be calculated from $I_Z \approx 6\text{mA} + I_{SW} (0.0015 + DC/40)$:

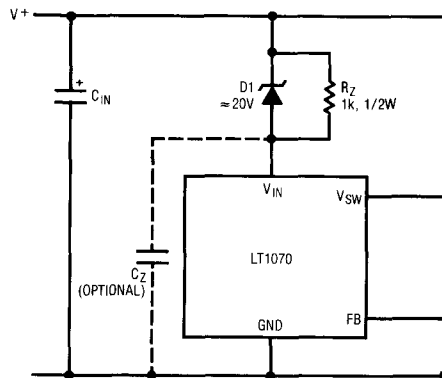
I_{SW} = LT1070 average switch current during "on" time
 DC = duty cycle

For $I_{SW} = 4\text{A}$, $DC = 30\%$; $I_Z = 42\text{mA}$.

A 20V zener would dissipate $(20)(42) = 0.84\text{W}$. Note that this power would be dissipated anyway in the LT1070, so no loss in efficiency occurs. The resistor, R_Z , is necessary for startup. Without it, a latch-off condition exists where the V_{IN} pin sits more than 16V negative with respect to the switch pin. If the LT1070 is not switching and the FB pin is below 0.5V, the LT1070 is in the "isolated flyback" mode where it is trying to regulate the V_{IN} to V_{SW} voltage. When this voltage exceeds 16V, the regulator thinks it should reduce duty cycle to zero, resulting in a permanent "no-switching" state. R_Z forces the V_{IN} pin to rise enough to initiate startup. The user need not be concerned that

the V_{IN} to ground pin voltage exceeds 40V during this state because R_Z is too large to allow harmful currents to flow.

Some attention needs to be paid to C_Z . The LT1070 is very tolerant of noise and ripple on the V_{IN} pin, but C_Z may be necessary in some applications. The problem is that D1 must charge C_Z when power is applied. If power comes up very rapidly, D1 might exceed its one cycle surge rating.



Discontinuous "Oscillations" (Ringing)

Many customers have called about oscillations occurring on the switch pin during a portion of the switch "off" time. These are not oscillations. They are a damped ringing caused by the transition to a zero-current state in the inductor or transformer primary. At light loads, or with low inductance values, inductor current will drop to zero during switch off time. This causes the inductor voltage to collapse toward zero. In doing so, however, energy is transferred back to the inductor from the parasitic capacitance of the switch, inductor, and catch diode. The inductor and capacitance form a parallel resonant tank which "rings." This ringing is not harmful as long as its peak amplitude does not result in a negative voltage on the switch pin. It can be damped, if desired, by paralleling the inductor/primary with a series R/C damper, typically $100\Omega - 1\text{k}\Omega$, and $50\text{pF} - 500\text{pF}$. Typical undamped ringing frequency is $100\text{kHz} - 1\text{MHz}$.

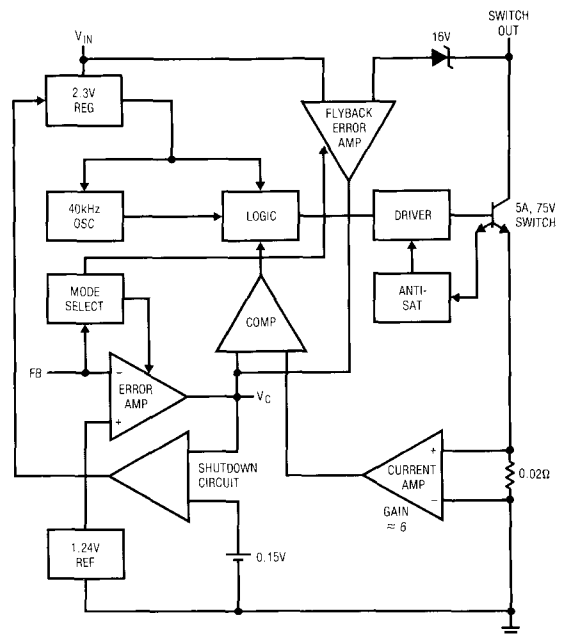
LT1070 OPERATION

The LT1070 is a current mode switcher. This means that switch duty cycle is directly controlled by switch current rather than by output voltage. Referring to the block diagram, the switch is turned "on" at the start of each oscillator cycle. It is turned "off" when switch current reaches a predetermined level. Control of output voltage is obtained by using the output of a voltage sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike ordinary switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at mid-frequencies in the energy storage inductor. This greatly simplifies closed loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short conditions. A low-dropout internal regulator provides a 2.3V supply for all internal circuitry on the LT1070. This low-dropout design allows input voltage to vary from 3V to 60V with virtually no change in device performance. A 40kHz oscillator is the basic clock for all internal timing. It turns "on" the output switch via the logic and driver circuitry. Special adaptive anti-sat circuitry detects onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

A 1.2V bandgap reference biases the positive input of the error amplifier. The negative input is brought out for output voltage sensing. This feedback pin has a second function; when pulled low with an external resistor, it programs the LT1070 to disconnect the main error amplifier output and connects the output of the flyback amplifier to the comparator input. The LT1070 will then regulate the value of the flyback pulse with respect to the supply voltage. This flyback pulse is directly proportional to output voltage in the traditional transformer coupled flyback topology regulator. By regulating the amplitude of the flyback pulse, the output voltage can be regulated with no direct connection between input and output. The output is fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings. A special delay network inside the LT1070 ignores the leakage inductance spike at the leading edge of the flyback pulse to improve output regulation.

The error signal developed at the comparator input is brought out externally. This pin (V_C) has four different functions. It is used for frequency compensation, current limit adjustment, soft starting, and total regulator shutdown. During normal regulator operation this pin sits at a voltage between 0.9V (low output current) and 2.0V (high output current). The error amplifiers are current output (gm) types, so this voltage can be externally clamped for adjusting current limit. Likewise, a capacitor coupled external clamp will provide soft start. Switch duty cycle goes to zero if the V_C pin is pulled to ground through a diode, placing the LT1070 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown, with only 50 μ A supply current for shutdown circuitry biasing.

Block Diagram



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PIN FUNCTIONS

Input Supply (V_{IN})

The LT1070 is designed to operate with input voltages from 3V to 40V (standard) or 60V (HV units). Supply current is essentially flat over this range at about 6mA (with zero output current). With increasing switch current, the supply current (during switch on-time) increases at a rate approximately 1/40 of switch current, corresponding to a forced h_{FE} of 40 for the switch.

Undervoltage lockout is incorporated on the LT1070 by sensing saturation of the lateral PNP pass transistor which drives an internal 2.3V regulator. A remote collector on this transistor conducts current and locks out the switch for input voltages below 2.5V. No hysteresis is used to maximize the useful range of input voltage. Operating the regulator right at the 2.5V threshold may result in a "burping" action as the LT1070 turns on and off in response to wobbles in input voltage, but this will not harm the device. External undervoltage lockout can be added if it is desirable to raise the threshold voltage. The circuit shown in Figure 1 is one example of how to implement this.

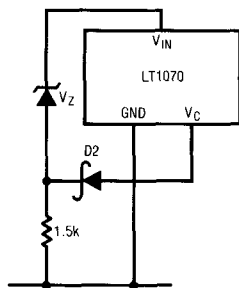


Figure 1. External Undervoltage Lockout

The threshold of this circuit is approximately $V_Z + 1.5V$. Below that voltage, D2 pulls the V_C pin low to shut off the regulator.

Ground Pin

The ground pin (case) of the LT1070 is important because it acts as both the negative sense point for the internal error amplifier and as the high current path for the 5A switch. This is not normally good design practice, but was necessary in a 5-pin package configuration. To avoid degradation of load regulation, Kelvin connections should be made to the ground pin. This is done on the TO-3 package by tying one end of the package to power ground and the other end to the feedback divider resistor (analog ground). This is illustrated in Figure 2.

For best load regulation, the resistance in the switch current path must be kept low. 0.01 Ω of wire resistance creates 50mV drop at 5A switch current. This is a 1% change in a 5V output, and actually causes the output to increase with increasing load current.

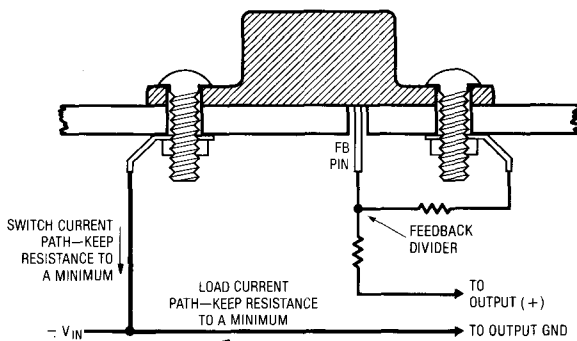


Figure 2

With the TO-220 package, (Figure 3) connect the feedback resistor directly to the ground pin with a separate wire if no case connection is made. The case can be used as a second ground pin if desired.

Avoid long wire runs to the ground pin to minimize load regulation effects and inductive voltages created by the high di/dt switch current. A ground plane will keep EMI to a minimum.

Feedback Pin

The feedback pin is the inverting input to a single stage error amplifier. The non-inverting input to this amplifier is internally tied to a 1.244V reference as shown in Figure 4.

Input bias current of the amplifier is typically 350nA with the output of the amplifier in its linear region. The amplifier is a

gm type, meaning that it has high output impedance with controlled voltage-to-current gain ($g_m \approx 4400 \mu\text{mhos}$). DC voltage gain with no load is ≈ 800 .

The feedback pin has a second function; it is used to program the LT1070 for normal or flyback-regulated operation (see description of block diagram). In Figure 4, Q53 is biased with a base voltage of approximately 1V. This clamps the feedback pin to about 0.4V when current is drawn out of the pin. A current of $\approx 10 \mu\text{A}$ or higher through Q53 forces the regulator to switch from normal operation to flyback mode, but this threshold current can vary from $3 \mu\text{A}$ to $30 \mu\text{A}$. *The LT1070 is in flyback mode during normal startup until the feedback pin rises above 0.45V.* The resistor divider used to set output voltage will draw current out of the feedback pin until the output voltage is up to about 33% of its regulated value.

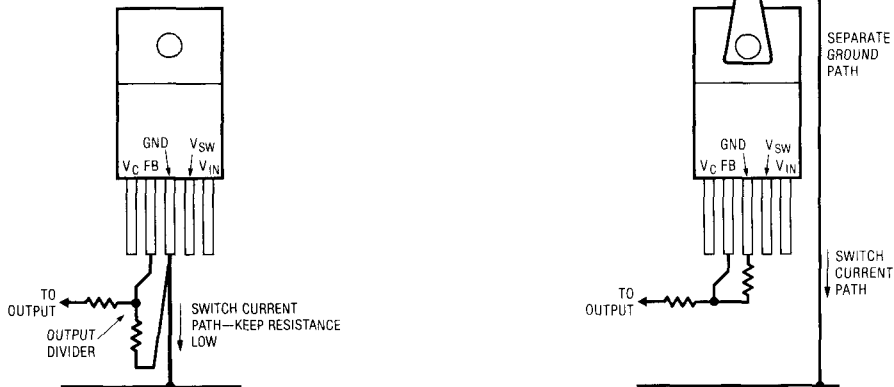


Figure 3

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If it is desired to run the LT1070 in the *fully isolated* flyback mode, a single resistor is tied from the feedback pin to ground. The feedback pin then sits at a voltage of $\approx 0.4V$ for $R = 8.2k\Omega$. The actual voltage depends on resistor value since the feedback pin has about 200Ω output impedance in this mode. $500\mu A$ in the resistor will drop the feedback pin voltage from $0.4V$ to $0.3V$. Minimum current through the resistor to guarantee flyback operation is $50\mu A$. Actual resistor value is chosen to fine-trim flyback regulated voltage. (See discussion of isolated flyback mode operation and graphs of feedback pin characteristics.)

An internal 30Ω resistor and $5.6V$ zener protect the feedback pin from overvoltage stress. Maximum transient voltage is $\pm 15V$. This high transient condition most commonly occurs during fast fall time output shorts if a feedforward capacitor is used around the feedback divider. If a feedforward capacitor is used for DC output voltages greater than $15V$, a resistor equal to $V_{OUT}/20mA$ should be used between the divider node and the feedback pin as shown in Figure 5.

Keep in mind when using the LT1070 that the feedback pin reference voltage is referred to the ground pin of the regulator, and the ground pin can have switch currents exceeding $5A$. Any resistance in the ground pin connection will degrade load regulation. Best regulation is obtained by tying the grounded end of the feedback divider directly to the ground pin of the LT1070, as a separate connection from the power ground. This limits output voltage errors to just the drop across the ground pin resistance instead of multiplying it by the feedback divider ratio. See discussion of ground pin.

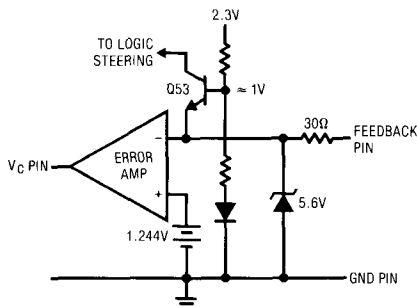


Figure 4

Compensation Pin (V_C)

The V_C pin is used for frequency compensation, current limiting, soft start, and shutdown. It is the output of the error amplifier and the input of the current comparator. The error amplifier circuit is shown in Figure 6.

Q57 and Q58 form a differential input stage whose collector currents are inverted and multiplied times four by Q55 and Q56. Q55 current is further inverted by Q60 and Q61 to generate a current fed balanced output which can swing from the $2.3V$ rail down to a clamp level of $\approx 0.4V$ as set by R21 and Q62. The $60\mu A$ tail current of the input transistors sets the g_m of the error amplifier at $4400\mu mhos$. Voltage gain with no load is limited by transistor output impedance at ≈ 800 . Maximum source and sink current is $\approx 220\mu A$.

The voltage on the V_C pin determines the current level at which the output switch will turn off. For V_C voltage below $0.9V$ ($@25^\circ C$), the output switch will be totally off (duty cycle = 0). Above $0.9V$, the switch will turn on at each oscillator cycle, then turn off when switch current reaches a trip level set by V_C voltage. This trip level is zero at $V_C = 0.9V$, and increases to about $9A$ when V_C reaches its upper clamp level of $2V$. These numbers are based on a duty cycle of 10%. Above 10%, switch turn-off is a function of both switch current *and* time. The time dependence is caused by a small ramp fed into the current amplifier input. This ramp starts at $\approx 40\%$ duty cycle, and is the source of the bend in the V_C vs duty cycle graph shown in Figure 7. This ramp is used to prevent a phenomenon peculiar to "current mode" switching regulators known as *subharmonic oscillation*. See section on Subharmonic Oscillations for further details.

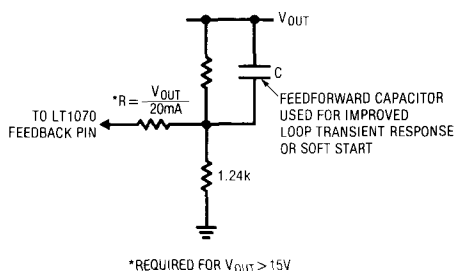


Figure 5

A second amplifier output is also tied to the V_C pin. This "flyback mode" amplifier is turned on only when current is drawn out of the feedback pin. This condition occurs during startup in the normal mode until the feedback divider has raised the voltage at the feedback pin above 0.45V. It is a permanent condition when the LT1070 is programmed for isolated flyback mode by tying a single resistor from the feedback pin to ground.

In the isolated flyback mode, S1 is closed and the feedback pin is low, totally disabling the main amplifier. S2 and S3 are turned on only during the "off" state of the output power transistor and then, only after a 1.5 μ s delay following output transistor turn-off. This prevents transient flyback spikes from causing poor regulation. S2 current is fixed at 30 μ A. S3 current can rise to a maximum of \approx 70 μ A, allowing the V_C pin to source 30 μ A and sink 40 μ A in the flyback mode. gm of the flyback amplifier is typically 300 μ mho.

When the V_C pin is externally pulled below 0.15V, a shutdown circuit is activated. Q24 and Q18 perform this function. Q24 is a special "high V_{BE} " diode whose forward voltage is about 150mV higher than Q18 V_{BE} . Pulling current out of Q18 activates shutdown and turns off all internal regulator functions except for a 50 μ A–100 μ A trickle current needed to bias Q18 and Q24. See characteristic curves for details of the VI properties of the V_C pin in shutdown.

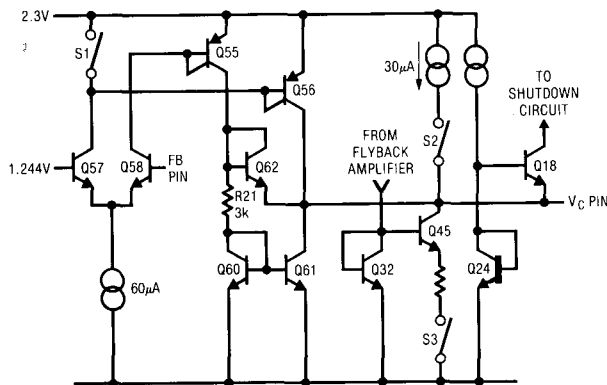


Figure 6. Error Amplifier

Loop frequency compensation can be performed with an RC network connected from the V_C pin to ground. An optional compensation is to connect the RC network between the V_C pin and the feedback pin. See Loop Frequency Compensation section.

Output Pin

The V_{SW} pin of the LT1070 is the collector of the internal NPN power switch. This NPN has a typical on resistance of 0.15 Ω and a breakdown voltage (BV_{CBO}) of 85V. Very fast switching times and high efficiency are obtained by using a special driver loop which automatically adapts base drive current to the minimum required to keep the switch in a quasi-saturation state. This loop is shown in Figure 8.

Q104 is the power switch. Its base is driven by Q101, whose collector is returned to V_{IN} . Q101 is turned on and off by Q102. In parallel with Q102 is a second, larger transistor (Q103) which pulls high reverse base current out of Q104 for rapid switch turn-off. The key element in the loop is the extra emitter on Q104. This emitter carries no current when Q104 collector is high (unsaturated). In this condition, the driver, Q101, can deliver very high base drive to the switch for fast turn-on. When the switch saturates, the extra emitter acts as a collector and pulls base current away from the driver. This linear feedback loop serves itself to keep the switch just at the

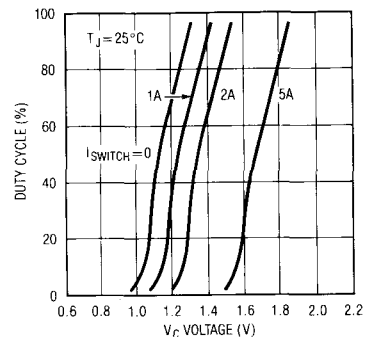


Figure 7. Duty Cycle vs V_C Voltage

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edge of saturation. Very low switch currents result in near-zero driver current, and high switch currents automatically increase driver current as necessary. The ratio of switch current to driver current is approximately 40:1. This ratio is determined by the sizing of the extra emitter and the value of I_1 . The quasi-saturation state of the switch permits rapid turn-off without the need for reverse base-emitter voltage drive.

Also tied to the V_{SW} pin is the input circuitry for the flyback mode error amplifier as shown in Figure 9. This circuitry draws no current from the V_{SW} pin when the switch pin is less than 16V above V_{IN} because the diodes block current. When V_{SW} is more than 16V above V_{IN} , $\approx 500\mu\text{A}$ is drawn out of the switch pin because the reference diodes (D1 and D2) and Q10 turn on. This $500\mu\text{A}$ current level is set by the ratio of collector areas on the two-collector lateral PNP Q10 and the value of I_2 . Q9 is reverse biased in this state. The 16V transition point sets the flyback mode reference voltage. The flyback reference voltage can be increased above 16V by drawing additional current through R1 via Q52. The amplitude of this current is determined by the size of the resistor tied to the feedback pin. See discussion of Isolated Flyback Mode Operation.

BASIC SWITCHING REGULATOR TOPOLOGIES

There are many possible switching regulator configurations, or "topologies". In any particular regulator requirement, the

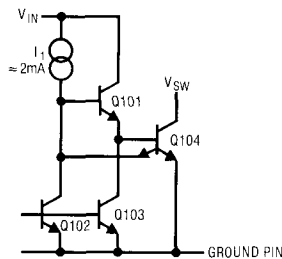


Figure 8

possible choices are narrowed somewhat by constraints of polarity, voltage ratio, and fault conditions (simple boost regulators cannot be current limited), but this may still leave the designer with several choices. To convert +28V to +5V, for instance, the list of possible topologies includes buck, flyback, forward and current boosted buck. The following discussion of topologies is limited to those which can be realized with the LT1070, but this covers nearly all the low to medium power DC-to-DC conversion requirements.

Buck Converter

Figure 10a shows the basic buck topology. S1 and S2 open and close alternately so that the voltage applied to L1 is either V_{IN} or zero. DC output voltage is then the average voltage applied to L1. If T_1 is the time S1 is closed, and T_2 is the time it is open, V_{OUT} is equal to:

$$V_{OUT} = V_{IN} \cdot \frac{T_1}{T_1 + T_2} = V_{IN} \cdot DC \quad (1)$$

where, by convention, duty cycle (DC) is defined as the ratio of T_1 to $T_1 + T_2$;

$$DC = T_1 / (T_1 + T_2) \quad (2)$$

Note that the definition of duty cycle allows only for values between 0 and 1. The formula for V_{OUT} therefore shows a basic property of buck converters; the *output voltage is always less than the input voltage*.

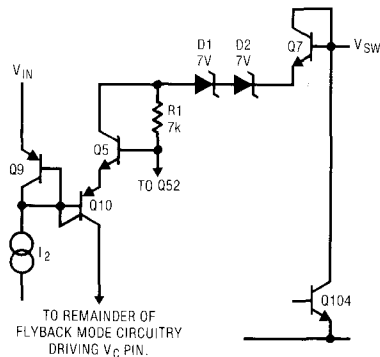


Figure 9

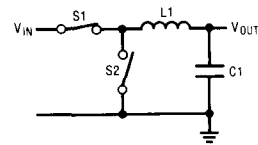
This simple formula also tells much about switching regulators in general. The most important point is what is *not* in the equation, and that includes L1, C1, frequency, and load current. To a first approximation, the output voltage of a switching regulator depends only on the duty cycle of the switching network, and input voltage. This is a very important point which must be kept firmly in mind when analyzing switching regulators.

Diodes may be used to replace switches when unidirectional current flow exists. In Figures 10b and 10c, single-switch buck regulators are shown with diodes used to replace S2. Diodes cause some loss in efficiency, but simplify the design, and reduce cost. Notice that when S1 is closed, D1 is reverse biased (off) and that when S1 opens, the current flow through L1 forces the diode to become forward biased (on). This duplicates the alternate switching action of two switches. There is an exception to this condition, however. If the load current is low enough, the current through L1 will drop to zero sometime during S1 off time. This is known as *discontinuous mode operation*. Buck regulators will be in discontinuous mode for any load current less than;

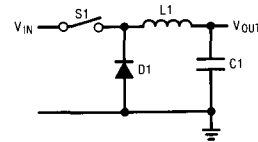
$$I_{OUT} \leq \frac{V_{OUT}}{2 \cdot f \cdot L1} \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad f = \text{switching frequency} \quad (3)$$

Discontinuous mode alters the original statement that output voltage depends only on input voltage and switch duty cycle because a third state of the switches now exists with diodes replacing S2; namely both switches off. Waveforms for voltage and current of S1, D1, L1, C1, and the input source are shown for both continuous and discontinuous modes of operation.

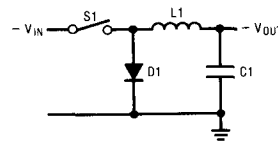
Normally it is *not* important to avoid discontinuous mode operation at light load currents. A possible exception to this would be when the "on" time of S1 cannot be reduced to a low enough value to prevent the lightly loaded output from drifting unregulated high. If this occurs, most switching regulators will begin "dropping cycles" wherein S1 does not turn on at all for one or more cycles. This mode of operation maintains control of the output, but the subharmonic frequencies generated may be unacceptable in certain situations.



a. Basic Topology



b. Positive Buck Using One Switch



c. Negative Buck Using One Switch

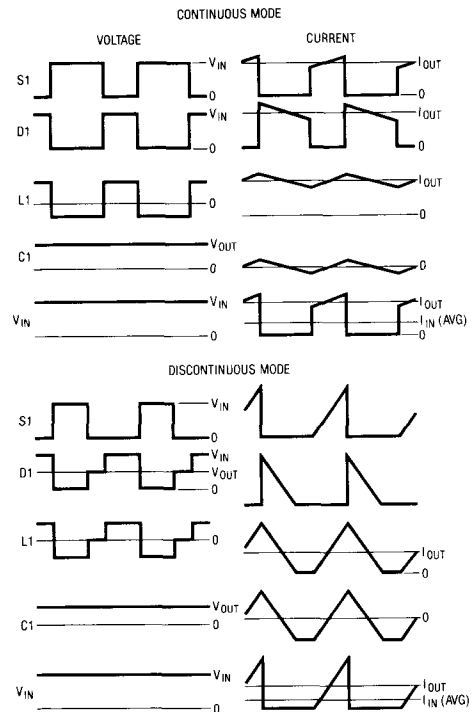


Figure 10. Buck Converter

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A general property of "perfect" switching regulators is that they do not dissipate power in the process of converting one voltage or current to another; in other words, they are 100% efficient. This is to be expected from an inspection of Figure 10a: *there are no components which dissipate power*; only switches, inductors and capacitors. The following formula can then be stated;

$$P_{OUT} = P_{IN} \text{ or, } (I_{OUT})(V_{OUT}) = (I_{IN})(V_{IN}) \quad (4)$$

$$\text{and} \\ I_{IN} = I_{OUT} \left(\frac{V_{OUT}}{V_{IN}} \right) \quad (5)$$

This shows that *the average current drawn by the input of a switching regulator can be much higher or lower than the load current*, depending on the ratio of output to input voltage. If this simple fact is ignored, the designer may realize too late that his low voltage to high voltage converter will draw more current from the low voltage supply than it is capable of handling.

Boost Regulators

The basic boost regulator shown in Figure 11a has an output voltage given by;

$$V_{OUT} = \frac{V_{IN}}{1 - DC} \text{ (continuous mode)} \quad (6)$$

DC is duty cycle, the ratio of S1 "on" time to "off" time, assuming that S1 and S2 open and close alternately. Duty cycle can take on values only between 0 and 1; therefore, *the output voltage of a boost regulator is always higher than the input voltage*.

In Figure 11b, a diode has replaced S2 to realize a boost regulator with a single switch. The voltage and current waveforms for all the components including the source are shown, both for continuous and discontinuous mode. Note that the current drawn from the input and delivered in pulses to the load is significantly higher than the output load current. The amplitude of input current and peak switch and diode current is equal to;

$$I_P = I_{OUT} \cdot \frac{V_{OUT}}{V_{IN}} \text{ (continuous mode)} \quad (7)$$

Average diode current is equal to I_{OUT} and average switch current is $I_{OUT} \cdot (V_{OUT} - V_{IN})/V_{IN}$, both of which are significantly less than peak current. The switch, diode, and output capacitor must be specified to handle the peak currents as well as average currents. Discontinuous mode requires even higher ratios of switch current to output current.

One drawback of boost regulators is that they cannot be current limited for output shorts because the current steering diode, D1, makes a direct connection between input and output.

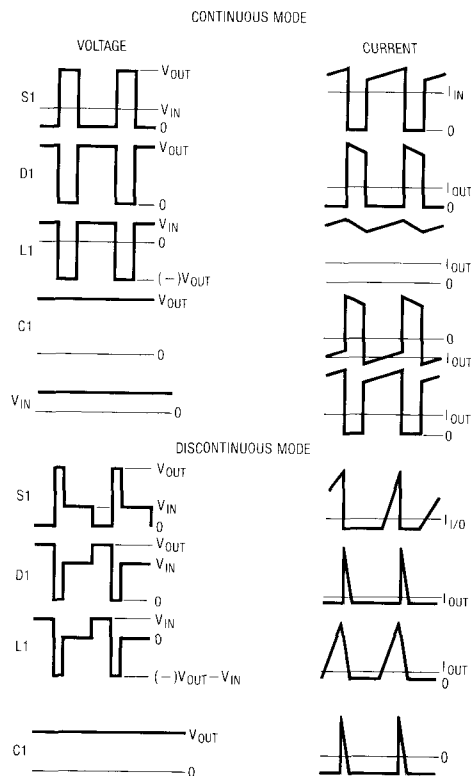
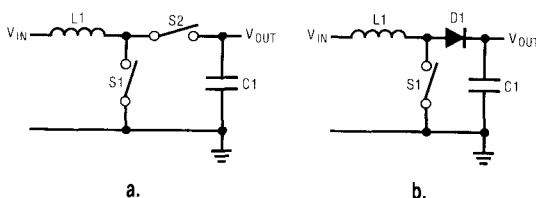


Figure 11. Boost Regulators

Combined Buck-Boost Regulator

Buck-boost regulators (Figure 12) are used to generate an output with the reverse polarity of the input. They look similar to a boost regulator except that the load is referred to the inductor side of the input instead of the switch side. Buck-boost regulators have an output voltage given by;

$$V_{OUT} = -V_{IN} \left(\frac{DC}{1 - DC} \right) \quad (8)$$

With duty cycle varying between 0 and 1, the output voltage can vary between zero and an infinitely high value. The current and voltage waveforms show that, like boost regulators, the peak switch, diode, and output capacitor currents can be significantly higher than output current and these components must be sized accordingly.

$$I_{PEAK} = \frac{I_{OUT}}{1 - DC} = I_{OUT} \frac{(V_{OUT} + V_{IN})}{V_{IN}} \text{ (continuous mode)} \quad (9)$$

Maximum switch voltage is equal to the sum of input plus output voltage. The forward turn-on time of D1 is therefore very important in higher voltage applications to prevent additional switch stress.

'Cuk Converter

The 'Cuk converter in Figure 13 is named after Slobodan 'Cuk, a professor at Cal Tech. It is like a buck-boost converter in that input and output polarities are reversed, but it has the

advantage of low ripple current at both input and output. The optimum topology version of the 'Cuk converter eliminates the disadvantage of needing two inductors by winding them both on the same core, with exact 1:1 turns ratio. With slight adjustments to L1 or L2, *either* input ripple current *or* output ripple current can be forced to zero. An improved version even exists which results in *both* ripple currents going to zero. This considerably eases the requirements on size and quality of input and output capacitors without requiring filters.

The switch must handle the *sum* of input and output current;

$$I_{PEAK}(S1) = I_{IN} + I_{OUT} = I_{OUT} \left(1 + \frac{V_{OUT}}{V_{IN}} \right) \quad (10)$$

The ripple current in C2 is equal to I_{OUT} , so this capacitor must be large. It can be electrolytic, however, so physical size is not normally a problem.

Flyback Regulator

Flyback regulators (Figure 14) use a transformer to transfer energy from input to output. During S1 "on" time, energy builds up in the core due to increasing current in the primary winding. At this time, the polarity of the output winding is such that D1 is reverse biased. When S1 opens, the total stored energy is transferred to the secondary winding and current is delivered to the load. The turns ratio (N) of the transformer can be adjusted for optimum power transfer from input to output.

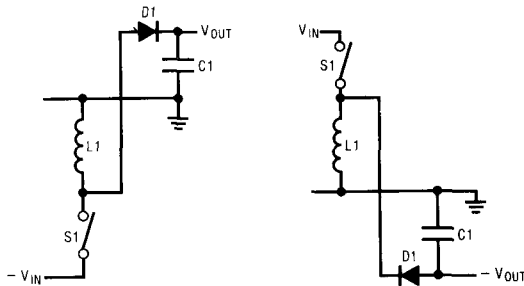


Figure 12. Inverting Topology

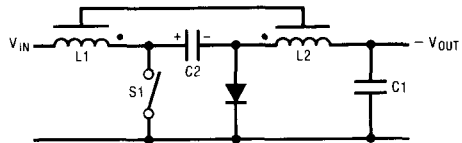


Figure 13. 'Cuk Converter

Application Note 19

Peak switch current in a flyback regulator is equal to;

$$I_{PEAK}(S1) = \frac{I_{OUT}(N V_{IN} + V_{OUT})}{V_{IN}} \text{ (continuous mode)}$$

Notice that peak switch current can be reduced to a minimum by using a very small value for N. This has two negative consequences however; the switch voltage and diode current become very large during switch off time. For a given maximum switch voltage, optimum power transfer occurs at $V_{IN} = 1/2 V_{MAX}$.

Both input ripple current *and* output ripple current are high in a flyback regulator, but this disadvantage is more than offset in many cases by the ability to achieve current or voltage gain and the inherent isolation afforded by the transformer. Output voltage is given by;

$$V_{OUT} = V_{IN} \cdot N \cdot \frac{DC}{1 - DC} \quad (11)$$

With any value of N, a duty cycle between 0 and 1 can be found which generates the required output. *Flyback regulators can have an output voltage which is higher or lower than the input voltage.*

A disadvantage of flyback regulators is the high energy which must be stored in the transformer in the form of DC current in the windings. This requires larger cores than would be necessary with pure AC in the windings.

Forward Converter

A forward converter (Figure 15) avoids the problem of large stored energy in the transformer core. It does this, however, at the expense of an extra winding on the transformer, two more diodes, and an additional output filter inductor. Power

is transferred from input to the load through D1 during switch "on" time. When the switch turns "off", D1 reverse biases and L1 current flows through D2. Output voltage is equal to;

$$V_{OUT} = V_{IN} \cdot N \cdot DC \quad (12)$$

The additional winding and D3 are required to define switch voltage during switch "off" time. Without this clamp, switch voltage would jump all the way to breakdown at the moment the switch is opened due to the magnetizing current flowing in the primary. This "reset" winding normally has a 1:1 turns ratio to the primary which limits switch duty cycle to 50% maximum. Above this duty cycle, switch current rises uncontrolled even with no load because the primary winding cannot maintain zero DC voltage. Reducing the number of turns on the reset winding will allow higher switch duty cycles at the expense of higher switch voltage.

Output voltage ripple of forward converters tends to be low because of L1, but input ripple current is high due to the low duty cycles normally used. A smaller core can be used for T1 compared to flyback regulators because there is no net DC current to saturate the core.

Current Boosted Boost Converter

This topology in Figure 16 is an extension of the standard boost converter. A tapped inductor is used to decrease the switch current for a given load current. This allows higher load currents at the expense of higher switch voltage. The increase in maximum output power over a standard boost converter is equal to;

$$\frac{P_{OUT}}{P_{BOOST}} = \frac{(N + 1)(V_{OUT})}{N(V_{OUT} - V_{IN}) + V_{OUT}} \quad (13)$$

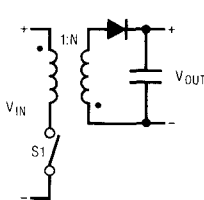


Figure 14. Flyback Converter

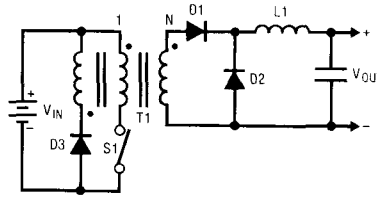


Figure 15. Forward Converter

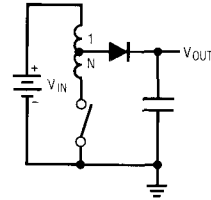


Figure 16. Current Boosted Boost Converter

Analysis of this equation shows that significant increases in power are possible when the input-output differential is low. Care must be used, however, to ensure that maximum switch voltage is not exceeded.

Current Boosted Buck Converter

The current boosted buck converter in Figure 17 uses a transformer to increase output current above the maximum current rating of the switch. It accomplishes this at the expense of increased switch voltage during switch "off" time. The increase in maximum output current over a standard buck converter is equal to:

$$\frac{I_{OUT}}{I_{BUCK}} = \frac{V_{IN}}{V_{OUT} + N(V_{IN} - V_{OUT})} \quad (16)$$

In a 15V to 5V converter, for instance, with $N = 1/4$,

$$\frac{I_{OUT}}{I_{BUCK}} = \frac{15}{5 + 1/4(15 - 5)} = 2$$

This is a 100% increase in output current.

Maximum switch voltage for a *current boosted* buck converter is increased from V_{IN} to:

$$V_{SWITCH} = V_{IN} + V_{OUT}/N \quad (17)$$

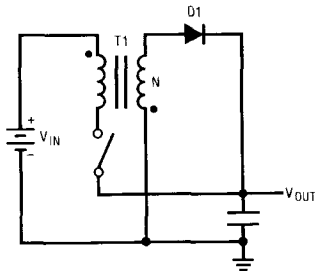


Figure 17. Current Boosted Buck Converter

APPLICATION CIRCUITS

BOOST MODE (output voltage higher than input)

The LT1070 will operate in the boost mode with input voltages as low as 3V and output voltages over 50V. Figure 18 shows the basic boost configuration for positive voltages. This circuit is capable of output power levels that depend mainly on input voltage.

$$P_{OUT(MAX)} \approx V_{IN} \cdot I_P \left[1 - I_P \cdot R \left(\frac{1}{V_{IN}} - \frac{1}{V_{OUT}} \right) \right] \quad (17)$$

- *This formula assumes that $L1 \rightarrow \infty$
- I_P = maximum switch current
- R = switch "on" resistance

With $V_{IN} = 5V$, $V_{OUT} = 12V$, $I_P = 5A$, $R = 0.2\Omega$:

$$P_{OUT(MAX)} = 5 \cdot 5 \left[1 - 5(0.2) \left(\frac{1}{5} - \frac{1}{12} \right) \right] = 22W$$

With higher input voltages, output power levels can exceed 100W. Power loss internal to the LT1070 in a boost regulator is approximately equal to:

$$P_{IC} \approx (I_{OUT})^2 \cdot R \left[\left(\frac{V_{OUT}}{V_{IN}} \right)^2 - \frac{V_{OUT}}{V_{IN}} \right] + \frac{I_{OUT}(V_{OUT} - V_{IN})}{40} \quad (18)$$

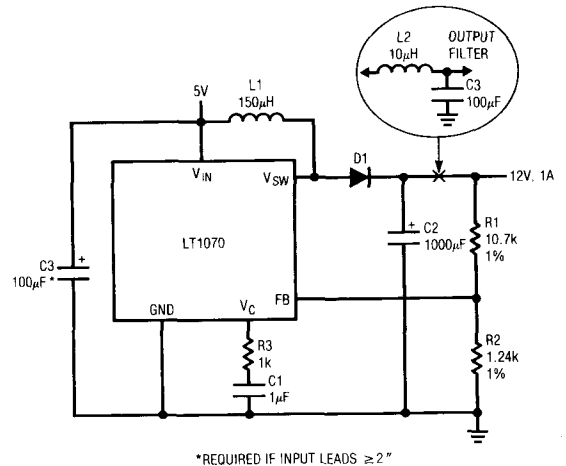


Figure 18. Boost Converter

Application Note 19

The first term of this equation is the power loss due to the “on” resistance of the switch (R). The second term is the loss from the switch driver. For the circuit in Figure 18, with $I_{OUT} = 1A$:

$$P_{IC} = (1)^2 \cdot (0.2) \left[\left(\frac{12}{5} \right)^2 - \frac{12}{5} \right] + \frac{(1)(12-5)}{40}$$

$$= 0.672 + 0.175 = 0.85W$$

The only other significant power loss in a boost regulator is in the diode, D1, as given by:

$$P_D = V_f \cdot I_{OUT} \quad (19)$$

V_f is the forward voltage of the diode at a current equal to $I_{OUT} \cdot V_{OUT}/V_{IN}$. In the example shown, with $I_{OUT} = 1A$ and $V_f = 0.8V$:

$$P_D = (0.8)(1) = 0.8W$$

Total power loss in the regulator is the sum of $P_{IC} + P_D$, and this can be used to calculate efficiency (E):

$$E = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} + P_{IC} + P_D} \quad (20)$$

$$E = \frac{(1A)(12V)}{(1)(12) + 0.85 + 0.8} = 88\%$$

With higher input voltages, efficiencies can exceed 90%.

Maximum output voltage in the boost mode is limited by the breakdown of the switch to 65V (standard part) or 75V (HV part). It may also be limited by maximum duty cycle if input voltage is low. The 90% maximum duty cycle of the LT1070 limits output voltage to ten times the input voltage. For the simple boost mode, higher ratios of output to input voltage require a tapped inductor.

Design procedure for a boost regulator is straightforward. R1 and R2 set the regulated output voltage. The feedback pin voltage is internally trimmed to 1.244V, so output voltage is equal to $1.244(R1 + R2)/R2$. R2 is normally set to 1.24k Ω and R1 is found from:

$$R1 = R2 \left(\frac{V_{OUT}}{1.244} - 1 \right) \quad (21)$$

The 1.24k Ω value for R2 is chosen to set divider current at 1mA, but this value can vary from 300 Ω to 10k Ω with negligible

effect on regulator performance. For proper load regulation, R2 must be returned directly to the ground pin of the LT1070, while R1 is connected directly to the load. For further details, see Pin Description section.

Inductor

Next, L1 is selected. The tradeoffs are size, maximum output power, transient response, input filtering, and in some cases, loop stability. Higher inductor values provide maximum output power and low input ripple current, but are physically larger and degrade transient response. Low inductor values have high magnetizing current which reduces maximum output power and increases input current ripple. Low inductance can also cause a subharmonic oscillation problem if duty cycle is above 50%.

With the aforementioned considerations in mind, a simple formula can be derived to calculate L1 based on the maximum ripple current (ΔI) to be allowed in L1.

$$L = \frac{V_{IN}(V_{OUT} - V_{IN})}{\Delta I \cdot f \cdot V_{OUT}} \quad (22)$$

Example: let $\Delta I = 0.5A$, $V_{IN} = 5V$, $V_{OUT} = 12V$, $f = 40kHz$

$$L = \frac{(5)(5 - 12)}{(0.5)(40 \times 10^3)(12)} = 146\mu H$$

A second formula will allow a calculation of maximum power output with this size inductor:

$$P_{(MAX)} = V_{IN} \left[I_P - \frac{V_{IN}(V_{OUT} - V_{IN})}{2 \cdot L \cdot f \cdot V_{OUT}} \right] \left[1 - \frac{I_P \cdot R}{V_{IN}} + \frac{I_P \cdot R}{V_{OUT}} \right] \quad (23)$$

I_P = maximum switch current

Using the values from the previous example, with $I_P = 5A$, $R = 0.2\Omega$.

$$P_{OUT(MAX)} = 5 \left[5 - \frac{5(12-5)}{2(146 \times 10^{-6})(40 \times 10^3)(12)} \right] \times$$

$$\left[1 - 5 \cdot (0.2) \left(\frac{1}{5} - \frac{1}{12} \right) \right]$$

$$= 5(5 - 0.25)(0.88) = 21W$$

Note that the second term in the first set of brackets is the only one which contains “L”, and that this term drops out of

the equation for large values of L. In this example, that term is equal to 0.25A, showing that *maximum effective switch current, and therefore maximum output power is reduced by one-half the inductor ripple current in a boost regulator.* In this example, peak effective switch current is reduced from 5A to 4.75A with 0.5A ripple current, a 5% loss. An additional 12% reduction of maximum available power is caused by switch "on" resistance. At higher input voltages, this switch loss is significantly reduced.

When continuous inductor current is desired, the value of L1 cannot be decreased below a certain limit if duty cycle of the switch exceeds 50%. Duty cycle can be calculated from:

$$DC = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (24)$$

In this example,

$$DC = \frac{12 - 5}{12} = 58.3\%$$

The reason for a lower limit on the value of L for duty cycles greater than 50% is a *subharmonic* oscillation which can occur in current-mode switching regulators. For further details of this phenomenon, see Subharmonic Oscillation section of this application section. The minimum value of L1 to ensure no subharmonic oscillations in a boost regulator is:

$$L1(\min) = \frac{V_{OUT} - 2V_{IN}}{2 \times 10^5} \quad (25)$$

$$= \frac{12 - 2(5)}{2 \times 10^5} = 10\mu\text{H}$$

Note that for $V_{OUT} \leq 2V_{IN}$, there is no restriction on inductor size. The minimum value of 10 μ H obtained in this example is below the value which would yield continuous inductor current, so it is an artificial restriction. Subharmonic oscillations do not occur if inductor current is discontinuous. The critical inductor size for continuous inductor current is:

$$L(\text{CRIT}) = \frac{V_{IN}^2 (V_{OUT} - V_{IN})}{2 \cdot f \cdot I_{OUT} (V_{OUT})^2} \quad (26)$$

$$= \frac{(5)^2 (12 - 5)}{2 (40 \times 10^3) (1) (12)^2} = 15.2\mu\text{H}$$

Discontinuous mode operation is sometimes chosen because it results in the smallest physical size for the inductor.

The maximum power output is considerably reduced, however, and can never exceed $2.5 \cdot (V_{IN})$ watts with the LT1070. The minimum inductor size required to provide a given output power in the discontinuous mode is given by:

$$L_{\text{MIN}}(\text{discontinuous}) = \frac{2 I_{OUT} (V_{OUT} - V_{IN})}{I_P^2 \cdot f} \quad (27)$$

Example: Let $V_{IN} = 5\text{V}$, $V_{OUT} = 12\text{V}$, $I_{OUT} = 0.5\text{A}$, $I_P = 5\text{A}$

$$L_{\text{MIN}}(\text{discontinuous}) = \frac{(2)(0.5)(12 - 5)}{(5)^2 \cdot (40 \times 10^3)} = 7\mu\text{H}$$

This formula does not take into account efficiency losses, so the minimum value of L should probably be increased by at least 50% for worst-case conditions. Efficiency is degraded when using minimum inductor sizes because of higher switch and diode peak currents.

In summation, to choose a value for L1:

1. Decide on continuous or discontinuous mode.
2. If continuous mode, calculate C1 based on ripple current and check maximum power and subharmonic limits.
3. If discontinuous mode, calculate L1 based on power output requirements and check to see that output power does not exceed limit for discontinuous mode ($P_{\text{MAX}} = 2.5V_{IN}$)

L1 must not saturate at the peak operating current. This value of current can be calculated from:

$$I_{L(\text{PEAK})} = I_{OUT} \frac{(V_{OUT} + V_f) - (I_{OUT} \cdot V_{OUT} \cdot R/V_{IN})}{(V_{IN} - I_{OUT} \cdot V_{OUT} \cdot R/V_{IN})} \quad (27)$$

$$+ \frac{V_{IN} (V_{OUT} - V_{IN})}{2L1 \cdot f \cdot V_{OUT}}$$

V_f = forward voltage of D1

R = "on" resistance of LT1070 switch

In this example, with $V_{IN} = 5\text{V}$, $V_{OUT} = 12\text{V}$, $V_f = 0.8\text{V}$, $I_{OUT} = 1\text{A}$, $R = 0.2\Omega$, $L1 = 150\mu\text{H}$, $f = 40\text{kHz}$;

$$I_{L(\text{peak})} = \frac{1(12 + 0.8 - 1 \cdot 12 \cdot (0.2)/5)}{5 - 1 \cdot 12 \cdot (0.2)/5}$$

$$+ \frac{5(12 - 5)}{2(150 \times 10^{-6})(40 \times 10^3)(12)}$$

$$= 2.73 + 0.24 = 3\text{A}$$

Application Note 19

A core must be selected for L1 which does not saturate with 3A peak inductor current.

Output Capacitor

The main criteria for selecting C2 is low ESR (effective series resistance), to minimize output voltage ripple. A reasonable design procedure is to let the *reactance* of the output capacitor contribute no more than 1/3 of the total peak-to-peak output voltage ripple (Vp-p), yielding:

$$C2 \geq \frac{V_{OUT} \cdot I_{OUT}}{f (V_{IN} + V_{OUT}) (0.33 V_{p-p})} \quad (28)$$

Using $V_{OUT} = 12V$, $I_{OUT} = 1A$, $V_{IN} = 5V$, $f = 40kHz$, and $V_{p-p} = 200mV$

$$C2 \geq \frac{(12)(1)}{(40 \times 10^3)(5 + 12)(0.33)(0.2)} = 268\mu F$$

This leaves 67% of the ripple attributable to ESR, giving;

$$\begin{aligned} ESR(\max) &= \frac{0.67 \cdot V_{p-p} \cdot V_{IN}}{I_{OUT} \cdot (V_{IN} + V_{OUT})} \quad (29) \\ &= \frac{(0.67)(0.2)(5)}{(1)(5 + 12)} = 0.04\Omega \end{aligned}$$

After C2 has been selected, output voltage ripple may be calculated from:

$$V_{p-p} = I_{OUT} \frac{(V_{IN} + V_{OUT})}{V_{IN}} \cdot ESR + \frac{V_{OUT}}{(V_{IN} + V_{OUT})(f)(C2)} \quad (30)$$

If lower output ripple is required, a larger output capacitor must be used with lower ESR. It is often necessary to use capacitor values much higher than calculated to obtain the required ESR. In the example shown, capacitors with guaranteed ESR less than 0.04Ω with a working voltage of 15V generally fall in the 1000–2000 μF range. Higher voltage units have lower capacitance for the same ESR.

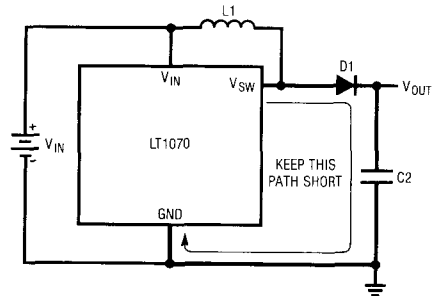
A second option to reduce output ripple is to add a small LC output filter. If the LC product of the filter is much smaller than $L1 \cdot C2$, it will not affect loop phase margin. Dramatic reduction in output ripple can be achieved with this filter, often at lower cost and less board space than simply increasing C2. See section on Output Filters for details.

Frequency Compensation

Loop frequency compensation is performed by R3 and C1. Refer to the frequency compensation part of this application section for R3 and C1 selection procedure.

Current Steering Diode

D1 should be a fast turn-off diode. Schottky diodes are best in this regard and offer better efficiency in the forward mode. With higher output voltages, the efficiency aspect is minimal and silicon fast turn-off diodes are a more economical choice. Turn-on time is important also with output voltages above 40V. Diodes with slow turn-on time will have a very high forward voltage for a short time after forward current starts to flow. This transient forward voltage can be anywhere from volts to tens of volts. It must be summed with output voltage to calculate worst-case switch voltage. To minimize switch transient voltage, the wiring of C2 and D1 should be short and close to the LT1070 as shown below.



Short Circuit Conditions

Boost regulators are *not* short circuit protected because the current steering diode (D1) connects the input to the output. The LT1070 will not be harmed for overloads up to 5A. Beyond that point, D1 can be permanently "on" and the LT1070 switch will be effectively shorted to the output. A fuse in series with the input voltage is the only simple means of protecting the circuit. Fuse sizing can be calculated from:

$$I_{IN} \approx \frac{I_{OUT} V_{OUT}}{V_{IN}} \quad (33)$$

The circuit in Figure 18 has $I_{OUT} = 1A$, $V_{OUT} = 12V$, $V_{IN} = 5V$, yielding:

$$I_{IN} = \frac{(1)(12)}{5} = 2.4A$$

A 4A fast-blow fuse would be a reasonable choice in this design.

NEGATIVE BUCK CONVERTER

The circuit in Figure 19 is a negative "buck" regulator. It converts a higher negative input voltage to a lower negative output voltage. Buck regulators are characterized by low output voltage ripple, but high input current ripple. The feedback path in this design must include a PNP transistor to level shift the output voltage sense signal to the feedback pin of the LT1070, which is referenced to the negative input voltage.

Output Divider

$$R1 \text{ and } R2 \text{ set output voltage; } R1 = \frac{(V_{OUT} - V_{BE})R2}{V_{REF}} \quad (34)$$

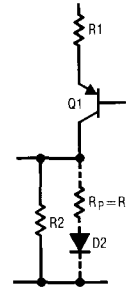
V_{REF} = LT1070 reference voltage = 1.244V

V_{BE} = Base-emitter voltage of Q1

R2 is nominally set to 1.24k. With the 5.2V output shown, and letting $V_{BE} = 0.6V$, R1 is:

$$R1 = \frac{(5.2 - 0.6)(1.24)}{1.244} = 4.585k\Omega$$

The nearest 1% value is 4.64k Ω . It will be apparent to experienced analog designers that the output voltage will have a temperature drift of 2mV/ $^{\circ}C$ caused by the temperature coefficient of V_{BE} . If this drift is too high, it can be compensated by a resistor/diode network in parallel with R2 as shown.



For zero output drift, R_p is made equal to R1 and R1 is now calculated from:

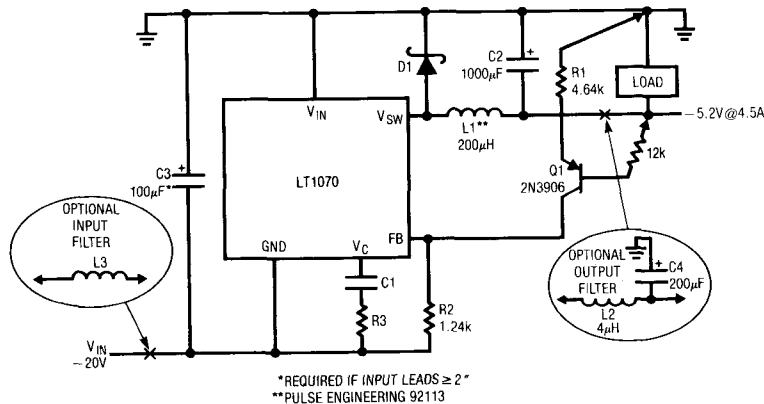
$$R1 = R_p = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) R2 \quad (36)$$

Duty Cycle

Duty cycle of buck converters in the continuous mode is given by;

$$DC = \frac{V_{OUT} + V_f}{V_{IN}}$$

V_f = forward voltage of D1



*REQUIRED IF INPUT LEADS $\geq 2^{\circ}$
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Figure 19. Negative Buck Regulator

Application Note 19

Inductor

The inductor, L1, is chosen as a tradeoff between maximum output power with minimum output voltage ripple, versus small physical size and faster transient response. A good starting point for higher-power designs is to choose a ripple current (ΔI). The LT1070 is capable of supplying up to 5A in the buck mode, so a reasonable upper limit on ripple current is 0.5A, or 10% of full load. This sets the value of L1 at:

$$L1 = \frac{(V_{IN} - V_{OUT})(V_{OUT})}{V_{IN}(\Delta I) \cdot f} \quad (37)$$

With the circuit in Figure 19, $V_{IN} = 20V$, $V_{OUT} = 5.2V$, $f = 40kHz$, $\Delta I = 0.5A$, giving:

$$L1 = \frac{(20 - 5.2)(5.2)}{20(0.5)(40 \times 10^3)} = 192\mu H$$

The inductor current will go discontinuous (= zero for part of the cycle) when output current is one half the ripple current. If continuous inductor current is desired for lower load currents, L1 will have to be increased.

Peak inductor and switch current is equal to output current plus one-half the peak-to-peak ripple current;

$$I_{L(\text{peak})} = I_{OUT} + \frac{(V_{IN} - V_{OUT})(V_{OUT})}{2 \cdot V_{IN} \cdot L \cdot f} \quad (37)$$

With the example shown, letting $I_{OUT} = 4.5A$, $L1 = 200\mu H$;

$$\begin{aligned} I_{L(\text{peak})} &= 4.5 + \frac{(20 - 5)(5)}{2 \cdot 20 \cdot (200 \times 10^{-6})(40 \times 10^3)} \\ &= 4.5 + 0.23 = 4.73A \end{aligned}$$

The core used for L1 must be sized so that it does not saturate at 4.73A in this example. For lower output current applications, a much smaller core can be used. The core need not be sized for peak current limit conditions (6A-10A) in most situations because the LT1070 pulse-by-pulse current limit functions even with saturated cores.

Lower values of L1 can be used if maximum output power and low ripple are not as important as physical size or fast transient response. Pure discontinuous mode operation yields the lowest value for L1, and L1 is chosen on the basis of required output current. Maximum output current in the discontinuous mode is one half maximum switch current and L1 is found from:

$$L1(\text{min}) = \frac{2V_{OUT} \cdot I_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{I_p^2 \cdot f} \quad (38)$$

Where I_p = maximum switch current

Example: Let $V_{OUT} = 5.2V$, $I_{OUT} = 2A$, $V_{IN} = 20V$, $I_p = 5A$

$$L1(\text{min}) = \frac{(2) \cdot (5.2)(2) \left(1 - \frac{5.2}{20}\right)}{(5)^2 (40 \times 10^3)} = 15.4\mu H$$

It is suggested that, in discontinuous mode, this calculated value be increased by approximately 50% in practice to account for variations in cores, input voltage, and frequency. The core must be sized to not saturate at a peak current of 5A for maximum output in discontinuous mode.

Output Capacitor

C2 is chosen for output ripple considerations. ESR of the capacitor may limit ripple voltage, so this parameter should be checked first. Maximum ESR allowed for a given peak-to-peak output ripple (V_{p-p}), assuming $C2 \rightarrow \infty$, is given by:

$$ESR(\text{max}) = \frac{V_{p-p} \cdot L1 \cdot f}{V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (39)$$

with $V_{p-p} = 25mV$, $L1 = 200\mu H$, $f = 40kHz$, $V_{IN} = 20V$, $V_{OUT} = 5.2V$:

$$ESR(\text{max}) = \frac{(0.025)(200 \times 10^{-6})(40 \times 10^3)}{5.2 \left(1 - \frac{5.2}{20}\right)} = 0.052\Omega$$

To obtain a reasonable value for C2, actual ESR should be no more than two thirds of the maximum value. In this example, ESR is selected at 0.035Ω. C2 may now be found:

$$C2 \geq \frac{1/(8Lf^2)}{\left[\frac{V_{p-p}}{V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} - \frac{ESR}{Lf} \right]} \quad (40)$$

$$\geq \frac{1/[8 \cdot (200 \times 10^{-6}) (40 \times 10^3)^2]}{\left[\frac{0.025}{5.2 \left(1 - \frac{5.2}{20}\right)} - \frac{0.025}{(200 \times 10^{-6}) (40 \times 10^3)} \right]} \geq 184\mu F$$

It is very likely that a 184μF capacitor of the right operating voltage cannot be found with an ESR of 0.035Ω max. C2 will have to be increased in value significantly to achieve the required ESR.

Output Filter

If low output ripple is required, C2 may acquire unreasonably large values. A second option is to add an output filter as shown. Exact calculations for the values of L2 and C4 in this filter are beyond the scope of this note, but a rough approximation can be made by assuming that the ESR of C2 and C4 are the limiting factors. This leads to a value for L2 independent of the actual capacitance of C4.

$$L2 \approx \frac{(ESR2)(ESR4)(V_{IN} - V_{OUT})(V_{OUT})}{V_{p-p} \cdot 2\pi(f)^2 \cdot L1 \cdot V_{IN}} \quad (41)$$

ESR2 = ESR of C2 and ESR4 = ESR of C4 and Vp-p = desired output ripple peak-to-peak.

If we assume ESR2 = ESR4 = 0.1Ω, and require Vp-p = 5mVp-p;

$$L2 = \frac{(0.1)(0.1)(20 - 5.2)(5.2)}{(0.005)(2\pi)(40 \times 10^3)^2 (200 \times 10^{-6})(20)} = 3.8\mu H$$

L2 may be increased above this value, but the L2 C4 product should be kept at least ten times smaller than L1 C2.

Input Filter

Buck regulators have high ripple current fed back into the input voltage supply. Peak-to-peak value of this current is equal to output current. This can cause intolerable EMI conditions

in some systems. An input filter formed by L3 and C3 will greatly reduce this ripple current. The major considerations for this filter are its attenuation ratio and the possible effect it has on the regulator loop stability. See discussion of Input Filters elsewhere in this application section for more details.

Frequency Compensation

R3 and C1 provide frequency compensation. See Frequency Compensation section for details of selecting these components.

Catch Diode

D1 is the current steering diode. During switch off-time, it provides a path for L1 current. This diode should be a high speed switching type with fast turn-on and turn-off. A Schottky type is suggested for lower output voltage applications to improve efficiency. Formulas for average and peak diode current plus diode power dissipation are shown below. These equations assume continuous inductor current with fairly low ripple.

$$I_{PEAK} \approx I_{OUT} \quad (42)$$

$$I_{AV} = I_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (43)$$

$$P_{DIODE} = V_f^* \cdot I_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (44)$$

*V_f is diode forward voltage at I = I_{PEAK}

NEGATIVE TO POSITIVE BUCK-BOOST CONVERTER

The circuit in Figure 20 looks similar to a positive boost regulator except that the output load is referred to the inductor termination (ground) instead of the switch. A transistor (Q1) is used to level shift the output voltage signal down to the feedback pin of the LT1070 which is referred to the negative input voltage.

Unlike buck or boost converters, inverting converters do not have any inherent limitation on input voltage relative to output voltage. Input levels may be either higher or lower than output voltage. The sum of input voltage plus output voltage cannot exceed the breakdown voltage of the LT1070 switch.

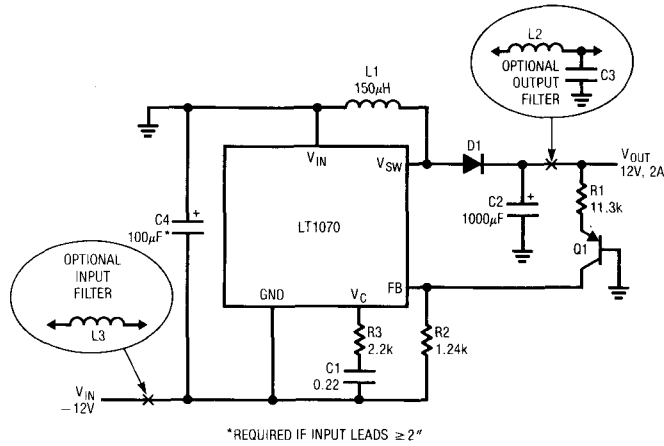


Figure 20. Negative to Positive Buck-Boost Converter

Output voltage is given by:

$$V_{OUT} = -V_{IN} \left(\frac{DC}{1-DC} \right) \quad (45)$$

DC = switch duty cycle (0 to 1)

With DC = 0, output voltage is zero, and as DC → 1, output voltage increases without limit.

Duty cycle of an inverting buck-boost converter is given by;

$$DC = \frac{|V_{OUT}|}{|V_{IN}| + |V_{OUT}|}$$

Maximum power output of a buck-boost converter is equal to:

$$P_{OUT(max)} = \frac{I_P \cdot V_{OUT} \cdot V_{IN} - \frac{(I_P)^2 \cdot R \cdot V_{OUT}}{V_{OUT} + V_{IN}}}{1 + V_f/V_{OUT}} \quad (46)$$

I_P = peak switch current — 1/2 L1 p-p ripple current

R = switch “on” resistance

V_f = forward voltage of D1

The first term on the top of the equation is the theoretical output power with no switch or diode (D1) losses. The second top term is the switch loss. The term on bottom accounts for diode losses.

With the circuit shown, $V_{IN} = -12V$, $V_{OUT} = +12V$, ripple current in L1 = 0.5Ap-p, peak switch current = 5A, $R = 0.2\Omega$, $V_f = 0.8V$,

$$P_{OUT(max)} = \frac{\frac{(4.75)(12)(12)}{12+12} - \frac{(4.75)^2(0.2)(12)}{12+12}}{1 + \frac{0.8}{12}} = 24.6W$$

Setting Output Voltage

R1 and R2 determine output voltage;

$$R1 = \frac{R2(V_{OUT} - V_{BE})}{V_{REF}} \quad (52)$$

V_{REF} = LT1070 reference voltage = 1.244V

V_{BE} = base-emitter voltage of Q1

In this example, $R2 = 1.24k$, $V_{OUT} = 12V$, and the V_{BE} of Q1 is $\approx 0.6V$, giving:

$$R1 = \frac{(1.24)(12 - 0.6)}{1.244} = 11.36k\Omega$$

The output voltage will have a $-2mV/^\circ C$ drift due to the temperature drift of V_{BE} . If this is undesirable, a resistor diode combination can be added in parallel with R2 to correct drift. See section on Negative Buck Converters for details.

Inductor

The inductor is normally calculated on the basis of maximum allowed ripple current, because high ripple currents reduce the maximum available output power and degrade efficiency. For a peak-to-peak ripple current (ΔI_L), L1 is equal to:

$$L1 = \frac{(V_{IN})(V_{OUT})}{(\Delta I_L)(V_{IN} + V_{OUT}) \cdot f} \quad (53)$$

f = LT1070 operating frequency = 40kHz

In this example, with ΔI chosen at 20% of maximum LT1070 switch current ($\Delta I = 1.0A$),

$$L1 = \frac{(12)(12)}{1.0(12 + 12)(40 \times 10^3)} = 150\mu H$$

Larger values for L1 will not raise power levels appreciably, will increase size and cost, and will degrade transient response. L1 is not acting as a ripple filter for either the input or the output, so large values will not improve ripple either.

If L1 is reduced in value, maximum power output will be degraded. Equation 46 defines I_p as the maximum allowed switch current minus 1/2 ΔI_L . Therefore I_p would have to be reduced from 5A to 2.5A if L1 were reduced to the point where the ripple current equaled 5A. This is a 2:1 reduction in maximum output power. Further reductions in L1 result in discontinuous current flow and equation 46 is invalid. The poor efficiency obtained with discontinuous current flow recommends it only for low power outputs when the physical size of L1 is critical. With discontinuous current flow, the minimum recommended size for L1 is:

$$L1(\text{min, discontinuous}) = \frac{2 V_{OUT} (I_{OUT})}{f \cdot (0.7 I_p)^2} \quad (54)$$

The (0.7) coefficient in front of I_p is a "fudge" factor to account for variations in f and L1, and switching losses.

Example, $V_{OUT} = 12V$, $I_{OUT} = 0.5A$, $f = 40kHz$, $I_p = 5A$.

$$L1 = \frac{(2)(12)(0.5)}{(40 \times 10^3)(0.7 \times 5)^2} = 24.5\mu H$$

Once L1 has been selected, peak inductor current in the continuous mode can be calculated from:

$$I_{L(\text{peak})} = I_{OUT} \left[1 + \frac{V_{OUT} + V_f}{V_{IN} - I_{OUT} \cdot R \cdot \frac{(V_{IN} + V_{OUT})}{V_{IN}}} \right] + \frac{(V_{IN})(V_{OUT})}{2 \cdot L1 (V_{IN} + V_{OUT}) \cdot f} \quad (55)$$

V_f = forward voltage of D1

R = LT1070 switch "on" resistance

With the circuit in Figure 20 with $L1 = 150\mu H$, and $V_f = 0.8V$, $I_{OUT} = 1.5A$, $R = 0.2\Omega$:

$$I_{L(\text{peak})} = 1.5 \left[1 + \frac{12 + 0.8}{12 - (1.5)(0.2) \frac{(12 + 12)}{12}} \right] + \frac{(12)(12)}{2(150 \times 10^{-6})(12 + 12)(40 \times 10^3)}$$

$$I_{L(\text{peak})} = 3.18 + 0.5 = 3.68A$$

3.18A is the *average* current through L1 and 0.5A is the peak AC ripple current. The core used for L1 must be large enough so that it does not saturate at $I_L = 3.68A$.

Peak inductor current for discontinuous mode operation is found from:

$$I_{L(\text{peak})}(\text{discontinuous mode}) = \sqrt{\frac{I_{OUT}(V_{OUT} + V_f) \cdot 2}{L1 \cdot f}} \quad (56)$$

Example, let $L1 = 20\mu H$, $I_{OUT} = 0.25A$, $V_f = 0.8V$

$$I_{L(\text{peak})} = \sqrt{\frac{(0.25)(12 + 0.8) \cdot 2}{(20 \times 10^{-6})(40 \times 10^3)}} = 2.83A$$

The core size for this discontinuous application can be considerably smaller than in the previous example. Core volume is approximately proportional to $I_L^2 \cdot L$. With $L1 = 100\mu H$, and $I_L = 3.93A$, $I_L^2 \cdot L = 1.5 \times 10^{-3}$. The $20\mu H$ inductor with $I_L = 2.83A$ has $I_L^2 \cdot L = 0.16 \times 10^{-3}$. The core can be nearly ten times smaller. This size difference is not free—the discontinuous circuit will supply much less current and have somewhat poorer efficiency.

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Output Capacitor

C2 must be a high quality (low ESR) switching capacitor because it does all the output filtering. L1 simply functions as an energy transfer element. A reasonable starting point for selecting C2 is to assume that the ESR (effective series resistance) of C2 contributes 2/3 of the output ripple and that the reactance of C2 contributes 1/3. With this in mind, a formula can be derived for ESR:

$$\text{ESR(max)} = \frac{V_{pp} \cdot V_{IN} \cdot (2/3)}{I_{OUT} (V_{IN} + V_{OUT})} \quad (57)$$

V_{pp} = peak-to-peak output voltage ripple

With V_{p-p} selected at 100mV, and $V_{IN} = 12V$, $V_{OUT} = 12V$, $I_{OUT} = 1.5A$, ESR is:

$$\text{ESR(max)} = \frac{(0.1)(12)(2/3)}{(1.5)(12+12)} = 0.0185\Omega$$

With ESR found, the value of C2 may now be computed:

$$C2 = \frac{(I_{OUT}) \cdot (V_{OUT})}{\left[V_{p-p} - I_{OUT} \cdot \text{ESR} \left(\frac{V_{IN} + V_{OUT}}{V_{IN}} \right) \right] (V_{OUT} + V_{IN}) \cdot (f)} \quad (58)$$

If we specify C2 ESR at 0.015 Ω max, C2 is:

$$C2 = \frac{(1.5)(12)}{\left[0.1 - (1.5)(0.015) \left(\frac{12+12}{12} \right) \right] (12+12)(40 \times 10^3)} \quad (59)$$

= 341 μ F

It is most likely that to find a capacitor with a maximum ESR of 0.015 Ω , the capacitance will have to be much larger than 341 μ F. If lower output ripple is desired, the value of C2 may become very large just to meet ESR requirements.

A second solution to the output ripple problem is to add an output filter at the point indicated in Figure 20. This filter can provide a large reduction in ripple with almost no effect on loop transient response, phase margin, or efficiency. See section on Output Filters for further details.

Current Steering Diode

D1 must be a fast recovery diode with an *average* current rating equal to I_{OUT} and a peak repetitive rating of $I_{OUT} (V_{OUT} + V_{IN})/V_{IN}$. If continuous output shorts can occur, D1 must be rated for 10A and heat sunk accordingly unless the LT1070 current limit is externally reduced. Power dissipation of D1 under normal load conditions is:

$$P_{(D1)} = I_{OUT} \cdot V_f$$

$$V_f \text{ is D1 forward voltage at } I_D = I_{OUT} \left(\frac{V_{OUT} + V_{IN}}{V_{IN}} \right) \quad (60)$$

Breakdown voltage of D1 must be at least $V_{IN} + V_{OUT}$. Turn-on time should be short to minimize the voltage spike across the LT1070 switch following switch turn off.

POSITIVE BUCK CONVERTER

Positive buck converters (Figure 21) using the LT1070 require a novel design approach because the negative side of the LT1070 switch is committed to the ground of the chip. This negative switch terminal is the inductor drive point in a positive buck converter. The ground pin of the LT1070 must therefore switch back and forth between the input voltage and converter ground. This is accomplished by tying the positive side of the switch (V_{SW}) to the input supply, and using a peak detected (C3, D3) bootstrapped supply voltage to operate the chip. As long as the LT1070 is switching, C3 will maintain the chip input-to-ground pin voltage at a voltage equal to the input supply voltage. *It is important to keep the value of C3 to a minimum* to ensure proper start-up of this topology. The 2.2 μ F value shown should not be increased unless careful tests are done to ensure proper start-up under worst-case *light* loads. If the LT1070 *does not* start, the lightly loaded output will go unregulated high. The minimum recommended load current in any case is 100mA.

The most unusual aspect of this design is the manner in which output voltage information is delivered to the LT1070 feedback pin. This pin is switching along with the LT1070 ground pin to which it is referenced, so the feedback circuit must float on the switching ground pin and at the same time be proportional to the DC value of the output voltage. This is accomplished by peak detecting the output voltage with D2 during the "off" time of the LT1070 switch. The voltage on the

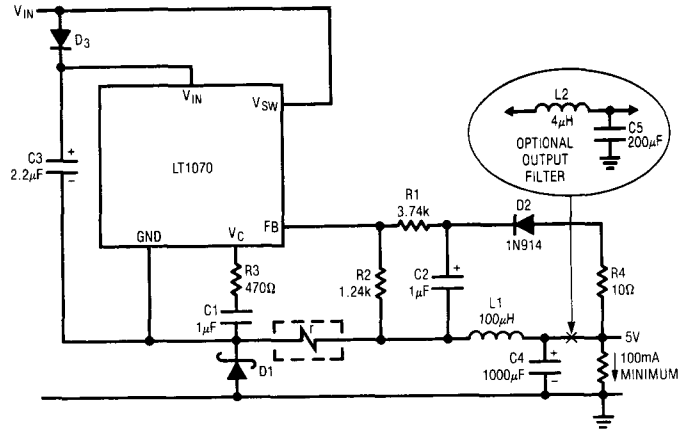


Figure 21. Positive Buck Converter

ground pin of the chip at this time is one diode drop (D1) negative with respect to system ground, because D1 is forward biased by load current flowing through L1. D2 also forward biases, giving a voltage across C2 of:

$$V_{C2} = V_{OUT} - V_{D2} + V_{D1} \quad (61)$$

V_{D1} = forward voltage of D1
 V_{D2} = forward voltage of D2

The feedback network, R1/R2, is therefore biased with a voltage very nearly equal to output voltage, and the LT1070 will regulate output voltage according to:

$$V_{OUT} = V_{C2} + V_{D2} - V_{D1} = \frac{V_{REF}(R1 + R2)}{R2} + V_{D2} - V_{D1} \quad (62)$$

V_{REF} = reference voltage of LT1070 = 1.244V

If V_{D1} is exactly equal to V_{D2} , output regulation will be perfect, but the forward voltage of D1 is load current dependent, while D2 operates at a fixed average current of 1mA. This can cause output voltage variations of 100–400mV if load current varies over a wide range. To minimize this effect, D1 should be conservatively rated with respect to operating current so that the effect of parasitic series resistance is minimized. The unit shown is rated at 10A average current. D1 should also be a fast turn-on type. (See diode discussion elsewhere in this application section.) A long turn-on time for D1 allows C2 to charge to a voltage *higher* than V_{OUT} , creating an abnormally

low output voltage. R4 is added to minimize this effect. A Schottky diode is recommended for D1 because these diodes have very fast switching times and their low forward voltage improves efficiency, especially for low output voltage.

Load regulation can be significantly improved in this application by inserting a small resistor (r , shown in dashed box) between D1 and L1. The voltage across r will be equal to $r \cdot I_{OUT}$. This voltage *increases* the voltage across R2, forcing the output voltage to *rise* under load. Perfect load regulation will result if the output *rise* created by r just cancels the output *drop* caused by the increased forward voltage of D1. The required value for r is found from:

$$r = r_d \cdot \frac{V_{REF}}{V_{OUT}} \quad (63)$$

r_d = forward series resistance of D1

V_{REF} = LT1070 reference voltage = 1.244V

Load regulation will never be perfect because r_d varies slightly from unit to unit and it is not constant with load current, but regulation better than 2% with $V_{OUT} = 5V$ is easily achieved even with load current varying over a 5:1 range. For higher output voltages, load regulation is even better.

For the circuit shown, with $r_d = 0.05\Omega$, r is:

$$r = \frac{(0.05)(1.244)}{5} = 0.0124\Omega$$

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This is most easily obtained by using 9 inches of #22 hookup wire.

Output voltage is determined by R1 and R2:

$$R1 = R2 \frac{(V_{OUT} - V_{REF})}{V_{REF}} \quad (64)$$

R2 is normally fixed at 1.24k Ω to set divider current to 1mA. This equation assumes that $V_{D1} = V_{D2}$. A slight adjustment in R1 will be required if $V_{D1} \neq V_{D2}$.

Duty Cycle Limitations

Maximum duty cycle for the LT1070 is 90%. This limits the minimum input voltage in buck regulators. Duty cycle can be calculated from:

$$DC = \frac{V_{OUT} + V_f}{V_{IN} - (I_{OUT})R + V_f} \quad (65)$$

V_f = forward voltage of D1

R = "on" resistance of LT1070 switch

Rearranging this formula for V_{IN} yields:

$$V_{IN(MIN)} = \frac{V_{OUT} + V_f}{DC} + R(I_{OUT}) - V_f \quad (66)$$

With a maximum duty cycle of 90%, (0.9) and $V_{OUT} = 5V$, $V_f = 0.6V$, $R = 0.2\Omega$, $I_{OUT} = 4A$:

$$V_{IN(MIN)} = \frac{5 + 0.6}{0.9} + (0.2)(4) - 0.6 = 6.4V$$

Inductor

The energy storage inductor in a buck regulator functions as both an energy conversion element and as an output ripple filter. This double duty often saves the cost of an additional output filter, but it complicates the process of finding a good compromise for the value of the inductor. Large values give maximum power output and low output ripple voltage, but they also can be bulky and give poor transient response. A reasonable starting point is to select a maximum peak-to-peak ripple current, (ΔI). This yields a value for L1 of:

$$L1 = \frac{(V_{IN} - V_{OUT})(V_{OUT})}{V_{IN}(\Delta I) \cdot f} \quad (67)$$

f = LT1070 operating frequency $\approx 40kHz$

ΔI = peak-to-peak inductor ripple current

With the circuit shown, $V_{IN} = 16V$, $V_{OUT} = 5V$, and ΔI set at 20% of 3.5A = 0.7A:

$$L1 = \frac{(16 - 5)(5)}{(16)(0.8)(40 \times 10^3)} = 122\mu H$$

The ripple current in L1 reduces the maximum output current by one-half ΔI . For lower output currents this is no problem, but for maximum output power, L1 may be raised by a factor of two to three. For lower output powers, L1 can be reduced to save on size and cost. Discontinuous mode operation will occur even near full load if L1 is reduced far enough. The LT1070 is not affected by discontinuous operation per se, but maximum output power is significantly reduced in discontinuous mode designs:

$$I_{OUT(MAX)} \text{ (discontinuous)} = \frac{(I_p)^2 \cdot L \cdot f}{2V_{OUT}} \left(\frac{V_{IN}}{V_{IN} - V_{OUT}} \right) \quad (68)$$

I_p = LT1070 peak switch current

With $L1 = 10\mu H$ for instance, and $I_p = 5A$:

$$I_{OUT(MAX)} = \frac{(5)^2 (10 \times 10^{-6}) (40 \times 10^3)}{2(5)} \left(\frac{16}{16 - 5} \right) = 1.4A$$

Efficiency is also reduced with discontinuous operation because of increased switch dissipation.

The load current where a buck regulator changes from continuous to discontinuous operation is:

$$I_{CRIT} = \frac{(V_{IN} - V_{OUT})(V_{OUT})}{2(V_{IN})(f)(L1)} \quad (69)$$

With a 100 μH value for L1, inductor current will go discontinuous at:

$$I_{CRIT} = \frac{(16 - 5)(5)}{2(16)(40 \times 10^3)(100 \times 10^{-6})} = 0.43A \quad (70)$$

I_{CRIT} can never exceed 2.5A (one half maximum LT1070 switch current).

Peak inductor current in a buck regulator with continuous mode operation is:

$$I_{L(PEAK)} = I_{OUT} + \frac{(V_{IN} - V_{OUT})(V_{OUT})}{2(V_{IN})(L1)(f)} \quad (71)$$

With $I_{OUT} = 3.5A$ and $L1 = 100\mu H$.

$$I_{L(PEAK)} = 3.5 + \frac{(16-5)(5)}{2(16)(100 \times 10^{-6})(40 \times 10^3)} = 3.93A$$

The core used for L1 must be able to handle 3.93A peak current without saturating.

Peak inductor currents in discontinuous mode are much higher than output current:

$$I_{L(PEAK)} \text{ (discontinuous)} = \sqrt{\frac{2 V_{OUT} \cdot I_{OUT} (V_{IN} - V_{OUT})}{V_{IN} \cdot L1 \cdot f}} \quad (72)$$

for $L1 = 10\mu H$, $I_{OUT} = 1A$;

$$I_{L(PEAK)} \text{ (discontinuous)} = \sqrt{\frac{2(5)(1)(16-5)}{16(10 \times 10^{-6})(40 \times 10^3)}} = 4.15A$$

The $10\mu H$ inductor, at 1A output current, must be sized to handle 4.14A peak current.

Output Voltage Ripple

See negative buck regulator section for calculation of output ripple.

Output Capacitor

C4 is chosen for output voltage ripple considerations. Its ESR (effective series resistance) is the most important parameter. For details, see the section on negative buck regulators.

Output Filter

For very low output voltage ripple, the value of C4 may become prohibitively high. An output filter, L2 and C5, may be used to reduce output ripple. See Output Filter section for details.

FLYBACK CONVERTER

Flyback converters (Figure 22) are able to regulate an output voltage either higher or lower than the input voltage by shuttling stored energy back and forth between the windings of a transformer. During switch "on" time, all energy is stored in the primary winding according to, $E = (I_{PRI})^2 (L_{PRI})/2$. When the switch turns off, this energy is transferred to the output

winding. The current in the secondary just after switch opening is equal to the reciprocal of turns ratio (1/N) times the current in the primary just prior to switch opening. Output voltage of a flyback converter is not constrained by input voltage as in buck or boost converters.

$$V_{OUT} = \frac{DC}{1-DC} N \cdot V_{IN} \quad (73)$$

$$DC = \text{switch duty cycle} = \frac{V_{OUT}}{V_{OUT} + N V_{IN}} \quad (74)$$

N = transformer turns ratio

By varying duty cycle between 0 and 1, output voltage can theoretically be set anywhere from 0 to ∞ . Practically, however, output voltage is constrained by switch breakdown voltage and the maximum output voltage is limited to:

$$V_{OUT(MAX)} = N (V_M - V_{SNUB} - V_{IN}) \quad (75)$$

V_{SNUB} = snubber voltage (see snubber details in this section)
 V_M = maximum allowed switch voltage

This still allows the LT1070 to regulate output voltages of hundreds or even thousands of volts by using large values of N.

In many applications, N can vary over a wide range without degrading performance. If maximum output power is desired however, N can be optimized:

$$N_{(OPT)} = \frac{V_{OUT} + V_f}{V_M - V_{IN(MAX)} - V_{SNUB}} \quad (76)$$

V_f = forward voltage of D1

In Figure 22, with $V_{OUT} = 5V$, $V_f = 0.7V$ (Schottky), $V_{IN(MAX)} = 30V$, $V_M = 60V$, $V_{SNUB} = 15V$;

$$N_{(OPT)} = \frac{5 + 0.7}{60 - 30 - 15} = 0.38$$

A turns ratio of 1:3 (0.33) was used in this circuit.

A second important transformer parameter which must be determined is primary inductance (L_{PRI}). For maximum output power, L_{PRI} should be high to minimize magnetizing current, but this can lead to unacceptably large core sizes. A reasonable design approach is to reduce the value of L_{PRI} to the

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point where primary magnetizing current (ΔI) is about 20% of peak switch current. The LT1070 is rated for 5A peak switch current, so for full power applications, ΔI can be set to 1A peak-to-peak. Maximum output current is reduced by one-half of the ratio of ΔI to peak switch current, or $\approx 10\%$ in this case.

With this design approach, L_{PRI} is found from:

$$L_{PRI} = \frac{(V_{IN})(V_{OUT})}{\Delta I \cdot f(V_{OUT} + N V_{IN})} \quad (77)$$

with $V_{IN} = 24V$, $V_{OUT} = 5V$, $\Delta I = 1A$, $N = 1/3$:

$$L_{PRI} = \frac{(24)(5)}{(1)(40 \times 10^3)(5 + 1/3 \cdot 24)} = 231 \mu H$$

Values of L_{PRI} higher than this will raise maximum output current only slightly and will require larger core size. Lower primary inductance may be used for lower output currents to reduce core size.

Maximum output current is a function of peak allowed switch current (I_P):

$$I_{OUT(MAX)} = \frac{E \left(I_P - \frac{\Delta I}{2} \right) (V_{IN})}{N \cdot V_{IN} + V_{OUT}} \quad (78)$$

$I_P = \text{max LT1070 switch current}$
 $E = \text{overall efficiency} \approx 75\%$

with $V_{IN} = 24V$, $V_{OUT} = 5V$, $I_P = 5A$, $\Delta I = 1A$, $N = 1/3$;

$$I_{OUT(MAX)} = \frac{0.75 \left(5 - \frac{1}{2} \right) (24)}{(1/3)(24) + 5} = 6.2A$$

The 75% efficiency number comes from losses in the snubber network ($\approx 6\%$), LT1070 switch ($\approx 4\%$), LT1070 driver ($\approx 3\%$), output diode ($\approx 8\%$), and transformer ($\approx 4\%$). Although this efficiency is not as impressive as the 85–95% obtainable with simple buck or boost designs, it is more than

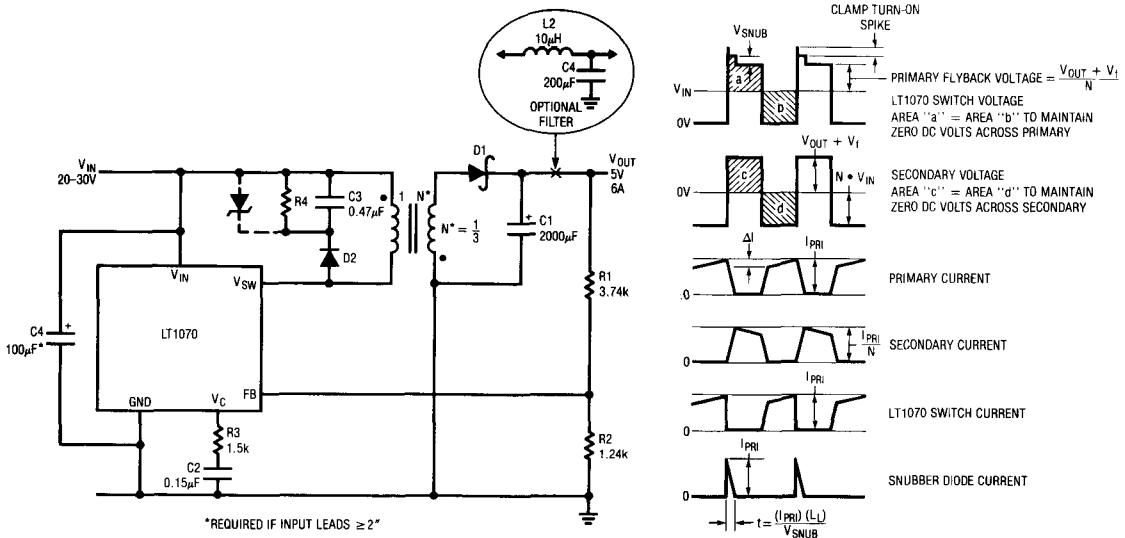


Figure 22. Flyback Converter

justified in many cases by the ability to use the variable N to generate high output currents or high output voltages and the option to add extra windings for multiple outputs.

Peak primary current is used to determine core sizing for the transformer:

$$I_{PRI} = \frac{I_{OUT}}{E} \left(\frac{V_{OUT}}{V_{IN}} + N \right) + \frac{(V_{IN})(V_{OUT})}{2 \cdot f \cdot L_{PRI} (V_{OUT} + N V_{IN})} \quad (79)$$

For an output current of 6A, with $V_{IN}=24V$, $V_{OUT}=5V$, $E=75\%$, $L_{PRI}=231\mu H$, $N=1/3$,

$$I_{PRI} = \frac{6}{0.75} \left(\frac{5}{24} + \frac{1}{3} \right) + \frac{(24)(6)}{2(40 \times 10^3)(231 \times 10^{-6})(5 + 1/3) \cdot 24}$$

$$= 4.33 + 0.5 = 4.83A$$

The core must be able to handle 4.83A peak current in the 231 μH primary winding without saturating. (See section on inductors and transformers for further details).

Output Divider

R1 and R2 set output voltage:

$$R1 = \frac{(V_{OUT} - V_{REF})}{V_{REF}} R2 \quad (80)$$

V_{REF} = feedback reference voltage of the LT1070 = 1.244V

R1 and R2 can vary over a wide range, but a convenient value for R2 is 1.24k Ω , a standard 1% value.

For a 5V output, $R1 = (5 - 1.244)(1.24)/1.244 = 3.756k\Omega$

Frequency Compensation

R3 and C2 provide a pole-zero frequency compensation. For details, see the section on frequency compensation elsewhere in this data sheet.

Snubber Design

Flyback converters using transformers require a clamp to protect the switch from overvoltage spikes. These spikes are created by leakage inductance in the transformer. Leakage inductance (L_L) is modeled as an inductor in series with the

primary winding which is not coupled to the secondary as shown in Figure 23.

During switch "on" time, a current is established in L_L equal to peak primary current (I_{PRI}). When the switch turns off, the energy stored in L_L ($E = I^2 \cdot L_L/2$) will cause the switch voltage to fly up to breakdown if the voltage is not clamped.

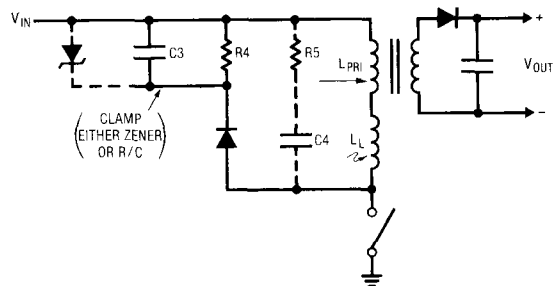


Figure 23. Snubber Clamping

If a zener diode is used for clamping, zener clamp voltage is selected by assigning a maximum switch voltage and maximum input voltage:

$$V_{ZENER} = V_M - V_{IN(MAX)}$$

V_M = max allowed switch voltage

The standard LT1070 maximum switch voltage is 65V, so V_M is typically set at 60V to allow a margin of 5V. If we assume $V_{IN(MAX)} = 30V$ for this circuit:

$$V_{ZENER} = 60 - 30 = 30V$$

Peak zener current is equal to peak primary current (I_{PRI}), and average power dissipation is equal to:

$$P_{ZENER} = \frac{(V_Z)(I_{PRI})^2 \cdot L_L \cdot f}{2 \left(V_Z - \frac{V_{OUT} + V_f}{N} \right)} \quad (81)$$

An important part of this equation is the term $V_Z - (V_{OUT} + V_f)/N$ in the denominator. This voltage is defined as snubber voltage (V_{SNUB}), and is the difference between the zener voltage and the normal flyback voltage of the primary. (See waveforms with Figure 22). If V_{SNUB} is too low, zener dissipation rises rapidly. A reasonable minimum for V_{SNUB} is 10V, so this should be checked before proceeding further:

$$V_{SNUB} = V_Z - \frac{V_{OUT} + V_f}{N} = 30 - \frac{5 + 0.7}{1/3} = 12.9V \quad (82)$$

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Leakage inductance in a transformer can be minimized by bifilar winding or by interleaving the primary and secondary. If this is done correctly, leakage inductance is usually less than 1% of primary inductance. If we wind T1 for $L_{PRI} = 230\mu\text{H}$, L_L should be less than $2.3\mu\text{H}$. Using this value, power dissipation in the zener at full load current is;

$$P_{ZENER} = \frac{(30)(4.83)^2 \cdot (2.3 \times 10^{-6})(40 \times 10^3)}{2 \left(30 - \frac{5+0.7}{1/3}\right)} = 2.5\text{W}$$

Zener dissipation under short circuit conditions is calculated from the same equation (81) by assuming that $V_{OUT} = 0$, and I_{PRI} is the current limit value of the LT1070. If we let $I_{PRI} = 9\text{A}$:

$$P_{ZENER} = \frac{(30)(9)^2 (3.5 \times 10^{-6})(40 \times 10^3)}{2 \left(30 - \frac{0.7}{1/3}\right)} = 4\text{W}$$

(output shorted)

The waveform of LT1070 switch voltage shows a narrow spike extending above the snubber clamp voltage. This spike is caused by the turn-on time of the clamp circuit, in particular the diode in series with the zener. This diode should be a Schottky or a very fast-turn-on type to minimize the height of this spike. It must be rated for peak currents equal to I_{PRI} . The reverse voltage rating of the diode must be at least $V_{IN(MAX)}$.

An alternative to zener clamping is an R/C clamp. This is less expensive, but has the disadvantage of a less well defined clamping level. The RC snubber also dissipates power even with no-load conditions. A value for R4 is found from:

$$R_{SNUB} = \frac{2(V_R^2 - V_R \cdot V_{OUT}/N)}{(I_{PRI})^2 (L_L) (f)} \quad (83)$$

V_R = voltage across snubber resistor

If we set $V_R = 30\text{V}$ (same as V_{ZENER}), and use full load conditions of $I_{PRI} = 4.83\text{A}$:

$$R_{SNUB} = \frac{2[(30)^2 - 30 \cdot 5/(1/3)]}{(4.83)^2 (2.3 \times 10^{-6})(40 \times 10^3)} = 419\Omega$$

Power dissipation in the snubber at full load is equal to:

$$P_R = V_R^2/R = (30)^2/419 = 2.15\text{W}$$

At very light loads, the voltage across the snubber resistor drops to the flyback voltage of the primary, $V_R = (V_{OUT} + V_f)/N$.

In this example, flyback voltage is 16.8V , resulting in a snubber dissipation of $(16.8)^2/419\Omega = 0.67\text{W}$.

This may be a consideration where high efficiency is necessary even with near-zero output loads. *Short circuit* power dissipation in the snubber resistor is approximately equal to:

$$P_R \approx \frac{(I_{PRI})^2 \cdot f \cdot L_L}{2} \quad (84)$$

(output shorted)

I_{PRI} in short circuit is the current limit of the LT1070. For $I_{PRI} = 9\text{A}$, snubber dissipation with the output shorted is $\approx 3.7\text{W}$ in this example.

The value of C3 is not critical, but it should be large enough to keep the ripple voltage across the snubber to only a few volts. This yields a capacitor value of:

$$C3 = \frac{V_R}{R \cdot f \cdot V_S} \quad (V_S = \text{voltage ripple across C3}) \quad (85)$$

$$\text{For } V_S = 3\text{V}, V_R = 30\text{V}, R = 419\Omega: = \frac{30}{(419)(40 \times 10^3)(3)} = 0.6\mu\text{F}$$

C3 should be a very low ESR (effective series resistance) film or ceramic type to keep spike voltage to a minimum.

C4 and R5 (shown in dashed lines) form an optional damper which eliminates primary ringing for light output load conditions when secondary current drops to zero during switch off time (discontinuous operation). Typical values are $R = 300\Omega$ to $1.5\text{k}\Omega$, $C = 500$ to 5000pF .

Output Diode (D1)

The output diode has an *average* forward current equal to output current, but the current flows in pulses with an amplitude equal to:

$$I_{D1(PEAK)} = I_{OUT} \left(1 + \frac{V_{OUT} + V_f}{N \cdot V_{IN}}\right) \quad (86)$$

For the circuit in Figure 22, with $I_{OUT} = 6\text{A}$:

$$I_{D1(PEAK)} = (6) \left(1 + \frac{5+0.7}{(1/3)(24)}\right) = 10.3\text{A}$$

To calculate diode power dissipation, use the forward voltage at this peak current multiplied times output current;

$$P_{D1} = (V_f)(I_{OUT})$$

$V_f = D1$ forward voltage at peak current

With $V_f = 0.55V$ and $I_{OUT} = 6A$, $D1$ power dissipation is 3.3W.

During start-up and overload conditions $D1$ current will increase significantly. Average diode current through $D1$ when the LT1070 is in current limit is equal to:

$$I_{D1} = \frac{\alpha \cdot (I_{LIM} \cdot V_{IN})}{N V_{IN} + V_{OUT} + V_f} \quad (87)$$

α is an empirical multiplier slightly less than unity. It is very complex to calculate, but it takes into account such things as switch resistance, leakage inductance, snubber losses, and transformer losses. If we assume $\alpha = 0.8$, $I_{LIM} = 9A$, $V_{IN} = 24V$, $N = 1/3$, $V_f = 0.55V$, and a shorted output, ($V_{OUT} = 0$):

$$I_{D1} = \frac{0.8(9 \cdot 24)}{1/3(24) + 0 + 0.8} = 20A$$

Peak diode current will be only slightly higher because the duty cycle of the diode is approaching 100% with $V_{OUT} = 0$.

Output short circuit current can be reduced if desired by clamping the V_C pin of the LT1070. The best way to do this and still be assured of maximum full load current is to clamp the V_C pin to a portion of output voltage. This generates a foldback current limit that will reduce short circuit current without affecting normal load current. The clamp network in Figure 24 will reduce shorted output current of the circuit in Figure 22 to $\approx 5A$.

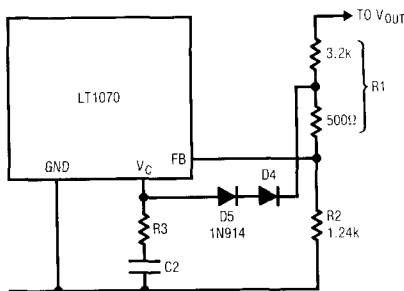


Figure 24. Foldback Current Limiting

The clamp point is generated by splitting $R1$ into two resistors such that the tap point voltage is $\approx 1.75V$ at normal output voltage. This ensures that $D4$ will not turn on until the output voltage begins to drop. When $V_{OUT} = 0V$, the voltage at the FB pin is clamped to approximately 0.35V by the internal mode select circuitry and the voltage at the $R1$ tap point will be approximately the same. The current through the diodes will be maximum available V_C pin current. This sets the clamp voltage on the V_C pin at $\approx 1.55V$, reducing output short circuit current to $\approx 5A$. Full load current can be reduced if desired by moving the tap point on $R1$ down, even to the point where it becomes part of $R2$.

Output Capacitor (C1)

Flyback converters do not use the inductance of the transformer as a filter, so the output capacitor must do all the filtering work. The output peak-to-peak voltage ripple is equal to:

$$V_{p-p} = \frac{I_{OUT}}{f \cdot C1} \left(1 + \frac{N \cdot V_{IN}}{V_{OUT}}\right) + (ESR)(I_{OUT}) \left(1 + \frac{V_{OUT}}{N \cdot V_{IN}}\right) \quad (88)$$

ESR = effective series resistance of $C1$

The first term is the ripple due to the *capacitance* of $C1$; the second term is ripple due solely to the ESR of the capacitor. As it turns out, commercially available capacitors in the range required for this application (100–10,000 μF) have ESR high enough to dominate the ripple voltage. A 2000 μF capacitor for instance, might have a guaranteed ESR of 0.02 Ω . For $I_{OUT} = 6A$, $V_{OUT} = 5V$, $V_{IN} = 24V$, $N = 1/3$, this gives:

$$\begin{aligned} V_{p-p} &= \frac{6}{(40 \times 10^3)(2000 \times 10^{-6})} \left(1 + \frac{(1/3)(24)}{5}\right) \\ &\quad + (0.02)(6) \left(1 + \frac{5}{(1/3)(24)}\right) \\ &= 28.8mV + 195mV = 224mV \end{aligned}$$

The ESR term dominates and will be the main criteria for selecting the size of the output capacitor.

An alternative to brute force output capacitance (to obtain low ESR) is to add an LC output filter (shown as $L1$ and $C4$ in Figure 22). A relatively small inductor and capacitor can greatly reduce output ripple. If we assume the ripple across

Application Note 19

C1 is due solely to ESR, and therefore rectangular, the ratio of filter output ripple to input ripple is:

$$\frac{V_{OUT(p-p)}}{V_{IN(p-p)}} = r = \frac{ESR4 (V_{OUT}) (N \cdot V_{IN})}{(L1) (f) (V_{OUT} + N \cdot V_{IN})^2} \quad (89)$$

ESR4 = effective series resistance of C4

This formula again assumes that the ESR of C4 dominates its total impedance. For ESR4 = 0.1Ω, L1 = 10μH, V_{OUT} = 5V, N = 1/3, V_{IN} = 24V

$$r = \frac{(0.1)(5)(1/3 \cdot 24)}{(10 \times 10^{-6})(40 \times 10^3)(5 + 1/3 \cdot 24)^2} = 0.059$$

This is a 16:1 reduction in ripple, greatly easing the requirements on C1. Total output ripple, with a filter, is given by:

$$V_{p-p} = \frac{(ESR1)(ESR4)(V_{OUT})(I_{OUT})}{(L1)(f)(V_{OUT} + N \cdot V_{IN})} \quad (90)$$

For ESR1 = 0.05Ω, ESR4 = 0.1Ω, V_{OUT} = 5V, V_{IN} = 24V, N = 1/3, I_{OUT} = 6A, L1 = 10μH, output ripple (p-p) is:

$$V_{p-p} = \frac{(0.05)(0.1)(5)(6)}{(10 \times 10^{-6})(40 \times 10^3)(5 + 1/3 \cdot 24)} = 28.8mV$$

TOTALLY ISOLATED CONVERTER

The LT1070 has a second operating mode called "isolated fly-back," as shown in Figure 25 (see Note 1 with figure). While in this mode, it does not use the feedback pin to sense output voltage; instead, it senses and regulates the transformer primary voltage during switch "off" time (t_{OFF}). This voltage is related to V_{OUT} by:

$$V_{OUT} = (N) (V_{PRI}) - V_f \quad (90)$$

(during t_{OFF})

N = turns ratio of transformer

V_f = forward voltage of output diode

V_{PRI} = primary voltage during switch "off" time

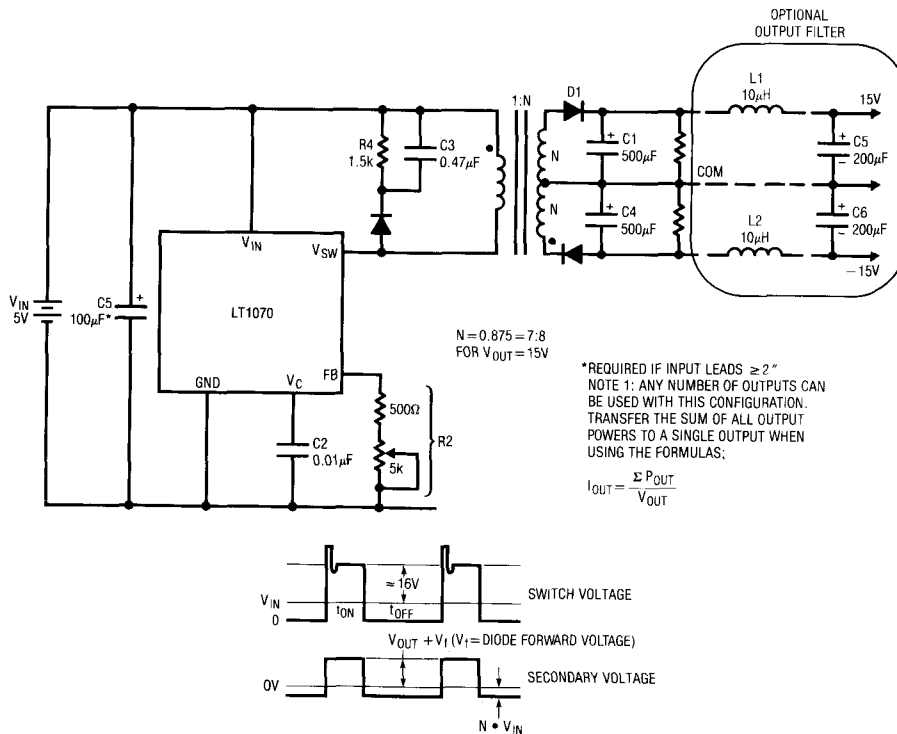


Figure 25. Totally Isolated Converter

The secondary output voltage will be regulated if V_{PRI} is regulated. The LT1070 switches from normal mode to regulated primary mode when the current *out* of the feedback pin exceeds $\approx 10\mu\text{A}$. An internal clamp holds the voltage (V_{FB}) on this pin at $\approx 400\text{mV}$. R_2 is used to put the LT1070 in isolated flyback mode. It also doubles as an adjustment in the regulated output. V_{PRI} is regulated to $16\text{V} + 7\text{k} (V_{FB}/R_2)$, where V_{FB}/R_2 is equal to the current through R_2 , and the 7k is an internal resistor. V_{OUT} is therefore equal to:

$$V_{OUT} = N \left[16 + 7\text{k} \left(\frac{V_{FB}}{R_2} \right) \right] - V_f \quad (91)$$

and the required transformer turns ratio is:

$$N = \frac{V_{OUT} + V_f}{16 + 7\text{k} \left(\frac{V_{FB}}{R_2} \right)} \quad (92)$$

The term, $7\text{k} (V_{FB}/R_2)$ is normally set to $\approx 2\text{V}$ to allow some adjustment range in V_{OUT} . Solving for N in Figure 25, with $V_{OUT} = 15\text{V}$:

$$N = \frac{15 + 0.7}{16 + 2} = 0.872$$

The smallest integer ratio with N close to 0.872 is $7:8 = 0.875$. T_1 is to be wound with this turns *ratio* for each output. The *total* number of turns is determined by the required primary inductance, (L_{PRI}). This inductance has no optimum value; it is a trade off between core size, regulation requirements, and leakage inductance effects. A reasonable starting value is found by assigning a maximum magnetizing current (ΔI) of 10% of the peak switch current of the LT1070. Magnetizing current is the difference between the primary current at the start of switch "on" time and the current at the end of switch "on" time. This gives a value for L_{PRI} of:

$$L_{PRI} = \frac{V_{IN}}{(\Delta I) (f) \left(1 + \frac{V_{IN}}{V_{PRI}} \right)} \quad (93)$$

ΔI = primary magnetizing current

V_{PRI} = regulated primary flyback voltage

For $V_{IN} = 5\text{V}$, $\Delta I = 0.5\text{A}$, $V_{PRI} = 18\text{V}$:

$$L_{PRI} = \frac{5}{(0.5)(40 \times 10^3)(1 + 5/18)} = 196\mu\text{H}$$

Again, this value is not an optimum figure, it is simply a compromise between maximum output current and core size.

A second consideration on primary inductance is the transition from continuous mode to discontinuous mode. At light output loads, the flyback pulse across the primary will drop toward zero before the end of switch "off" time. The LT1070 interprets this as a drop in output voltage and raises duty cycle to compensate. This results in an abnormally high output voltage. To avoid this situation, the output should have a minimum load equal to:

$$I_{OUT(MIN)} = \frac{(V_{PRI} \cdot V_{IN})^2}{(V_{PRI} + V_{IN})^2 (2 V_{OUT}) (f) (L_{PRI})} \quad (94)$$

with $V_{PRI} = 18\text{V}$, $V_{IN} = 5\text{V}$, $V_{OUT} = 15\text{V}$, $L_{PRI} = 200\mu\text{H}$:

$$I_{OUT(MIN)} = \frac{(18 \cdot 5)^2}{(18 + 5)^2 (2 \cdot 15) (40 \times 10^3) (200 \times 10^{-6})} = 64\text{mA}$$

This current may be shared equally on each output at 32mA per output. If a lighter minimum load is desired, primary inductance must be increased. This also increases leakage inductance, so some care must be used.

Leakage inductance is a portion of the primary which is not coupled to the secondary. This leakage inductance will create a flyback spike following switch opening. The height of this spike must be clamped with a snubber (R_4 , C_3 , D_2) to avoid overvoltage on the switch. (Please read snubber details in the section on normal mode flyback regulators). The *width* of the leakage inductance spike is equal to:

$$t_L = \frac{(I_{PRI}) (L_L)}{V_M - V_{PRI} - V_{IN}} \quad (95)$$

L_L = leakage inductance

I_{PRI} = peak primary current

V_M = peak switch voltage

This spike width is important because it must be less than $1.5\mu\text{s}$ wide. The LT1070 has internal blanking for $\approx 1.5\mu\text{s}$ following switch turn-off. This blanking time ensures that the flyback error amplifier will not interpret the leakage inductance spike as the actual flyback voltage to be regulated. To avoid poor regulation, the spike must be less than the blanking time.

If transformer T_1 is trifilar wound for minimum leakage inductance, L_L may have a typical value of 1.5% of L_{PRI} . Assuming

Application Note 19

$L_{PRI} = 200\mu\text{H}$, L_L would be $3\mu\text{H}$. To calculate t_L , we still need to assign a value to V_M . In this case, with $V_{IN} = 5\text{V}$, a conservative value for maximum switch voltage would be $V_M = 50\text{V}$. If we assume a maximum primary current of 5A for maximum output current, spike width is:

$$t_L = \frac{(5)(3 \times 10^{-6})}{50 - 18 - 5} = 0.56\mu\text{s}$$

This is well within the maximum value of $1.5\mu\text{s}$. Note, however, that the pulse width grows rapidly as the sum of $V_{PRI} + V_{IN}$ approaches maximum switch voltage. The following formula will allow one to calculate the maximum ratio of leakage inductance to primary inductance in a given situation.

$$\frac{L_L}{L_P}(\text{MAX}) = \frac{t_L \cdot (V_M - V_P - V_{IN})(\Delta I)(f) \left(1 + \frac{V_{IN}}{V_P}\right)}{I_{PRI}(V_{IN})} \quad (96)$$

With a fairly large V_{IN} (36V), even if we use a less conservative value of 60V for V_M , with $t_L = 1.5\mu\text{s}$, $V_P = 18\text{V}$, $\Delta I = 0.5\text{A}$, and $I_{PRI} = 5\text{A}$:

$$\frac{L_L}{L_P}(\text{MAX}) = \frac{(1.5 \times 10^{-6})(60 - 18 - 36)(0.5)(40 \times 10^3) \left(1 + \frac{36}{18}\right)}{(5)(36)} = 0.003 = 0.3\%$$

This low ratio of leakage inductance to primary inductance would be nearly impossible to wind, so some compromises must be made. If maximum output current is not required, I_{PRI} will be less than 5A , (see formula 99). Ripple current (ΔI) can also be increased. Finally, an LT1070HV (high voltage) part can be used, with a switch rating of 75V . Substituting $I_{PRI} = 2.5\text{A}$, $\Delta I = 1\text{A}$, $V_M = 70\text{V}$ into the above calculation yields $L_L/L_{PRI} = 3\%$, which is easily achievable.

Maximum output power with an isolated flyback converter is less than an ordinary flyback converter because transformer turns ratio is fixed by output voltage. This fixes duty cycle at:

$$\text{DC} = \frac{V_{PRI}}{V_{PRI} + V_{IN}} \quad (97)$$

and maximum power is limited to:

$$P_{OUT(\text{MAX})} = \left(\frac{V_{PRI}}{V_{PRI} + V_{IN}}\right) \left[V_{IN} \left(I_P - \frac{\Delta I}{2} \right) - (I_P)^2 R \right] (0.8) \quad (98)$$

$R = \text{LT1070 switch "on" resistance}$

$I_P = \text{maximum switch current}$

$0.8 = \text{fudge factor to account for losses in addition to } R$

With V_{PRI} at a nominal 18V , $V_{IN} = 5\text{V}$, $I_P = 5\text{A}$, $\Delta I = 0.5\text{A}$, duty cycle is 78% and maximum output power is:

$$P_{OUT(\text{MAX})} = \left(\frac{18}{18+5}\right) \left[5 \left(5 - \frac{0.5}{2} \right) - (5)^2 (0.2) \right] (0.8) = 11.74\text{W}$$

An analysis of the power formula shows that at low V_{IN} , maximum output power is proportional to V_{IN} , and at high V_{IN} , maximum power approaches 50W .

Peak primary current for loads less than the maximum is found from:

$$I_{PRI} = \frac{(V_{OUT})(I_{OUT})(V_{PRI} + V_{IN})}{0.8(V_{PRI})(V_{IN})} + \frac{\Delta I}{2} + \sqrt{\frac{(I_{PRI})^2 R}{V_{IN}}} \quad (99)$$

This formula is actually a quadratic, but rather than solve it explicitly, a much simpler technique, for the range of I_{PRI} involved, is to calculate the first two terms on the right, then use this value of I_{PRI} to calculate the last term. For the circuit in Figure 25 with $I_{OUT} = 0.25\text{A}$ on each output, $V_{PRI} = 18\text{V}$, $V_{IN} = 5\text{V}$, $\Delta I = 0.5\text{A}$, $R = 0.2\Omega$:

$$I_{PRI} = \underbrace{\frac{(15)(0.5)(18+5)}{0.8(18)(5)}}_{2.64\text{A}} + \frac{0.5}{2} + \frac{(2.64)^2(0.2)}{5} = 2.92\text{A}$$

The transformer must be sized so that the core does not saturate with 2.92A in the primary winding. Note that there is plenty of margin on 5A maximum switch current. A smaller core could be used if ΔI were increased to 1A , cutting primary inductance in half. (See section on inductors and transformers.)

Output Capacitors

Flyback regulators do not utilize the inductance of the transformer as a filter, so all filtering must be done by the output

capacitors, C1 and C4. They should be low ESR types to minimize output ripple. In general, output ripple is limited by the ESR of the capacitor, not the actual capacitance. Output ripple in peak-to-peak volts is given by:

$$V_{p-p} = \frac{I_{PRI}}{2 \cdot N} (\text{ESR}) \quad \text{*This factor of 2 is used because of dual outputs.} \quad (100)$$

With $I_{PRI} = 2.92\text{A}$, $N = 0.872$, and assigning an ESR of 0.1Ω , output ripple is:

$$V_{p-p} = \frac{(2.92)(0.1)}{(2)(0.872)} = 167\text{mV}_{p-p} \text{ @ full load}$$

Had we based the output ripple formula on the actual output capacitance, rather than its ESR, the result would have been $\approx 10\text{mV}$, showing that ESR effects do dominate. The 0.1Ω value chosen for ESR is probably *higher than typical* for a good $500\mu\text{F}$ capacitor, but *less than guaranteed maximum*. Note that one reason for high output ripple in this circuit is that the converter is operating at a rather high duty cycle of 78% because of the low input voltage. This leaves only 22% of the time for the secondary to be delivering current to the load. As a consequence, secondary peak currents, and therefore output ripple, are high.

If low output ripple is required, an output filter may be a better choice than simply using huge output capacitors. See section on Output Filters.

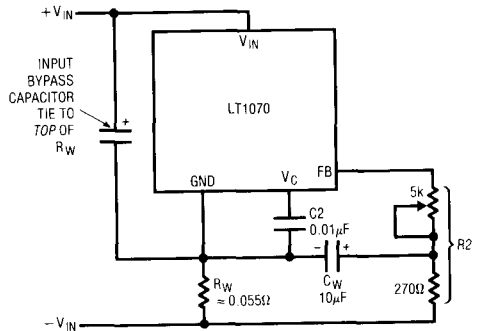
Load and Line Regulation

Load and line regulation are affected by many "open loop" factors in this circuit because the actual output voltage is not sensed—only the primary. Some of these factors are core nonlinearities, diode resistance, leakage inductance, winding resistance, (including skin effect) capacitor ESR, and secondary inductance. A typical load regulation for this circuit with a load variation from 20% to 100% is $\approx 3\%$. Line regulation at light loads is better than 0.3% for $V_{IN} = 4.5\text{V}$ to 5.5V , but degrades to $\approx 1\%$ for full loads.

With multiple output supplies obtained from a single switching loop, the problem of cross regulation appears. In this supply, an *increase* in load current from 50mA to 200mA on one output, with a constant 50mA load on the second output, will cause the loaded output to *drop* 280mV and the constant load output to *rise* 100mV .

If improved line and load regulation are necessary, a modification can be made to the basic circuit as shown below:

Load Current Compensation



R_2 is split into two resistors with the center tap coupled to the ground pin of the LT1070 through C_W . A small resistor R_W is inserted in series with the ground pin. When a load is applied to the output, input current flowing through R_W causes the voltage drop across R_2 to increase. This increases regulated primary voltage and thereby output voltage, cancelling the open loop load regulation effects mentioned earlier. Line regulation is also significantly improved at full load.

The value of R_W is found from:

$$R_W = \frac{(r_O)(V_{IN})(E)(R_2)}{(V_{OUT})(7k)(N)^*} \quad (101)$$

r_O = output resistance without compensation = $\Delta V_{OUT}/\Delta I_{OUT}$
 E = efficiency ≈ 0.75

*Multiply N by two for dual outputs

For the circuit in Figure 25, r_O is found by loading both outputs simultaneously, and summing the changes of the two outputs. With 3% load regulation, @ $\Delta I_{OUT} = 200\text{mA}$, this is a total output change of 900mV . r_O is then 900mV divided by a current change of 200mA , or 4.5Ω . V_{OUT} is the sum of the two outputs, = 30V , N is $0.875 \times 2 = 1.75$, and R_2 is $\approx 1.2\text{k}$:

$$R_W = \frac{(4.5)(5)(0.75)(1,200)}{(30)(7k)(1.75)} = 0.055\Omega$$

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This low value of resistance preserves the efficiency of the converter, but is sometimes hard to find "off the shelf". A 15" length of #26 hookup wire was used for the breadboard. To minimize inductance, the wire is folded in half before winding around a form.

C_W must be made large enough to prevent loop oscillation problems. The product of C_W times the parallel resistance of the two halves of R_2 should be several times larger than the basic regulator settling time constant.

With load regulation compensation, the effects of cross regulation are worse than with no compensation. Multiple output supplies should be carefully evaluated for all expected conditions of output loading.

Frequency Compensation

The frequency compensation capacitor C_2 , is much lower in this design than in others because the gm of the LT1070 is much lower in the isolated mode than in the normal mode. See frequency compensation section for details.

POSITIVE CURRENT BOOSTED BUCK CONVERTER

A current boosted buck converter is shown in Figure 26. It can supply more output current than a standard buck converter or a flyback converter for larger input-output differentials because current flows to the output both when the switch is on *and* when it is off. The "on" cycle can supply up to 5A to the load. The off cycle will deliver 1/N times that much current. With $N = 1/3$, current delivered to the load during switch off time will be 15A. Total available load current will depend on switch duty cycle, which in turn is fixed by input voltage.

An operational amplifier must be added to generate a feedback signal which floats on top of the regulated output because that is where the ground pin of the LT1070 is tied. A1 is an LM308 selected because its output goes *low* when both its inputs are equal to the op amp negative supply voltage. This condition occurs at $V_{OUT} = 0$ during start-up. If the op-amp output went *high* during this condition, the LT1070 would never start up. R1 and R2 set output voltage, with the bottom of R1 returned directly to the load for "low" sensing. R4 and

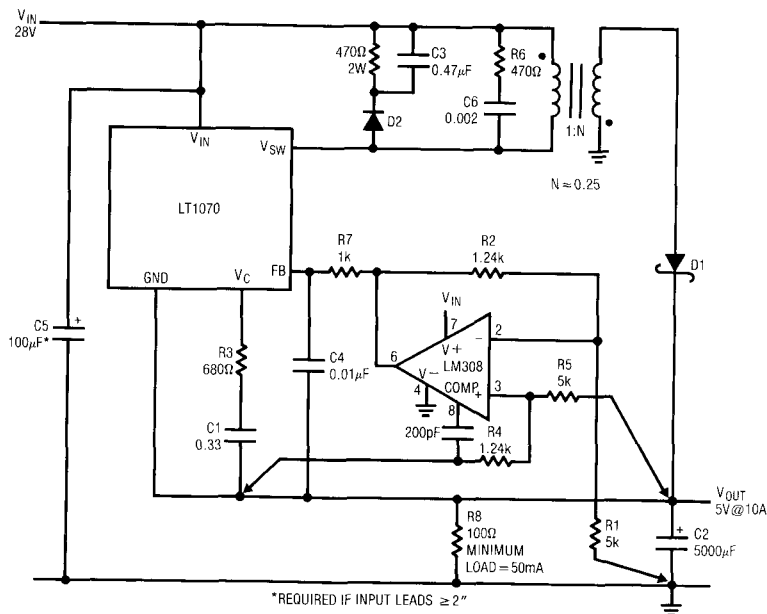


Figure 26. Positive Current Boosted Buck Converter

R5 force Kelvin sensing between the output and the ground pin of the LT1070. It appears that these resistors are shorted out, but the voltage drop across the wire from the ground pin of the LT1070 to the output will cause load regulation problems unless it is "sensed" by R4 and R5. These resistors can be eliminated if that wire is heavy gauge and less than 2" long.

The following equations should be helpful in designing variations of this circuit.

$$R5 = \frac{(V_{OUT}) \cdot (R1)}{V_{REF}} = \frac{(V_{OUT}) \cdot (1.24k)}{1.244V} \quad (102)$$

$$\frac{R5}{R4} = \frac{R1}{R2} \quad (103)$$

$$N_{(MIN)} = \frac{V_{OUT} + V_f}{V_M - V_{IN} - V_{SNUB}} \quad (104)$$

$$DC = \frac{V_{OUT} + V_f}{V_{OUT} + V_f + N(V_{IN} - V_{OUT})} \quad (105)$$

$$L_{PRI} = \frac{V_{OUT}}{(\Delta I) \cdot f \cdot \left(N + \frac{V_{OUT}}{V_{IN} - V_{OUT}} \right)} \quad (106)$$

$$V_{p-p} = (ESR) (I_{OUT}) \frac{\left(\frac{V_{OUT}}{N} + V_{IN} - V_{OUT} \right) (1 - N)}{V_{IN}} \quad (107)$$

$$I_{OUT(MAX)} = \left(I_P - \frac{\Delta I}{2} \right) \left[\frac{V_{IN}}{V_{OUT} + V_f + N(V_{IN} - V_{OUT})} \right] \quad (0.8) \quad (108)$$

$$I_{PRI} = \frac{I_{OUT}}{V_{IN}} [V_{OUT} + N(V_{IN} - V_{OUT})] \quad \left(\text{Add } \frac{\Delta I}{2} \text{ for peak primary current} \right) \quad (109)$$

- N = turns ratio
- V_M = LT1070 maximum switch voltage
- V_{SNUB} = snubber voltage (see flyback section)
- V_f = forward voltage of D1
- DC = switch duty cycle
- ΔI = peak-to-peak primary ripple current
- ESR = effective series resistance of C2
- I_{PRI} = average primary current during switch on time
- V_{p-p} = peak-to-peak output ripple voltage
- I_P = max rated switch current for LT1070

The value for N_(min) is based on switch breakdown. Low values give higher output current, but also higher switch voltage. ΔI is normally chosen at 20 to 40% of I_{PRI}. Note that the ripple equation contains the term (1 - N) in the numerator, implying that output ripple current and voltage will be zero for N = 1. This is because of the simplifying assumption that ripple current into the output capacitor is the difference between primary and secondary current. This difference is zero for N = 1, and the equation is no longer valid.

NEGATIVE CURRENT BOOSTED BUCK CONVERTER

The negative buck converter in Figure 27 is capable of much higher output current than the standard buck converter upper limit of 5A. For design details, see positive current boosted buck converter and standard negative buck converter.

NEGATIVE INPUT-NEGATIVE OUTPUT FLYBACK CONVERTER

This circuit in Figure 28 is normally used for negative output voltages *higher* than the negative input. If voltages *lower* than the input are required, see negative buck converter or negative current boosted buck converter and standard negative buck converter.

The voltage divider, R1 and R2, is required to prevent forward bias on Q1. Connect R1, R2, and R3 exactly as shown for proper output sensing. Further design details may be taken from positive flyback converter section.

POSITIVE TO NEGATIVE FLYBACK CONVERTER

The positive input-negative output flyback converter in Figure 29 requires an external op-amp to generate the feedback signal for the LT1070. R1 and R2 set output voltage with R1 scaled at 1kΩ/V. The bottom of R1 goes directly to the output for sensing. R3 and R4 provide the ground (low) sense. Any voltage drop between the ground pin of the LT1070 and the actual ground (+) output can cause load regulation problems. These are eliminated if R3 and R4 are connected exactly as shown. R3 and R4 can be eliminated if the LT1070 ground pin is connected directly to output ground with a very short heavy wire.

For design details, see positive flyback converter.

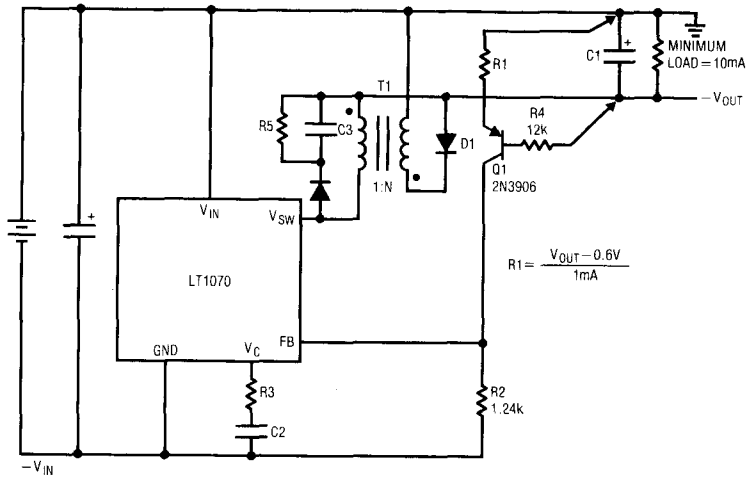


Figure 27. Negative Current Boosted Buck Converter

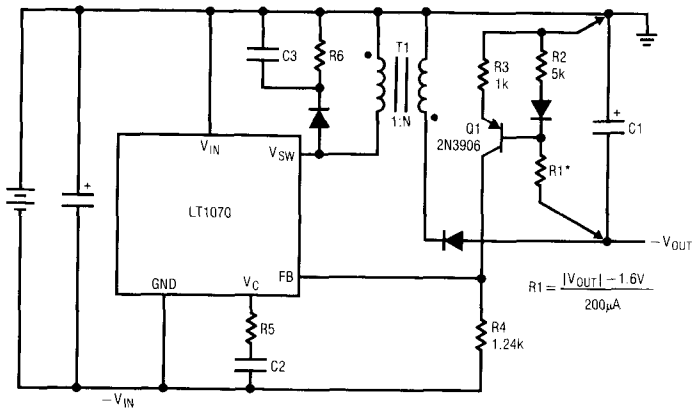


Figure 28. Negative Input-Negative Output Flyback Converter

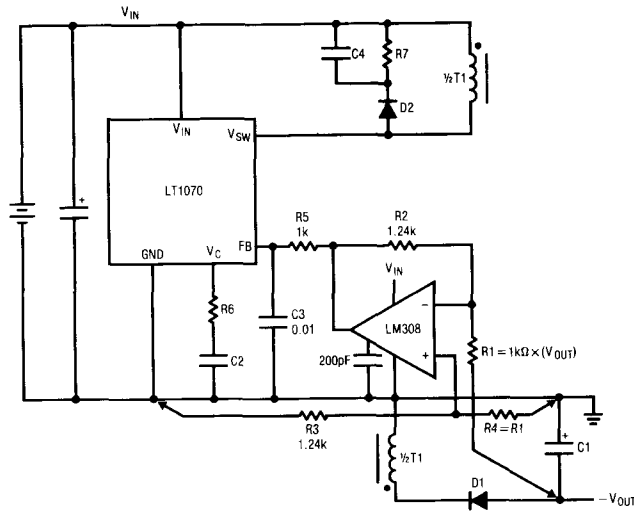


Figure 29. Positive Input-Negative Output Flyback Converter

VOLTAGE BOOSTED BOOST CONVERTER

The standard boost converter has a maximum output voltage slightly less than the maximum switch voltage of the LT1070. If higher voltages are desired, the inductor can be tapped as shown in Figure 30. The effect of the tap is to reduce peak switch voltage by;

$$(V_{OUT} - V_{IN}) \left(\frac{N}{1 + N} \right) \text{ volts.}$$

A large value for N will allow high output voltages to be regulated without exceeding maximum switch voltage.

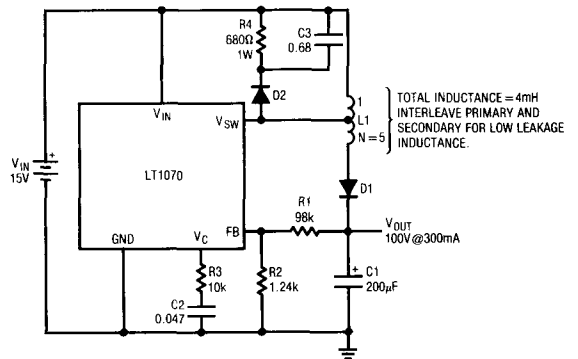


Figure 30. Voltage Boosted Boost Converter

Application Note 19

A snubber is needed now to handle leakage inductance of the tap point. The following formulas will be helpful for variations on this design.

$$N(\text{min}) = \frac{V_{\text{OUT}} - V_M + V_{\text{SNUB}}}{V_M - V_{\text{IN}} - V_{\text{SNUB}}} \quad (\text{Use max } V_{\text{IN}}) \quad (110)$$

$$\text{DC} = \frac{V_{\text{OUT}} - V_{\text{IN}}}{V_{\text{OUT}} + (N) \cdot (V_{\text{IN}})} \quad (111)$$

$$I_{\text{OUT(MAX)}} = \frac{I_P - \frac{\Delta I}{2} (V_{\text{IN}})}{V_{\text{OUT}} + (N) \cdot (V_{\text{IN}})} \quad (112)$$

$$I_{\text{PRI}} = \frac{I_{\text{OUT}} (V_{\text{OUT}} + N V_{\text{IN}})}{(V_{\text{IN}})} \quad \text{Average during switch on time. For peak, add } \frac{\Delta I}{2} \quad (113)$$

$$L_{\text{PRI}} = \frac{V_{\text{IN}} (V_{\text{OUT}} - V_{\text{IN}})}{(\Delta I) (f) (V_{\text{OUT}} + N V_{\text{IN}})} \quad (114)$$

$$\Delta I \approx 20 \text{ to } 40\% \text{ of } I_{\text{PRI}}$$

$$V_{\text{p-p}} = \frac{(I_{\text{OUT}}) (\text{ESR}) (V_{\text{OUT}} + N V_{\text{IN}})}{V_{\text{IN}} (N + 1)} \quad (115)$$

DC = switch duty cycle

V_{SNUB} = snubber voltage (see flyback section for details)

V_M = maximum allowed LT1070 switch voltage

I_P = maximum LT1070 switch current

ΔI = peak-to-peak primary current ripple

ESR = effective series resistance of C

$V_{\text{p-p}}$ = peak-to-peak output voltage ripple

L1 should be wound for minimum leakage inductance by using bifilar winding or interleaved windings. R3 and C2 are selected using the technique described in the frequency compensation section. For snubber details see flyback description section. This regulator is not short-circuit proof because L1 and D1 short input to ground when output is shorted.

NEGATIVE BOOST CONVERTER

The LT1070 can be used as a negative boost regulator as shown in Figure 31 by using the same diode-coupled feedback technique used in the positive buck mode. Basically, D2 and C3 create a peak detector which gives a voltage across C3 equal to the output voltage. R1 and R2 act as a voltage divider to set output voltage at $(V_{\text{REF}}) (R1 + R2)/R2$. C3 also acts as a floating power supply for the LT1070. The ground pin of the LT1070 switches back and forth between the output voltage and ground to drive the inductor, L1. For proper circuit operation, a minimum preload of 10mA is required on the output (shown as R_0).

For further design information, see positive boost converter for details on L1, C1, D1, and output filters. The feedback scheme used here is discussed in more detail in the positive buck section. A refinement in the feedback is that the power transistor driver current flowing into the V_{IN} pin must come from D2 and C3. This tends to compensate for the series resistance of D1 as it affects load regulation.

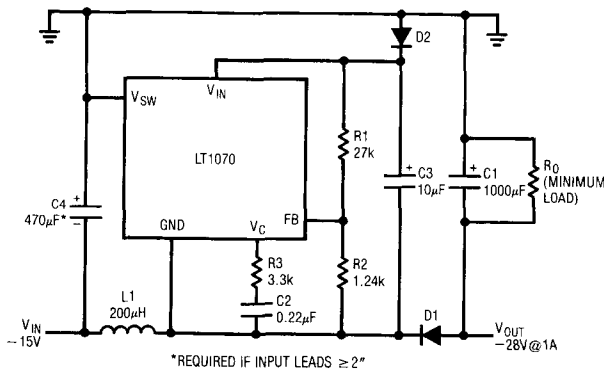


Figure 31. Negative Boost Regulator

POSITIVE TO NEGATIVE BUCK-BOOST CONVERTER

This positive to negative converter uses the same feedback technique as the positive buck converter. Normal feedback cannot be used because the ground pin of the LT1070 is switching back and forth between $+V_{IN}$ and $-V_{OUT}$. To generate a floating feedback signal, D2 peak detects the output voltage during the LT1070 switch off time. This voltage appears across C3 as a floating DC level which is used as feedback to the LT1070. Output voltage is set by the ratio of R1 to R2. R4 is used to limit the effect of turn-on spikes across the main catch diode, D1. Without this resistor, D1 turn-on spikes would cause C3 to charge to an abnormally high voltage and the output voltage would sag down at high load currents.

D3 and C4 are used to generate a floating supply for the LT1070. The voltage across C4 will peak detect to (V_{OUT}) volts. R5 is added to ensure start-up. R6 is a preload, required only if the normal load can drop to zero current.

For further design details on this circuit, the basic formulas from the negative to positive buck/boost converter may be used, along with the feedback explanation from the positive buck converter.

CURRENT BOOSTED BOOST CONVERTER

This tapped-inductor version of the boost converter can offer significant increases in output power when the input-output voltage differential is not too high. The ratio of output current for this converter compared to a standard boost converter is:

$$\frac{I_{OUT}}{I_{BOOST}} = \frac{N + 1}{N \left(1 - \frac{V_{IN}}{V_{OUT}}\right) + 1}$$

If $V_{OUT} - V_{IN}$, the increase in output current approaches $N + 1$. Maximum N , however, is limited by switch breakdown voltage;

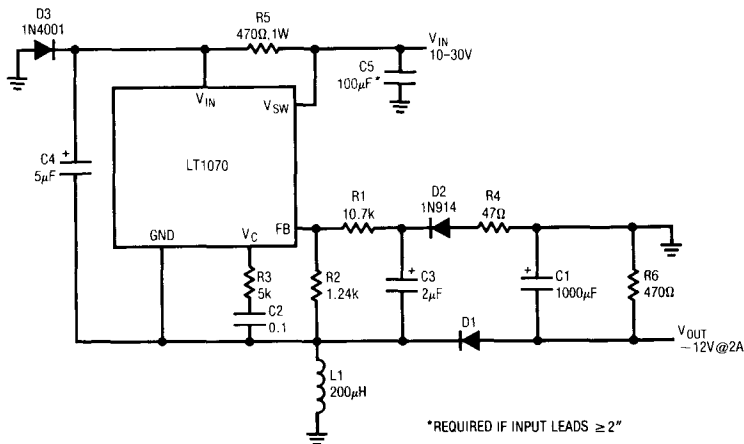
$$N(\max) = \frac{V_M - V_{OUT} - V_{SNUB}}{V_{OUT} - V_{MIN}}$$

V_M = maximum LT1070 switch voltage
 V_{SNUB} = snubber voltage (see Flyback section)
 V_{MIN} = minimum input voltage

For $V_M = 60V$, $V_{OUT} = 28V$, $V_{SNUB} = 8V$, $V_{MIN} = 16V$

$$N(\max) = \frac{60 - 28 - 8}{28 - 16} = 2$$

Positive to Negative Buck-Boost Converter



*REQUIRED IF INPUT LEADS ≥ 2 "

Application Note 19

The increase in output current is;

$$\frac{I_{OUT}}{I_{BOOST}} = \frac{2+1}{2 \left(1 - \frac{16}{28}\right) + 1} = 1.62 = 62\%$$

Actual maximum output current is:

$$I_{OUT(max)} = \frac{(I_P - \Delta I/2)}{\frac{V_{OUT}}{V_{MIN}} - \frac{N}{N+1}} = \frac{(5 - 0.5)}{\frac{28}{16} - \frac{2}{3}} = 4.15A$$

I_P = maximum LT1070 switch current

ΔI = increase in inductor current during switch on time

$$\Delta I = \frac{V_{OUT} - V_{IN}}{(L)(f) \left(\frac{V_{OUT}}{V_{IN}} - \frac{N}{N+1} \right)} \quad (L = \text{total inductance})$$

operating duty cycle is given by;

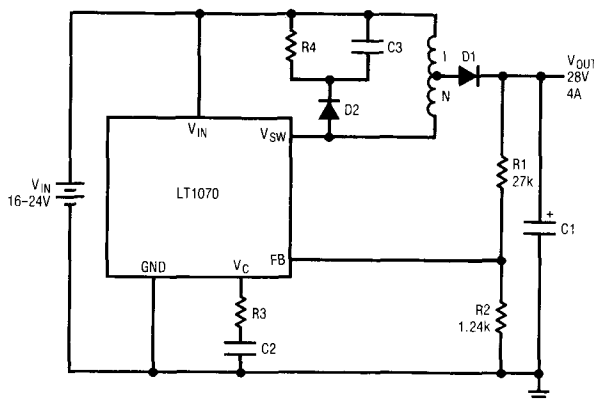
$$DC = \frac{V_{OUT} - V_{IN}}{V_{OUT} - \left(\frac{N}{N+1} \right) (V_{IN})}$$

A reasonable value for total inductance is found by assuming that this circuit is used near peak switch current of 5A, and allowing a 20% increase in switch current during switch on time – $\Delta I = 1A$

$$L(\text{total}) = \frac{V_{OUT} - V_{MIN}}{(f)(\Delta I) \left(\frac{V_{OUT}}{V_{MIN}} - \frac{N}{N+1} \right)} = \frac{28 - 16}{(40 \cdot 10^3)(1) \left(\frac{28}{16} - \frac{2}{3} \right)} = 277 \mu H$$

Snubber values are empirically selected to limit snubber voltage to the value chosen ($\approx 8V$). For lowest snubber losses, the "1" and "N" sections of the inductor should be wound for maximum coupling (consult manufacturers).

Current Boosted Boost Converter



FORWARD CONVERTER

Forward converters can use smaller cores than flyback converters because they do not need to store energy in the core. Energy is transferred directly to the output during switch "on" time. The output secondary (N) is positive and delivering current through D1 when the LT1070 switch is on (V_{SW} low). At switch turn off, the output winding goes negative and output current flows through D2 as in a buck regulator. A third winding (M) is needed in a single switch forward converter to define switch voltage during switch off time. This "reset" winding, however, limits the maximum duty cycle allowed for the switch. The voltage across the switch during its off state is:

$$V_{SW} = V_{IN} + \frac{V_{IN}}{M} + V_{SNUB}$$

V_{SNUB} = snubber voltage spike caused by leakage inductance

By rearranging this formula, a minimum value for M can be found:

$$M(\min) = \frac{V_{IN(\max)}}{V_M - V_{IN(\max)} - V_{SNUB}}$$

V_M = maximum LT1070 switch voltage

$V_{IN(\max)}$ = maximum input voltage

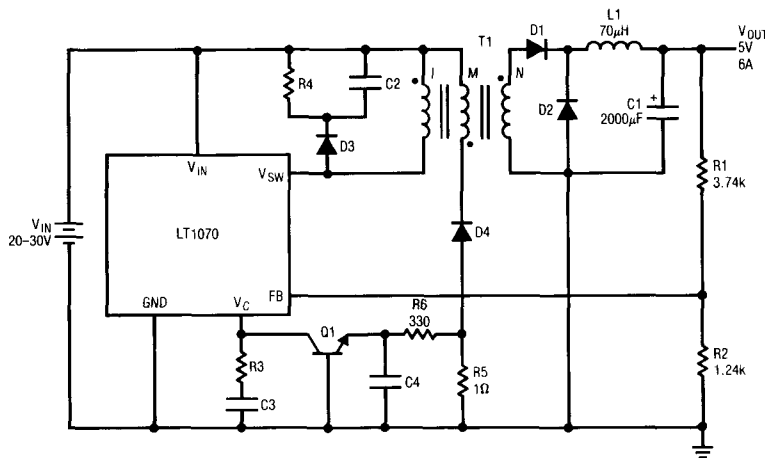
For the circuit shown, with $V_{IN(\max)} = 30V$, and selecting $V_{SNUB} = 5V$, and $V_M = 60V$:

$$M(\min) = \frac{30}{60 - 30 - 5} = 1.2$$

The value of M will define maximum switch duty cycle. If the LT1070 attempts to operate at a duty cycle above this limit, the core will saturate because the volt-second product across the primary in the switch off state will not be enough to keep flux balance. Duty cycle is limited to:

$$DC(\max) \frac{1}{1+M} = \frac{1}{1+1.2} = 45\%$$

Forward Converter



Application Note 19

For maximum output current, N should be as small as possible. Smaller values of N, however, require larger duty cycles, so N is limited to a minimum of:

$$N(\min) = \frac{(M + 1)(V_{OUT} + V_f)}{V_{IN(LOW)}}$$

V_f = D1 and D2 forward voltage

$V_{IN(LOW)}$ = minimum input voltage

For the circuit shown, with $V_f = 0.6V$, $V_{IN(LOW)} = 20V$:

$$N(\min) = \frac{(1.2 + 1)(5 + 0.6)}{20} = 0.62$$

To avoid core saturation during normal operation, primary inductance must be a minimum value determined by core volume and core flux density:

$$L_{PRI} \geq \left(\frac{V_{OUT} + V_f}{N \cdot B_M \cdot f} \right)^2 \left(\frac{0.4\pi \cdot \mu_e}{V_e \cdot 10^{-8}} \right)$$

B_M = maximum operating flux density

f = LT1070 operating frequency (40kHz)

V_e = core volume

μ_e = effective core permeability

For $B_M = 2000$ gauss (typical for ferrites), $V_e = 6cm^3$, and $\mu_e = 1500$, $V_{OUT} + V_f = 5.6V$, $N = 0.62$:

$$L_{PRI} \geq \left[\frac{5.6}{(0.62)(2000)(40 \times 10^3)} \right]^2 \frac{(0.4\pi)(1500)}{(6)(10^{-8})} = 400\mu H$$

The operating flux density of forward converters is often limited by temperature rise rather than saturation. At 2000 gauss, the core loss of a typical ferrite is $0.25W/cm^3$. Total core loss @ $V_e = 6cm^3 \approx 1.5W$. When this is combined with copper winding losses, there may be excess core temperatures. Larger cores will allow more space for copper, or can be operated at lower flux density with the same copper loss. See Transformer Design guide for further details.

Conventional forward converters use a flip-flop to limit maximum duty cycle to 50% and set $M = 1$. The LT1070 will let duty cycle go to $\approx 95\%$ during start up and low input voltage conditions. This would cause core saturation and subsequent primary and switch currents of up to 10A. To avoid this, Q1 and R5 have been added. Onset of core

saturation will cause a voltage drop across R5 high enough to turn on Q1 at each cycle. This pulls down on the V_C pin, reducing duty cycle and maintaining normal switch currents. R6 and C4 filter out spikes.

Operating duty cycle is given by:

$$DC = \frac{V_{OUT} + V_f}{N \cdot V_{IN}}$$

The output filter inductor (L1) is chosen as a tradeoff between maximum output power, output ripple, physical size, and loop transient response. A reasonable value is one which gives a peak-to-peak inductor ripple current (ΔI_L) of $\approx 20\%$ of I_{OUT} . This leads to a value for L1 of:

$$L1 = \frac{V_{OUT}(N \cdot V_{IN} - V_{OUT})}{(0.2 I_{OUT})(N \cdot V_{IN} \cdot f)}$$

for $I_{OUT} = 6A$, $V_{IN} = 25V$, $V_{OUT} = 5V$, $N = 0.62$:

$$L1 = \frac{5[(0.62)(25) - 5]}{(0.2)(6)(0.62)(25)(40 \times 10^3)} = 70\mu H$$

Larger values of L1 will increase maximum output current only slightly. Output ripple voltage will go down inversely with larger L1, but physical size will quickly become a problem for large values because the inductor must handle large DC currents. Peak inductor current is equal to $I_{OUT} + \Delta I_L/2$.

Maximum output current for this forward converter is given by:

$$I_{OUT(MAX)} = \left[\frac{I_P}{N} - \frac{\Delta I_L}{2} - \frac{\Delta I_{PRI}}{N} \right] 0.9$$

I_P = maximum LT1070 switch current

ΔI_{PRI} = peak primary magnetizing current

$$= V_{OUT}/(f \cdot N \cdot L_{PRI})$$

ΔI_L = peak-to-peak output inductor current

0.9 = fudge factor for losses

For $I_P = 5A$, $N = 0.62$, $\Delta I_L = 1.2A$, $\Delta I_{PRI} = 0.5A$;

$$I_{OUT(MAX)} = \left[\frac{5}{0.62} - \frac{1.2}{2} - \frac{0.5}{0.62} \right] 0.9 = 6A$$

Output voltage ripple (p-p) is assumed to be set by L1 and the ESR of C1:

$$V_{p-p} = (\Delta I_L) (ESR1) = \frac{ESR1 (V_{OUT}) (N \cdot V_{IN} - V_{OUT})}{(L1) (f) (N) (V_{IN})}$$

ESR1 = effective series resistance of C1

If we assume 0.02Ω for ESR1, and $V_{IN} = 25V$,

$$V_{p-p} = \frac{(0.02) (5) (0.62 \cdot 25 - 5)}{(70 \times 10^{-6}) (40 \times 10^3) (0.62) (25)} = 24mV_{p-p}$$

If less output ripple is desired, the most effective method may be to add an LC filter. See section on output filters.

FREQUENCY COMPENSATION

Although the architecture of the LT1070 is simple enough to lend itself to a mathematical approach to frequency compensation, the added complication of input and/or output filters, unknown capacitor ESR, and gross operating point changes with input voltage and load current variations all suggest a more practical empirical method. Many hours spent on breadboards have shown that the simplest way to optimize the frequency compensation of the LT1070 is to use transient response techniques and an "RC box" to quickly iterate toward the final compensation network.

There are many ways to inject a transient signal into a switching regulator, but the suggested method is to use an AC coupled output load variation. This technique avoids problems of injection point loading and is general to all switching topologies. The only variation required may be an amplitude adjustment to maintain small signal conditions with adequate signal strength. Figure 32 shows the set-up.

A function generator with 50Ω output impedance is coupled through a 50Ω/1000μF series RC network to the regulator output. Generator frequency is non-critical. A good starting point is ≈50Hz. Lower frequencies may cause a blinking scope display which is annoying to work with. Higher frequencies may not allow sufficient settling time for the output transient. Amplitude of the generator output is typically set at 5Vp-p to generate a 100mA-p-p load variation. For lightly loaded outputs ($I_{OUT} < 100mA$), this level may be too high for small signal

response. If the positive and negative transition settling waveforms are significantly different, amplitude should be reduced. Actual *amplitude* is not particularly important because it is the *shape* of the resulting regulator output waveform which indicates loop stability.

A two-pole oscilloscope filter with $f = 10kHz$ is used to block switching frequencies. Regulators without added LC output filters have switching frequency signals at their outputs which may be much higher amplitude than the low frequency settling waveform to be studied. The filter frequency is high enough to pass the settling waveform with no distortion.

Oscilloscope and generator connections should be made exactly as shown to prevent ground loop errors. The oscilloscope is synced by connecting channel "B" probe to the generator output, with the ground clip of the second probe connected to exactly the same place as channel "A" ground. The standard 50Ω BNC sync output of the generator should *not* be used because of ground loop errors. It may also be necessary to isolate *either* the generator or oscilloscope from its third wire (earth ground) connection in the power plug to prevent ground loop errors in the 'scope display. These ground loop errors are checked by connecting channel "A" probe tip to exactly the same point as the probe ground clip. Any reading on channel "A" indicates a ground loop problem.

Once the proper set-up is made, finding the optimum values for the frequency compensation network is fairly straightforward. Initially, C2 is made large ($\geq 2\mu F$), and R3 is made small ($\approx 1k\Omega$). This nearly always ensures that the regulator will be stable enough to start iteration. Now, if the regulator output waveform is single-pole over-damped, (see the waveforms in Figure 33) the value of C2 is *reduced* in steps of about 2:1 until the response becomes slightly under-damped. Next, R3 is *increased* in steps of 2:1 to introduce a loop "zero". This will normally improve damping and allow the value of C2 to be further reduced. Shifting back and forth between R3 and C2 variations will now allow one to quickly find optimum values.

If the regulator response is under-damped with the initial large value of C, R should be increased immediately before larger values of C are tried. This will normally bring about the over-damped starting condition for further iteration.

Application Note 19

Just what is meant by "optimum values" for R3 and C2. This normally means the smallest value for C2 and the largest value for R3 which still guarantee no loop oscillations, and which result in loop settling that is as rapid as possible. The reason for this approach is that it minimizes the variations in output voltage caused by *input ripple voltage* and *output load transients*. A switching regulator which is grossly overdamped will never oscillate, but it may have unacceptably large output transients following sudden changes in input voltage or output loading. It may also suffer from excessive overshoot problems on start-up or short circuit recovery.

To guarantee acceptable loop stability under all conditions, the initial values chosen for R3 and C2 should be checked under all conditions of input voltage and load current. The simplest way of accomplishing this is to apply load currents of minimum, maximum, and several points in between. At each load current, input voltage is varied from minimum to maximum while observing the settling waveform. The additional time spent "worst-casing" in this manner is definitely necessary. Switching regulators, unlike linear regulators, have large shifts in loop gain and phase with operating conditions.

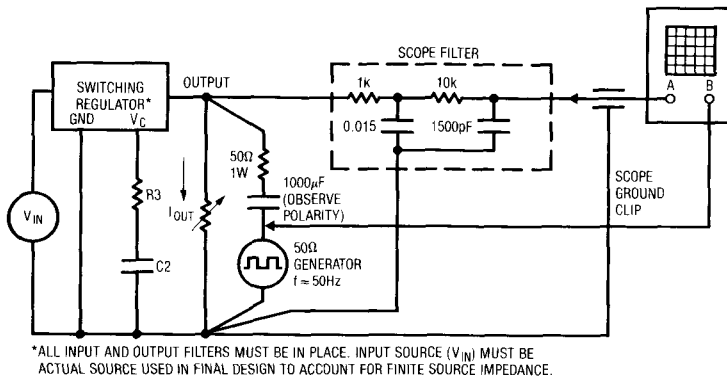


Figure 32. Testing Loop Stability

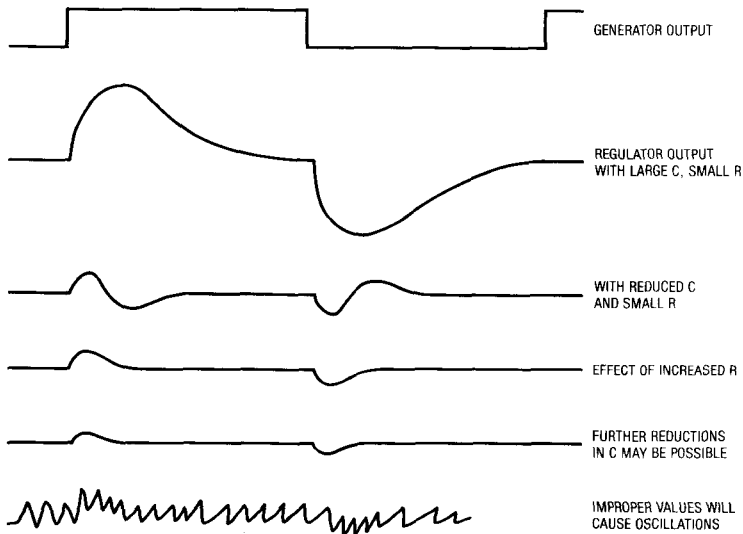


Figure 33. Output Transient Response

If large temperature variations are expected for the regulator, stability checks should also be done at the temperature extremes. There can be significant temperature variations in several key component parameters which affect stability; in particular, input and output capacitor value and their ESR, and inductor permeability. LT1070 parametric variations also need some consideration. Those which affect loop stability are error amplifier gm, and the transfer function of V_C pin voltage versus switch current (listed as a transconductance under electrical specifications.) For modest temperature variations, conservative over-damping under worst-case room temperature conditions is usually sufficient to guarantee adequate stability at all temperatures.

Check Margins

One measure of stability "margin" is to vary the selected values of both R and C by 2:1 in all possible combinations. If the regulator response remains reasonably well damped under all line and load conditions, the regulator can be considered fairly tolerant of parametric variations. Any tendency towards an under-damped (ringing) response indicates that a more conservative compensation may be needed.

There are several large signal dynamic tests which should also be done on a completed regulator design. The first is to check response to the worst-case large-amplitude load variation. A sudden change from light-load to full-load current may cause the regulator to have an unacceptably large transient dip in output voltage. The simplest cure for this is to increase the size of the output capacitor. Lower inductor values and less conservative frequency compensation also help. A second consideration is the output overshoot created when a

large load is suddenly removed. This is potentially more dangerous than a dip because a large overshoot may destroy loads still connected to the regulator output.

Eliminating Start-Up Overshoot

Another transient condition to be checked is *start-up overshoot*. When input voltage is first applied to a switching regulator, the regulator dumps full short-circuit current into the output capacitor attempting to bring the output up to its regulated value. The output can then overshoot well beyond its design value before the control loop is able to idle back the output current. The amplitude of the overshoot can be anywhere from millivolts to tens of volts depending on topology, line and load conditions, and component values. This same overshoot possibility exists for output recovery from output shorts. Again, larger output capacitors, smaller inductors, and faster loop response help reduce overshoot. There are also several ways to force slow start-up to eliminate the overshoot. The first is to put a capacitor across the output voltage divider. This creates a time-dependent output voltage setting during start-up and usually eliminates overshoot. This capacitor also has an effect on feedback loop characteristics during normal operation, and it can create unacceptably large negative transients on the feedback pin if the output voltage is high and a sudden output short occurs. The transient problem is eliminated by inserting a resistor in series with the feedback pin (see Feedback Pin part of pin description section). If undesirable loop characteristics are created by the capacitor, they can be eliminated by diode coupling the capacitor as shown in Figure 34.

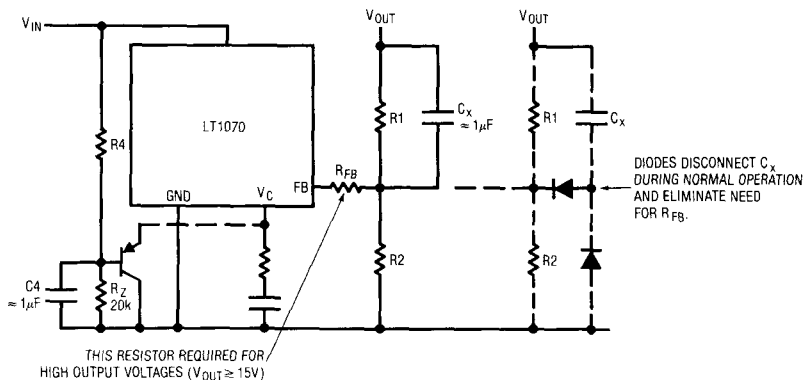


Figure 34. Eliminating Start-Up Overshoot

Application Note 19

Another general technique for forcing slow start-up is to clamp the V_C pin to a capacitor, C_4 . The value of R_4 is chosen to give a voltage across R_2 of 2V at worst-case *low* input voltage. ($I_{R_4} = 100\mu\text{A}$). C_4 is then selected to ramp V_C slow enough to eliminate start-up overshoot. C_4 should be made no larger than necessary to prevent long reset times. A momentary drop to zero volts at the input may not allow enough time for C_4 to discharge fully. If input drop-outs of less than 5R4C4 seconds are anticipated, R_4 should be paralleled with a diode (cathode to input) for fast reset.

EXTERNAL CURRENT LIMITING

The LT1070 has internal *switch* current limiting which operates on a cycle-by-cycle basis and limits peak switch current to $\approx 9\text{A}$ at low duty cycles and $\approx 6\text{A}$ at high duty cycles. The actual *output* current limit value may be much *higher or lower* depending on topology, input voltage, and output voltage. The following formulas give an approximate value for output current limit under short circuit output conditions and at the point where output voltage just begins to fall below its regulated value.

	OVERLOAD CURRENT (AMPS)	SHORT CIRCUIT CURRENT (AMPS)
Buck	5 to 8	≈ 8
Boost	$(5 \text{ to } 8)(V_{IN}/V_{OUT})$	Not Allowed
Buck-Boost (Inverting)	$(5 \text{ to } 8)(1 + V_{OUT}/V_{IN})$	≈ 8
Current Boosted Buck	$(5 \text{ to } 8) \left(\frac{V_{IN}}{V_{OUT} + N(V_{IN} - V_{OUT})} \right)$	$\approx 8/N$
Voltage Boosted Boost	$(5 \text{ to } 8) \left(\frac{V_{IN}}{V_{OUT} + N V_{IN}} \right)$	Not Allowed
Flyback (Continuous)	$\frac{5 \text{ to } 8}{(V_{OUT}/V_{IN}) + N}$	$\approx 8/N$
Flyback (Discontinuous)	Depends on L	$\approx 8/N$
Current Boosted Boost	$\frac{5 \text{ to } 8}{\left(\frac{V_{OUT}}{V_{IN}} \right) - \left(\frac{N}{N+1} \right)}$	Not Allowed
Forward	5 to 8/N	$\approx 8/N$

These formulas show that short circuit current can be much higher than full load current for some topologies. If either full load current or short circuit is much higher than is required for a specific application, external current limiting can be added. This has the advantage of reducing stress on external components, avoiding overload on the input supply, and reducing heatsink requirements on the LT1070 itself.

The LT1070 is externally current limited by clamping the V_C pin. The techniques shown in Figures 35-39 are just a few of the ways this can be accomplished.

The relationship between *switch* current limit point and V_C clamp voltage is *approximately*:

$$I_{SW(MAX)} = 9(V_C - 1) - 3 \cdot (\text{DC}) \text{ amps}$$

DC = switch duty cycle

This relationship is somewhat temperature dependent. The current limit point falls at about 0.3%/°C, so the value set at room temperature should be factored to allow for adequate current limit at higher temperatures. Also, the factor "9" and "3" vary $\pm 30\%$ in production, so a conservative design will normally clamp switch current to about twice the value needed for maximum load current. This can result in rather high short circuit currents, so the current limit scheme may want to include "foldback", wherein the peak switch current is clamped to a lower value with $V_{OUT} = 0\text{V}$. By varying the amount of foldback, the short circuit current can be made greater than, equal to, or less than full load current.

Simple current limiting is shown in Figure 35. V_x is an external voltage which could be a separate regulated voltage or the unregulated input voltage. R_2 is selected to give approximately 2V across R_1 . The value of R_1 is kept to 500Ω or below to keep the knee of the current limit as sharp as possible. If individual adjustment is not necessary, R_1 can be replaced with a fixed resistor. (Note that in some topologies the ground, V_C , and FB pins of the LT1070 are switching at high voltage levels. This will require V_x to be referenced to the LT1070 ground pin, not system ground.)

In Figure 36, D_1 has been replaced with a PNP transistor to reduce the current drain through R_1 to $100\mu\text{A}$. This is helpful in situations where the LT1070 is used in the total shutdown mode.

In Figure 37, *foldback* current limiting is generated by clamping the V_C pin to an output voltage divider. This will reduce short circuit current by an amount which depends on the relative values of R_3 , R_4 , and R_5 . R_5 is needed to prevent "latch off", wherein the output current drops to zero during short circuit and stays at zero even if the short is removed. If this latching action is desirable, R_5 can be eliminated. A normally closed "start" switch can then be placed in series with $D1$. If *non-zero* short circuit current is desired, R_5 is selected to give desired short circuit current and R_4 is adjusted for full load current limit. There is some interaction, so R_4 should be set to about midspan for initial selection of R_5 . If less interaction is desired between R_4 and R_5 adjustments, a 470Ω resistor can be inserted in series with the wiper on R_4 to form a voltage divider with R_5 .

A current transformer ($T1$) is used in Figure 38 to generate a more precise current limit. The primary is placed in series with the output switching diode for buck, flyback, and buck/boost configurations. Output diode *peak* current is limited to:

$$I_{PEAK} = \frac{N}{R_5} \left(V_{BE} + \frac{V_{OUT} R_4}{R_3 + R_4} \right)$$

V_{BE} = base-emitter voltage of $Q1$

The $R3/R4$ divider provides foldback as shown in the formula, with short circuit diode current limited to $N \cdot V_{BE}/R_5$. In a typical application, R_3 is selected to set the voltage across R_4 to $\approx 1V$ at normal output voltage. Then R_5 is calculated from:

$$R_5 = \frac{N (V_{BE} + V_{R4})}{I_{PEAK(PRIMARY)}}$$

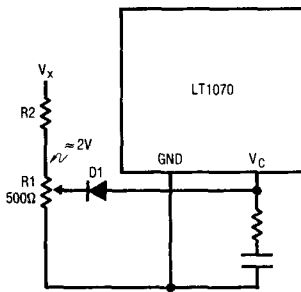


Figure 35. External Current Limit

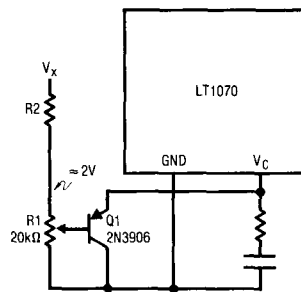


Figure 36. External Current Limit

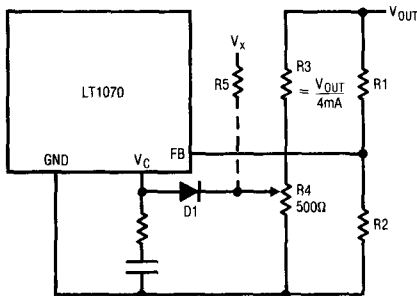


Figure 37. Foldback Current Limit

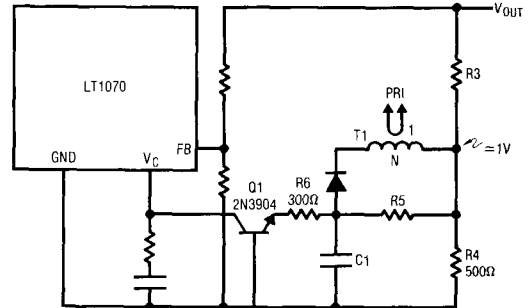


Figure 38. Transformer Current Limit

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The effective secondary current limit sense voltage is $V_{BE} + V_{R4}$ at full output voltage and just V_{BE} during short circuit, giving $\approx 2.7:1$ foldback ratio. The diode in T1 secondary allows the secondary to "reset" between current pulses, so that true peak-to-peak diode current is controlled. C1 is used to filter out spikes and noise.

In Figure 39 a current limit sense resistor (R_S) is placed in series with the ground pin of the LT1070. Peak switch current is limited to $V_{BE}(Q1)/R_S$. This circuit is useful only in situations where the negative input line and the negative output line do not have to be common. Power dissipation in R_S will be fairly high; $P \approx (0.6V)(I_{PEAK})(DC)$, where DC is the duty cycle of the switch. R1 and C1 filter out noise spikes and catch diode reverse turn-off current spikes.

DRIVING EXTERNAL TRANSISTORS

High input voltage applications using the LT1070 require an external high voltage transistor. The transistor is connected in a common gate or common base mode as shown in Figures 40 and 41. This allows the LT1070 internal current sensing to continue functioning and operates the external transistor in a mode which maximizes both operating voltage and switching speed capability.

In Figure 40, the LT1070 drives an N channel power MOSFET. A separate low voltage supply is used to power the LT1070

and to establish forward gate drive to the MOSFET. Typical gate drive requirement is 10V, with 20V as a typical maximum. The forward gate drive applied to the MOSFET is equal to the supply voltage minus the saturation voltage of the LT1070 switch (saturation voltage is typically under 1V). D1 is used to clamp the source during turn-off; it does not slow down turn-off. Diode requirements are that it withstand narrow (100ns) current spikes equal to drain current and that it turn "on" rapidly to provide proper clamping.

In Figure 41, the LT1070 drives an NPN bipolar transistor. These devices require high surge base currents at turn-on and turn-off to ensure fast switching times. R1 establishes DC base drive which might be $\approx 1/5$ of collector current. C1 provides a forward base current surge at turn-on. Typical values are in the range of 0.005–0.05 μ F. D1 clamps the emitter voltage at turn-off. It prevents full collector current from flowing out the base lead during the turn-off delay time (0.5–2 μ s). D2 and R1 establish the reverse base turn-off current. The voltage across R2 during turn-off delay time is approximately one diode drop. With $R2 = 3\Omega$, and a diode drop of 800mV, this would create ≈ 270 mA reverse base current during turn off. Reverse leakage in the "off" state is not a problem with this circuit because D1 and D2 force the emitter-base voltage to zero bias when the LT1070 switch is off. D1 should be selected for fast turn on. It must handle currents equal to

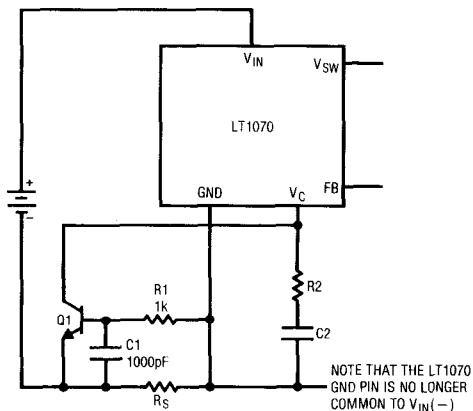


Figure 39. External Current Limit

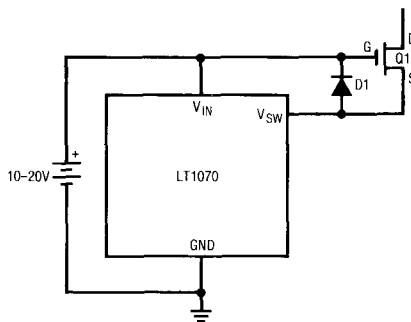


Figure 40. Driving External MOSFET

collector current for times equal to the turn-off time of the transistor. D2 can be any medium speed diode rated for several hundred mA forward current spikes (1N914, etc.).

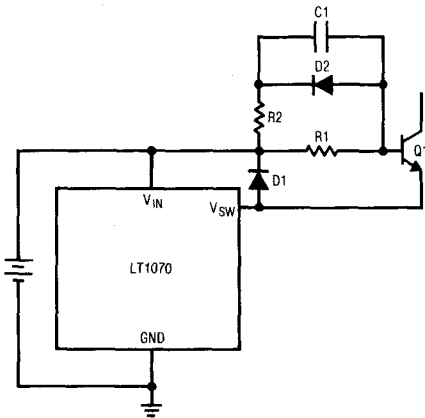


Figure 41. Driving External NPN

OUTPUT RECTIFYING DIODE

The output diode is often the major source of power loss in switching regulators, especially with output voltages below 10V. It is therefore very important to be able to calculate diode peak current and average power dissipation to ensure

adequate diode ratings. The chart in Figure 42 lists average diode power dissipation and peak diode current for normal loads. It also lists diode current under shorted output conditions where the diode duty cycle approaches 100%, and peak and average currents are essentially the same.

The value for diode forward voltage (V_f) used in the average power formulas is the voltage specified for the diode under peak current conditions listed in the next column. The peak current formulas assume no ripple current in the inductor or transformer, but average power calculations will be reasonably close even with fairly high ripple. Boost converters in particular are hard on output diodes when the output voltage is significantly higher than the input voltage. This gives peak diode currents much higher than the average, and manufacturers current ratings must be used with caution.

The most stressful condition for output diodes is overload or short circuit conditions. The internal current limit of the LT1070 is typically 9A at low switch duty cycles. This is almost a factor of two higher than the 5A rated switch current, so that even if the regulator is used near its limit at full load, the output diode current may double under current limit conditions. If full load output current requires only a fraction of the 5A rated switch current, the ratio of diode short circuit current to full load current may be much higher than two to

TOPOLOGY	AVERAGE DIODE DISSIPATION P_D (WATTS)	PEAK DIODE CURRENT		PEAK DIODE VOLTAGE
		@ FULL LOAD (AMPS)	SHORT CIRCUIT (AMPS)	
Buck	$(I_{OUT}) (V_f) \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$	$I_{OUT} + \frac{\Delta I}{2}$	≈ 8	V_{IN}
Current Boosted Buck	$(I_{OUT}) (V_f) \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$	$\frac{I_{OUT}}{V_{IN}} \left(\frac{V_{OUT}}{N} - V_{OUT} + V_{IN}\right)$	$\approx 8/N$	$(N \cdot V_{IN}) + V_{OUT}$
Boost	$(I_{OUT}) (V_f)$	$\frac{I_{OUT} (V_{OUT})}{V_{IN}} + \frac{\Delta I}{2}$	Not Allowed	V_{OUT}
Current Boosted Boost	$(I_{OUT}) (V_f)$	$I_{OUT} \left[\frac{V_{OUT}}{V_{IN}} + N \left(\frac{V_{OUT}}{V_{IN}} - 1 \right) \right] + \frac{\Delta I_{PRI} (N+1)}{2}$	Not Allowed	$V_{OUT} - V_{IN} \left(\frac{N}{N+1} \right)$
Voltage Boosted Boost	$(I_{OUT}) (V_f)$	$\frac{I_{OUT} (N \cdot V_{IN} + V_{OUT})}{V_{IN} (N+1)}$	Not Allowed	$V_{OUT} + N(V_{IN})$
Inverting (Buck-Boost)	$(I_{OUT}) (V_f)$	$\frac{I_{OUT} (V_{IN} + V_{OUT})}{V_{IN}} + \frac{\Delta I}{2}$	≈ 8	$V_{OUT} + V_{IN}$
Flyback (Continuous)	$(I_{OUT}) (V_f)$	$I_{OUT} \left(1 + \frac{V_{OUT}}{N \cdot V_{IN}} \right) + \frac{\Delta I_{PRI}}{2N}$	$\approx 7/N$	$V_{OUT} + (N) (V_{IN})$
Flyback (Discontinuous)	$(I_{OUT}) (V_f)$	$\frac{1}{N} \sqrt{\frac{2 (I_{OUT}) (V_{OUT})}{f (L_{PRI})}}$	$\approx 7/N$	$V_{OUT} + (N) (V_{IN})$

Figure 42

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one. A regulator designed to withstand continuous short conditions must either use diodes rated for the full short circuit current shown in the fourth column, or it must incorporate some form of external current limiting. See current limit section for more details.

The last column in Figure 42 shows maximum reverse diode voltage. When calculating this number, be sure to use worst-case high input voltage. Transformer or tapped inductor designs may have an additional damped "ringing" waveform which adds to peak diode voltage. This can be reduced with a series R/C damper network in parallel with the diode.

Switching diodes have two important transient characteristics; reverse recovery time, and forward turn-on time. Reverse recovery time occurs because the diode "stores" charge during its forward conducting cycle. This stored charge causes the diode to act like a low impedance conductive element for a short period of time after reverse drive is applied. Reverse recovery time is measured by forward biasing the diode with a specified current, then forcing a second specified current backwards through the diode. The time required for the diode to change from a reverse *conducting* state to its normal reverse *non-conducting* state, is reverse recovery time. Hard turn-off diodes switch abruptly from one state to the other following reverse recovery time. They therefore dissipate very little power even with moderate reverse recovery times. Soft turn-off diodes have a gradual turn-off characteristic that can cause considerable diode dissipation during the turn-off interval. Figure 43 shows typical current and voltage waveforms for several commercial diode types used in an LT1070 boost converter with $V_{IN} = 10V$, $V_{OUT} = 20V$, 2A.

Long reverse recovery times can cause significant extra heating in the diode or the LT1070 switch. Total power dissipated is given by:

$$P_{rr} = V \cdot f \cdot t_{rr} \cdot I_f$$

V = reverse diode voltage

f = LT1070 switching frequency

t_{rr} = reverse recovery time

I_f = diode forward current just prior to turn-off

With the circuit mentioned, I_f is 4A, $V = 20V$, and $f = 40kHz$. Note that diode "on" current is twice output current for this

particular boost configuration. A diode with $t_{rr} = 300ns$ creates a power loss of:

$$P_{rr} = (20)(40 \times 10^3)(300 \times 10^{-6})(4) = 0.96W$$

If this same diode had a forward voltage of 0.8V at 4A, its forward loss would be 2A (*average* current) times 0.8V, equals 1.6W. Reverse recovery losses in this example are nearly as large as forward losses. It is important to realize, however, that reverse losses may not necessarily increase *diode* dissipation significantly. A hard turn-off diode will shift much of the power dissipation to the LT1070 switch, which will undergo a high current *and* high voltage condition during the duration of reverse recovery time. This has not shown to be harmful to the LT1070, but the power loss remains.

Diode *turn-on* time can potentially be more harmful than reverse turn-off. It is normally assumed that the output diode clamps to the output voltage and prevents the inductor or

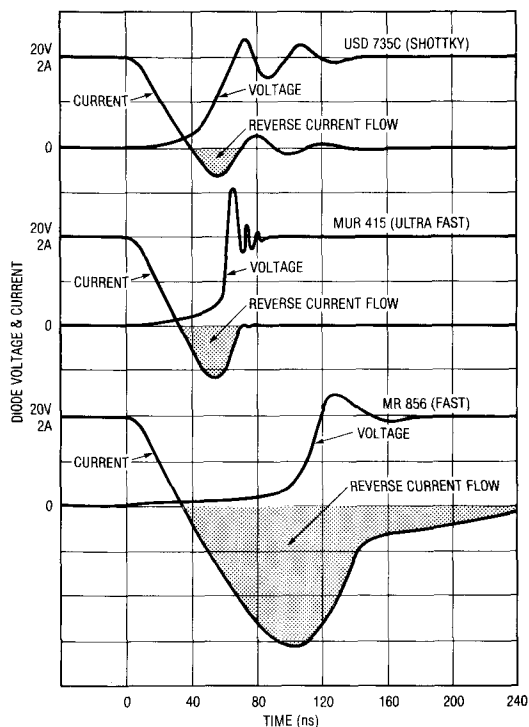


Figure 43. Diode Turn-Off Characteristics

transformer connection from rising higher than the output. A diode that turns "on" slowly can have a very high forward voltage for the duration of turn-on time. The problem is that this increased voltage appears across the LT1070 switch. A 20V turn-on spike superimposed on a 40V boost mode output pushes switch voltage perilously close to the 65V limit. The graphs in Figure 44 show diode turn-on spikes for three common diode types, fast, ultra-fast, and Schottky. The height of the spike will be dependent on rate of rise of current and the final current value, but these graphs emphasize the need for fast turn-on characteristics in applications which push the limits of switch voltage.

Fast diodes can be useless if the stray inductance is high in the diode, output capacitor, or LT1070 loop. 20 gauge hook-up wire has $\approx 30\text{nH/in.}$ inductance. The current fall-time of the LT1070 switch is $\approx 10^8\text{A/sec.}$ This generates a voltage of $(10^8)(30 \times 10^{-9}) = 3\text{V per inch}$ in stray wiring. Keep the diode, capacitor, and LT1070 ground/switch lead lengths short.

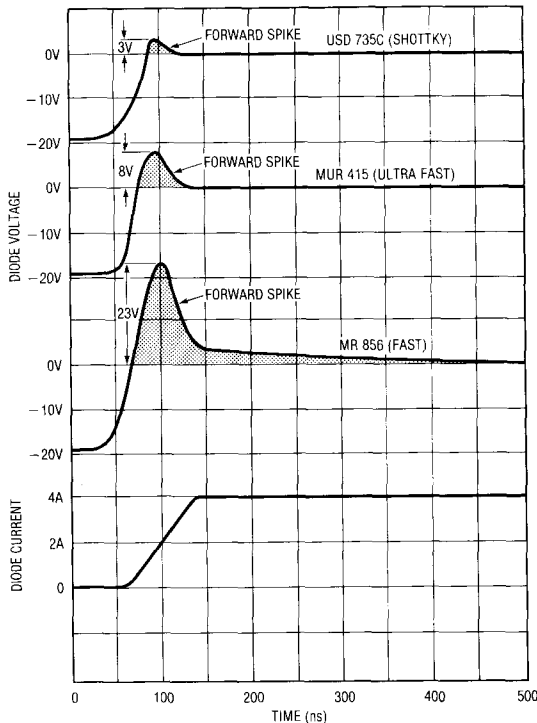


Figure 44. Diode Turn-On Spike

INPUT FILTERS

Most switching regulator designs draw current from the input supply in pulses. The peak-to-peak amplitude of these current pulses is often equal to or higher than the load current. There is significant high frequency energy in the pulses which can cause EMI problems in some systems. The addition of a simple LC filter between the supply and the switching regulator can reduce the amplitude of this EMI by more than an order of magnitude at the switching frequency, and several orders of magnitude at higher harmonic frequencies. The basic filter shown in Figure 45 can be added to any switching regulator.

The two major design considerations for the filter are the *reverse current transfer function* which determines ripple attenuation, and the *filter output impedance function* which must satisfy regulator stability criteria. The stability problem occurs because switching regulators have a *negative input impedance* at low frequencies:

$$Z_{IN}(DC) = - \frac{(V_{IN})^2}{(V_{OUT})(I_{OUT})}$$

The output impedance of the filter has a sharp peak at the LC resonant frequency. If the output impedance is not well below the negative input impedance of the regulator at frequencies up to the bandwidth of the regulator control loop, the possibility for oscillation exists.

There is a basic conflict in the two filter requirements. High ripple attenuation is obtained with a large LC *product* with high Q, but this also tends to aggravate oscillation problems. This conflict is minimized by using large C with smaller L to get the required LC product, but size requirements may also limit this approach. An additional "fix" is to lower the Q of the filter by paralleling L with a small resistor (R_f). This has the

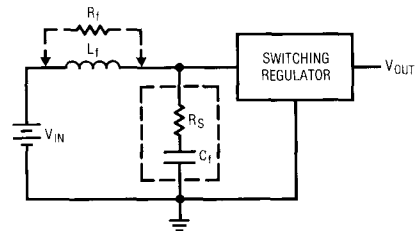


Figure 45.

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disadvantage of limiting the filter attenuation at high frequencies. Filter Q is also reduced by the ESR (R_S) of the capacitor, but deliberately increasing ESR exacts a heavy penalty in ripple attenuation and power loss.

Ripple attenuation of an input filter may be calculated from:

$$\frac{I_{OUT}(p-p)}{I_{IN}(p-p)} = \frac{R_S}{R_f} + \frac{R_S(DC)(1-DC)}{(L)(f)}$$

R_S = effective series resistance of C

DC = switching regulator duty cycle

Note that this formula does not contain the value of C. This is because large electrolytic capacitors have a total impedance at 20kHz and above which is essentially equal to ESR. For ripple attenuation, therefore, the value of C is not important; the capacitor is selected on the basis of its ESR.

A typical filter might consist of a 10 μ H inductor and a 500 μ F capacitor with $R_S = 0.05\Omega$. Filter attenuation is *least effective* at 50% duty cycle (DC = 0.5), so we will use this number now for worst-case purposes. Ripple attenuation of this filter with $R_f = \infty$ is:

$$\frac{I_{OUT}}{I_{IN}} = \frac{(0.05)(0.5)(1-0.5)}{(10 \times 10^{-6})(40 \times 10^3)} = 0.031 = 32:1$$

The formula assumes rectangular wave inputs with triangular outputs and yields the ratio of peak-to-peak values. Higher frequency components of the square wave current are attenuated much more than the overall attenuation figure.

Output impedance of the filter given by:

$$Z_{OUT} = \frac{1}{\frac{1}{R_f} - \frac{j}{\omega L} + \frac{j\omega C}{1 + (\omega R_S C)^2} + \frac{R_S(\omega C)^2}{1 + (\omega R_S C)^2}}$$

ω = radian frequency = $2\pi f$

This formula has a DC ($\omega = 0$) value of zero and a high frequency value equal to R_S in parallel with R_f . If R_S is simply the ESR of the capacitor, both high and low frequency output impedance of the filter is very low. Unfortunately, the output impedance of the filter at its resonant frequency can be significantly higher, and this resonant frequency is typically in the range where switching regulators have negative input

impedance. Resonant frequency and peak output impedance formulas are shown below.

$$f = \frac{1}{2\pi\sqrt{LC - (R_S)^2 \cdot C^2}}$$

If R_S is simply the ESR of C, the filter resonant frequency is usually closely approximated by:

$$f = \frac{1}{2\pi\sqrt{LC}} \quad \left(\frac{R_S^2 \cdot C}{L} \ll 1 \right)$$

$$Z_{OUT(PEAK)} = \frac{R_f(LC)}{LC + (R_S \cdot R_f \cdot C^2)}$$

Resonant frequency for a 500 μ F, 10 μ H filter is ≈ 2 kHz. Peak output impedance with $R_f = \infty$, and $R_S = 0.05\Omega$ is $\approx 0.4\Omega$.

The criteria for regulator stability is that the filter impedance be much lower than the input impedance of the regulator:

$$\frac{R_f(LC)}{LC + R_S \cdot R_f \cdot C^2} \ll Z_{IN}$$

The worst-case occurs with switching regulators which have low input voltage. If we let $V_{IN} = 5V$, and $V_{OUT} = 20V$, $I_{OUT} = 1A$, regulator input impedance at low frequencies is $(5^2)/(20 \cdot 1) = 1.25\Omega$. The peak filter impedance was calculated at 0.4Ω , so it seems that stability criteria is met. There is the problem, however, of the *too good* a capacitor in the filter. If the ESR of C drops to 0.02Ω , peak filter impedance rises to 1Ω , and stability becomes questionable. To bring peak filter impedance down, R_f may have to be added. If R_f is set at 1Ω , peak filter impedance drops to 0.5Ω . The penalty in ripple attenuation is a reduction from 32:1 to 12:1 for $R_S = 0.05\Omega$.

In all this discussion, the output impedance of the actual input *source* was assumed to be zero. This is not the actual case obviously, and source impedance may have a significant effect on stability.

The point of all this is that input filters tend to have resonant frequencies and impedances which fall into the range where they can cause stability problems in switching regulators. It is important, therefore, to include the filter design into the overall regulator design from the beginning. The selected filter must be *in place* when the regulator is checked for closed loop stability, and the actual source should be used.

EFFICIENCY CALCULATIONS

The primary reason for using switching regulators is efficiency, so it is important to be able to estimate that factor with some degree of accuracy. In many cases, the overall efficiency is not as critical as the power loss in the individual components. For reliable operation, each power dissipating component must be properly sized or heat sunk to ensure that maximum operating temperature is not exceeded. Overall efficiency is then found by dividing output power by the sum of all losses plus output power:

$$E = \frac{(I_{OUT})(V_{OUT})}{\Sigma P_L + (I_{OUT})(V_{OUT})}$$

Sources of power loss include the LT1070 quiescent current, switch driver current, and switch "on" resistance; the output diode; inductor/transformer winding and core losses; and snubber dissipation.

LT1070 Operating Current

The LT1070 draws only 6mA quiescent current in its idle state, but this is specified with a voltage on the V_C pin such that the output switch never turns on—duty cycle equals zero. When the V_C pin is servoed by the feedback loop to initiate switching, supply current at the input pin increases in two ways. First, there is a DC increase proportional to V_C pin voltage. This is the result of increasing bias current for the switch driver to ensure adequate switch drive at high switch currents. Second, there is driver current which is "on" only when the output switch is on. The ratio of switch driver current to switch current is $\approx 1:40$. Total *average* current into the LT1070 V_{IN} pin is then:

$$I_{IN} \approx 6mA + I_{SW}(0.0015 + DC/40)$$

I_{SW} = switch current

DC = switch duty cycle

Use of this formula requires knowledge of switch duty cycle and switch current. This information is available in the sections which deal with each particular switching configuration. A typical example is a buck converter with 28V input and 5V, 4A output. Duty cycle is $\approx 20\%$, and switch current is 4A. This yields a total supply current of:

$$I_{IN} = 6mA + 4(0.0015 + (0.2)/40) = 32mA$$

Total power loss due to bias and driver current is equal to input voltage times current:

$$P_{BD} = I_{IN} \cdot V_{IN} = (32mA)(28V) = 0.9W$$

LT1070 Switch Losses

Switch "on" resistance losses are proportional to the square of switch current multiplied times duty cycle:

$$P_{SW} = (I_{SW})^2 \cdot R_{SW} \cdot DC$$

R_{SW} = LT1070 switch "on" resistance

The maximum specified value for R_{SW} is 0.24Ω at maximum rated junction temperature, with 0.15Ω typical value at room temperature. If we use the worst-case number of 0.24Ω , this yields a switch loss in this example of:

$$P_{SW} = (4)^2 (0.24) (0.2) = 0.77W$$

It is pure coincidence that switch and driver losses are nearly equal in this example. At low switch currents and high input voltages, P_{BD} dominates, whereas switch losses dominate at low input voltages and high switch currents.

AC switching losses in the LT1070 are minimal. Rate of switch current rise and fall is $\approx 10^8 A/sec$. This reduces switching times to under 50ns, and makes the AC losses small compared to DC losses. An exception to this is the AC switch loss attributable to output diode reverse recovery time. See Output Diode section.

Output Diode Losses

For low to moderate output voltages, the output diode is often the major source of power loss. For this reason, Schottky switching diodes are recommended for minimum forward voltage and reverse recovery time. Diode losses for most topologies can be approximated by the following formula, but please consult the Output Diode section for further details:

$$P_D \approx (I_{OUT})(V_f)(K) + (V)(f)(t_{rr})(I_f)$$

V_f = diode forward voltage at *peak* diode current

V = diode reverse voltage

t_{rr} = diode reverse recovery time

I_f = diode forward current at turn-off

$K = \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$ for buck converters and 1 for most other topologies

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In the buck regulator example, with $I_{OUT} = 4A$, and letting $V_f = 0.7V$, $t_{rr} = 100ns$;

$$P_D = (4)(0.7) \left(1 - \frac{5}{28}\right) + (28)(40 \times 10^3)(10^{-7})(4)$$

$$= 2.3 + 0.45 = 2.75W$$

Inductor and Transformer Losses

See section on inductors and transformers.

Snubber Losses

See section on flyback design.

Total Losses

In this example of a buck regulator, inductor losses might be $\approx 1W$, and snubber losses are zero. Total losses therefore are:

$$\Sigma P_L = P_{BD} + P_{SW} + P_D + P_L + P_{SNUB}$$

$$= 0.9 + 0.77 + 2.75 + 1 + 0 = 5.42W$$

Efficiency is equal to:

$$E = \frac{V_{OUT} \cdot I_{OUT}}{\Sigma P_L + V_{OUT} \cdot I_{OUT}} = \frac{(5)(4)}{5.42 + (5)(4)} = 78.7\%$$

This number is typical of a fairly high efficiency 5V buck regulator. The efficiency of 5V switching supplies is lower than higher voltage outputs because of the high diode losses. A 15V output for instance might have $E \approx 86\%$.

OUTPUT FILTERS

Output voltage ripple of switching regulators is typically in the range of tens to hundreds of millivolts if no additional output filter is used. A simple output filter can reduce this ripple by a factor of ten to one hundred at little additional cost. The high frequency "spikes" which may be superimposed on the ripple are attenuated even more.

The presence of high amplitude spikes at the output of switching regulators is often puzzling to first time designers. These spikes occur in switching regulators which, by their topology, cannot use the energy storage inductor as an output filter. These include boost, flyback, and buck/boost designs. The output of these converters can be modeled as a switched current source driving the output capacitor as shown in Figure 46.

The output capacitor is shown as C_{OUT} . Its model includes parasitic resistance (R_S) and inductance (L_S). It is the inductance which creates the output voltage spike. The amplitude of this spike can be calculated if the slew rate (di/dt) of the switch is known. For simple inductor designs operating at full switch current, di/dt for the LT1070 switch is approximately $10^8 A/sec$. Voltage across L_S is;

$$V = L_S \left(\frac{di}{dt}\right) = L_S (10^8)$$

Straight wire has an inductance of about $0.02\mu H$ per inch. If we assume one inch of wire on each end of the output capacitor, including board trace length, this represents $0.04\mu H$. Allowing an additional $0.02\mu H$ internal inductance, L_S has a total value of $0.06\mu H$, yielding:

$$V = (0.06 \times 10^{-6})(10^8) = 6V$$

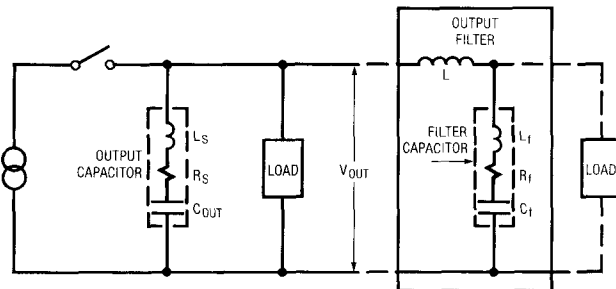


Figure 46. Output Filter

These spikes are very narrow (<100ns) and are usually attenuated significantly in the wire runs and load bypass capacitors, but these calculations point out the importance of *short lead lengths* on the output capacitor.

Output voltage ripple at the regulator switching frequency is usually of two types. With boost, flyback, and inverting (buck/boost) designs, ripple is determined almost totally by the ESR of the output capacitor (R_S).

The *reactance* $1/(2\pi fC)$, of the capacitor at 40kHz is normally so low compared to R_S that it can be ignored. The output ripple is therefore a square wave with amplitude V_{p-p} , and duty cycle DC. A formula for V_{p-p} and DC is given in the discussions of these topologies.

The second type of output ripple is triangular. It occurs in switching regulators which utilize the storage inductor as an output filter. These include buck converters, forward converters, and Cuk converters. Again, the amplitude of the ripple is determined by R_S , not C, but the waveform is triangular with amplitude V_{p-p} and duty cycle DC.

The attenuation of an output filter with *rectangular inputs* is:

$$\frac{V_{OUT}(p-p)}{V_{p-p}} = \frac{DC(1-DC)(R_f)}{f \cdot L}$$

DC = duty cycle of rectangular inputs (50% = 0.5)

Notice that attenuation is the same for complementary duty cycles, that is 10% and 90% are equal, and 40% and 60% are equal. 50% is the point of poorest attenuation. A converter running at 40% duty cycle with an output filter consisting of a $10\mu\text{H}$ inductor and a $200\mu\text{F}$ capacitor with $R_f = 0.05\Omega$ would have a filter attenuation of:

$$\frac{V_{OUT}(p-p)}{V_{p-p}} = \frac{(0.4)(0.6)(0.05)}{(40 \times 10^3)(10 \times 10^{-6})} = 0.03 = 33:1$$

The rectangular input is converted to a triangular output whose peak-to-peak amplitude is 1/33 of the peak-to-peak input. Harmonics of the switching frequency are reduced much more; the third harmonic for instance is attenuated 112:1 with $L_f = 0.06\mu\text{H}$. There are no second harmonics.

With buck, forward, and Cuk converters the ripple voltage into the filter is already triangular. The output ripple of the fil-

ter is of the form $V(t) = mt^2$. Attenuation ratio is given by:

$$\frac{V_{OUT}(p-p)}{V_{p-p}} = \frac{R_f}{8 \cdot L \cdot f}$$

For the same conditions of $R_f = 0.05\Omega$, $L = 10\mu\text{H}$:

$$\frac{V_{OUT}(p-p)}{V_{p-p}} = \frac{0.05}{(8)(10 \times 10^{-6})(40 \times 10^3)} = 0.0156 = 64:1$$

The ripple voltage of these converters is already lower because of the main inductor filtering, so the output filter inductor can often be only a few μH to obtain adequate filtering. The inductor can even be an air core type. A 1/2" diameter, 3/4" long air-wound coil with 13 turns of #16 wire will have an inductance of $1\mu\text{H}$, giving a 6:1 attenuation with $R_f = 0.05\Omega$.

INPUT AND OUTPUT CAPACITORS

Large electrolytic capacitors used on switching regulators have several important design considerations. The most important is usually effective series resistance (ESR). This is simply the equivalent parasitic resistance in series with the capacitor leads. At frequencies of 10kHz and above, the total impedance of the capacitor is almost identically equal to ESR, and this parasitic resistance limits the filtering effectiveness of the capacitor. The design equations for capacitors used with the LT1070 most often deal simply with ESR; the actual capacitance value is of secondary importance. The following formulas are a very rough guide to maximum ESR vs capacitance for several types of commercially available switching supply capacitors. ESR changes over temperature are shown in Figure 47.

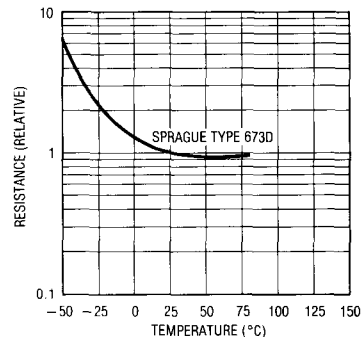


Figure 47. Typical Capacitor ESR vs Temperature

Application Note 19

Sprague type 673D or 674D

$$ESR = \frac{400 \times 10^{-6}}{(C)(V)^{0.6}} \Omega$$

Mallory type VPR

$$ESR = \frac{200 \times 10^{-6}}{(C)(V)^{0.6}} \Omega$$

Cornell Dubilier Type UFT

$$ESR = \frac{430 \times 10^{-6}}{(C)(V)^{0.25}} \Omega$$

C = capacitance value

V = rated working voltage

Note that higher voltage ratings yield lower ESR. This is because higher voltage capacitors are physically larger! Nothing's free, folks. Common design practice is to parallel several capacitors to achieve low ESR and acceptable component height.

A second consideration in capacitor selection is ripple current rating. After a capacitor has been selected, its ripple current rating should be checked to verify that operating ripple is less than the maximum allowed by the manufacturer. Keep in mind, however, that ripple current ratings are normally selected to limit temperature rise in the capacitor. Power dissipation is given by $(I_{RMS})^2 \times ESR$. For ambient temperatures below the capacitor's maximum rating, it may be possible to increase ripple current. Consult the capacitor manufacturer. RMS ripple current in the output capacitor for boost, buck-boost, and flyback designs can be calculated from output current and switch duty cycle:

$$I_{RMS} = I_{OUT} \sqrt{\frac{DC}{1-DC}}$$

For buck converters, RMS current in the output capacitor is approximately equal to $0.3\Delta I$, where ΔI is the peak-to-peak ripple current in the inductor (continuous mode).

Ripple current in the input capacitor for flyback and buck-boost designs is:

$$I_{RMS} = \frac{(I_{OUT})(V_{OUT})}{V_{IN}} \sqrt{\frac{1-DC}{DC}}$$

For buck designs it is:

$$I_{RMS} = I_{OUT} \sqrt{DC - (DC)^2}$$

and for boost designs; input capacitor ripple current is:

$$I_{RMS} = 0.3\Delta I$$

INDUCTOR AND TRANSFORMER BASICS

The inductors and transformers used with the LT1070 are very important to the overall performance of the converter, especially with respect to parameters such as efficiency, maximum output power, and overall physical size. The many tradeoffs associated with the inductance values and the volume of the core require the designer to have a sound basis for selecting the optimum inductor or transformer for each application. Specific guidelines for inductance values are given in the discussion of suggested applications elsewhere in this section, but a general understanding of inductor theory is also needed.

The three important characteristics of a simple two-terminal inductor used in switching regulators are; inductance value (L, in henries), maximum energy storage ($I^2 \cdot L/2$, in ergs), and power loss (watts). Basic definitions of the parameters which determine these characteristics are shown below.

μ = core permeability. This is basically the *increase* in inductance which is obtained when the inductor is wound on a core instead of just air. A μ of 2000, for instance, will increase inductance by 2000:1.

ℓ = magnetic path length. In a simple toroid this is the average circumference of the core (see sketch).

A = cross-sectional area of the core (see sketch).

g = thickness of air gap (if any) used to increase the energy storage capability of a core (see sketch).

B = magnetic flux density in the core. If B rises too high, the core will "saturate", allowing μ and therefore L, to drop drastically.

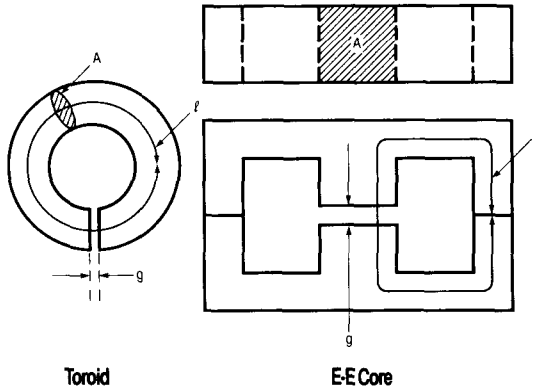
N = number of turns in the winding

I = instantaneous winding current

V_C = volume of actual core material

In most converter applications, the required inductance is determined by constraints such as maximum output power, ripple requirements, input voltage, and transient response. I

is determined by load current. For purposes of this discussion, therefore, it is assumed that L and I are known quantities, and the quantities to be determined are N , A , ℓ , V_C , and g .



Inductance is determined by core permeability, path length, cross-sectional area, and number of turns:

$$L = \frac{\mu \cdot A \cdot N^2}{\ell} (0.4\pi \times 10^{-8}) \quad (\text{no gap})$$

Magnetic flux density is a function of winding current, number of turns and path length:

$$B = \frac{I \cdot N \cdot \mu}{\ell} (0.4\pi) \quad (\text{no gap})$$

A properly selected inductor must provide the right value of L without exceeding the maximum limit on flux density, (B_M). In other words, the core must not "saturate" under conditions of peak winding current, I_p . By combining the formulas for inductance and flux density, it can be shown that core volume (V_C) required is a direct function of the energy to be stored by the inductor:

$$\text{stored energy} = E = \frac{I_p^2 \cdot L}{2}$$

$$V_C = A \cdot \ell = \frac{I_p^2 \cdot L \cdot \mu \cdot (0.4\pi)}{B^2 \cdot 10^{-8}} = (E) \frac{2\mu \cdot (0.4\pi)}{B^2 \cdot 10^{-8}}$$

In any given application, the value of I_p can be determined from maximum load current and duty cycle. Formulas for maximum I_p are provided in the individual sections on each topology.

In many cases, the maximum load current is much less than the LT1070 is capable of providing. A core designed to handle only full load current may saturate under overload or short circuit conditions. The *cycle-by-cycle current limiting of the LT1070 protects the regulator against damage even with saturated cores*. This considerably improves the reliability of converters using the LT1070 and eases the design complexity.

Although core volume is the main criteria for selecting a given core, the volume still consists of two variables, A and ℓ . For minimum overall size of the inductor it is generally best to increase A as much as possible at the expense of ℓ , thereby minimizing the number of turns required to obtain the desired inductance. This process can be taken only so far before the "window" in the core becomes too small to accommodate the windings.

Cores with Gaps

The energy storage capability of a core can be increased by "gapping" the core. A significant portion of the total energy is stored in the air gap. The drawback of a gapped core is that the effective permeability drops, requiring many more turns to achieve the required inductance. More turns require a larger winding window. The overall size of the inductor, however, can be considerably less with a properly gapped core, especially with high-permeability core material. The formula for inductance with a gapped core is:

$$L = \frac{\mu \cdot A \cdot N^2 (0.4\pi \times 10^{-8})}{\ell \left(1 + \frac{\mu g}{\ell}\right)}$$

Inductance drops by the factor, $\left(1 + \frac{\mu g}{\ell}\right)$.

With a μ of 2000, $\ell = 2"$, and $g = 0.02"$, inductance will drop by 22:1, requiring that N be increased by $\sqrt{22}$ to maintain constant inductance. Increase in energy storage is equal to the decrease in permeability.

$$\frac{E_{MAX}(\text{with gap})}{E_{MAX}(\text{no gap})} = 1 + \frac{\mu \cdot g}{\ell}$$

There are several practical limits on the amount which gap size may be increased. First, large gaps require many more turns to achieve the same inductance. This requires smaller

diameter wire which increases copper losses from I^2R heating. Secondly, with large gaps the *effective* gap size is considerably less than the actual gap because of fringing fields around the gap.

When using commercially available cores, data sheet information on ℓ , A and μ is usually given in *effective* values. The theoretical value of μ , for instance, is the bulk value for the core material. The *effective* value for a single piece core may approach the bulk value, but with two-piece cores, the tiny air spaces left in the mating surfaces can reduce the *effective* permeability by as much as 2:1. This may sound unreasonably pessimistic, but a core with bulk $\mu = 3000$, and $\ell = 1.5"$, will lose half its permeability for $g = 0.0005"$. Data sheets for gapped cores list *effective* values of μ for each gap size to make calculations simple. They may also list a parameter, "inductance per (turn)²" for each gap to further simplify inductance calculations.

There are two types of core material which are effectively self-gapped; iron powder, and permalloy. These materials distribute the gap evenly throughout the core, allowing gapless core to be constructed with much higher energy storage capability. The permeability of this material is much reduced, but if the winding window will accommodate the extra turns, the current handling capability of the inductor will be much higher for the same inductance compared to a high- μ formulation.

Iron powder cores are cheaper than ferrite and can be custom tailored quickly, but high core loss limits their application to low AC flux density applications such as inductors. A significant advantage of iron powder is that it saturates very "softly," preventing catastrophic total loss of inductance for large over-current conditions. Note that commercially available powdered iron inductors are typically "optimized" so that core losses and winding (I^2R) losses are the same order of magnitude. Core loss is dependent on peak-to-peak ripple current which depends on the voltage-time product applied to the inductor. The inductors are therefore specified for a maximum DC current and a maximum volt•microsecond product to limit heating. For applications which require highest possible efficiency, consider using oversized cores or permalloy, which is more expensive, but has much lower core loss. Consult with inductor manufacturers about trading off DC current for ripple current, or vice versa.

Inductor Selection Process

The simplest way to select an inductor is to find an off-the-shelf unit which meets the minimum inductance and current requirements. This may not be cost effective, however, if the standard types are not fairly close to your requirements. The next best approach is to have the unit custom wound by one of the many companies in the business. They will select the best core and winding combination for your particular application. A third approach is to scan the literature for standard core types which you can custom wind to meet your particular requirement. This is a quick way to get a prototype up and running. It can also be very cost effective for some production situations. At the end of this data sheet is a list of core and inductor/transformer manufacturers.

The procedure for selecting a do-it-yourself core starts with defining the values of peak winding current and inductance. If the LT1070 is to be used at or near full output power, peak winding current will approach 5A, so a conservative value of 5A should be used for core calculations. If external current limiting is used or if output power levels are lower, peak winding currents can be calculated from the equations supplied in the discussions of each topology. Likewise, inductance values are calculated from specific equations in these sections. Actual values for L generally fall into the range of 50 μ H to 1000 μ H, with 200 μ H to 500 μ H being most typical.

For ferrite cores, the next step is to calculate the core volume required to prevent saturation:

$$V_e = \frac{I_p^2 \cdot L \cdot \mu_e \cdot (0.4\pi)}{B_0^2 \cdot 10^{-8}} \quad (\text{ferrite cores})$$

L = required inductance (henries)
 I_p = peak inductor current (amps)
 μ_e = effective relative permeability
 B_0 = maximum operating flux density } supplied on core data sheets
 (gauss)
 V_e = effective core volume

Example; let $L = 200\mu\text{H}$, $I_p = 5\text{A}$, $\mu_e = 100$, $B_0 = 2500$ gauss

$$V_e = \frac{(5)^2 \cdot (200 \times 10^{-6}) (100) (0.4\pi)}{(2500)^2 \cdot 10^{-8}} = 10\text{cm}^3$$

The values chosen for μ_e and B_0 are typical for a gapped ferrite core. Some cores come with several standard gaps.

Others are left ungapped with the user supplying spacers for setting gap length. Custom gapped cores are also available. A reasonable place to start is with a gap length of 0.02 inches. A core with $\mu = 3000$ and path length (ℓ_e) of 2 inches would have an effective permeability of $\mu_e = \mu / (1 + \mu_g / \ell_g) = 3000 / (1 + 3000 \cdot 0.02/2) = 97$. Notice that by simply selecting a large gap we can arbitrarily reduce the required core volume. The problem with attempting to use a large gap is that the effective permeability drops so low that a large number of turns are required to achieve the desired inductance. This forces the use of small diameter wire where the copper losses get high enough to cause overheating of the core.

Powdered iron cores, because of their high core loss, and ability to operate at very high DC flux densities, generally have a different design procedure based on temperature rise due to core loss and winding loss. AC flux densities generally need to be kept below 400 gauss. This leads to a volume formula based on AC flux density:

$$V_C = \frac{(\Delta I)^2 (L) (\mu) (0.4\pi)}{4 \cdot (B_{AC})^2 (10^{-8})}$$

ΔI = peak to peak ripple current

For $\Delta I = 1A$, $L = 200\mu H$, $\mu = 75$, and $B_{AC} = 300$ gauss,

$$V_C = \frac{(1)^2 (200 \times 10^{-6}) (75) (0.4\pi)}{4 \cdot (300)^2 (10^{-8})} = 5.25 \text{ cm}^3$$

To reduce core size, inductance (L) must be *increased*. This seems backwards according to the formula, but ΔI is inversely proportional to L, so the $(\Delta I)^2$ term drops rapidly as L is increased, reducing required core volume. The penalty is increased wire (copper) loss due to the increased turns required.

After a tentative core is selected based on volume, a check must be done to see if the power losses from the winding(s) and the core itself are within the allowed limits.

The first step is to calculate the number of turns required:

$$N = \sqrt{\frac{L \cdot \ell_e}{\mu_e \cdot A_e \cdot (0.4\pi \times 10^{-8})}}$$

N = turns
 ℓ_e = effective magnetic path length (cm)
 A_e = effective core area (cm²)
 μ_e = effective permeability (with gap)

} supplied on core data sheets

Using the ferrite example, and assigning $\ell_e = 9\text{cm}$, $A_e = 1.2\text{cm}^2$, $\mu_e = 100$, a 200 μH inductor would require:

$$N = \sqrt{\frac{(200 \times 10^{-6})(9)}{(100)(1.2)(0.4\pi \times 10^{-8})}} = 34.6 \text{ turns (use 35)}$$

To calculate wire size, the usable winding window area (A_w) must be ascertained from the core dimensions. Many data sheets list this parameter directly. The usable window area must allow for bobbin thickness and clearances. Total copper area is only about 60% of window area due to air gaps around the wire. We can now express the required wire gauge in terms of N and A_w .

$$\text{Wire gauge (AWG)} = 10 \left(\log \frac{0.08 \cdot N}{0.6 \cdot A_w} \right)$$

0.08 factor = area of #1 gauge wire

0.6 factor = air space loss around wire

If we assume a value for A_w of 0.2in² and use $N = 35$:

$$\text{AWG} = 10 \log \frac{(0.08)(35)}{(0.6)(0.2)} = 13.68 \text{ (use \#14)}$$

The next step is to determine the number of winding layers. This is determined by bobbin length, or toroid inside circumference:

$$\text{Layers} = \frac{N (D + 0.01)}{L_B} = \frac{N \left(0.32 \cdot 10^{\frac{-\text{AWG}}{20}} + 0.01 \right)}{L_B}$$

D = wire diameter in inches

L_B = bobbin length or toroid inside circumference

0.01 = allowance for enamel and spacing

For $N = 35$, AWG = #14; $L_B = 0.9''$

$$\text{Layers} = \frac{35 \left(0.32 \cdot 10^{\frac{-14}{20}} + 0.01 \right)}{0.9} = 2.87$$

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The reason for calculating layers is that the *AC copper losses* are very dependent on the number of layers in a winding. To calculate AC losses, a table is used (Figure 48) which requires a factor K:

$$K = D\sqrt{f} \cdot F_P$$

D = wire diameter or foil thickness

For foil conductors, F_P is 1. For round wires it is equal to:

$$F_P = \frac{(T_L + 1)(N_C)(D)}{L_W}$$

T_L = turns per layer

N_C = number of paralleled conductors (bifilar → $N_C = 2$)

D = wire diameter

L_W = length of winding ($\approx L_B$)

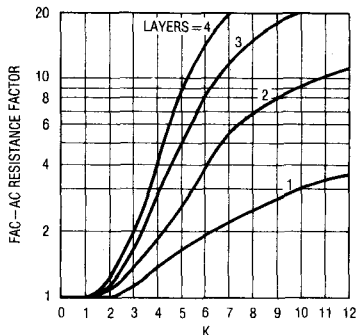


Figure 48. AC Resistance Factor

For 35 turns and 3 layers, $T_L \approx 12$. #14 wire has $D = 0.064$. N_C for a single wire is 1. With $L_W = 0.9$ ”;

$$F_P = \frac{(12 + 1)(1)(0.064)}{0.9} = 0.92$$

K is now equal to:

$$K = D\sqrt{f} \cdot F_P = 0.064\sqrt{(40 \times 10^3)}(0.92) = 12.3$$

This is a very high K factor; in fact it is slightly off the graph in Figure 48, but for now it illustrates the importance of AC resistance calculations. The various lines on the graph represent the number of layers. With 3 layers, the AC resistance

factor is off scale at approximately 23. This means that AC resistance is *23 times* DC resistance. Now we can calculate winding losses. DC winding resistance is found from:

$$R_{DC} = \frac{N \cdot \ell_m}{12} \cdot 10^{\frac{AWG}{10} - 4}$$

ℓ_m = mean turn length (core specification)

For $N = 35$, $\ell_m = 2.4$ ”, $AWG = \#14$:

$$R_{DC} = \frac{(35)(2.4)}{12} \cdot 10^{\frac{AWG}{10} - 4} = 0.0176\Omega$$

AC resistance is then DC resistance multiplied by AC resistance factor (F_{AC})

$$R_{AC} = R_{DC} \cdot F_{AC} = (0.0176)(23) = 0.404\Omega$$

To calculate total losses, DC and AC losses are summed:

$$P_W = (I_{DC})^2(R_{DC}) + (I_{AC})^2(R_{AC})$$

Formulas for I_{DC} and I_{AC} are shown in Figure 50. If we assume $I_{DC} = 5A$, and $I_{AC} = 1A$, total winding losses are:

$$P_W = (5)^2(0.0176) + (1)^2(0.404) = 0.44 + 0.4 = 0.94W$$

In this example, AC losses are about equal to DC losses. Simple inductors used in buck, boost, and buck/boost designs may have the ratio of AC to DC losses in the range of 0.25 to 4.0. Transformer designs like flyback usually have AC losses *much* higher than DC losses. Losses in the primary and secondary are calculated separately. In many cases, multiple strands of smaller wire or copper foil must be used to reduce the AC resistance factor to acceptable limits.

After winding losses are found, core loss must be calculated. The first step is to find peak AC flux density:

$$B_{AC} = \frac{L(\Delta I)}{2N \cdot A_e \cdot 10^{-8}}$$

ΔI = peak-to-peak winding ripple current

ΔI is the *ripple* current in the winding. It is the *change* in winding current during the time current is flowing in the winding. For $L = 200\mu H$, $\Delta I = 2A$, $N = 35$, and $A_e = 1.2cm^2$:

$$B_{AC} = \frac{(200 \times 10^{-6})(2)}{(35)(1.2)(10^{-8})} = 476 \text{ gauss}$$

Core loss per unit volume (F_{fe}) is found from the manufacturers tables (see Figure 49) of F_{fe} versus flux density and frequency or from the following formula for typical $M_N Z_N$ ferrite material (ferroxcube type 3C8):

$$F_{fe} = (1.3 \cdot 10^{-14}) (B_{AC})^2 \cdot f^{1.45}$$

For $B_{AC} = 476$ gauss, $f = 40$ kHz:

$$F_{fe} = (1.3 \times 10^{-14}) (476)^2 (40 \times 10^3)^{1.45} = 0.014 \text{ W/cm}^3$$

Total core loss is F_{fe} times core volume:

$$P_C = F_{fe} \cdot V_e = (0.014) (10) = 0.14 \text{ W}$$

$$V_e = \text{effective core volume (cm}^3\text{)}$$

Core loss for a powdered iron core is approximately 25 times higher than for ferrite. At a lower flux density of 150 gauss, a powdered iron core would still have core losses 2.5 times that of ferrite. Copper losses would also be higher because of the higher inductance required to reduce AC flux density. Powdered iron cores must be carefully designed to avoid overheating.

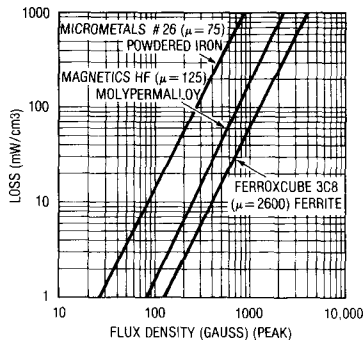


Figure 49. Core Loss vs Flux Density

Overall losses in the ferrite core are the sum of winding losses plus core losses:

$$P = P_W + P_C = 0.94 + 0.14 = 1.08 \text{ W}$$

This loss reflects on regulator efficiency, and more importantly, core temperature rise. A 10 cm^3 core might have a typical thermal resistance of 20°C/W . Temperature rise in this core with $P = 1.08 \text{ W} = (1.08) (20) = 21.6^\circ \text{C}$. 40°C rise is considered a typical design criteria, so this core is being under utilized.

Transformer Design Example

Requirements: A flyback converter with $V_{IN} = 28 \text{ V}_{DC}$, $V_{OUT} = 5 \text{ V}$, $I_{OUT} = 6 \text{ A}$. From previous calculations it is found that $N = 1/3$, $L_{PRI} = 200 \mu\text{H}$, and $I_{PRI(\text{peak})} = 4.5 \text{ A}$, with $\Delta I = 1 \text{ A}$.

1. Calculate volume of core required with a gapped core. First assume an effective permeability of ≈ 150 , and $B_0 = 2500$ gauss:

$$V_e = \frac{(I_{PRI})^2 \cdot L \cdot \mu_e (0.4\pi)}{(B_0)^2 \cdot 10^{-8}}$$

$$= \frac{(4.5)^2 \cdot (200 \times 10^{-6}) (150) (0.4\pi)}{(2500)^2 \cdot 10^{-8}} = 12 \text{ cm}^3$$

A Pulse Engineering core #0128.005 has $V_e = 13.3 \text{ cm}^3$, $A_e = 1.61 \text{ cm}^2$, $\ell_e = 8.26 \text{ cm}$, $\mu = 2000$.

2. Calculate required gap:

$$g = \frac{\ell_e \left(\frac{\mu}{\mu_e} - 1 \right)}{\mu}$$

$$= \frac{(8.26) \left(\frac{2000}{150} - 1 \right)}{2000} = 0.051 \text{ cm} = 0.02''$$

If an ungapped core is used with spacers, spacer thickness should be $0.02/2 = 0.01''$.

3. Calculate required turns:

$$N = \sqrt{\frac{L \cdot \ell_e}{\mu_e \cdot A_e \cdot (0.4\pi \times 10^{-8})}}$$

$$= \sqrt{\frac{(200 \times 10^{-6}) (8.26)}{(150) (1.61) (0.4\pi \times 10^{-8})}} = 23.3$$

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4. Calculate wire size. Allocate 1/2 the window space for the primary winding. Window height (build) for the 0128.005 core is 0.25" and coil length is 0.782", giving a window area = (0.25)(0.782) = 0.196in²:

$$\text{AWG} = 10 \log \frac{0.08N}{0.6 \cdot A_w} = 10 \log \frac{(0.08)(23)}{(0.6) \left(\frac{0.196}{2} \right)}$$

$$= 14.95 \text{ (use \#16)}$$

5. Calculate layers:

$$\text{Layers} = \frac{N \left(0.32 \cdot 10^{\frac{-\text{AWG}}{20}} + 0.01 \right)}{L_B}$$

$$= \frac{(23) \left(0.32 \cdot 10^{\frac{-16}{20}} + 0.01 \right)}{0.782}$$

$$= 1.79 \text{ (assume 2 layers)}$$

6. Calculate K factor (#16 wire has D = 0.05):

$$F_p = \frac{(T_L + 1)(N_c)(D)}{L_w} = \frac{\left(\frac{23}{2} + 1 \right) (1)(0.05)}{0.782} = 0.8$$

$$K = D\sqrt{f} \cdot F_p = 0.05\sqrt{(40 \times 10^3)}(0.8) = 8.94$$

7. Calculate DC winding resistance:

$$R_{DC} = \frac{N \cdot \ell_m}{12} \cdot 10^{\left(\frac{\text{AWG}}{10} - 4 \right)} = \frac{(23)(3) \cdot 10^{\left(\frac{16}{10} - 4 \right)}}{12} = 0.023\Omega$$

(ℓ_m for this core is $\approx 3''$)

8. Use graph to find AC resistance factor. Interleaving of primary and secondary reduces effective layers by two only if primary and secondary conduct simultaneously, which they *do not* in a flyback design. Use layers = 2 line:

$$F_{AC} = 8.3 \text{ (from graph, for } K = 8.95)$$

9. Calculate AC winding resistance:

$$R_{AC} = R_{DC} \cdot F_{AC} = (0.023)(8.3) = 0.19\Omega$$

10. Calculate primary winding losses.

First, primary AC RMS current must be calculated. From the chart in Figure 50:

$$I_{AC} = \frac{I_{OUT}}{E} \sqrt{\frac{N \cdot V_{OUT}}{V_{IN}}}$$

$$= \frac{6}{0.75} \sqrt{\frac{1/3 \cdot 5}{28}} = 1.95A$$

$$I_{DC} = \frac{I_{OUT}}{E} \sqrt{\frac{V_{OUT}(V_{OUT} + N \cdot V_{IN})}{(V_{IN})^2}}$$

$$= \frac{6}{0.75} \sqrt{\frac{5(5 + 1/3 \cdot 28)}{(28)^2}} = 2.4A$$

Power loss in the primary winding is:

$$P_w = (I_{AC})^2 R_{AC} + (I_{DC})^2 R_{DC}$$

$$= (1.95)^2 (0.19) + (2.4)^2 (0.023) = 0.85W$$

11. Calculate secondary winding loss.

Turns ratio is 1/3, so the secondary will have 23/3 = 7.67 turns. Use 8 turns:

$$\text{AWG} = 10 \log \frac{0.08N}{0.6 A_w} = 10 \log \frac{(0.08)(8)}{(0.6) \left(\frac{0.196}{2} \right)} = 10.4$$

This is rather large, stiff wire and the large diameter will lead to large AC winding losses. A good solution might be to use multiple smaller diameter wire wound in parallel. If we use the length of the coil divided by 2N, it will tell us what diameter wire can be bifilar wound to just fill one layer:

$$D = \frac{L_B}{2N} = \frac{0.782}{(2)(8)} = 0.049''$$

The next smallest standard wire diameter is #18. Two #18 wires have three times the DC resistance of a single #10 wire, but AC resistance will not increase nearly that much. Assume one layer bifilar wound #18 secondary interleaved between the two primary layers (to reduce leakage inductance).

$$R_{DC} = \left(\frac{N \cdot \ell_m}{12} \right) \cdot 10^{\frac{AWG}{10} - 4} = \left(\frac{8 \cdot 3}{12} \right) \cdot 10^{\frac{18}{10} - 4}$$

$$= 0.013\Omega \text{ per wire}$$

With 2 wires, total $R_{DC} = 0.013/2 = 0.0065\Omega$.

$$F_P = \frac{(T_L + 1)(N_C)(D)}{L_w} = \frac{(8 + 1)(2)(0.04)}{0.782} = 0.92$$

$$K = D\sqrt{f} \cdot F_P = 0.04\sqrt{(40 \times 10^3)(0.92)} = 7.7$$

From graph, with layers = 1, $F_{AC} = 2.3$:

$$R_{AC} = R_{DC} \cdot F_{AC} = (0.0065)(2.3) = 0.015\Omega$$

From the chart in Figure 50:

$$I_{AC} = I_{OUT} \sqrt{\frac{V_{OUT}}{N \cdot V_{IN}}} = 6 \sqrt{\frac{5}{1/3 \cdot 28}} = 4.4A$$

$$I_{DC} = I_{OUT} \sqrt{\frac{V_{OUT} + N \cdot V_{IN}}{N \cdot V_{IN}}}$$

$$= 6 \sqrt{\frac{5 + 1/3 \cdot 28}{1/3 \cdot 28}} = 7.4A$$

$$P_W = (4.4)^2(0.015) + (7.4)^2(0.0065) = 0.65W$$

Topology	DC Primary I	AC Primary I	DC Secondary I	AC Secondary I
Flyback	$I_o \sqrt{\frac{V_o(V_o + N \cdot V_i)}{(V_i)^2}}$	$I_o \sqrt{\frac{N \cdot V_o}{V_i}}$	$I_o \sqrt{\frac{V_o + N \cdot V_i}{N \cdot V_i}}$	$I_o \sqrt{\frac{V_o}{N \cdot V_i}}$
Buck	I_o	$(0.29)(\Delta I)$	NA	NA
Current Boosted Buck	$I_o \sqrt{\frac{V_o[V_o + N(V_i - V_o)]}{(V_i)^2}}$	$I_o \sqrt{\frac{N \cdot V_o(V_i - V_o)}{(V_i)^2}}$	$I_o \sqrt{\frac{(V_i - V_o)[V_o + N(V_i - V_o)]}{N(V_i)^2}}$	$I_o \sqrt{\frac{V_o(V_i - V_o)}{N(V_i)^2}}$
Boost	$I_o \left(\frac{V_o}{V_i} \right)$	$(0.29)(\Delta I)$	NA	NA
Voltage Boosted Boost	$I_o \left(\frac{V_o}{V_i} \right)$	$I_o \cdot N \sqrt{\frac{(V_o - V_i)}{V_i(N+1)}}$	$I_o \sqrt{\frac{V_o + N \cdot V_i}{V_i(N+1)}}$	$I_o \sqrt{\frac{V_o - V_i}{V_i(N+1)}}$
Current Boosted Boost	$I_o \sqrt{\frac{(V_o - V_i)[V_o + V_i(N+1)]}{(V_i)^2}}$	$I_o \sqrt{\frac{N(V_o - V_i)}{V_i}}$	$I_o \sqrt{\frac{V_o + V_i(N+1)}{N \cdot V_i}}$	$I_o \sqrt{\frac{V_o - V_i}{N \cdot V_i}}$
Buck-Boost (Inverting)	$I_o \left(1 + \frac{V_o}{V_i} \right)$	$(0.29)(\Delta I)$	NA	NA
Forward	$I_o \sqrt{\frac{N \cdot V_o}{V_i}}$	$I_o \sqrt{\frac{V_o(N \cdot V_i - V_o)}{(V_i)^2}}$	$I_o \sqrt{\frac{V_o}{N \cdot V_i}}$	$I_o \sqrt{\frac{V_o(N \cdot V_i - V_o)}{(N \cdot V_i)^2}}$
Cuk	$I_o \left(\frac{V_o}{V_i} \right)$	"O" or $(0.29\Delta I)$	I_o	"O" or $(0.29\Delta I)$

I_o = DC output current
 V_o = DC output voltage
 V_i = DC input voltage

Figure 50. AC and DC Winding Currents (RMS Equivalent)

Application Note 19

12. Calculate core loss.

Core loss is proportional to AC flux density which is determined by *change* in primary current (ΔI) during primary current flow period. For $\Delta I = 1A$:

$$B_{AC} = \frac{L(\Delta I)}{2 \cdot N \cdot A_e \cdot 10^{-8}} = \frac{(200 \times 10^{-6})(1)}{2(23)(1.61) \cdot 10^{-8}} = 270 \text{ gauss}$$

$$F_{fe} = (1.3 \times 10^{-14})(B_{AC})^2 \cdot f^{1.45} = 0.0045 \text{ W/cm}^3$$

$$P_C = F_{fe} \cdot V_e = (0.0045)(13.3) = 0.06 \text{ W}$$

Total power loss with this core is:

$$P = P_W + P_C = 0.85 + 0.65 + 0.06 = 1.56 \text{ W}$$

The 0128.005 core is specified at 2.78W for a 40°C temperature rise, yielding $\theta = 40/2.78 = 14.4^\circ\text{C/W}$

$$\Delta T(\text{core}) = P \cdot \theta = (1.56)(14.4) = 22^\circ\text{C}$$

This is a very conservative design. If minimum core size is required, the procedure now is to go back to step 1 and assume a lower effective permeability (μ_e), perhaps 100. This would reduce core volume and require a larger gap. More turns would be required and the available space for copper would go down, so copper losses would go up. Flux density remains constant, so core loss drops. Thermal resistance goes up however, so the smaller core gets hotter. In addition, the increased number of turns will increase leakage inductance, which will increase snubber losses. It isn't easy folks!

HEATSINKING INFORMATION

The efficiency of the LT1070 allows it to be used without a heatsink in many applications, but for full-power output a heatsink is required. The equations contained in the efficiency section of this data sheet will allow the user to estimate fairly accurately the total power dissipation of the chip under full load conditions. Short-circuit power dissipation can be either *more or less* than full load, depending on the topology. Calculation of short circuit power dissipation in the LT1070 is very complicated because the "on" time of the switch is strongly dependent on parasitic effects such as diode and inductor series resistance, wiring losses, and leakage inductance. If continuous output shorts must be tolerated, it is strongly suggested that a temperature probe be used to ensure that maximum junction is not exceeded. Thermal re-

sistance from junction to case is 2°C/W maximum, and short circuit power dissipation almost never exceeds 10W, so a case temperature of 100°C for commercial units and 130°C for military units will ensure that maximum junction temperature is not exceeded.

Heat sink size for the LT1070 can be calculated if maximum power dissipation and maximum ambient temperature are known.

$$\theta_{HS} = \frac{T_J - T_A - (P)(\theta_{JC})}{P}$$

θ_{HS} = heat sink thermal resistance

P = LT1070 power dissipation

θ_{JC} = LT1070 junction-to-case thermal resistance (2°C/W)

T_J = LT1070 maximum junction temperature

T_A = maximum ambient temperature

For $T_J = 100^\circ\text{C}$, $T_A = 60^\circ\text{C}$, $P = 5\text{W}$;

$$\theta_{HS} = \frac{100 - 60 - (5)(2)}{5} = 6^\circ\text{C/W}$$

TROUBLE SHOOTING HINTS

The following is a list of "gotchas" we've put together to help you avoid some of the pitfalls of switching power supply design. They range from obvious to subtle and serious to hilarious. The LT1070 was specifically designed to eliminate many of the problems commonly found in power supply design and be easy to use. The problem is that there are a significant number of easily overlooked mistakes in breadboarding switching regulators which result in either instant death of the IC or electrical characteristics which are puzzling to even highly experienced power supply designers. So here's the list we've collected so far. We hope your problem is on it to save you time and frustration. If not, give us a call and we'll help fix the problem.

WARNING

Before reading this section, be aware that the intent of the author is not to insult, but rather to relate in an attention-getting manner a list of goofs that, in many cases, he personally has had to own up to.

1. Transformer Wired Backwards

Those dots indicate polarity, not smashed flies.

2. Electrolytic Capacitors Installed Backwards

This is no problem until you bend over to see what is wrong—then “bang”, a personal demonstration of explosive venting.

3. LT1070 Input and Switch Pins Reversed

The catalog and some preliminary datasheets got out with the wrong pinout for the plastic TO-220 package. Our apologies. *Pin 5 is input on TO-220 packages.*

4. No Input Bypass Capacitor

Switching regulators draw current from the input supply in pulses. Long input wires can cause dips in the input voltage at the switching frequency. *Breadboards should have a large ($\geq 100\mu\text{F}$) input capacitor up close to the regulator.*

5. Fred's Inductor (Or Transformer)

Inductors are not like lawn mowers. If you want to borrow the one out of Fred's drawer, make sure it's the right value for your application.

A $50\mu\text{H}$ inductor with 50V applied will have a current increasing with time at the rate of 1 amp per microsecond. It doesn't take a calculator to see that things can get out of hand quickly during the $25\mu\text{s}$ period of a 40kHz switcher. Likewise, if “Fred's inductor” is 50 millihenries, it will probably saturate at such low current levels that it is useless, not to mention the fact that the transient response can be measured on a Simpson VOM. *Use the formulas in the application note to get a ball park inductance value before starting a breadboard.*

6. Wimpy Magnetic Cores

Core sizes for the LT1070 will vary from 3–20 cubic centimeters of core material for properly designed inductors or transformers. A thumbnail size core will simply saturate and get hot when asked to operate at ampere current levels. *Breadboard with man-sized cores, then optimize the core size for production.*

7. Rats Nest Wiring

The LT1070 is not a jelly bean op amp that can be wired up with two-foot clip leads. It achieves its high efficiency by switching current at very high speeds. Long wires will cause every component connected to them to look like an inductor at these speeds. This not only causes totally unpredictable operation; it can generate fatal (to components) transient voltages. *Use very short wires to interconnect power components on the breadboard, including bypass capacitors, catch diodes, LT1070 pins, transformer leads, etc.*

8. No Snubber Network

The LT1070 will tolerate a lot of abuse, but it cannot be over-voltaged on the switch pin and survive to tell the tale. The 65V maximum switch voltage must be observed. Any design using a transformer or tapped inductor will have enough leakage inductance to cause transients well above 65V if no snubber network is used. Load currents and input voltages should be increased slowly while monitoring switch voltage to ensure that the initial snubber design is adequate.

9. 60Hz Diodes

The LT1070 will eat 1N914 and 1N4001 diodes, and not even burp. Diode currents, especially during startup, can exceed 5 amps. This takes care of the 1N914's. The 1N4001's will last for a little while, until the heat generated by their horribly slow turn-off characteristics causes them to self-destruct. *Use diodes designed for switching applications, with adequate current ratings. Turn-on time is also important to avoid overvoltage stress on other components.* (See diode section.)

10. Something from Nothing

The first step in designing with the LT1070 is to see if it will provide the required power level. Each topology has a different maximum output power that it can provide, depending on things such as input voltage, output voltage, and transformer turns ratio. Secondary

effects such as inductance values and switch resistance may also limit power. *The power graph on page 70 is a rough guide to maximum power levels. Use it as a quick guide only.* More exact formulas are contained in the application section. Oh by the way, if you thought about paralleling LT1070's for more power—sorry it won't work. You can't get to the internal 40kHz oscillator to get them in sync.

11. Input Supply Gets Clobbered

The LT1070 can draw input currents of up to 6 amps during startup. It has to charge up the large output capacitor and it does this at a rate set by the internal current limit unless optional soft start is added. *The start-up surge may trip over-current latches on some supplies, causing them to stay off until power is recycled.*

Steady-state problems can also occur. Switching regulators try to deliver constant load voltage. With a given load, this means constant load power. For a high efficiency system, input power also remains constant, *so input current increases as input voltage decreases. Low input voltage conditions may require such high input currents that the input supply current limits. This causes the supply voltage to drop further, forcing a permanent latch condition.* See current limit and soft start sections.

12. Didn't Read the Datasheet

Then you shall have no pie.

13. Stray Coupling to the V_C or FB Pins

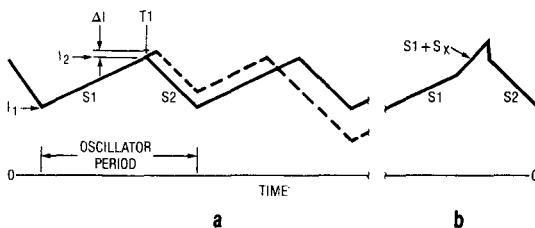
Voltages on the FB and V_C pin are referenced to the LT1070 ground pin. In some topologies the ground pin is switching between input voltage and system ground. *Stray capacitance between V_C or FB pins and system ground will act like coupling to a switching*

source. *Minimize this capacitance.* The problem is particularly acute when using an RC box to iterate frequency compensation on the V_C pin. Even configurations which have the LT1070 ground pin "grounded" may have problems if the RC box picks up switching energy.

SUBHARMONIC OSCILLATIONS

Current mode switching regulators which operate with a duty cycle greater than 50% and have continuous inductor current can exhibit a duty cycle instability known as subharmonic oscillations. This effect is not harmful to the regulator and in many cases it does not even affect the output regulation. Its most annoying effect is to produce a high-pitched squeal from power components which effectively have their 40kHz operating frequency *modulated* by submultiple frequencies; 20kHz, 10kHz, etc. Subharmonic oscillations do *not* depend on the closed loop characteristics of the regulator. They can occur even when zero feedback is used. Ordinary closed loop instabilities can also cause audible sounds from switching regulators, but they tend to be in the range of hundreds of hertz to several kilohertz.

The source of subharmonic oscillations is the simultaneous conditions of fixed frequency and fixed peak amplitude of inductor current as shown in part a of the accompanying figure.



The inductor current starts at I_1 , at the beginning of each switch on cycle. Current increases at a rate (S_1) equal to input voltage divided by inductor value. When current reaches the trip level, I_2 , the current mode loop shuts off the switch and current begins to fall at a rate S_2 until the switch is again turned on by the oscillator. Now watch what happens when the point T_1 is perturbed so that the current exceeds I_2 by ΔI . The time left for the current to fall is *reduced* so that the *minimum* current point is *increased* by $\Delta I + \Delta I S_2/S_1$. This will cause the minimum current on the *next* cycle to *decrease* by $(\Delta I + \Delta I S_2/S_1) (S_2/S_1)$. On each succeeding cycle the current perturbation is multiplied by S_2/S_1 . If S_2/S_1 is greater than 1, the system is unstable. The condition $S_2/S_1 \geq 1$ occurs at a duty cycle of 50% or higher.

Subharmonic oscillations can be eliminated if an artificial ramp is superimposed on the inductor current waveform as shown in part b of the figure. If this ramp has a slope of S_X , the requirement for stability is that $S_X + S_1$ be larger than S_2 . This leads to the following equation:

$$S_X \geq \frac{S_1(2DC - 1)}{1 - DC} \quad DC = \text{duty cycle}$$

For duty cycles less than 50% ($DC = 0.5$), S_X is a negative number and is not required. For larger duty cycles, S_X takes on values dependent on S_1 and duty cycle. S_1 is simply V_{IN}/L . This yields an equation for the minimum value of inductance for a fixed value of S_X :

$$L_{MIN} \geq \frac{V_{IN}(2DC - 1)}{S_X(1 - DC)}$$

The LT1070 has an internal S_X voltage ramp fed into the current amplifier whose equivalent current referred value is 2×10^5 A/sec. A sample calculation for minimum inductance with $V_{IN} = 15V$, $DC = 60\%$ is shown

$$L_{MIN} = \frac{(15)(2 \cdot 0.6 - 1)}{(2 \times 10^5)(1 - 0.6)} = 37.5 \mu H$$

Remember that for discontinuous operation, no subharmonic oscillations can occur. Likewise, with duty cycle less than 50%, there is no restriction on inductor size.

Application Note 19

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
LT1070/71HV (See Note 1)	60V
LT1070/71 (See Note 1)	40V
Switch Output Voltage	
LT1070/71HV	75V
LT1070/71	65V
Feedback Pin Voltage (Transient, 1ms)	± 15V
Operating Junction Temperature Range	
LT1070/71HVM, LT1070/71M	-55°C to +150°C
LT1070/71HVC, LT1070/71C (Oper.)	0°C to +100°C
LT1070/71HVC, LT1070/71C (Sh. Ckt.)	0°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10sec)	300°C

Note 1: Minimum switch "on" time for the LT1070/LT1071 in current limit is $\approx 1.0\mu\text{sec}$. This limits the maximum input voltage during short circuit conditions, in the buck and inverting modes only, to $\approx 35\text{V}$. Normal (unshorted) conditions are not affected. Mask changes are being implemented which will reduce minimum "on" time to $\leq 1\mu\text{sec}$, increasing maximum short circuit input voltage above 40V. If the present LT1070/LT1071 (contact factory for package date code) is being operated in the buck or inverting mode at high input voltages and short circuit conditions are expected, a resistor must be placed in series with the inductor, as follows:

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
	LT1070/LT1071HVMK LT1070/LT1071MK LT1070/LT1071HVCK LT1070/LT1071CK
	LT1070/LT1071HVCT LT1070/LT1071CT

The value of the resistor is given by:

$$R = \frac{t \cdot f \cdot V_{IN} - V_f - R_L}{I_{LIMIT}}$$

t = Minimum "on" time of LT1070/LT1071 in current limit, $\approx 1\mu\text{s}$

f = Operating frequency (40kHz)

V_f = Forward voltage of external catch diode at I_{LIMIT}

I_{LIMIT} = Current limit of LT1070 ($\approx 8\text{A}$), LT1071 ($\approx 4\text{A}$)

R_L = Internal series resistance of inductor

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $V_{IN} = 15\text{V}$, $V_C = 0.5\text{V}$, $V_{FB} = V_{REF}$, output pin open.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{REF}	Reference Voltage	Measured at Feedback Pin	1.224 1.214	1.244 1.244	1.264 1.274	V
I_B	Feedback Input Current	$V_{FB} = V_{REF}$		350	750 1100	nA
gm	Error Amplifier Transconductance	$\Delta I_C = \pm 25\mu\text{A}$	3000 2400	4400	6000 7000	μmho
	Error Amplifier Source or Sink Current	$V_C = 1.5\text{V}$	150 120	200	350 400	μA
	Error Amplifier Clamp Voltage	Hi Clamp, $V_{FB} = 1\text{V}$ Lo Clamp, $V_{FB} = 1.5\text{V}$	1.8 0.25	0.38	2.3 0.52	V
	Reference Voltage Line Regulation	$3\text{V} \leq V_{IN} \leq V_{MAX}$			0.03	%/V
A_V	Error Amplifier Voltage Gain	$0.7\text{V} \leq V_C \leq 1.4\text{V}$	500	800	2000	V/V
	Minimum Input Voltage			2.6	3.0	V
I_Q	Supply Current	$3\text{V} \leq V_{IN} \leq V_{MAX}$, $V_C = 0.6\text{V}$		6	9	mA
	Control Pin Threshold	Duty Cycle = 0	0.8 0.6	0.9	1.08 1.25	V
	Normal/Flyback Threshold on Feedback Pin		0.4	0.45	0.54	V
V_{FB}	Flyback Reference Voltage	$I_{FB} = 50\mu\text{A}$	15 14	16.3	17.6 18	V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $V_{IN} = 15V$, $V_C = 0.5V$, $V_{FB} = V_{REF}$, output pin open.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{FB}	Change in Flyback Reference Voltage	$0.05 \leq I_{FB} \leq 1mA$	4.5	6.8	8.5	V
	Flyback Reference Voltage Line Regulation	$I_{FB} = 50\mu A$ $3V \leq V_{IN} \leq V_{MAX}$		0.01	0.03	%/V
	Flyback Amplifier Transconductance (gm)	$\Delta I_C = \pm 10\mu A$	150	300	500	μmho
	Flyback Amplifier Source and Sink Current	$V_C = 1.5V$ Source $I_{FB} = 50\mu A$ Sink	● 15 ● 25	32 40	70 70	μA μA
BV	Output Switch Breakdown Voltage	$3V \leq V_{IN} \leq V_{MAX}$ LT1070/LT1071 $I_{SW} = 5mA$ LT1070HV/LT1071HV	● 65 ● 75	90 90		V V
V_{SAT}	Output Switch (Note 1) "On" Resistance	LT1070 LT1071	●	0.15 0.3	0.24 0.5	Ω Ω
	Control Voltage to Switch Current Transconductance	LT1070 LT1071		8 4		A/V A/V
I_{LIM}	Switch Current Limit (LT1070)	Duty Cycle $\leq 50\%$ $T_j \geq 25^\circ C$ Duty Cycle $\leq 50\%$ $T_j < 25^\circ C$ Duty Cycle = 80% (Note 2)	● 5 ● 5 ● 4		10 11 10	A A A
I_{LIM}	Switch Current Limit (LT1071)	Duty Cycle $\leq 50\%$ $T_j \geq 25^\circ C$ Duty Cycle $\leq 50\%$ $T_j < 25^\circ C$ Duty Cycle = 80% (Note 2)	● 2.5 ● 2.5 ● 2		5 5.5 5	A A A
$\frac{\Delta I_{IN}}{\Delta I_{SW}}$	Supply Current Increase During Switch On-Time			25	35	mA/A
f	Switching Frequency		● 35 33	40 47	45	kHz
DC (max)	Maximum Switch Duty Cycle		90	92	97	%
	Flyback Sense Delay Time			1.5		μs
	Shutdown Mode Supply Current	$3V \leq V_{IN} \leq V_{MAX}$ $V_C = 0.05V$		100	250	μA
	Shutdown Mode Threshold Voltage	$3V \leq V_{IN} \leq V_{MAX}$	● 100 50	150	250 300	mV mV

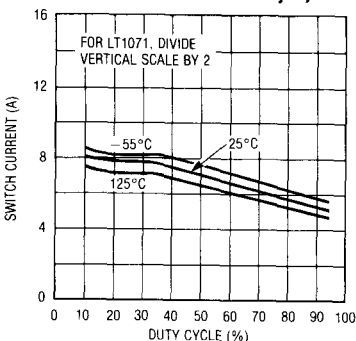
The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Measured with V_C in hi clamp, $V_{FB} = 0.8V$, $I_{SW} = 4A$ for LT1070 and 2A for LT1071.

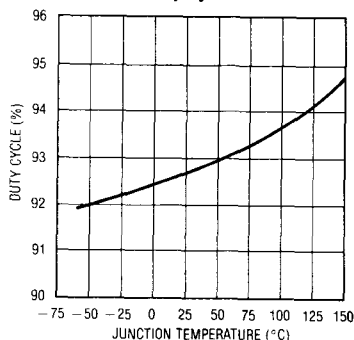
Note 2: For duty cycles (DC) between 50% and 80%, minimum guaranteed switch current is given by $I_{LIM} = 3.33(2 - DC)$ for the LT1070 and $I_{LIM} = 1.67(2 - DC)$ for the LT1071.

TYPICAL PERFORMANCE CHARACTERISTICS

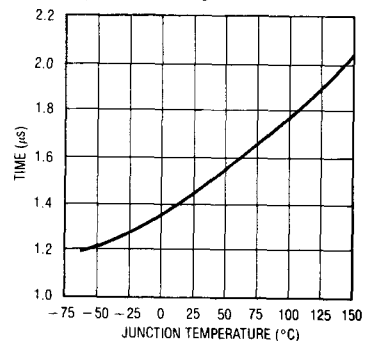
Switch Current Limit vs Duty Cycle



Maximum Duty Cycle

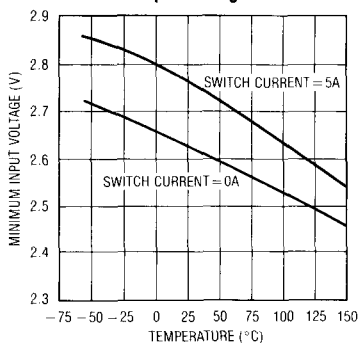


Flyback Blanking Time

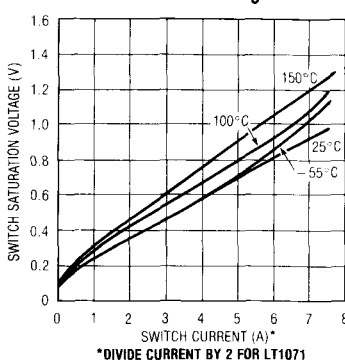


TYPICAL PERFORMANCE CHARACTERISTICS

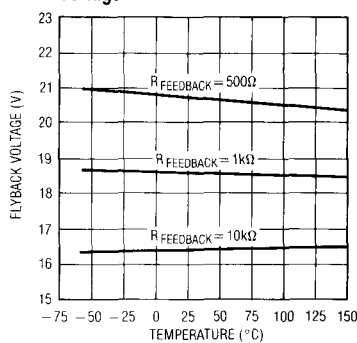
Minimum Input Voltage



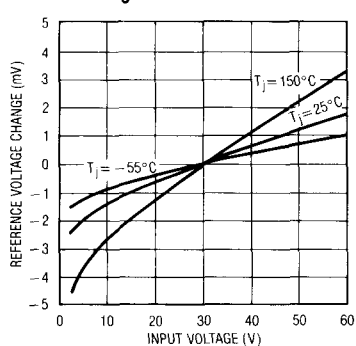
Switch Saturation Voltage



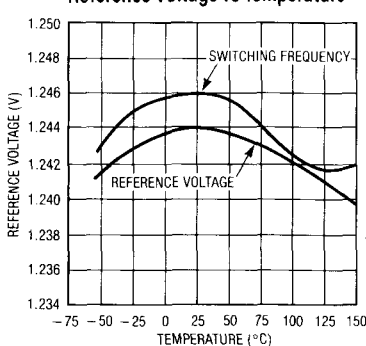
Isolated Mode Flyback Reference Voltage



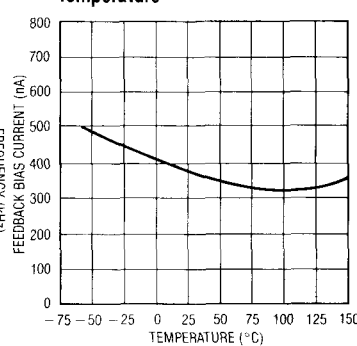
Line Regulation



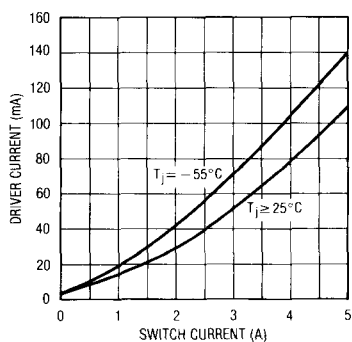
Reference Voltage vs Temperature



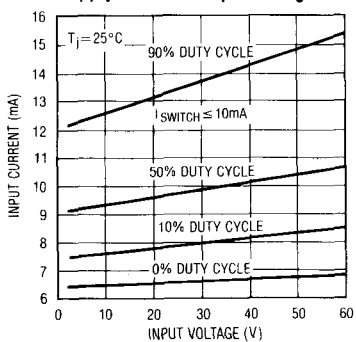
Feedback Bias Current vs Temperature



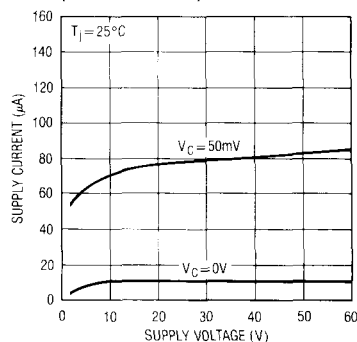
Driver Current* vs Switch Current



Supply Current vs Input Voltage*



Supply Current vs Supply Voltage (Shutdown Mode)

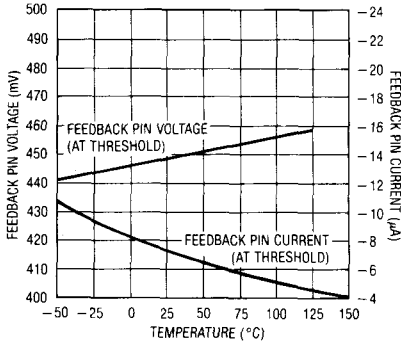


* AVERAGE LT1070 POWER SUPPLY CURRENT IS FOUND BY MULTIPLYING DRIVER CURRENT BY DUTY CYCLE, THEN ADDING QUIESCENT CURRENT.

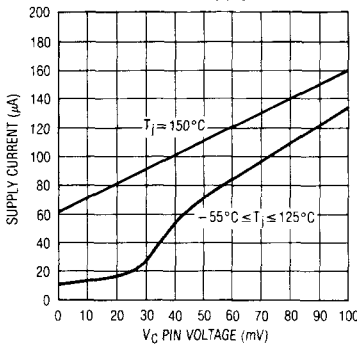
* UNDER VERY LOW OUTPUT CURRENT CONDITIONS, DUTY CYCLE FOR MOST CIRCUITS WILL APPROACH 10% OR LESS.

TYPICAL PERFORMANCE CHARACTERISTICS

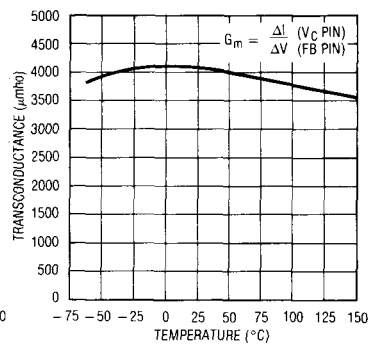
Normal/Flyback Mode Threshold on Feedback Pin



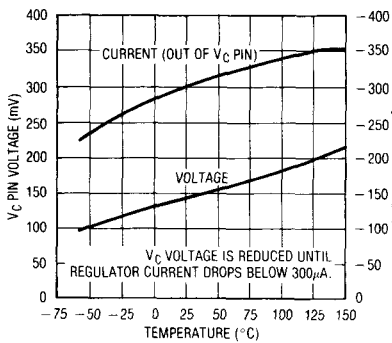
Shutdown Mode Supply Current



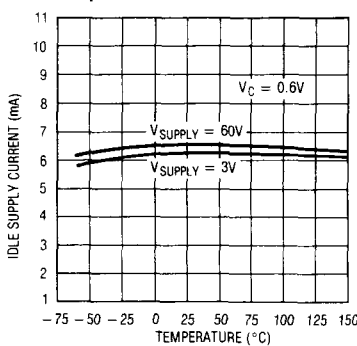
Error Amplifier Transconductance



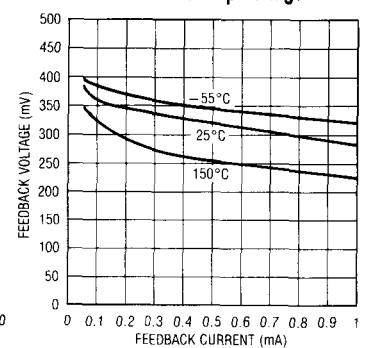
Shutdown Thresholds



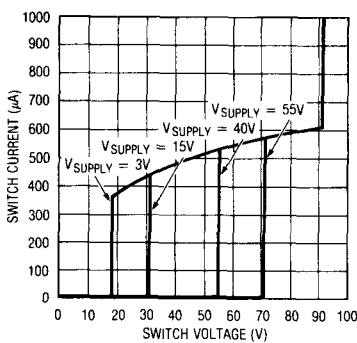
Idle Supply Current vs Temperature



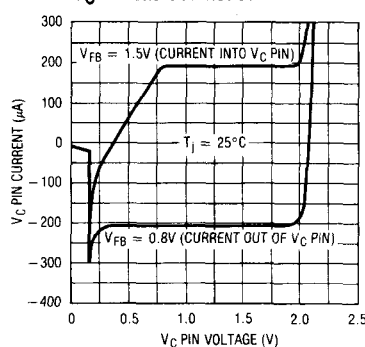
Feedback Pin Clamp Voltage



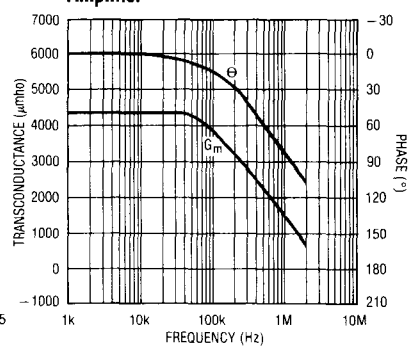
Switch "Off" Characteristics



V_C Pin Characteristics



Transconductance of Error Amplifier



Application Note 19

INDUCTOR/TRANSFORMER MANUFACTURERS

Pulse Engineering Inc. (619/268-2400)
 P.O. Box 12235, San Diego, CA 92112
 Hurricane Electronics Lab (801/635-2003)
 P.O. Box 1280, Hurricane, UT 84737
 Coilcraft Inc. (312/639-2361)
 1102 Silver Lake Rd., Cary, IL 60013
 Renco Electronics, Inc. (516/586-5566)
 60 Jefryn Blvd. East, Deer Park, NY 11729

CORE MANUFACTURERS

Ferroxcube (ferrites) (914/246-2811)
 5083 Kings Highway, Saugerties, NY 12477
 Micrometals (powdered iron) (714/630-7420)
 1190 N. Hawk Circle, Anaheim, CA 92807
 Pyroferic International Inc. (powdered iron) (217/849-3300)
 200G Madison St., Toledo, IL 62468
 Fair-Rite Products Corp. (ferrites) (914/895-2055)
 P.O. Box J, Wallkill, NY 12589
 Stackpole Corp., Ferrite Products Group (814/781-1234)
 Stackpole St., St. Mary's, PA 15857
 Magnetics Division—Spang & Co. (ferrites) (412/282-8282)
 P.O. Box 391, Butler, PA 16003

TDK Corp. of America, Industrial Ferrite Products
 (312/679-8200) 4709 W. Golf Rd., Skokie, IL 60076

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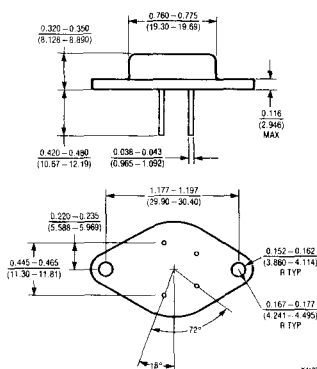
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"Linear Ferrite Magnetic Design Manual", Ferroxcube Inc., Saugerties, New York.

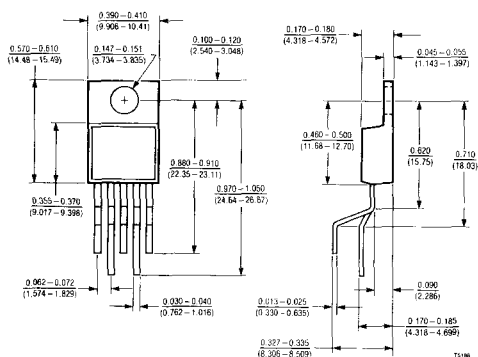
"Design Manual for SMPS Power Transformers", Pulse Engineering Inc., San Diego, Calif.

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

TO-3 Type Metal Can (Steel)
 K Package



TO-220 Type Plastic
 T Package



	T _{JMAX}	θ _{JC}	θ _{JA}
LT1070MK, LT1070HVMK	150°C	2°C/W	35°C/W
LT1070CK, LT1070HVCK	100°C	2°C/W	35°C/W

	T _{JMAX}	θ _{JC}	θ _{JA}
LT1070CT, LT1070HVCT	100°C	2°C/W	75°C/W

Application Considerations for an Instrumentation Lowpass Filter

Nello Sevastopoulos

Description

The LTC1062 is a versatile, DC accurate, instrumentation lowpass filter with gain and phase that closely approximate a 5th order Butterworth filter. The LTC1062 is quite different from presently available lowpass switched capacitor filters because it uses an external (R, C) to isolate the IC from the input signal DC path, thus providing DC accuracy. Figure 1 illustrates the architecture of the circuit. The output voltage is sensed through an internal buffer, then applied to an internal switched capacitor network which drives the bottom plate of an external capacitor to form an input-to-output 5th order lowpass filter. The input and output appear across an external resistor and the IC part of the overall filter handles only the AC path of the signal. A buffered output is also provided (Figure 1) and its maximum guaranteed offset voltage over temperature is 20mV. Typically the buffered output offset is 0-5mV and drift is 1 μ V/ $^{\circ}$ C. As will be explained later, the use of an input (R, C) provides other advantages, namely lower noise and antialiasing.

Tuning the LTC1062

Choosing the external (R, C)

In Figure 1, the filter function is formed by using an external (R, C) to place the LTC1062 inside an AC loop. Be-

cause of this, the value of the (R x C) product is critically related to the filter passband flatness and to the filter stability. The internal circuitry of the LTC1062 is driven by a clock which also determines the filter cutoff frequency. For a maximally flat amplitude response, the clock should be 100 times the desired cutoff frequency and the (R, C) should be chosen such as:

$$\frac{f_c}{1.62} \leq \frac{1}{2\pi RC} \leq \frac{f_c}{1.63}$$

where

f_c = filter cutoff frequency, (-3dB point).

For instance, to make a maximally flat filter with a -3dB frequency at 10Hz, we need a 100 x 10Hz = 1kHz internal or external clock and an external (R, C) such as:

$$\frac{1}{2\pi RC} = \frac{10\text{Hz}}{1.62} = 6.17\text{Hz.}$$

The minimum value of the resistor, R, depends upon the maximum signal we want to attenuate, and the current sinking capability of Pin 1 which is typically 1mA. The 10Hz filter of the previous example should attenuate a 40Hz signal by 60dB. If the instantaneous amplitude of this signal is 1V peak, the minimum value of the external resistor should be 1k Ω .

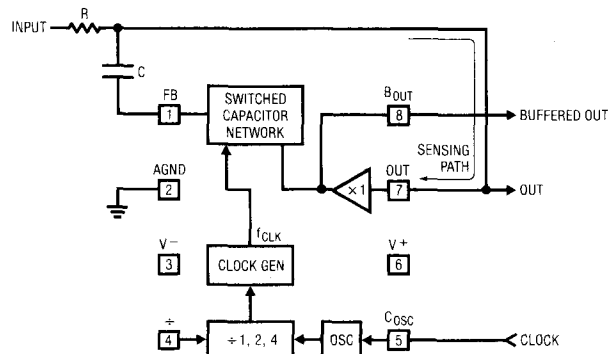


Figure 1. LTC1062 Architecture

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Figure 2 shows the high accuracy of the passband response for values of $1/2\pi RC$ around $(f_c/1.62)$. If maximum flatness is required, the $(R \times C)$ product should be well controlled. Figures 3 and 4 are similar to Figure 2 but with wider range of $(1/2\pi RC)$ values. When the input (R, C) cutoff frequency approaches the cutoff frequency of the filter, the filter peaks and the circuit may become oscillatory. This can accidentally happen when using input ceramic capacitors with strong negative temperature coefficient. As the temperature increases, the value of the external capacitor decreases and if the clock driving the LTC1062 stays constant, the resulting $(1/2\pi RC)$ approaches the filter cutoff frequency. On the other hand, if the external $(R \times C)$ has a strong positive temperature coefficient, the filter passband at high temperatures will become droopy. It is important to note that the filter attenuation slope is mainly set by the internal LTC1062 circuitry and it is quasi-independent from the values of the external (R, C) . This is shown in Figure 4, where a 100kHz cutoff frequency LTC1062 was tested with an external 10kHz clock and for:

$$\frac{f_c}{3.24} \leq \frac{1}{2\pi RC} \leq \frac{f_c}{1.13}$$

Also, Figure 4 shows that the -30dB/octave slope remains constant even though the external $(R \times C)$ changes.

LTC1062 Clock Requirements

Using an external clock: the internal switched capacitor network is clock driven and the clock frequency should be 100 times the desired filter cutoff frequency. Pin 5 of the LTC1062 is the clock input and an external clock swinging close to the LTC1062 power supplies will provide the clock requirements for the internal circuitry. The typical logic threshold levels of Pin 5 are the following:

V SUPPLY	V _{th+}	V _{th-}
±2.5V	+0.9V	-1V
±5V	+1.3V	-2.1V
±6V	+1.7V	-2.5V
±7V	+1.75V	-2.9V
±8V	+1.95V	-3.3V
±9V	+2.15V	-3.7V

The temperature coefficient of the threshold levels is $-1\text{mV}/^\circ\text{C}$.

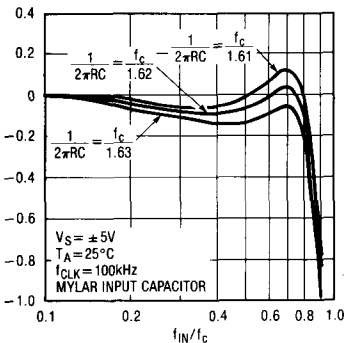


Figure 2. Passband Gain vs Input Frequency

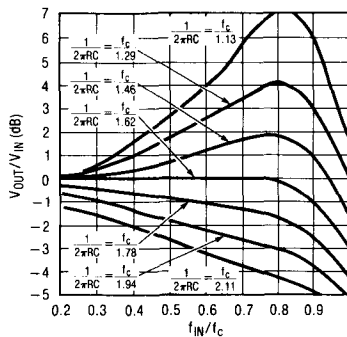


Figure 3. Passband Gain vs Input Frequency

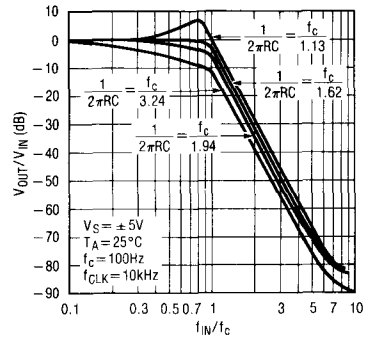


Figure 4. Filter Frequency Response for Various (R, C) Values and Constant Clock

Because the trip levels of Pin 5 are asymmetrically centered around ground and because $(V_{th}^+ - V_{th}^-)$ is less than the positive supply voltage V^+ , CMOS level clocks operating from V^+ and ground can be AC coupled into Pin 5 and drive the IC, Figure 5A.

Internal Oscillator

A simple oscillator is internally provided and it is overridden when an external clock is applied to Pin 5. The internal oscillator can be used for applications for clock requirements below 130kHz and where maximum passband flatness over a wide temperature range is not required. The internal oscillator can be tuned for frequencies below 130kHz by connecting an external capacitor, C_{OSC} , from Pin 5 to ground (or negative supply). Under this condition, the clock frequency can be calculated by:

$$f_{CLK} \approx 130\text{kHz} \left(\frac{33\text{pF}}{33\text{pF} + C_{OSC}} \right) \quad (1)$$

Due to process tolerances, the internal 130kHz frequency varies and also has a negative temperature coefficient. The LTC1062 data sheet publishes curves characterizing the internal oscillator. To tune the frequency of the internal oscillator to a precise value, it is necessary to adjust the value of the external capacitor, C_{OSC} , or to use a potentiometer in series with the C_{OSC} , Figure 5B. The new

clock frequency, f'_{CLK} , can be calculated by:

$$f'_{CLK} = \frac{f_{CLK}}{(1 - 4R C_{OSC} f_{CLK})} \quad (2)$$

where f_{CLK} is the value of the clock frequency, when $R=0$, from (1). When an external resistor (potentiometer) is used, the new value of the clock frequency is always higher than the one calculated in (1). To achieve a wide tuning range, calculate from (1) the ideal (f_{CLK}, C_{OSC}) pair, then double the value of C_{OSC} and use a 50k potentiometer to adjust f'_{CLK} .

Example: To obtain a 1kHz clock frequency, from (1) C_{OSC} typically should be 4250pF. By using 8500pF for C_{OSC} and a 50k potentiometer, the clock frequency can be adjusted from 500Hz to 3.3kHz as calculated by (2).

The internal oscillator frequency can be measured directly at Pin 5 by using a low capacitance probe.

Clock Feedthrough

Clock feedthrough is defined as the amount of clock frequency appearing at the output of the filter. With $\pm 5V$ supplies the measured clock feedthrough was $420\mu V_{RMS}$, while with $\pm 7.5V$ supplies it increased to $520\mu V_{RMS}$. The clock feedthrough can be eliminated by using an (R, C) at the buffered output, Pin 8, provided that this pin is used as an output. If an external op amp is used to buffer the DC

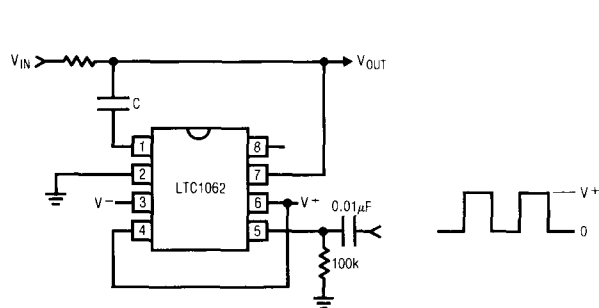


Figure 5A. AC Coupling an External CMOS Clock Powered from a Single Positive Supply, V^+ .

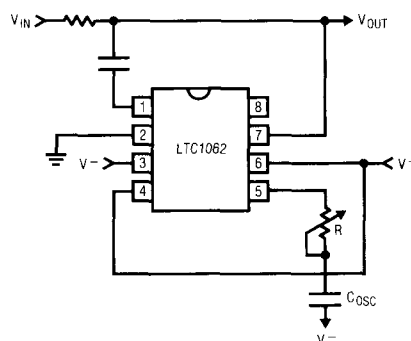


Figure 5B. Adding a Resistor in Series with C_{OSC} to Adjust the Internal Clock Frequency

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accurate output of the LTC1062, an input (R, C) can be used to eliminate the clock feedthrough, Figure 6, and to further increase the attenuation floor of the filter. Note that this (R, C) does not really improve the noise floor of the circuit since the major noise components are located near the filter cutoff frequency.

Single 5V Supply Operation

Figure 7 shows the LTC1062 operating with a single supply. The analog ground, Pin 2, as well as the buffer input, Pin 7, should be biased at 1/2 supply. The value of resistors R1 should conduct 100 μ A or more. In Figure 7, the resistor R' DC biases the buffer and the capacitor C' isolates the buffer bias from the DC value of the output. Under these conditions the external (R, C) should be adjusted such that $(1/2\pi RC) = f_c/1.84$. This accounts for the extra AC loading of the (R', C') combination.

The resistor and capacitor (R', C') are not needed if the input voltage has a DC value around 1/2 supply.

If an external capacitor is used to activate the internal oscillator, its bottom plate should be tied to system ground.

Dynamic Range and Signal/Noise Ratio

There is some confusion with these two terminologies. Because monolithic switched capacitor filters are inherently more noisy than (R, C) active filters, it is necessary to take a hard look at the way some IC manufacturers describe the S/N ratio of their circuit. For instance, when dividing the filter's typical RMS swing by its wideband noise, the result is called "best-case" S/N ratio. But this is definitely not "dynamic range". Under max swing conditions, many monolithic filters exhibit high harmonic distortion. This indicates poor dynamic range even though the S/N ratio looks great on paper.

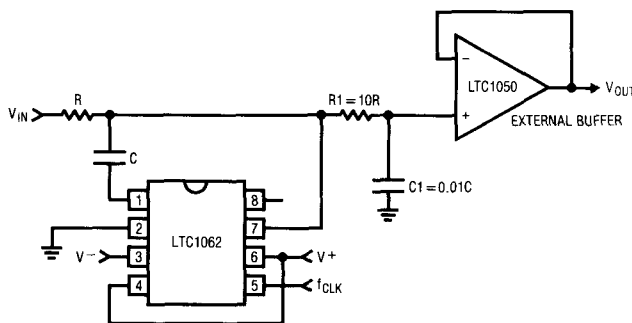


Figure 6. Adding an External (R1, C1) to Eliminate the Clock Feedthrough and to Improve the High Frequency Attenuation Floor

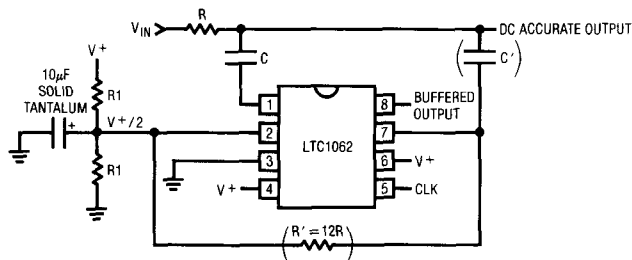


Figure 7. Single Supply Operation

With $\pm 5V$ supplies and higher, the LTC1062 has a typical $100\mu V_{RMS}$ wideband noise. With $1V_{RMS}$ output levels, the signal/noise ratio is 80dB. The test circuit of Figure 8 is used to illustrate the harmonic distortion of the device. The worst-case occurs when the input fundamental frequency equals 1/2 or 1/3 the filter cutoff frequency. This causes the 2nd or 3rd harmonics of the output to fall into the filter's passband edge, Figures 9A and 9B.

Figure 9C shows an input frequency of 700Hz and the filter's dynamic range under this condition is in excess of

80dB. This is true because the harmonics of the 700Hz input fall into the filter's stopband. With $\pm 7.5V$ supplies (or single 15V), the THD of the LTC1062 lies between 76 and 83db, depending on where the harmonics occur with respect to the circuit's band edge. A slight improvement, Figure 9D, can be achieved by increasing the value of the input resistor, R, such as $(1/2\pi RC) = f_c/1.93$. Under this condition, the filter no longer approximates a max flat ideal response since it becomes "droopy" above 30% of its cutoff frequency, as shown in Figure 3.

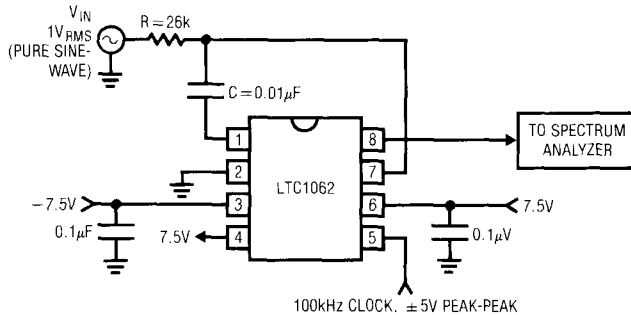


Figure 8. 1kHz Cutoff Frequency, 5th Order LP Filter, Test Circuit for Observing Distortion

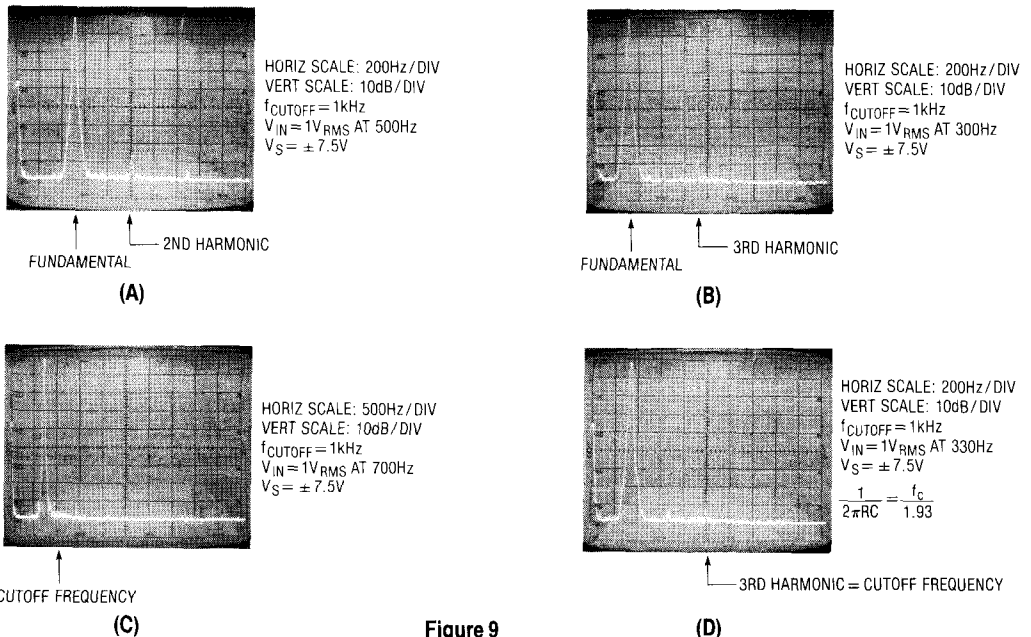


Figure 9

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Step Response and Burst Response

The LTC1062 response to an input step approximates that of an ideal 5th order Butterworth lowpass filter. Butterworth filters are “ringy”, Figure 10A, even though their passband is maximally flat. Figures 10B and 10C show a more damped step response which can be obtained by increasing the input ($R \times C$) product and thereby sacrificing the maximum flatness of the filter’s amplitude response. Figures 11A and 11B show the response of the LTC1062 to a 2V peak to peak sinewave burst which frequency is respectively equal to $2 \times f_c$ and $4 \times f_c$. It is interesting to compare Figure 11B to Figure 10A: In both figures the overshoots and the settling times are about equal since, from the filter’s point of view, a high frequency burst looks like a step input.

LTC1062 Shows Little Aliasing

Aliasing is a common phenomenon in sampled data circuits especially when signals approaching the sampling frequency are applied as inputs. Generally speaking, when an input signal of frequency (f_{IN}) is applied, an alias frequency equal to $(f_{CLK} \pm f_{IN})$ appears at the filter’s output. If f_{IN} is less than $(f_{CLK}/2)$, then the amplitude of the alias frequency equals the magnitude of f_{IN} multiplied by the gain of the filter at f_{IN} , times the $(\sin x/x)$ function of the circuit. For a lowpass filter, the gain around $(f_{CLK}/2)$ is essentially limited by the attenuation floor of the filter and the $(f_{CLK} \pm f_{IN})$ alias signal is buried into the filter noise floor. The problem arises when the input signal’s frequency is greater than $(f_{CLK}/2)$ and especially when it approaches f_{CLK} . Under these conditions $(f_{CLK} - f_{IN})$ falls either into the

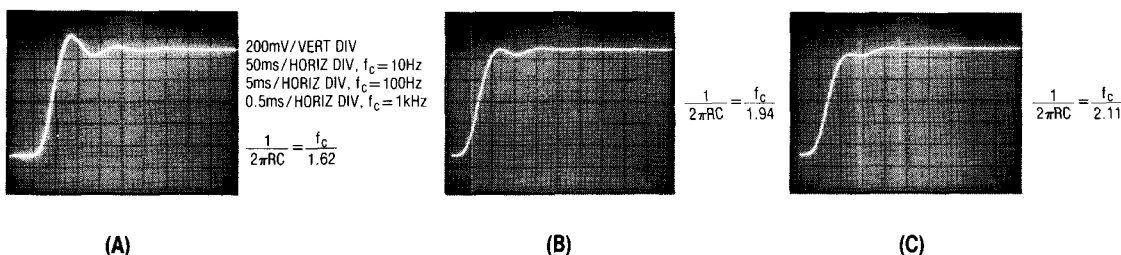


Figure 10. Step Response to a 1V Peak Input Step

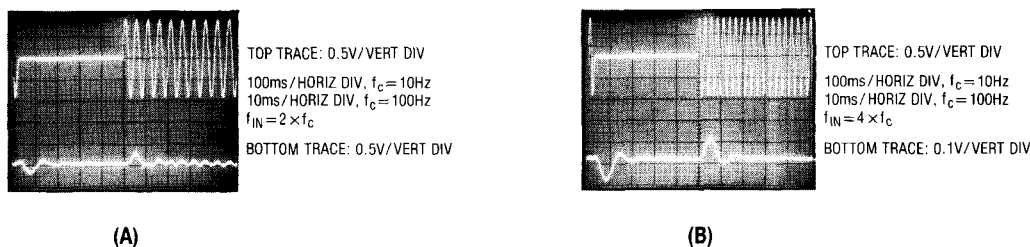


Figure 11. LTC1062 Response to a 2Vp-p Sinewave Burst

filter's passband or into the attenuation slope, and then aliasing occurs. If for instance a 5th order Butterworth switched capacitor ladder filter has a 1kHz corner frequency and operates with a 50kHz clock, a 49kHz, 1V_{RMS} input signal will cause an alias (1kHz, 0.7V_{RMS}) signal to appear at the output of the circuit; a 48kHz input will appear as a 2kHz output attenuated by 30dB.

The LTC1062 internal circuitry has a 4th order sampled data network so, in theory, it will be subject to the above aliasing phenomenon. In practice, however, the input (R, C) band limits the incoming, clock-approaching signals, and aliasing is nearly eliminated. Experimental work showed the following data:

f_{IN} , 0dB LEVEL	LTC1062 V_{OUT} AT ($f_{CLK} - f_{IN}$)	STANDARD 6th ORDER SWITCHED CAPACITOR LOWPASS FILTER V_{OUT} AT ($f_{CLK} - f_{IN}$)
$0.97 \times f_{CLK}$	-77dB	-22.0dB
$0.98 \times f_{CLK}$	-64dB	-3.5dB
$0.99 \times f_{CLK}$	-43dB	0dB
$0.995 \times f_{CLK}$	-45dB	0dB
$0.999 \times f_{CLK}$	-60dB	0dB

Cascading the LTC1062

Two LTC1062s can be cascaded with or without intermediate buffers. Figure 12 shows a DC accurate 10th order lowpass filter where the second LTC1062 input is taken directly from the DC accurate output of the first one. Because loading the junction of the input (R, C) causes passband error, the second resistor R' should be much larger than R. The recommended ratio of (R'/R) is about 117/1; beyond this, the passband error improvement is not worth the large value of R'. Also, under this condition $(1/2\pi RC) = f_c / 1.57$ and $(1/2\pi R'C') = f_c / 1.6$. For instance, a 10th order filter was designed with a cutoff frequency, f_c , of 4.16kHz, $f_{CLK} = 416$ kHz and $R = 909\Omega$, $R' = 107k$, $C = 0.066\mu F$ and $C' = 574$ pF. The maximum passband error was -0.6dB occurring around $0.5 \times f_c$. Figure 13 repeats the circuit of the previous figure but the second LTC1062 is fed from the buffered output of the first one. The filter's offset is the offset of the first LTC1062 buffer (which is typically under ± 5 mV and guaranteed 20mV over the full temperature range of the device). By using this intermediate buffer, impedance scaling is no longer required and the

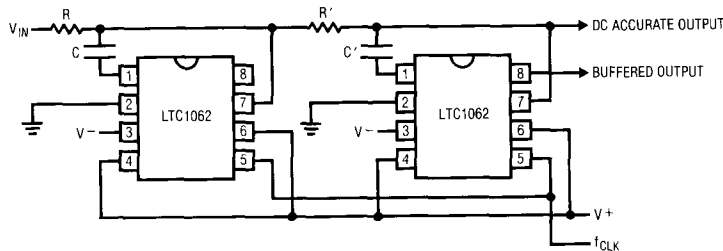


Figure 12. Cascading Two LTC1062s

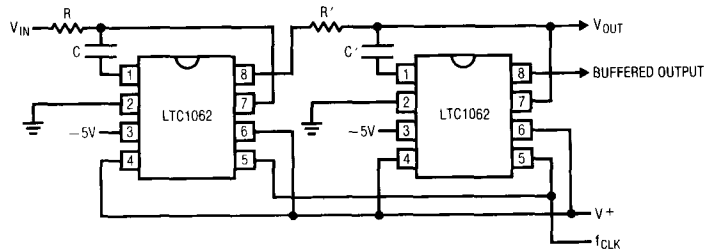


Figure 13. Cascading Two LTC1062s. The 2nd Stage is Driven by the Buffered Output of the First Stage.

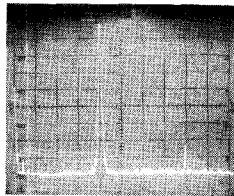
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values of R and R' can be similar. With this approach the passband gain error is reduced to -0.2dB . The recommended equation of the two (R, C) s are the following: $(1/2\pi RC) = f_c / 1.59$ and $(1/2\pi R' C') = f_c / 1.64$ or vice versa.

A 4kHz lowpass filter was tested with the circuit of Figure 13. The measured component values were $R = 97.6\text{k}$ and $C = 676\text{pF}$, $R' = 124\text{k}$ and $C' = 508\text{pF}$. The wideband noise of the filter was $140\mu\text{V}_{\text{RMS}}$ and the worst-case second har-

monic distortion occurred with $f_{\text{IN}} = 0.5 \times f_c$ as shown in Figure 14. With 1V_{RMS} input levels, the signal to noise ratio is 77dB and the worst-case dynamic range is 73dB .

Figure 15 illustrates a 12th order filter using two LTC1062s and a precision dual op amp. The first op amp is used as a precision buffer and the second op amp is used as a simple second order non-inverting lowpass filter to provide the remaining two poles and to eliminate any clock noise.



VERT SCALE: -10dB/DIV
HORIZ SCALE: 500Hz/DIV

↑
2ND HARMONIC = CUTOFF FREQUENCY

Figure 14. Response of the Filter of Figure 13 to a 2kHz 1V_{RMS} Input Sinewave. The 2nd Harmonic (Worst-Case) Occurs at the Filter's Cutoff Frequency.

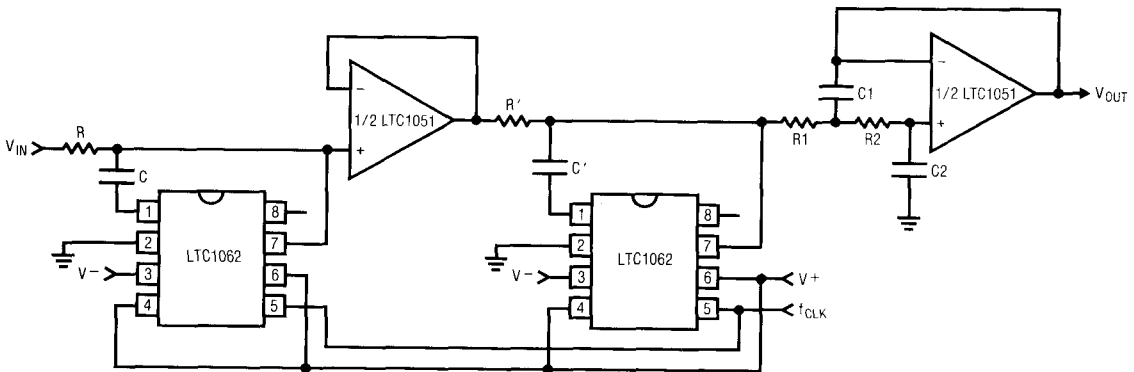


Figure 15. A Very Low Offset, 12th Order, Max Flat Lowpass Filter
 $R = 59\text{k}$, $C = 0.001\mu\text{F}$, $R1 = 5.7\text{k}$, $C1 = 0.01\mu\text{F}$
 $R1 = R2 = 39.8\text{k}$, $C1 = 2000\text{pF}$, $C2 = 500\text{pF}$, $f_{\text{CLK}} = 438\text{kHz}$, $f_c = 4\text{kHz}$

The output filter is tuned at the cutoff frequency of the LTC1062s and has a $Q=1$ to improve the passband error around the cutoff frequency. For gain and Q equal to unity, the design equation for the center frequency, f_o , is simple: let $C1/4C2$ and $R1=R2$, then $f_o=1/(\pi R1C1)$. The filter's overall frequency response is shown in Figure 16 with a 438kHz clock. The measured DC output offset of the filter was $100\mu V$, although the maximum guaranteed offset of each op amp over temperature would be $400\mu V$. Because the active (R, C) output filter is driven directly from the DC accurate output of the second LTC1062, impedance scaling is used with the resistor R' . The noise and distortion performance of this circuit is very similar to the one described for Figure 13.

Using the LTC1062 to Create a Notch

Filters with notches are generally difficult to design and they require tuning. Universal switched capacitor filters can make very precise notches, but their useful bandwidth

should be limited well below half the clock frequency; otherwise, aliasing will severely limit the filter's dynamic range.

The LTC1062 can be used to create a notch because the frequency where it exhibits -180° phase shift is inside its passband as shown in Figure 17. It is repeatable and predictable from part-to-part. An input signal can be summed with the output of the LTC1062 to form a notch as shown in Figure 18. The 180° phase shift of the LTC1062 occurs at $f_{CLK}/118.3$ or 0.85 times the lowpass cutoff frequency. For instance, to obtain a 60Hz notch, the clock frequency should be 7.098kHz and the input $1/(2\pi RC)$ should be approximately 70.98Hz/1.63. The optional (R2C2) of the LTC1062 filters the clock feedthrough. The $1/(2\pi R2C2)$ should be 12-15 times the notch frequency. *The major advantage of this notch is its wide bandwidth. The input frequency range is not limited by the clock frequency because the LTC1062 by itself does not alias.*

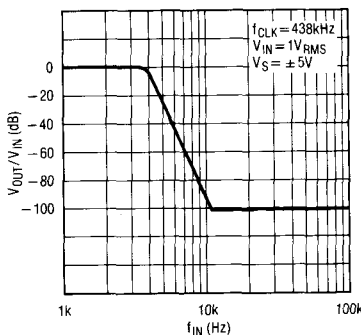


Figure 16. Frequency Response of the 12th Order Filter of Figure 15

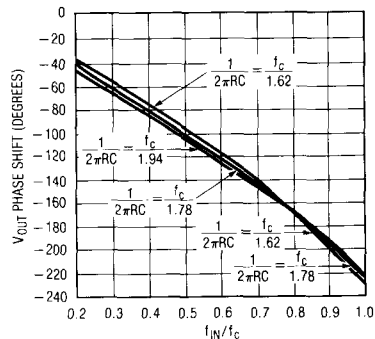


Figure 17. Phase Response of the LTC1062 for Various Input (R, C)s

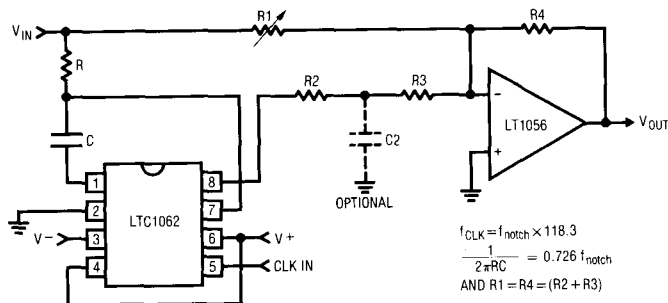


Figure 18. Using the LTC1062 to Create a Notch

Application Note 20

The frequency response of the notch circuit is shown in Figure 19 for a 25Hz notch. From part-to-part, the notch depth varies from 32 to 50dB but it can be optimized by tuning resistor R1. Figure 20 shows an example of the wideband operation of the circuit. These pictures were taken with the filter operating with a 3kHz clock frequency and forming a 25Hz notch. Figure 20A shows the circuit's response to an input 1kHz, 1V_{RMS} sinewave; Figure 20B shows the response to a 10kHz, 1V_{RMS} sinewave. The high frequency distortion of the filter will depend on the quality

of the external op amp and not on the filter. The measured wideband noise from DC to 20kHz was 138V_{RMS} and the measured noise from 50Hz to 20kHz was 30μV_{RMS}.

The circuit of Figure 21 is an extension of the previous notch filter. The input signal is summed with the lowpass filter output through A1, as previously described; then, the output of A1 is again summed with the input voltage through A2.

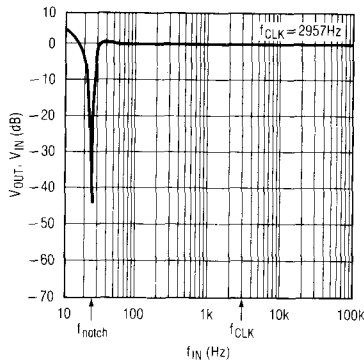
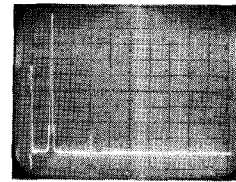
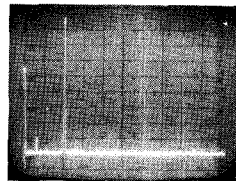


Figure 19



(A) Response of a 25Hz Notch Filter to a 1kHz, 1V_{RMS} Input Sinewave



(B) Same as Above but the Input is a 10kHz Sinewave

Figure 20

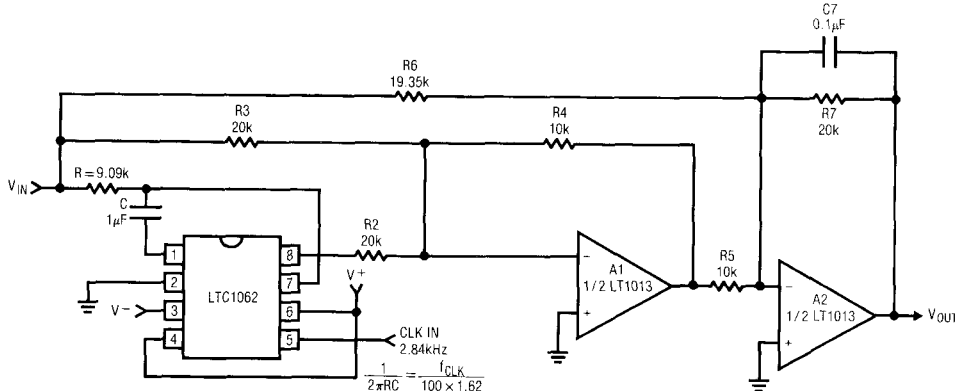


Figure 21. A Lowpass Filter with a 60Hz Notch

If $R6 = R2 = R3 = R7$ and $R4 = R5 = 0.5R7$, the output of A2, at least theoretically, should look like the output of LTC1062 Pin 8. If the ratio of $(R6/R5)$ is slightly less than 2, a notch is introduced in the stopband of the LTC1062 as shown in Figure 22. The overall filter response looks pseudoelliptic lowpass. The frequency of the notch is at $f_{CLK}/47.3$ and the value of the resistor ratio $(R6/R5)$ should be equal to 1.935.

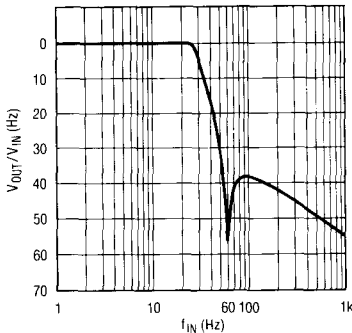


Figure 22. Amplitude Response of the Filter, Figure 21

Comments on Capacitor Types

Experimental work, done in a laboratory environment, shows that the passband gain error is the same when mylar, polystyrene and polypropylene capacitors are used. All the experiments done for this application note used mylar capacitors for $0.001\mu\text{F}$ and up and silver mica for less than 1000pF .

Solid tantalum capacitors connected back-to-back, as shown in Figure 23, introduce an additional passband error of 0.05dB to 0.1dB . For cutoff frequencies well below 10Hz and for limited temperature range, the back-to-back solid tantalum capacitor approach offers an economical and board saving solution provided that their leakage and tolerances are acceptable. When disc ceramic capacitors were used as part of the required input (R, C) of the LTC1062, the passband accuracy of the filter was similar to that obtained with solid tantalum capacitors. Ceramic capacitors should be avoided primarily because of their large and unpredictable temperature coefficient. NPO ceramic capacitors, however, are highly recommended especially for military temperature range. Their maximum available value is of the order of $0.1\mu\text{F}$, their physical size is reasonable and they are available with $\pm 20\text{ppm}/^\circ\text{C}$ tempo.

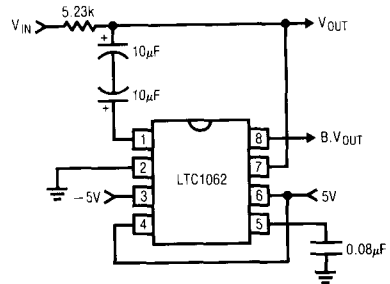


Figure 23. A Low Frequency, 5Hz Filter using Back-to-Back Solid Tantalum Capacitors

Clock Circuits

Application Note 12 describes in detail various clock generation techniques which can be applied for the LTC1062 requirements. Two basic circuits are repeated and explained below:

1. Low frequency oscillators: A simple (R, C) oscillator is shown in Figure 24. It uses a medium speed comparator with hysteresis and a feedback (R1, C1) as timing elements. The capacitor, C1, charges and discharges to $2V^+/3$ and $V^+/3$ respectively. Because of this, the frequency of oscillation is, at least theoretically, independent from the power supply voltage. If the comparator swings to the supply rails, if the pull-up resistor is much smaller than the resistors R_h and if the propagation delay is negligible compared to the RC time constant, the oscillation frequency is:

$$f_{\text{OSC}} = \frac{0.72}{R1C1}$$

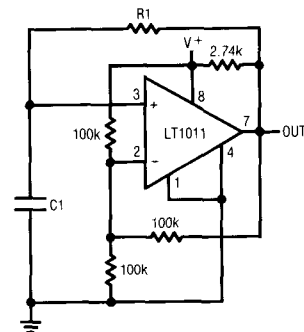


Figure 24. A Low Frequency, Precision (R, C) Oscillator. For Bipolar $\pm 5\text{V}$ Output Swing Refer the Ground Connection to -5V .

Application Note 20

For LT111 or LT1011 type comparators, this holds for $f_{osc} \leq 3\text{kHz}$. The circuit of Figure 24 is adequate to drive an LTC1062 tuned in the vicinity of 10–30Hz cutoff frequency. Also, when the input (R, C) of the LTC1062 and the (R1, C1) of the comparator have the same temperature coefficient, the cutoff frequency will drift but the passband error will be temperature independent since:

$$\frac{1}{(2\pi RC)} \cong \frac{f_c}{1.63} = \frac{0.72}{163 \times R1C1} \text{ or}$$

$$(R1C1/RC) = 1/36.$$

For $C = 10C1$, then $R = 3.6R1$, which yields a reasonable resistor and capacitor value spread.

- The RC oscillator of Figure 24 can also be used up to 110kHz but the frequency of oscillation is about equal to $0.66/R1C1$ and the duty cycle 60%. Again the major frequency drift component will be due to the drift of the $R1C1$. If the cutoff frequency of the filter should be made as temperature independent as possible, the $(R \times C)$ and $(R1 \times C1)$ products should also be made temperature independent. This can be achieved by choosing resistors and capacitors of nearly opposite temperature coefficients. For instance, TRW MTR-5/ + 120ppm/°C resistors can be used with - 120ppm/°C ± 30ppm WESCO type 32-P capacitors.

- Crystal oscillators: Figure 25 shows an LT1011 comparator biased in its linear mode and using a crystal to establish its resonant frequency. With this circuit we can achieve a few hundred kHz, temperature independent clock frequency with nearly 50% duty cycle. Many

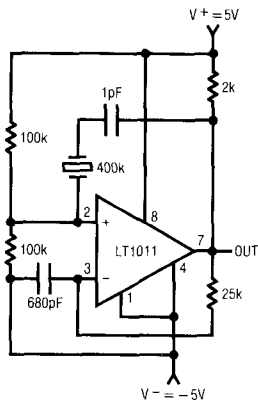


Figure 25. Crystal Oscillator with 50% Duty Cycle

systems already have a crystal oscillator using digital gates as active elements, Figure 26. Their frequency, however, is usually above 1MHz and should be divided down before being applied to the LTC1062. Figure 27 shows an inexpensive discrete crystal oscillator using a single transistor as gain element. Its output can directly drive Pin 5 of the LTC1062 and its Pin 4, should they be converted to analog ground or negative supply to activate the internal divide by 2 or 4 of the circuit. This is necessary because the duty cycle at the collector of the crystal oscillator is not 50%.

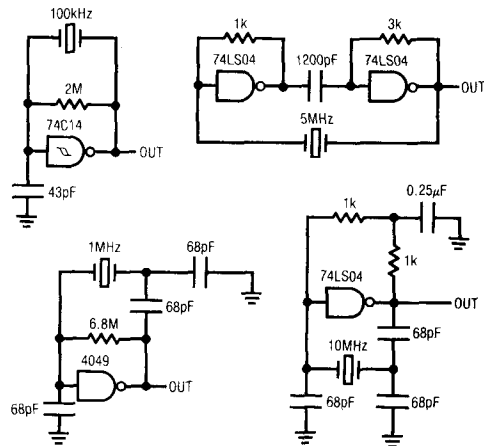


Figure 26. Typical Gate Oscillators

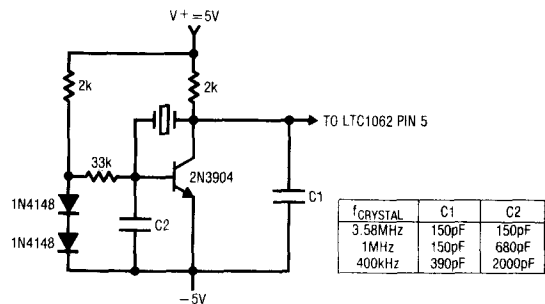


Figure 27. Discrete, Low Cost Oscillator using Parallel Type AT-CUT Crystal

Acknowledgement

For this application note, the laboratory work was done by Guy Hoover whose meticulousness and contributions are greatly appreciated.

Composite Amplifiers

Jim Williams

Amplifier design, regardless of the technology utilized, is a study in compromise. Device limitations make it difficult for a particular amplifier to achieve optimal speed, drift, bias current, noise and power output specifications. As such, various amplifier families emphasizing one or more of these areas have evolved. Some amplifiers are very good attempts at doing everything well, but the best achievable performance figures are limited to dedicated designs.

Practical applications often require an amplifier that has extremely high performance in several areas. For example, high speed and DC precision are often needed. If a single device cannot simultaneously achieve the desired characteristics, a composite amplifier made up of two (or more) devices can be configured to do the job. Composite designs combine the best features of two or more amplifiers to achieve performance unobtainable in a single device. More subtly, composite designs permit circuit approaches which are normally impractical. This is par-

ticularly true of high speed stages which may be designed with little attention to DC biasing considerations if a separate stabilizing stage is employed.

Figure 1 shows a composite made up of an LT1012 low drift device and an LT1022 high speed amplifier. The overall circuit is a unity gain inverter, with the summing node located at the junction of three 10k resistors. The LT1012 monitors this summing node, compares it to ground and drives the LT1022's positive input, completing a DC stabilizing loop around the LT1022. The 10k-300pF time constant at the LT1012 limits its response to low frequency signals. The LT1022 handles high frequency inputs while the LT1012 stabilizes the DC operating point. The 4.7k-220Ω divider at the LT1022 prevents excessive input overdrive during start-up. This circuit combines the LT1012's 35μV offset and 1.5V/°C drift with the LT1022's 23V/μs slew rate and 300kHz full power bandwidth. Bias current, dominated by the LT1012, is about 100pA.

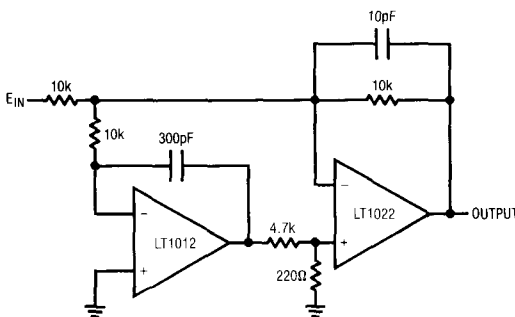


Figure 1. Basic DC Stabilized Fast Amplifier

Application Note 21

Figure 2 is similar, but uses discrete FETs to more than triple the speed. Here A1's input stage is turned off by connecting its inputs to the negative rail. The differentially connected FETs bias the second stage via A1's offset pins. This connection replaces A1's input stage, reducing bias current and increasing speed. FET mismatch would normally result in excessive offset and drift. A2 corrects this by monitoring the summing point (the junction of the two 4.7k resistors) and forcing Q2's gate to eliminate overall offset. The 10k-1000pF pair limits A2's response to low frequency, and the 1k divider chain prevents overdrive to Q2 on start-up. The 1k-10pF damper at the summing node aids high frequency stability. Figure 3 shows pulse response. Trace A is the input and Trace B the output. Slew rate exceeds $100\text{V}/\mu\text{s}$, with clean damping. Full power bandwidth is about 1MHz, and input bias current is in the 100pA range. DC offset and drift are similar to Figure 1.

Figure 4 shows a highly stable unity gain buffer with good speed and high input impedance. Q1 and Q2 constitute a simple, high speed FET input buffer. Q1 functions as a source follower, with the Q2 current source load setting the drain-source channel current. The LT1010 buffer provides output drive capability for cables or whatever load is required. Normally, this open loop configuration would be quite drift because there is no DC feedback. The LTC1052 contributes this function to stabilize the circuit. It does this by comparing the filtered circuit output to a similarly filtered version of the input signal. The amplified difference between these signals is used to set Q2's bias, and hence Q1's channel current. This forces Q1's V_{GS} to whatever voltage is required to match the circuit's input and output potentials. The 2000pF capacitor at A1 provides stable loop compensation. The RC network in A1's output prevents it from seeing high speed edges coupled

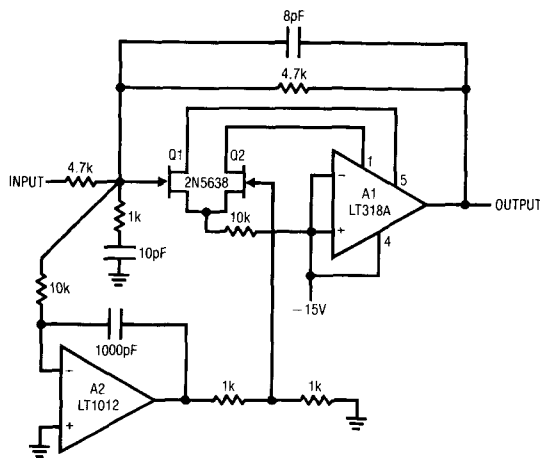


Figure 2. Fast DC Stabilized FET Amplifier

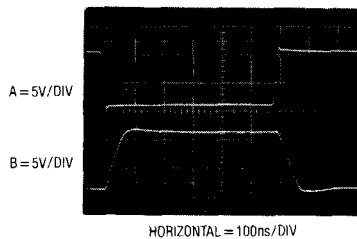


Figure 3. Figure 2's Waveforms

through Q2's collector-base junction. A2's output is also fed back to the shield around Q1's gate lead, bootstrapping the circuit's effective input capacitance down to less than 1pF.

The LT1010's 15MHz bandwidth and 100V/ μ s slew rate, combined with its 150mA output, are fast enough for most circuits. For very fast requirements, the alternate discrete component buffer shown will be useful. Although its out-

put is current limited at 75mA, the GHz range transistors employed provide exceptionally wide bandwidth, fast slewing and very little delay. Figure 5 shows the LTC1052 stabilized buffer circuit's response using the discrete stage. Response is clean and quick, with delay inside 4ns. Slew exceeds 2000V/ μ s with full power bandwidth approaching 50MHz. Note that rise time is limited by the pulse generator and not the circuit. For either stage, offset is set by the LTC1052 at 5 μ V, with gain about 0.95.

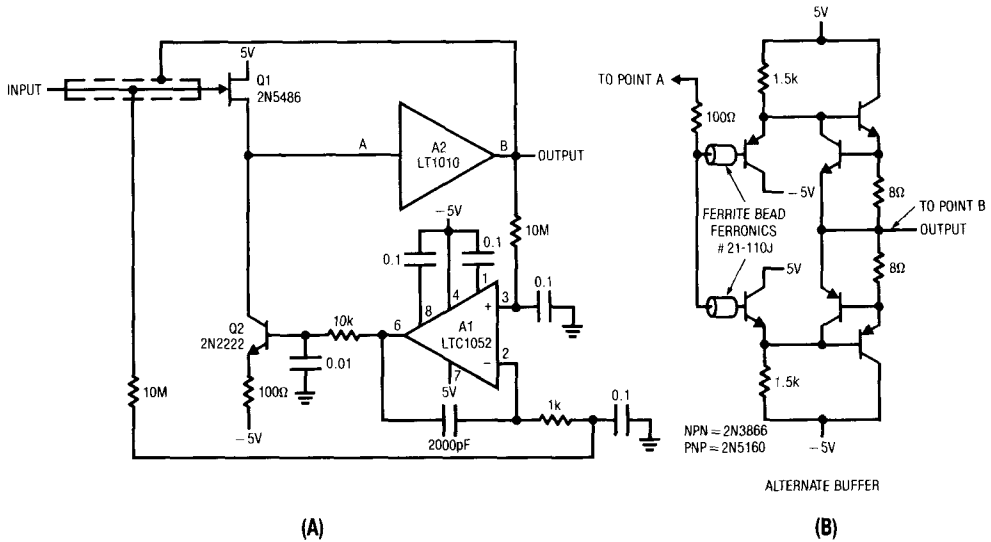


Figure 4. Wideband FET Input Stabilized Buffer

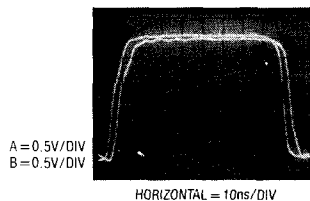


Figure 5. Figure 4's Waveforms

Application Note 21

A potential difficulty with Figure 4's circuit is that the gain is not quite unity. Figure 6 maintains high speed and low bias while achieving a true unity gain transfer function.

This circuit is somewhat similar to Figure 4, except that the Q2-Q3 stage takes gain. A2 DC stabilizes the input-output path, and A1 provides drive capability. Feedback is to Q2's emitter from A1's output. The 1k adjustment allows the gain to be precisely set to unity. With the LT1010 output stage slew and full power bandwidth (1Vp-p) are 100V/ μ s and 10MHz, respectively. -3dB bandwidth exceeds 35MHz. At A = 10 (e.g., 1k adjustment set at 50 Ω) full

power bandwidth stays at 10MHz while the -3dB point falls to 22MHz.

With the optional discrete stage, slew exceeds 1000V/ μ s and full power bandwidth (1Vp-p) is 18MHz. -3dB bandwidth is 58MHz. At A = 10, full power is available to 10MHz, with the -3dB point at 36MHz.

Figures 7A and B show response with both output stages. The LT1010 is used in Figure 7A (Trace A = input, Trace B = output). Figure 7B uses the discrete stage and is slightly faster. Either stage provides more than adequate

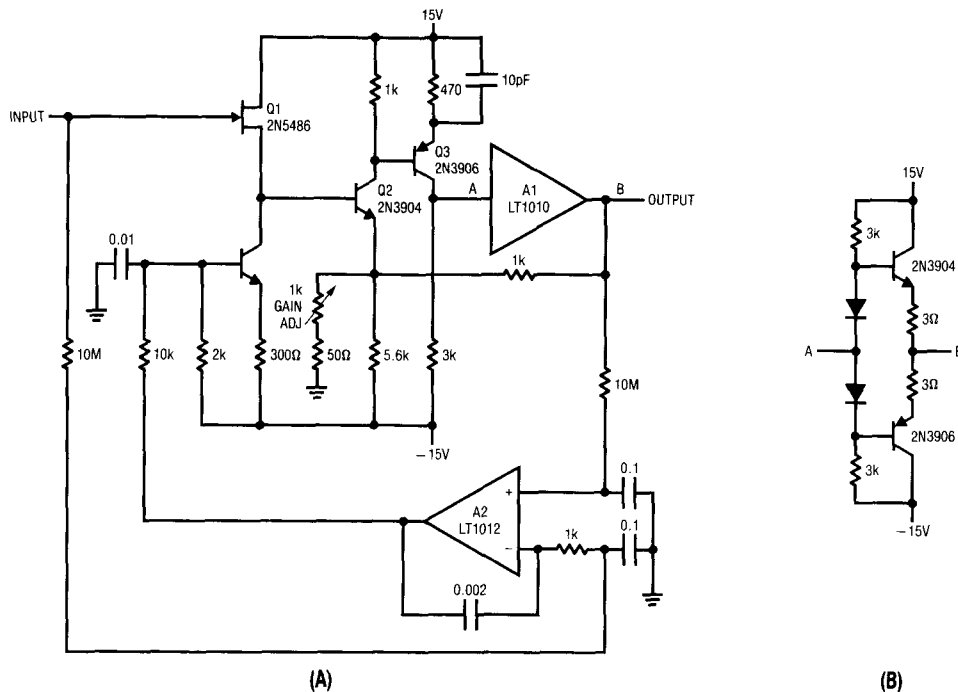


Figure 6. Gain Trimmable Wideband FET Amplifier

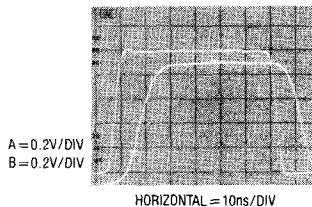


Figure 7A. Figure 6's Waveforms Using LT1010

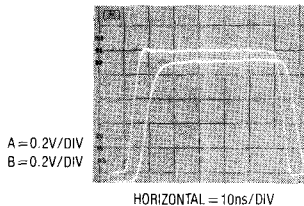


Figure 7B. Figure 6's Waveforms Using Discrete Stage

performance for driving video cable or data converters, and the LT1012 maintains DC stability under all conditions.

Figure 8 is another DC stabilized fast amplifier which functions over a wide range of gains (typically 1-10). It combines the LT1010 and a fast discrete stage with an LT1008 based DC stabilizing loop. Q1 and Q2 form a differential stage which single-ends into the LT1010. The circuit delivers 1Vp-p into a typical 75Ω video load. At A = 2, the gain is within 0.5dB to 10MHz with the -3dB point occurring at 16MHz. At A = 10, the gain is flat (± 0.5 dB to 4MHz) with a -3dB point at 8MHz. The peaking adjustment should be optimized under loaded output conditions.

Normally, the Q1-Q2 pair would be quite drifty, but the LT1008 corrects for this. This correction stage is similar to

the one in Figures 4 and 6, except that the feedback is taken from a divided down sample of the fast amplifier. The ratio of this divider should be set to the same value as the circuit's closed loop gain. Frequency roll-off of this stage is set by the 1M-0.022μF filters in the LT1008's input lines. The 0.22μF capacitor at the amplifier eliminates oscillations. The DC loop servo controls drift by biasing the DC operating point of Q2's collector to force zero error between the LT1008's inputs.

This is a simple stage for fast applications where relatively low output swing is required. Its 1Vp-p output works nicely for video circuits. A possible problem is the relatively high bias current, typically 10μA. Additional swing is possible, but more circuitry is needed.

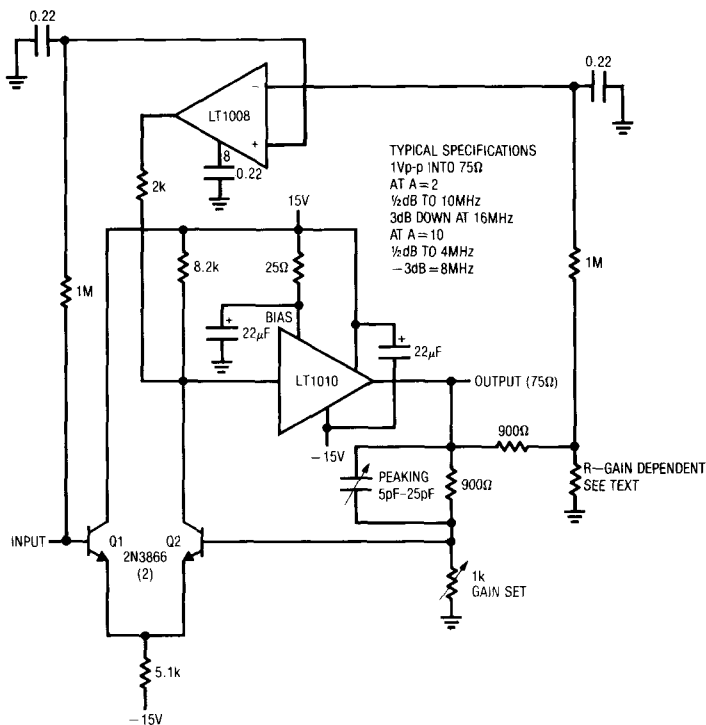


Figure 8. Fast, Stabilized Non-Inverting Amplifier

Application Note 21

Figure 9's circuit addresses these issues. It trades speed for output swing and reduced bias current. As before, a separate loop maintains DC stability. This circuit is a good example of an approach made practical by composite techniques. Without the separate stabilizing loop, the DC imbalances in the signal path would preclude any level of operation.

In this arrangement a PNP level shifting stage (Q4) has been added to Figure 8's circuit to increase available swing at the LT1010 output. This is obtained at the expense of available bandwidth and amplifier stability. The 33pF capacitor from Q4's collector to the circuit's summing node (Q3's gate) affords stable loop compensation.

Figure 8's bias current errors are eliminated by Q3, an FET source follower. This device buffers the summing point from the relatively high bias current required by Q2. Normally, this configuration would cause volts of offset, due to Q3's gate-source voltage. Here, A1 closes a DC restoration loop, forcing Q1's base to whatever point is required to compensate for the offset. Thus, A1's operation not only provides low DC error but permits a simplistic approach to minimizing summing point bias current. Figure 10 shows operating waveforms for a 10V output. Trace A is the input, while Trace B is the output. Slew rate is about $100\text{V}/\mu\text{s}$, with a full power bandwidth of 1MHz. The LT1010 allows 100mA outputs and makes cable driving practical at these speeds.

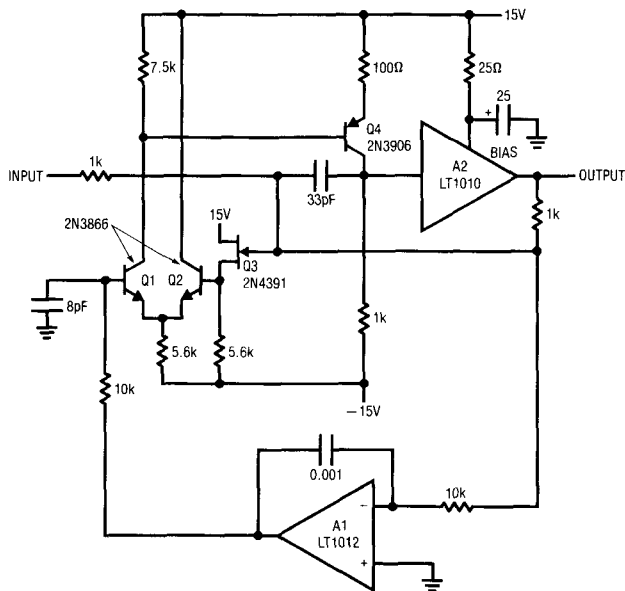


Figure 9. Fast, Stabilized Inverting Amplifier with Low Summing Point Bias Current

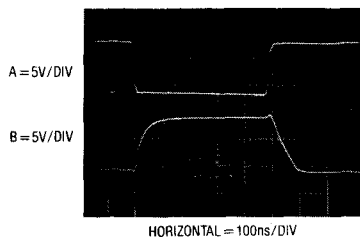


Figure 10. Figure 9's Pulse Response

Figure 11 shows another fast stage with wide output swing. The circuit is non-inverting, and has higher input impedance than Figure 9. Additionally, its operation is based on an arrangement commonly referred to as "current mode" feedback. This technique, well established in RF design and also employed in some monolithic instrumentation amplifiers, permits fixed bandwidth over a wide range of closed loop gains. This contrasts with normal feedback schemes, where bandwidth degrades as closed loop gain increases.

The overall amplifier is composed of two LT1010 buffers and a gain stage, Q1 and Q2. A3 acts as a DC restoration loop. The 33Ω resistors sense A1's operating current, biasing Q1 and Q2. These devices furnish complementary voltage gain to A2, which provides the circuit's output. Feedback is from A2's output to A1's output, which is a low impedance point.

A3's stabilizing loop compensates large offsets in the signal path, which are dominated by mismatch in Q1 and

Q2. Correction is implemented by controlling the current through Q3, which shunts Q2's base bias resistor. Adequate loop capture range is assured by deliberate skewing of Q1's operating point via the 330Ω unit. The 9k-1k feedback divider feeding A3 is selected to equal the gain ratio of the circuit, in this case 10.

The feedback scheme makes A1's output look like the negative input of the amplifier, with closed loop gain set by the ratio of the 470Ω and 51Ω resistors. The outstanding feature of this connection is that bandwidth becomes relatively independent of closed loop gain over a reasonable range. For this circuit, full power bandwidth remains at 1MHz over gains of 1 to about 20. The loop is quite stable, and the 15pF value at A2's input provides good damping over a wide range of gains. The LT1010 buffers limit bandwidth in this circuit. Dramatic speed improvement is possible if they are replaced by discrete stages.

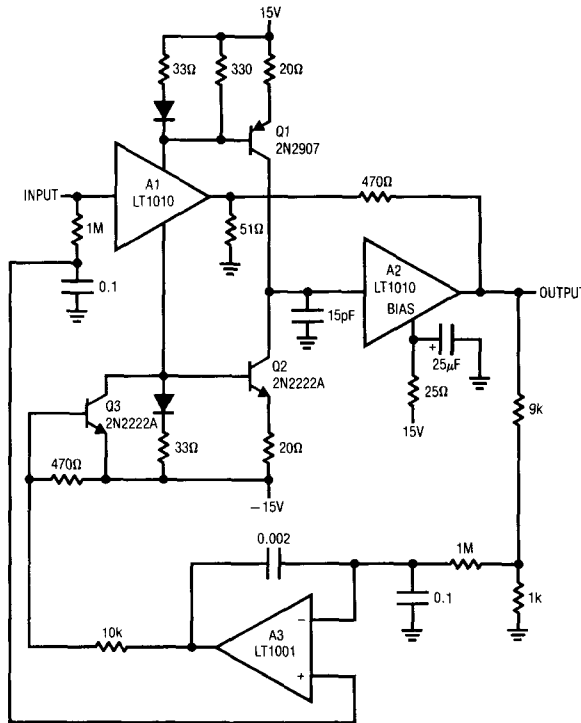


Figure 11. "Current Mode Feedback" Amplifier

Application Note 21

Figure 12 substitutes discrete elements for Figure 11's LT1010s. Although this arrangement is substantially more complex, it provides an extraordinarily wideband amplifier. This composite design is composed of three ampli-

fiers; the discrete wideband stage, a quiescent current control amp and an offset servo. Q1-Q4 replace Figure 11's A1, although complementary voltage gain is taken at the collectors of Q3 and Q4. Q5 and Q6 provide

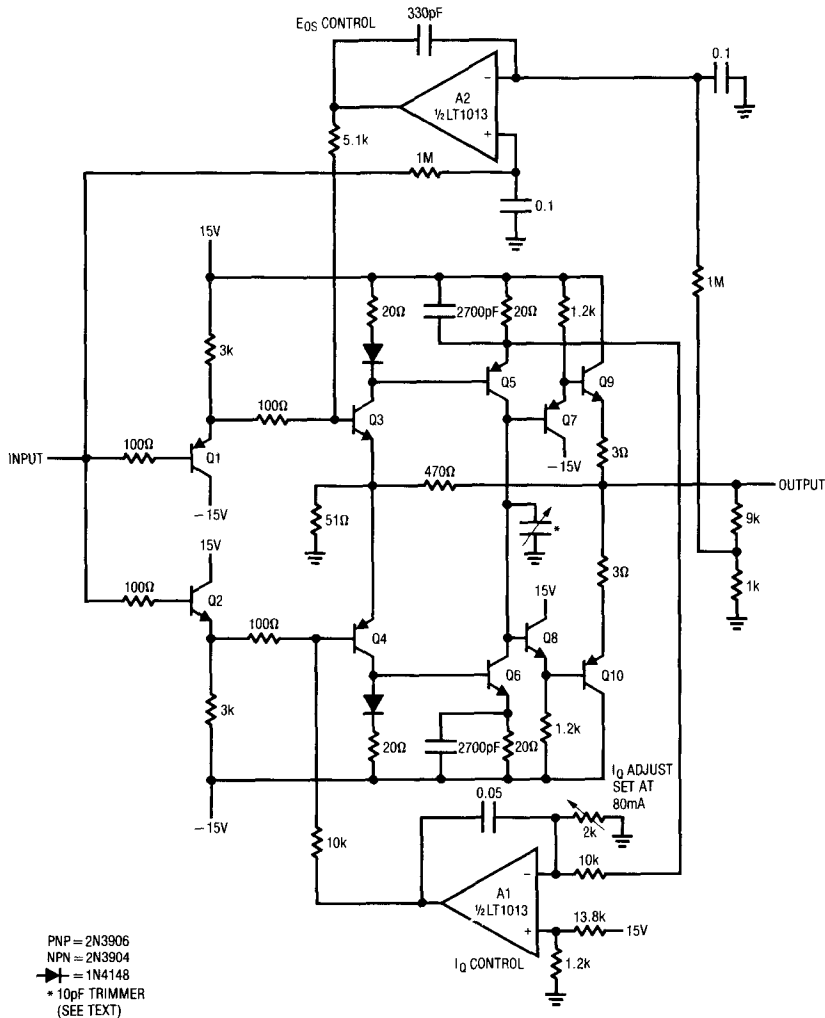


Figure 12. Stabilized, Ultra-Wideband "Current Mode Feedback" Amplifier (Son of Godzilla Amplifier)

additional gain, similar to Q1 and Q2 in Figure 11. Q7-Q10 form the output buffer stage. The feedback scheme is identical to Figure 11's, with summing action at the Q3-Q4 emitter connection. To obtain maximum bandwidth, quiescent current is quite high. Without closed loop control, the circuit will quickly go into thermal runaway and destroy itself. A1 provides the required servo control of quiescent current. It does this by sampling a resistively divided version of the voltage across Q5's emitter resistor and comparing it to a power supply derived reference. A1's output biases Q4, completing a loop which forces fixed current through Q5. This action effectively controls overall quiescent current in the discrete stage. Simultaneously, A2 corrects for offset by forcing Q3's base to equalize the DC input and output values at the discrete stage. Because the closed loop gain is set at 10 (470 Ω and 51 Ω ratio), A2 samples the output via the 10:1 divider. Both A1 and A2 have local roll-off, limiting their response to low frequency. Casual consideration of A1 and A2's operation might raise concern about interaction, but detailed analysis shows

this is not so. The offset and quiescent current loops do not influence each others operation.

When this circuit is constructed using high frequency layout techniques and a ground plane, performance is quite impressive. For gains of 1 to 20, full power bandwidth remains at 25MHz, with the -3dB point beyond 110MHz. Slew rate exceeds 3000V/ μ s. These figures can be improved upon by using RF transistors, although the types shown are inexpensive and readily available. Figure 13 shows pulse response for a $\pm 12V$ output (Trace B) at a gain of 10 (input is Trace A). Delay is about 6ns, with rise-time limited by the input pulse generator. Damping is optimized with the 10pF trimmer at the Q5-Q6 collector line. To use this circuit, adjust the I_Q level to 80mA **IMMEDIATELY** after turn on. Next, set A2's input resistor divider to a ratio appropriate to the closed loop circuit gain. Finally, adjust the 10pF trimmer for best response. Note that, in the interests of speed, this circuit has no output protection.

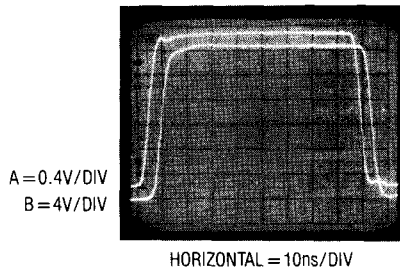


Figure 13. Figure 12's Pulse Response (Measurement Limited by Pulse Generator)

Application Note 21

Although speed and offset combinations are the most common area for composite techniques, other circuits are possible. Figure 14 shows a way to combine a low drift chopper stabilized amplifier with an ultra-low noise bipolar amplifier. The LTC1052 measures the DC error at the LT1028's input terminals and biases its offset pins to force offset to a few microvolts. The 1N758 zeners allow the LTC1052 to function from $\pm 15V$ rails. The offset pin biasing at the LT1028 is arranged so the LTC1052 will always

be able to find the servo point. The $0.01\mu F$ capacitor rolls off the LTC1052 at low frequency, and the LT1028 handles high frequency signals. The combined characteristics of these amplifiers yield the following performance;

Offset Voltage	$5\mu V$ max.
Offset Drift	$50nV/^{\circ}C$ max.
Noise	$1.1nV/\sqrt{Hz}$ max.

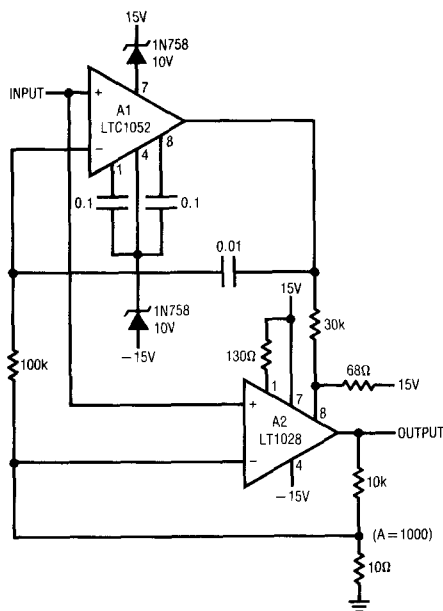


Figure 14. DC Stabilized, Low Noise Amplifier

Figure 15 plots noise amplitude over time in a 0.1-10Hz bandwidth.

fact that noise decreases by the \sqrt{N} of the number of devices in parallel. For example, for nine paralleled amplifiers, noise would decrease by a factor of three, to about $0.33\text{nV}/\sqrt{\text{Hz}}$ at 1kHz. A potential penalty of this connection is that the input current noise increases by \sqrt{N} devices.

Figure 16 uses multiple LT1028 low noise amplifiers in a statistical noise reduction technique. It is based on the

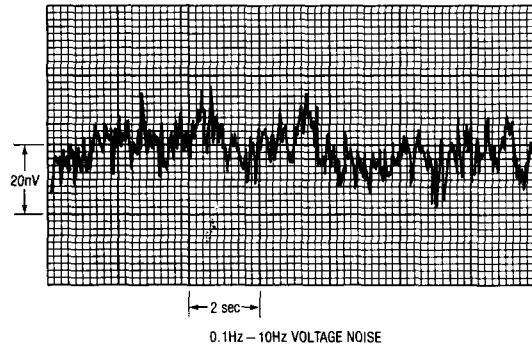


Figure 15. Figure 14's Noise vs Time

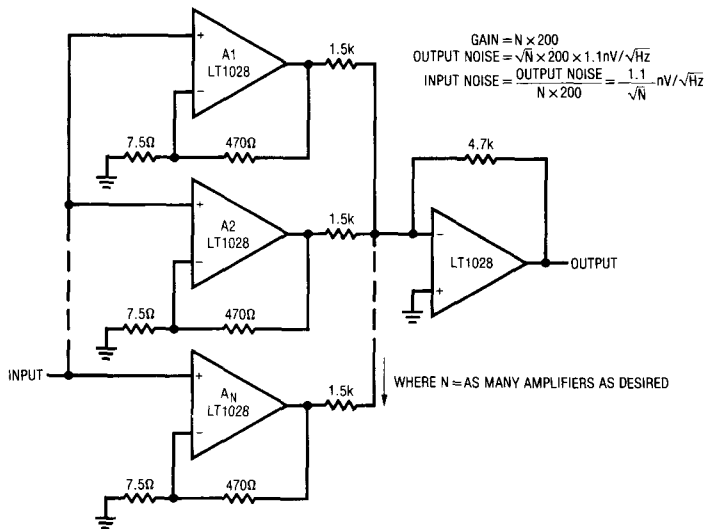


Figure 16. Low Noise Amplifier Using Paralleled Amplifiers

Application Note 21

A final circuit, Figure 17, uses a composite of paralleled LT1010 buffers to create a simple, high current stage. Parallel operation provides reduced output impedance, more drive capability and increased frequency response under load. Any number of LT1010s can be directly paralleled as long as the increased dissipation in individual units caused by mismatches of output resistance and offset voltage is taken into account.

When the inputs and outputs of two buffers are connected together, a current, ΔI_{OUT} , flows between the outputs:

$$\Delta I_{OUT} = \frac{V_{OS1} - V_{OS2}}{R_{OUT1} + R_{OUT2}},$$

where V_{OS} and R_{OUT} are the offset voltage and output resistance of the respective buffers.

Normally, the negative supply current of one unit will increase and the other decrease, with the positive supply current staying the same. The worst-case ($V_{IN} \rightarrow V^+$) increase in standby dissipation can be assumed to be $\Delta I_{OUT} V_T$, where V_T is the total supply voltage.

Offset voltage is specified worst-case over a range of supply voltages, input voltage and temperature. It would be unrealistic to use these worst-case numbers above because paralleled units are operating under identical conditions. The offset voltage specified for $V_S = \pm 15V$, $V_{IN} = 0$ and $T_A = 25^\circ C$ will suffice for a worst-case condition.

Output load current will be divided based on the output resistance of the individual buffers. Therefore, the available output current will not quite be doubled unless output resistances are matched. As for offset voltage above, the $25^\circ C$ limits should be used for worst-case calculations.

Parallel operation is not thermally unstable. Should one unit get hotter than its mates, its share of the output and its standby dissipation will decrease.

As a practical matter, parallel connection needs only some increased attention to heat sinking. In some applications a few ohms equalization resistance in each output may be wise. Only the most demanding applications should require matching, and then just of output resistance at $25^\circ C$.

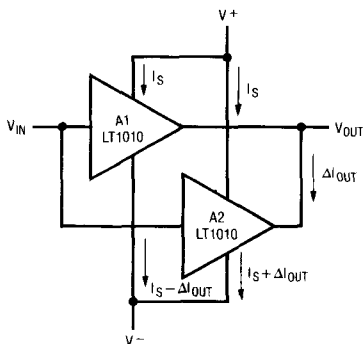


Figure 17. Paralleling Scheme for High Current Output

A Monolithic IC for 100MHz RMS-DC Conversion

Jim Williams

Previous monolithic circuits that converted waveforms to their DC-RMS equivalents utilized logarithmic techniques. This method limits bandwidth to below 1MHz and crest factor performance to about 10:1. Practically speaking, a waveform's RMS value is defined as its heating value in the load. Specialized instruments employ thermally based assemblies that compute the RMS value of the input. The thermal method provides substantially improved bandwidth and crest factor capability compared to logarithmically based converters.

Applications such as wideband RMS voltmeters, RF leveling loops, wideband AGC, high crest factor measurements, SCR power monitoring and high frequency noise measurements require the advantages of thermally based conversion.

Thermal RMS-DC converters are direct acting, thermo-electronic analog computers. The thermal technique is explicit, relying on "first principles." The simple operation permits wideband performance unattainable with implicit, indirect methods based on logarithmic computing.

Previously, thermally based converters were large and expensive to produce. A new IC, the LT1088, brings the advantages of thermal conversion to the circuit board in a 14 pin DIP, and at reasonable cost. Before discussing the LT1088, it is worthwhile reviewing thermal RMS-DC conversion.

Figure 1 shows a conceptual thermal RMS-DC converter. The input waveform warms the heater, resulting in increased output from the temperature sensor. The heating is related to the RMS value of the input waveform. The temperature sensor's DC output represents this heating.

Although simple, this method has some problems. The temperature sensor cannot distinguish between signal and ambient induced temperature changes. This issue could be addressed by summing in ambient temperature information, but a more significant problem remains. Even if the electrical portions of the design are perfectly linear, overall response is not. The power produced by the heater is non-linearly related to the input voltage ($P = I^2R$); hence temperature rise is similarly non-linearly proportioned.

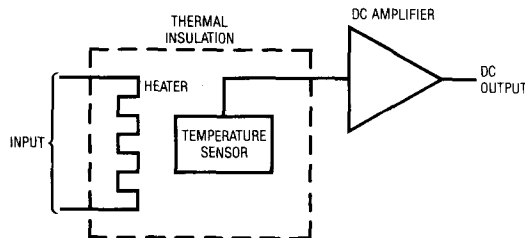


Figure 1. Conceptual RMS-DC Converter (with some problems)

Application Note 22

Additional non-linear signal conditioning is necessary for an output which linearly corresponds to the input voltage.

Figure 2 shows a classic scheme which corrects both of Figure 1's deficiencies. Here, the DC amplifier forces a second, identical, heater-sensor pair to the same thermal conditions as the input driven pair. This differentially sensed, feedback enforced loop makes ambient temperature shifts a common-mode term, eliminating their effect. Also, although the voltage and thermal interaction is non-linear, the input-output voltage relationship is linear with unity gain.

The ability of this arrangement to reject ambient temperature shifts depends on the heater-sensor pairs being isothermal. This is achievable by thermally insulating them with a time constant well below that of ambient shifts. If the time constants to the heater-sensor pairs are matched, ambient temperature terms will affect the pairs equally in phase and amplitude. The DC amplifier will reject this common-mode term. Note that, although the pairs are isothermal, they are insulated from each other. Any thermal interaction between the pairs reduces the system's thermally based gain terms. This would cause unfavorable signal-to-noise performance, limiting dynamic operating range.

Figure 2's output is linear because the matched thermal pair's non-linear voltage-temperature relationships cancel each other.

The advantages of this approach have made its use popular in thermally based RMS-DC measurements. Typically, the assembly is composed of matched heater resistors, sensors and thermal insulation. These assemblies are relatively large and expensive to produce. In theory, monolithic IC techniques can be used to replace such assemblies, but the thermal insulation requirements present problems.

A simplified monolithically based circuit which accomplishes this function appears in Figure 3. It is quite similar to Figure 2's generalized approach. Here, the input drives R1, producing heating which lowers the value of D1's voltage. A1 responds by driving R2 to heat D2, closing a loop around the amplifier. Because the transistors and resistors are matched, A1's DC output equals the RMS value of the input, regardless of input frequency or waveshape. The aforementioned thermal terms limit the circuit's practical performance. In particular, thermal cross-coupling between the R1-D1 and R2-D2 pairs degenerates gain, degrading available signal. Also, differences in the dissipation constants and thermal capacity of the R-D pairs

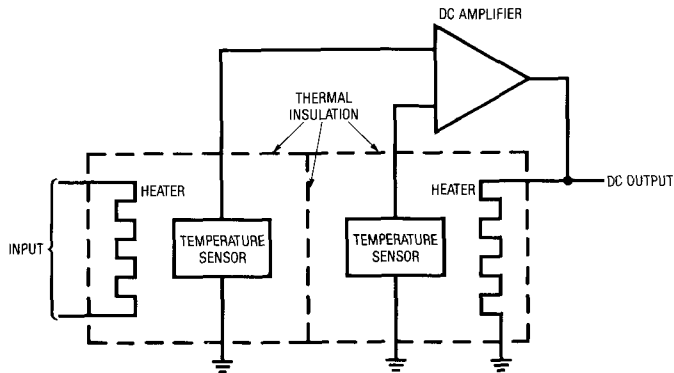


Figure 2. (A Better) Conceptual Thermal RMS-DC Converter

result in overall gain errors. Additionally, thermal resistance to ambient must be high to maximize D1-D2 signal output for reasonable input drive. Finally, the thermal path between the mated resistor-transistor pairs must be designed for efficient, low loss heat transfer.

Although the converter's basic principle is a straightforward extension of Figure 2, the electro-thermal design must be carefully addressed to produce a practical monolithic circuit. These thermal considerations dominate the design and form of the circuit.

Figure 4 shows a simple electro-analog of the thermal terms in the converter. The overall lumped matching of these terms heavily influences achievable performance. In particular, the die attach thermal resistance dominates

the thermal impedance path. If this resistance is made very high, the effects of mismatch in the other terms are minimized.

Thermal cross-coupling is almost entirely eliminated by using separate, identical die for the diode-heater pairs. This eliminates cross heating more effectively than any possible single die approach. A gain error, which is corrected by introducing a corresponding gain trim, is caused by residual mismatch in thermal terms. These include die size, dissipation constant, and thermal capacity differences. The most significant term is differing amounts and distribution of the die attach material. The gain correcting trim is introduced by altering the gain of the output stage in Figure 3.

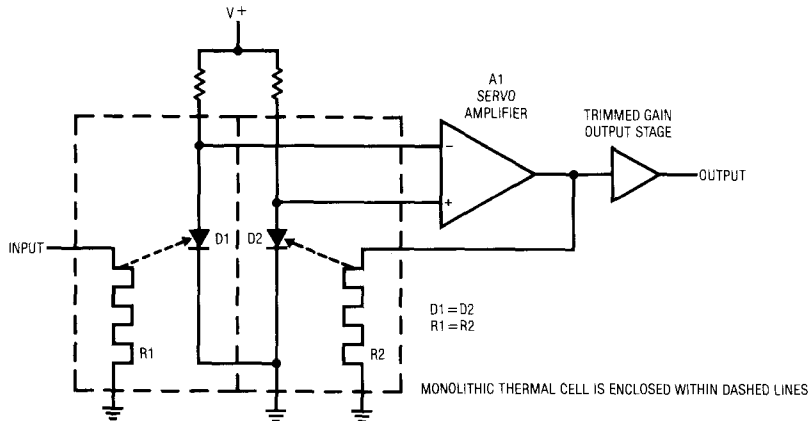


Figure 3. Simplified Monolithic Thermal RMS-DC Converter

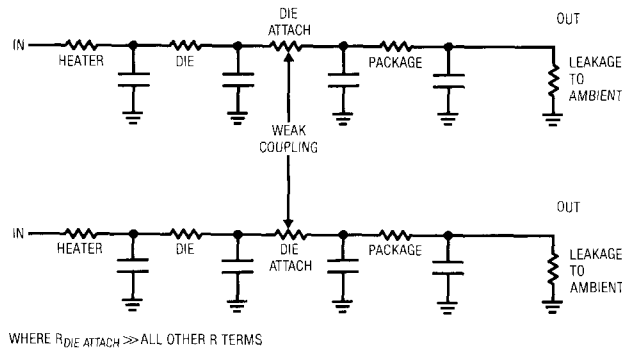


Figure 4. Simplified Electro-Analog of the LT1088

Application Note 22

Because the die attach resistance is so important (see Box Section, "Measuring Thermal Resistance") it must be carefully considered. Figure 5 shows results for various die attach methods. As might be suspected, die suspended in free air offer the highest thermal resistance, although the approach is impractical. Conversely, standard eutectic bonding gives low thermal resistance but is easy to produce. Another die attach method, air impregnated polymer, is nearly as good as air suspension, and is practical. The OTT™ process (Oracular Thermal Transfer) was developed to allow use of air impregnated polymer die attach. Figure 6 is a side-on die photo showing the results of OTT processing beneath the die. Large areas beneath the die are filled with air, resulting in the high thermal resistance noted in Figure 5. Sufficient amounts of polymer attach material ensure a reliable die attach.

OTT™ is a trademark of Linear Technology Corp.

Die Attach Type	Thermal Resistance°C Per Watt
Air Suspended	460
Air Impregnated Polymer	300
Epoxy/2 Mil Polymer Barrier	250
Glass-10 Mil	115
Epoxy/1 Mil Polymer Barrier	107
Eutectic	54

Figure 5 Thermal Resistance vs Die Attach Types

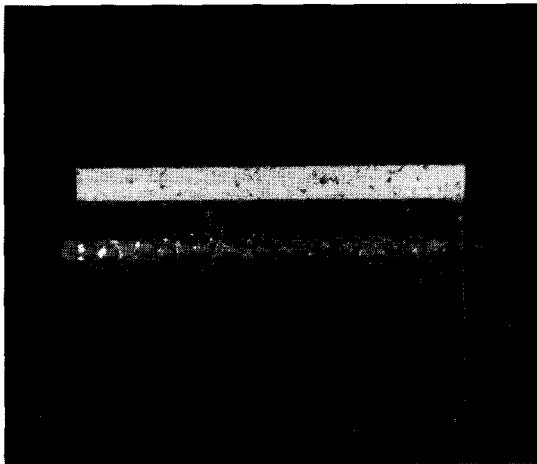


Figure 6. Side-On Chip Photo Details the Air Impregnated Die Attach Produced by the OTT Process. The Two Distinct Die Regions are Caused by Scribe and Break Operations.

Figure 7 is a die shot of one heater resistor-diode pair of the LT1088. The circular, concentric heater resistors promote evenly distributed, isothermal characteristics. The placement and aspect ratio of the heater rings is optimized for an even thermal flow across the die. The sensing diode is actually a paralleled quad located symmetrically about the die center. This quad arrangement provides improved temperature sensing characteristics over a single device. The separate heater rings allow the user to select either a 50Ω or 250Ω input. The test structure in the die center is not used. It is designed to offset effects described by Counts Theorem (see References). Note that the IC contains only the basic thermal components to maintain isothermal conditions. Inclusion of support circuitry would add thermally based error terms, degrading performance.

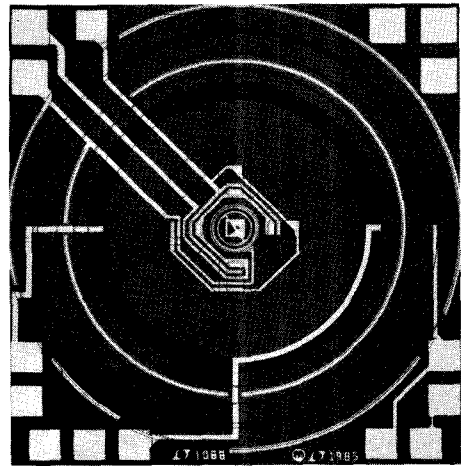


Figure 7. Die Photo of the LT1088 Showing 50Ω (inner ring) and 250Ω (outer ring) Heaters

Figure 8 shows a detailed circuit using the LT1088. Typical performance specifications are given in Figure 9. The LT1088's temperature sensing diodes are biased from the supply. A1, set up as a differential servo amplifier with a

gain of 9000, extracts the diode's difference signal and biases Q1. Q1 drives one of the LT1088's heaters, completing a loop. The 3300pF capacitor gives a stable roll-off. The 1.5M-0.022μF combination improves settling by reducing

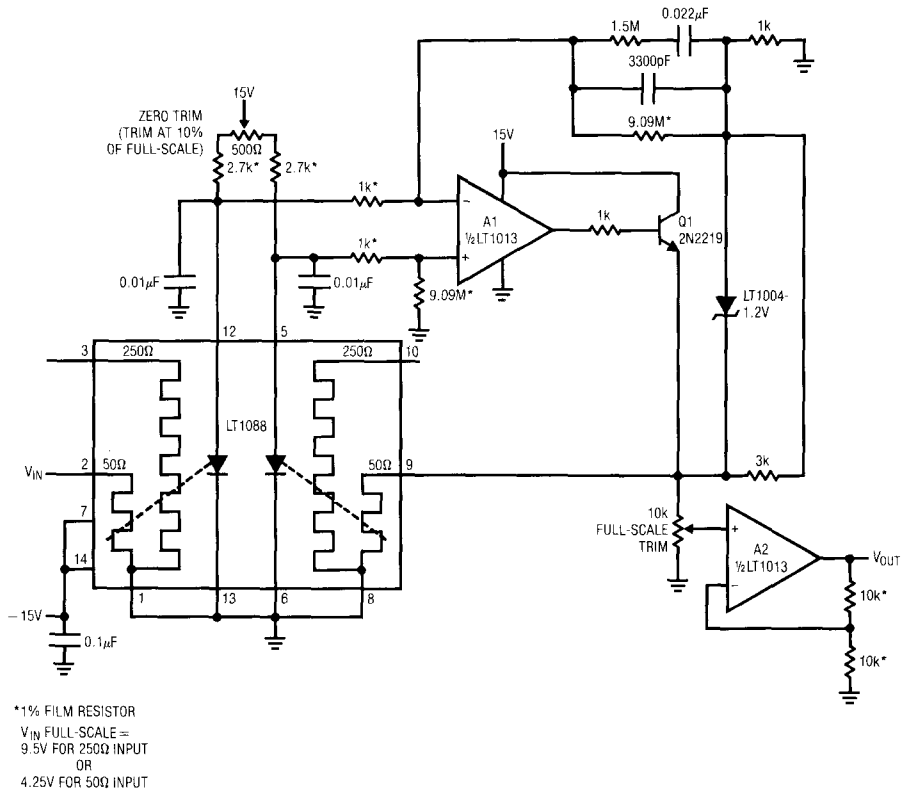


Figure 8. Practical Circuit for the LT1088

Accuracy:	Crest Factor:
50Ω Input	50Ω Input 50:1
DC to 50MHz 1% FS	250Ω Input 40:1
DC to 100MHz 2% FS	3dB Bandwidth 300MHz
250Ω Input	Full-Scale Settling Time (1%) 500ms
DC to 20MHz 1% FS	Input Voltage Range
Temperature Effect on Accuracy 100ppm/°C	50Ω Input 4.25V
Dynamic Range 20:1	250Ω Input 9.5V

Figure 9. Typical Specifications for Figure 8's Circuit

Application Note 22

gain during output slew. The square-law thermal gain of the LT1088 means overall loop gain is lower for small inputs. Normally, this would result in slow settling for values below about 10–20% of scale. The LT1004 1k-3k network is a simple breakpoint, boosting amplifier gain in this region to improve settling. A2, a gain trimmable output stage, serves to compensate for gain variations in the two sides of the LT1088. To trim the circuit, put in about a 10% scale DC signal (e.g., 1V for the 250 Ω input, 500mV for the 50 Ω input). Adjust the “zero trim” so that $V_{OUT} = V_{IN}$. Next, apply a full-scale DC input and set the “full-scale trim” to that value at the output. Repeat the trims until both are fixed well within 1% of full-scale. An alternate trim scheme involves applying no input, grounding Q1’s base and setting the “zero trim” until A1’s output is active. Then, unground Q1’s base and apply a full-scale input and trim the “full-scale” adjustment for that value at the output.

At frequencies above 10MHz, input connections require care. Parasitic inductance builds quickly in wire runs, so the LT1088’s input heater lead should be *directly* con-

nected to the source to be measured. It is also wise to shield the input line from the rest of the circuit. Figure 10 shows one way to do this. A simple copper RF shield isolates the circuitry from the input. The LT1088 is mounted so the input pin is as close as possible to the input connector pin. An additional precaution is to mount the 0.01 μ F bypass capacitors right at the LT1088 package. These units minimize the effects of RF pick-up by the temperature sensing diodes. Another layout concern involves thermal considerations. Because the LT1088’s operation depends on thermal symmetry, it is sensitive to external temperature gradients. This is particularly the case for small inputs which force the device to run very close to ambient temperature. The device should be mounted in an area which is isothermal and free of drafts. Power generating components should be kept away from the LT1088 and particular caution taken in fan cooled equipment. Under normal conditions no thermal baffle or enclosure is required. Under no circumstances should a heat sink be used.

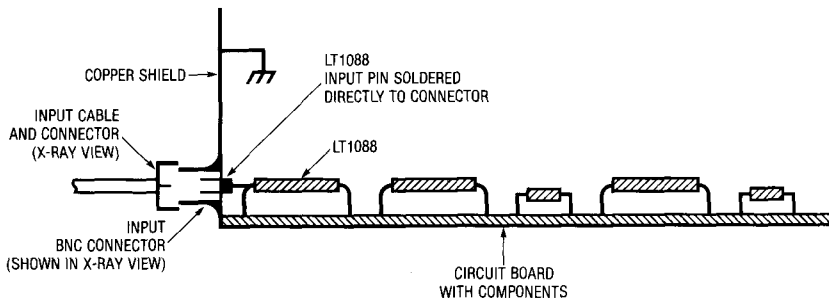


Figure 10. Recommended Layout

Figure 11 is a plot of output error vs input frequency using the 50Ω input at full-scale. There is no degradation of bandwidth for smaller inputs. Thermal transfer standards (Fluke Model 540B with A-55 converters) certified to 50MHz were used as references. The data above 50MHz was also taken with these references, although the individual units used had not been certified at these frequencies. The accuracy of units of this type which have been certified is normally inside the tolerances listed, so there is good probability the data is valid. Figure 12 is a similar plot but over extended ranges of frequency and flatness. Unfortunately, equipment and test set-up limitations imposed uncertainties at the highest frequencies, but the data probably approximates actual performance. The peaking followed by the steep roll-off is most likely due to the LT1088's high frequency limitations. In particular, bond wire inductance becomes increasingly significant as frequency increases. Also, capacitance between the heater and sensing diode permits RF pumping of the

diode, almost certainly causing deleterious results. The 1% error point using the 250Ω range is lower. The parasitics described combine with the higher input voltage swing to limit 1% bandwidth to about 20MHz.

The low end of the frequency spectrum is limited by loop time constants. For Figure 8's values, the circuit begins to follow the input below about 50Hz. Lower frequency operation requires longer loop time constants (e.g., increasing the 3300pF value), increasing settling time.

Crest factor performance is set by IC breakdown limits and the usable low input power range. Breakdown limits are a function of processing. The usable low input power range is a basic signal-to-noise conflict. Low input power produces small amounts of signal. This makes accurate, stable discrimination between desired inputs and ambient thermal phenomena uncertain and noisy.

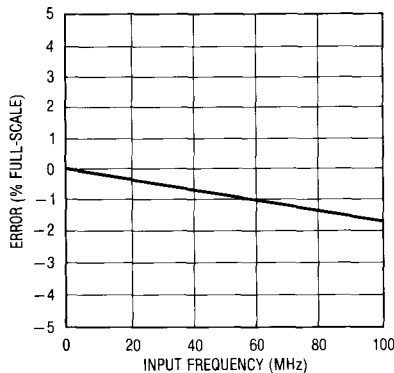


Figure 11. Error vs Frequency

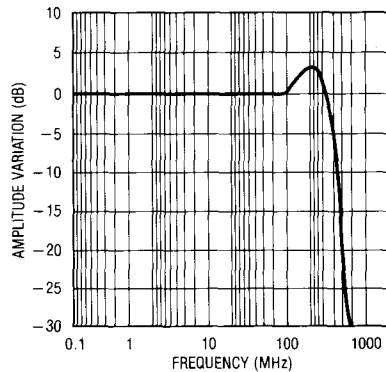


Figure 12. Extended Plot of LT1088 Frequency Response

Application Note 22

Step response is determined by the servo electronics roll-off. Figure 13 shows response for a full-scale step into the 250Ω heater. Loop response is nicely damped. The small glitching at the beginning of the step is due to the gain breakpoint in A1's feedback loop. Figure 14 shows the negative going step. Although the response appears clean (again, the gain glitch is due to A1's breakpoint network), Figure 15 reveals the loop coming to a new value well after it appears to have settled. This photo is a slower version of Figure 14 (initial negative going step is just visible at the extreme left). Almost 5 seconds after settling apparently occurs the loop abruptly assumes a new value. This effect

is due to the loop being driven into saturation. The allowable low range operating area (defined by the dynamic range specification) has been exceeded, forcing the servo into saturation. This causes thermal imbalances in the LT1088, resulting in the extended length of time before the loop becomes active again.* Figure 16 shows response when the input is kept within the specified operating range. Settling on both edges is clean, and the loop quickly assumes and maintains its final value.

*As an interesting exercise, consider what would happen if the servo amplifier could somehow extract, as well as supply, heat to the system.

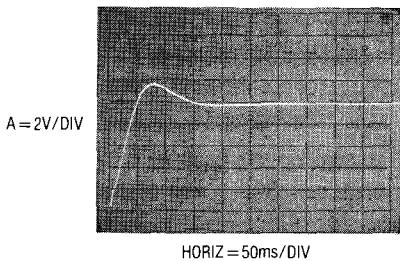


Figure 13. Loop Response for Input Step

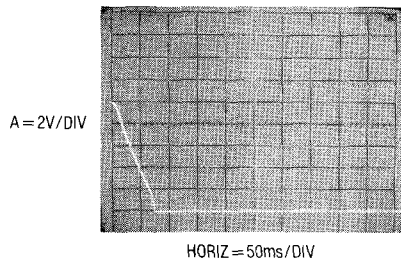


Figure 14. Falling Edge with Loop Driven into Cut-Off

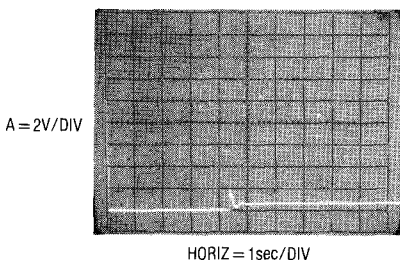


Figure 15. Loop Recovery from Cut-Off

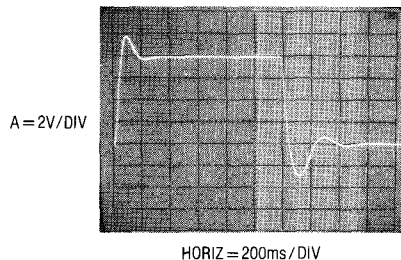


Figure 16. Loop Response with Input Kept in the Linear Region

Some applications may drive the LT1088 outside its operating range, forcing thermal imbalance. If fast settling is required, Figure 17's circuit is useful. This scheme speeds settling by applying an open loop heating correction when thermal imbalance occurs. When the input (Trace A, Figure 18) steps negatively, A1's output (Trace B) slews. Loop delays cause A1 to overshoot, turning off

heater drive and thermally imbalancing the LT1088. Diode steering at the LT1010 buffer's output sinks current from the 250Ω input heater (Trace C). This produces heating, tending to compensate the thermal imbalance, thereby decreasing settling time. Trace D, A2's output, settles fairly quickly after it recovers from the open loop correction.

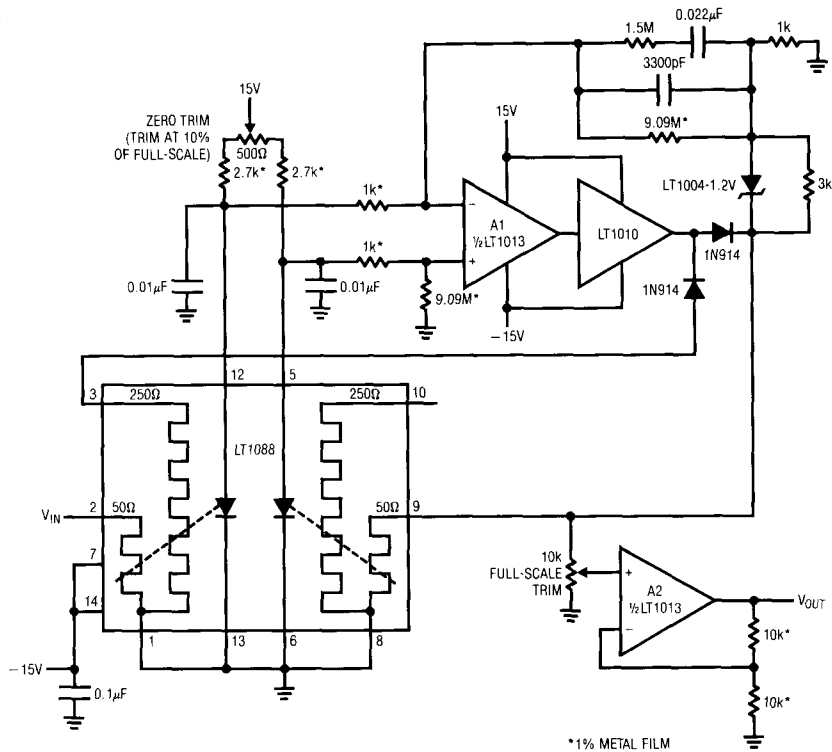


Figure 17. Fast Recovery Circuit (diode steering provides compensation for thermal imbalance)

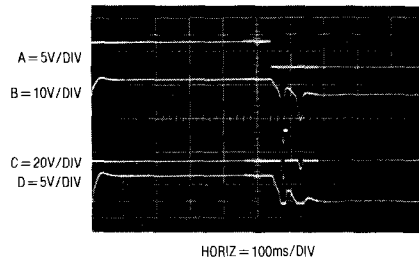


Figure 18. Waveforms for Fast Recovery Circuit

Application Note 22

Any study of LT1088 dynamics must consider that although the output voltage has settled, internal die temperature may still be moving towards final value. It is important to distinguish between voltage and thermal dynamics when observing LT1088 operation.

Most LT1088 failures will be caused by excessive heater drive. Input power (25°C) is specified at 375mW continuous with 30 second excursions to 435mW permitted. These figures are derated by $-3\text{mW}/^\circ\text{C}$ above 25°C. Figure 19 plots safe operating limits for input duty cycle vs input voltage. Accidental heater overdrives can damage or destroy the LT1088. In situations where overdrive may occur, some form of heater protection should be employed.

Figure 20 shows a heater protection circuit which responds quickly enough to prevent damage from most overloads. C1's input is connected to the output of the LT1088 servo circuit. If the LT1088 circuit's output exceeds the threshold at C1's other input, C1 trips, discharging the $2\mu\text{F}$ capacitor. This causes C2's output to go low, energizing the relay and breaking the heater circuit. The 560k resistor provides a long recharge for the capacitor, preventing "chattering" action. This arrangement's speed of response is limited by the RMS circuit's slew rate, about 0.2V/ms. For reasonable overloads, the LT1088's temperature increases about $1^\circ\text{C}/\text{ms}$. A 10V LT1088 output step takes 50ms, causing a temperature rise of about 50°C .

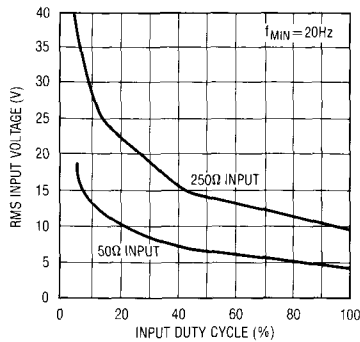


Figure 19. LT1088 Safe Operating Limits

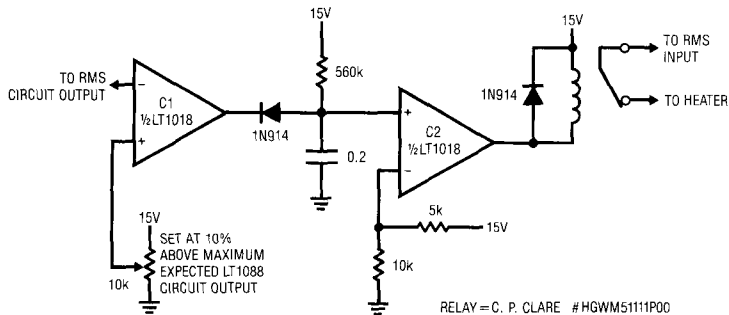


Figure 20. Servo-Sensed Heater Protection Circuit

Severe overloads will cause faster heating, and this circuit may not act quickly enough to prevent damage. Figure 21's circuit is faster, but requires a trim. It works by directly sensing the temperature of the LT1088, instead of the servo amplifier output. Circuit action is similar to Figure 20, except that the input is taken from the LT1088's input temperature sensing diode. Figure 22 shows waveforms. Excessive drive to the LT1088 (Trace A, Figure 22) forces the servo amplifier (Trace B) into slew. The sensing diode, responding more quickly than the servo, causes the circuit to switch the relay (Trace C), removing heater drive in 15ms. Because loop response lags temperature, the servo amplifier's output peaks at only 6V, about one-third of the input step. This circuit has the disadvantage of requiring a trim, due to initial diode tolerances. To trim, measure diode output at 25°C and set

C1's negative input to the desired temperature cut-off point. Assume a diode slope of 1.8mV/°C.

Some applications may require buffering the LT1088's relatively low input impedance. This is not easy if the device's wide bandwidth and accuracy must be preserved. With an LT1010 buffer, bandwidths in the low megahertz region are achievable. Figure 23's circuit, a FET input, complementary emitter follower output design, extends bandwidth out to 25MHz. If gain is desired, Figure 24 furnishes low megahertz performance at a gain of ten. Figure 25's design, although complex, has 32MHz bandwidth at a gain of ten. Detailed discussion of Figures 24 and 25 appears in Application Note 21, "Composite Amplifiers." Figure 26's table summarizes performance of the buffer amplifiers.

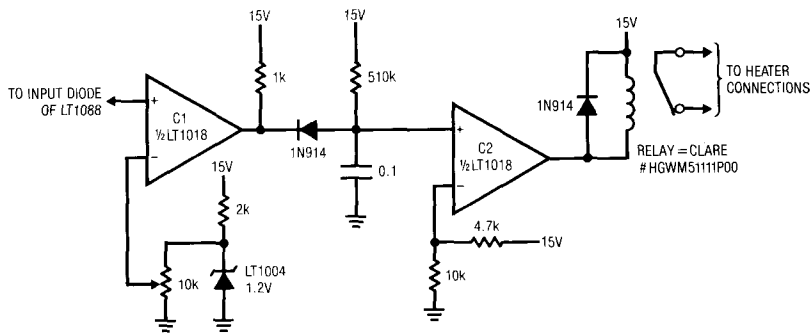


Figure 21. Diode Sensed Heater Protection Circuit

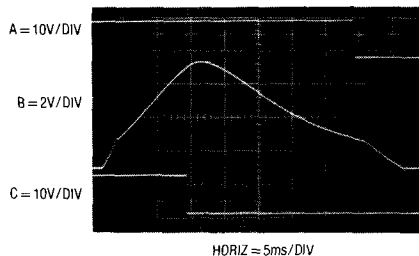


Figure 22. Response of Diode Sensed Heater Protection Circuit

Application Note 22

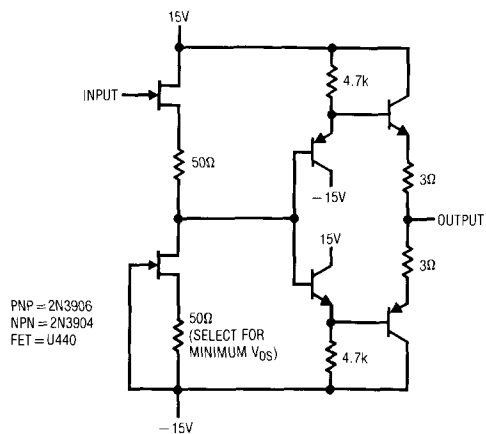


Figure 23. Input Buffer for the LT1088

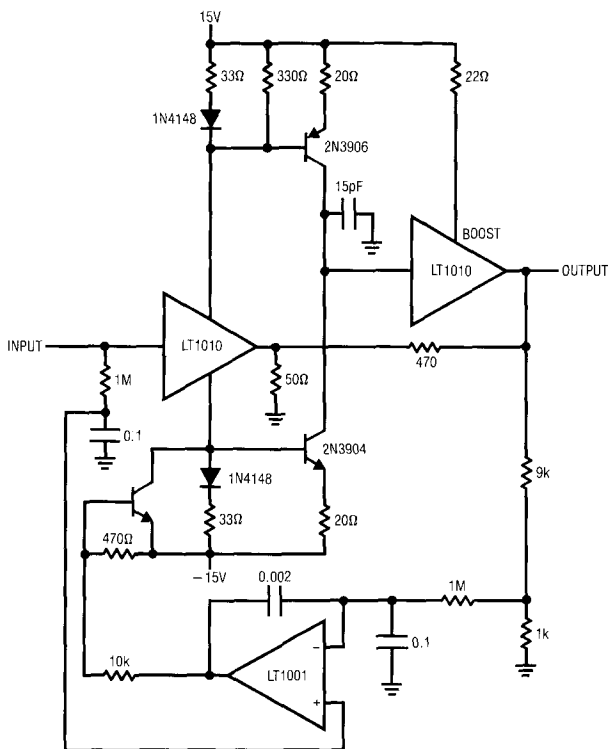


Figure 24. Fast, "Current Mode" Amplifier-Buffer

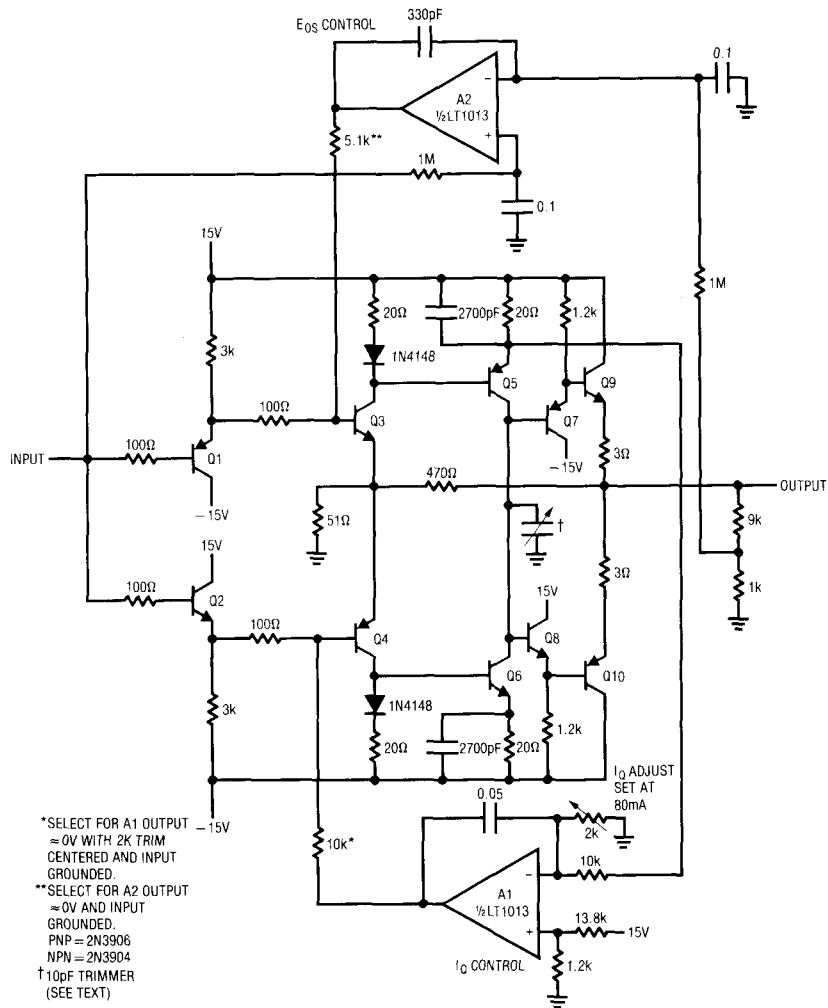


Figure 25. Ultra-Wideband "Current Mode Feedback" Buffer Amplifier

Type of Buffer	Slew Rate	1% Error Bandwidth	
		250Ω Load (±10V _{OUT})	50Ω Load (±5V _{OUT})
Discrete—A = 10	3000V/μs	25MHz	32MHz
LT1010 Based—A = 10	100V/μs	0.75MHz	2MHz
Discrete—A = 1	2000V/μs	15MHz	25MHz
LT1010 Based—A = 1	100V/μs	0.75MHz	2MHz

Figure 26. Summary of Buffer Characteristics

Application Note 22

Applications for the LT1088's wideband capability exist in AC voltmeters, SCR power monitoring, wideband AGC, noise measurement and RF leveling loops. Figure 27 shows a 10MHz RF leveling loop. The RF input is applied to the AD539 wideband multiplier. The multiplier's output drives an RF amplifier. The discrete transistors furnish gain with the LT1010 serving as an output buffer. The LT1012 DC stabilizes the stage (for operating details of this circuit, see Application Note 21). The RF amplifier's output is converted to DC by the LT1088 based RMS-DC converter. A servo amplifier compares this output with a

settable DC reference and biases the multiplier's control channel, completing a loop. The $0.33\mu\text{F}$ capacitor provides frequency compensation by rolling off gain at a frequency well below the response of the LT1088 servo. The loop maintains the output's 10MHz RMS amplitude at the DC reference's value. Changes in load, input, power supply and other variables are rejected. Figure 28 shows loop response for a step test signal injected at the servo amplifier's positive input (Trace A). Response (Trace B) is clean, with settling occurring in about a second.

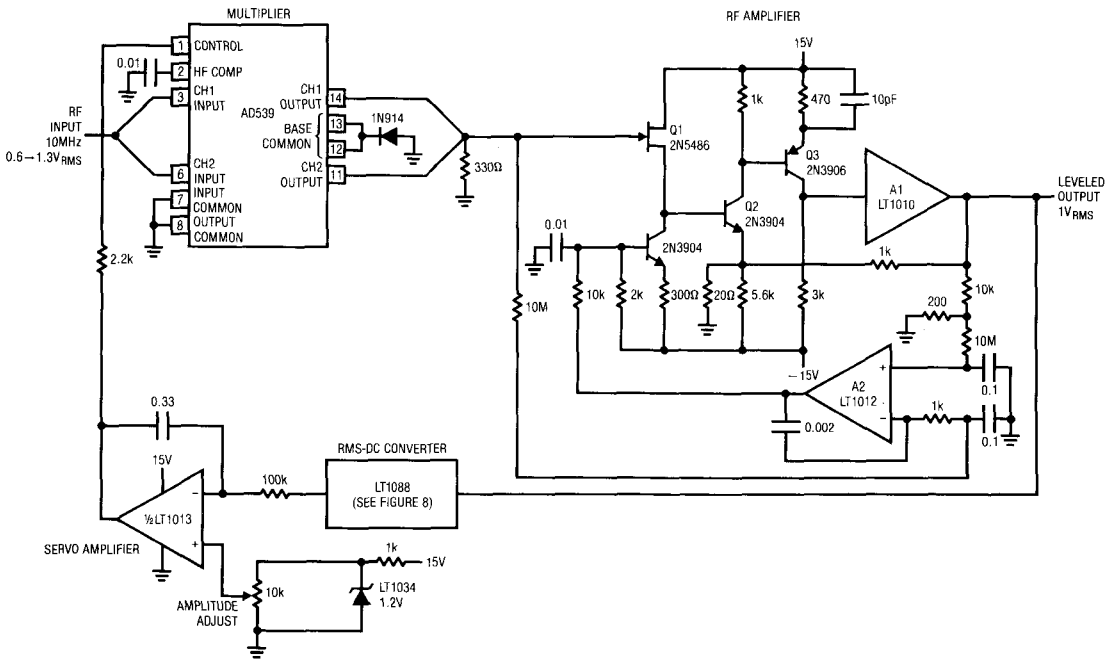


Figure 27. RF Leveling Loop

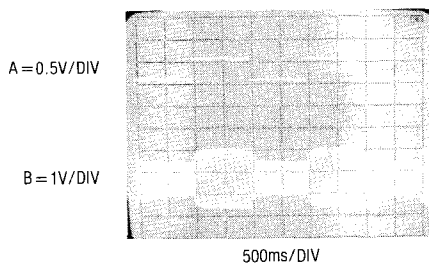


Figure 28. RF Leveling Loop Response

BOX SECTION

Measuring Thermal Resistance

Establishing, maintaining and verifying proper thermal resistance between the LT1088 and ambient is extremely important to its operation. Because thermal resistance is a gain term, it must be constant with time, cycling and power level. Additionally, it must fall within limits. Low thermal resistance results in poor sensitivity to downscale inputs, limiting dynamic range. Too high a thermal resistance causes excessive die heating, leading to failure.

Thermal crosstalk, the heat conduction between the two die, must be minimized. Such thermal conduction between die lowers available gain, degrading performance for small inputs.

Ensuring proper thermal resistance for both cases requires an accurate measurement technique. Figure B1 shows a circuit which reliably measures thermal resistance. It works by supplying constant wattage to the LT1088 heater, regardless of its resistance. Because heater resistance moves with die temperature, the circuit must continually control the $E \times I$ product supplied to the heater. It does this by measuring heater current and forcing voltage to keep the $E \times I$ product at a constant, calibrated value. The resultant die temperature rise, picked up

by the diode sensor, allows thermal resistance to be determined. A1, measuring heater current across the 1Ω shunt, feeds the Y input of an analog multiplier. The voltage across the heater is differentially sensed at the multiplier's X input. The multiplier's $E \times I$ product output is compared to a scaled, adjustable reference at A2. A2's output biases Q1, closing a loop around the heater. The $0.22\mu\text{F}$ capacitor stabilizes the loop. To trim this circuit, put a 50Ω , 1W resistor in place of the LT1088 heater. Next, adjust the 2k potentiometer so the measured heater wattage (E across heater times I through the 1Ω shunt) corresponds to the voltage at the potentiometer wiper. Scale factor will be 10V/W . Disconnect the 50Ω resistor and the circuit is ready for use.

To measure thermal resistance, adjust the wattage control for 350mW , place the switch in the "25°C" position and read the diode potential. Then, switch to "hot" and read the diode voltage when it has settled. Assuming $1.8\text{mV}/^\circ\text{C}$, calculate the thermal resistance in $^\circ\text{C/W}$. Thermal crosstalk is measured the same way, except that the sensing diode and heater are not on the same die.

Application Note 22

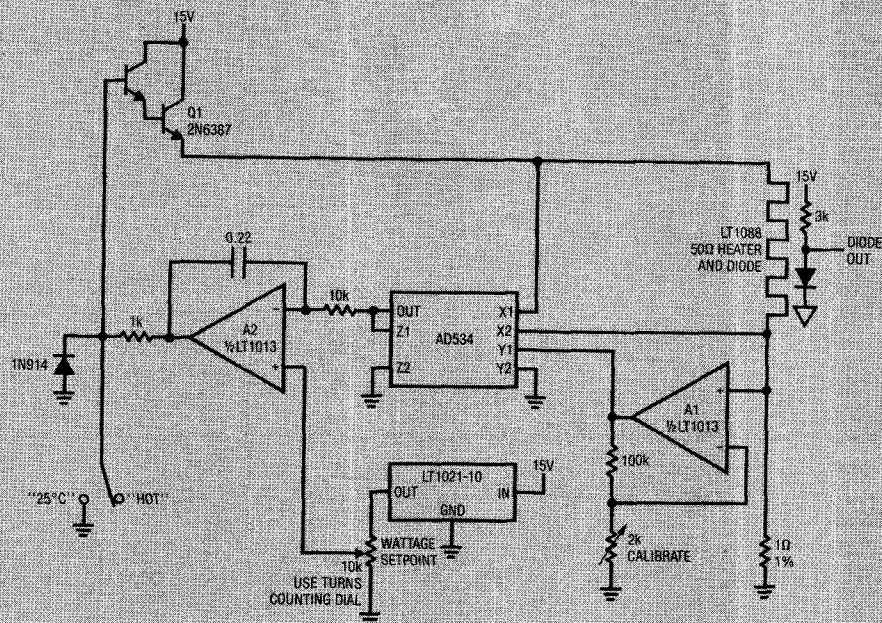


Figure B1. Adjustable Wattage Source

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6. RMS to DC Conversion Application Guide, Analog Devices, Norwood, Massachusetts.
7. Williams, J., "50MHz Thermal RMS-DC Converter." Linear Technology Corporation, Application Note 5.

Micropower Circuits for Signal Conditioning

Jim Williams

Low power operation of electronic apparatus has become increasingly desirable. Medical, remote data acquisition, power monitoring and other applications are good candidates for battery driven, low power operation. Micropower analog circuits for transducer based signal conditioning present a special class of problems. Although micropower ICs are available, the interconnection of these devices to form a functioning micropower circuit requires care. (See Box Sections, "Some Guidelines for Micropower Design and an Example" and "Parasitic Effects of Test Equipment on Micropower Circuits.") In particular, trade-offs between signal levels and power dissipation become painful when performance in the 10 to 12-bit area is desirable. Additionally, many transducers and analog signals produce in-

herently small outputs, making micropower requirements complicate an already difficult situation. Despite the problems, design of such circuits is possible by combining high performance micropower ICs with appropriate circuit techniques.

Platinum RTD Signal Conditioner

Figure 1 shows a simple circuit for signal conditioning a platinum RTD. Correction for the platinum sensor's non-linear response is included. Accuracy is 0.25°C over a 2°C – 400°C sensed range. One side of the sensor is grounded, highly desirable for noise considerations. For a 2°C sensed temperature, current consumption is $250\mu\text{A}$, increasing to $335\mu\text{A}$ for a 400°C sensed temperature.

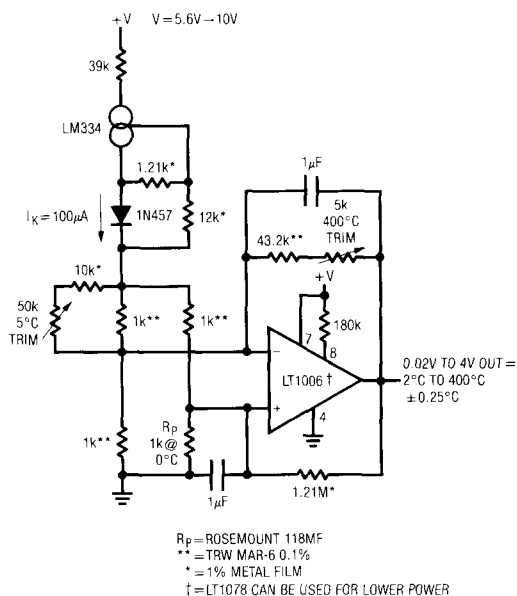


Figure 1. Platinum RTD Signal Conditioner with Curvature Correction

Application Note 23

The platinum sensor is placed in a current driven bridge with the 1k resistors. The LM334 current source drives the bridge and its associated resistors set a $100\mu\text{A}$ operating level. The diode provides temperature compensation (see LM334 datasheet). The 39k resistor deliberately sustains voltage drop, minimizing LM334 die temperature rise to ensure good temperature tracking with the diode. The $100\mu\text{A}$ current is split by the bridge. This light current saves power, but restricts the platinum sensor's output to about $200\mu\text{V}/^\circ\text{C}$. The circuit's 0.25°C accuracy specification requires the LT1006 low power precision op amp for stable gain. The LT1006 takes the signal differentially from the bridge to provide the circuit's output. Normally, the platinum sensor's slightly non-linear response would cause several degrees error over the sensed temperature range. The 1.2M resistor gives slight positive feedback to correct for this. The amplifier's negative feedback path dominates, and the configuration is stable. The $1\mu\text{F}$ capacitors give a high frequency roll-off and the 180k resistor programs the LT1006 for $80\mu\text{A}$ quiescent current.

To calibrate this circuit, substitute a precision decade box (e.g., General Radio 1432) for R_p . Set the box to the 5°C value (1019.9Ω) and adjust the "5°C trim" for 0.05V output at the LT1006. Next, set the box for the 400°C value (2499.8Ω) and adjust the "400°C trim" for 4.000V output. Repeat this sequence until both points are fixed. The resistance values given are for a nominal 1000.0Ω (0°C) sensor. Sensors deviating from this nominal value can be used by factoring in the deviation from 1000.0Ω . This deviation, which is manufacturer-specified for each individual sensor, is an offset term due to winding tolerances during fabrication of the RTD. The gain slope of the platinum is primarily fixed by the purity of the material and is a very small error term.

Thermocouple Signal Conditioner

Figure 2 is another temperature sensing circuit, except the transducer is a thermocouple. Accuracy is within 1.5°C over a 0°C – 60°C sensed temperature and current consumption is about $125\mu\text{A}$.

Thermocouples are inexpensive, have low impedances and feature self-generating outputs. They also produce low level outputs and require cold junction compensation, complicating signal conditioning. The bridge network, composed of the thermistor and R1-R4, provides cold junction compensation with the LT1004 acting as a voltage reference. The lithium battery noted allows the bridge to float and the thermocouple to be ground referred, eliminating the requirement for a differential amplifier. For the battery specified, life will approach 10 years. This is a good way to avoid the additional power drain of a multi-amplifier differential stage. The LT1006 is set up with a gain scaled to produce the output shown and the 270k resistor programs it for low current drain. Note that this circuit requires no trims.

Sampled Strain Gauge Signal Conditioner

Strain gauge bridge based transducers present a challenge where low power operation is needed. The 350Ω impedance combined with low signal outputs (typically 1–3mV output per volt of drive) presents problems. Even with only 1V of drive, bridge consumption still approaches 3mA. Dropping drive to 100mV reduces current to acceptable levels, but precludes high accuracy operation due to the minuscule output available. In many situations, continuous transducer information is unnecessary and sampled operation is viable. Short sampling duty cycle

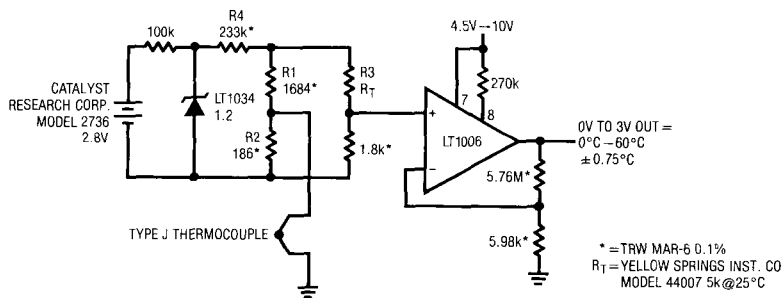


Figure 2. Thermocouple Signal Conditioner with Cold Junction Compensation

permits high current bridge drive while maintaining low power operation. Figure 3 uses such a scheme to achieve dramatic power saving in a strain gauge application (for a discussion of sampled operation considerations, see Box Section B, "Sampling Techniques and Components for Micropower Circuits").

In this circuit, Q2 is off when the "sample command" is low. Under these conditions only A4 and the CD4016 receive power, and current drain is inside $125\mu\text{A}$. When the sample command is pulsed high, Q2's collector (trace A, Figure 4) goes high, providing power to all other circuit elements. The 10Ω - $1\mu\text{F}$ RC at the LT1021 prevents the strain

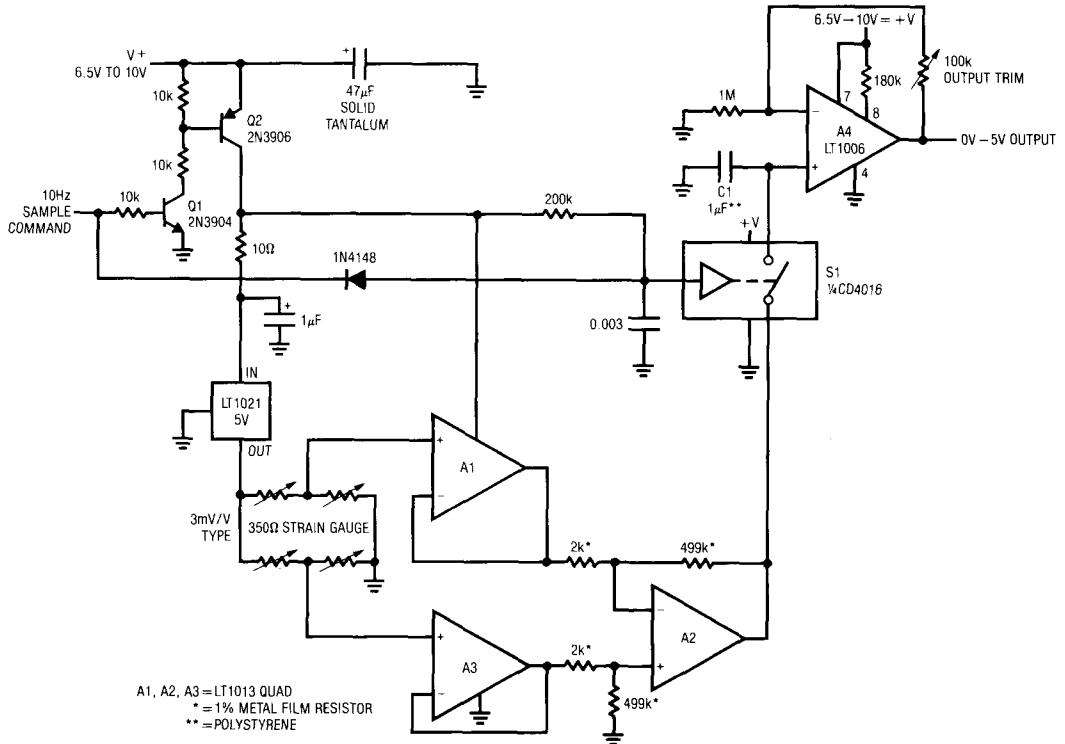


Figure 3. Sampled Strain Gauge Bridge Signal Conditioner

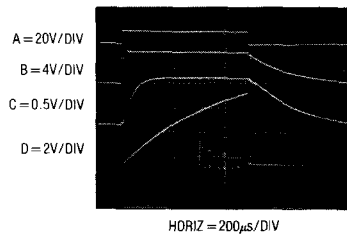


Figure 4. Waveforms for the Sampled Strain Gauge Signal Conditioner

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bridge from seeing a fast rise pulse which could cause long term transducer degradation. The LT1021-5 reference output (trace B) drives the strain bridge, and differential amplifier A1-A3's output appears at A2 (trace C). Simultaneously, S1's switch control input (trace D) ramps toward Q2's collector. At about one-half Q2's collector voltage (in this case just before mid-screen) S1 turns on, and A2's output is stored in C1. When the sample command drops low, Q2's collector falls, the bridge and its associated circuitry shut down and S1 goes off. C1's stored value appears at gain scaled A4's output. The RC delay at S1's control input ensures glitch free operation by preventing C1 from updating until A2 has settled. During the 1ms sampling phase, supply current approaches 20mA, but a 10Hz sampling rate cuts effective drain below 200μA. Slower sampling rates will further reduce drain, but C1's droop rate (about 1mV/100ms) sets an accuracy constraint. The 10Hz rate provides adequate bandwidth for most transducers. For 3mV/V slope factor transducers, the gain trim shown allows calibration. It should be rescaled for other types. This circuit's effective current drain is about 300μA, and A4's output is accurate enough for 12-bit systems.

Strobed Operation Strain Gauge Bridge Signal Conditioner

Figure 5's circuit also switches power to minimize strain bridge caused losses, but is not intended for continuously sampled operation. This circuit is designed to sit in the quiescent state for long periods with relatively brief on-times. A typical application would be remote weight information in storage tanks where weekly readings are sufficient. This circuit has the advantage of not requiring a differential amplifier, despite the strain bridge's floating output. Additionally, it provides almost full rated drive to the strain bridge, enhancing accuracy. Quiescent current is about 150μA with on-state current typically 50mA.

With Q1's base unbiased, all circuitry is off except the LT1054 plus-to-minus voltage converter, which draws a 150μA quiescent current. When Q1's base is pulled low, its collector supplies power to A1 and A2. A1's output goes high, turning on the LT1054. The LT1054's output (pin 5) heads toward -5V and Q2 comes on, permitting bridge current to flow. To balance its inputs, A1 servo controls the LT1054 to force the bridge's midpoint to 0V. The bridge

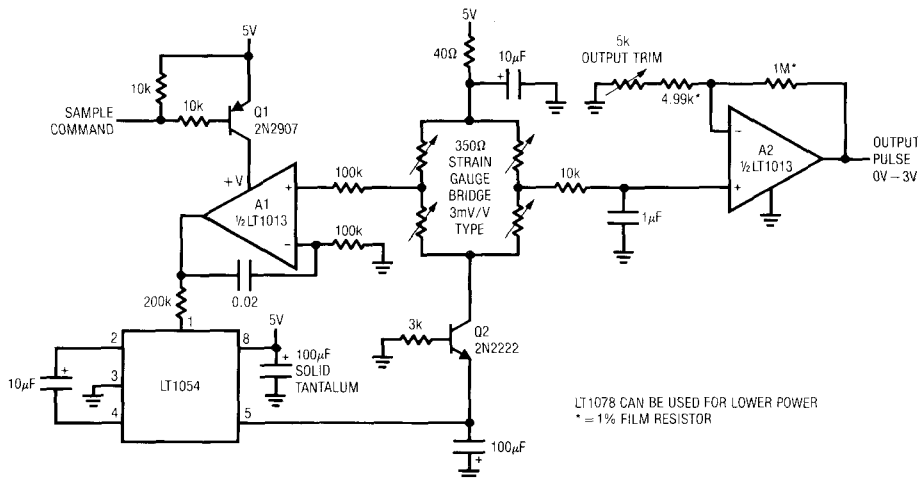


Figure 5. Strobed Power Strain Bridge Signal Conditioner

ends up with about 8V across it, requiring the 100mA capability LT1054 to sink about 24mA. The 0.02 μ F capacitor stabilizes the loop. The A1-LT1054 loop negative output sets the bridge's common-mode voltage to zero, allowing A2 to take a simple single ended measurement. The "output trim" scales the circuit for 3mV/V type strain bridge transducers, and the 100k-0.1 μ F combination provides noise filtering.

Thermistor Signal Conditioner for Current Loop Application

4-20mA "current loop" control is common in industrial environments. Circuitry used to modulate transducer data into this loop must operate well below the 4mA minimum current.

Figure 6 shows a complete 2-wire thermistor temperature transducer interface with a 4-20mA output. Over a 0°C-100°C range, accuracy is $\pm 0.3^\circ\text{C}$ and the circuit is current loop powered. No external supply is required. The

LM134 current source absorbs the 40V input, preventing the LTC1040 from seeing too high a supply potential. It does this by fixing the current well below the 4mA loop minimum. The LTC1040 (detailed data on this device appears in Box Section B, "Sampling Techniques and Components for Micropower Circuits") senses the YSI thermistor network output and forces this voltage across the output resistor to set total circuit current. Current is adjusted by varying the gate voltage on the 2N6657 FET. Note that the comparator output operates in pulse-width-modulation mode, with the FET gate voltage filtered to DC by the 1M-1 μ F combination. An important LTC1040 feature is that very little current, on the order of nanoamperes, flows from the V⁻ supply. This allows the V⁻ supply to be connected to ground with negligible current error in the output sensing resistor. The differential input of the LTC1040 can sense the current through R_{OUT} because its common-mode range includes the V⁻ supply. Trims shown are for 0°C and 100°C and are made by exposing the thermistor to those temperatures or by electrically simulating the conditions (see manufacturer's datasheet).

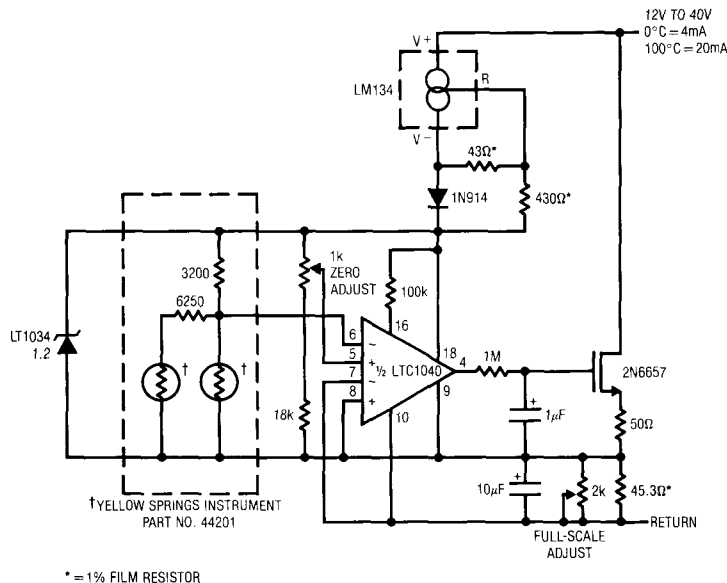


Figure 6. Thermistor Based Current Loop Signal Conditioner

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Microampere Drain Wall Thermostat

Figure 7 shows a battery powered thermostat using the LTC1041 (See Box Section B for details on this device). Temperature is sensed using a thermistor connected in a bridge with a potentiometer to set the desired temperature.

The bridge is not driven from the battery but from pin 7 on the LTC1041. Pin 7 is the pulsed power (V_{PP}) output and turns on only while the LTC1041 is sampling the inputs. With this pulse technique, average system power consumption is quite small. In this application the total system current is below $1\mu\text{A}$! This is far less than the self discharge rate of the battery, meaning battery life is shelf life limited. A lithium battery will run this circuit for 10 to 20 years.

An external RC network sets the sampling frequency. When an internal sampling cycle is initiated, power is turned on to the comparators and to the V_{PP} output. The analog inputs are sampled and the resultant outputs are stored in CMOS latches. Power is then switched off although the outputs are maintained. The unlocked CMOS logic consumes almost no DC current. The sampling process takes approximately $80\mu\text{s}$. During this $80\mu\text{s}$ interval, the LTC1041 draws typically 1.7mA of current at $V^+ = 6\text{V}$. Because the sample rate is low, average power is extremely small.

The low sample rate is adequate for a thermostat because of the low rate of change normally associated with temperature.

A power MOSFET in a diode bridge switches 26VAC to the heater control circuitry. The MOSFET is a voltage controlled device with no DC current required from the battery.

The voltage from DELTA (pin 5) to GND (pin 4) sets the dead-band. Dead-band is desirable to prevent excessive heater cycling. The dead-band equals two times DELTA and is independent of both V_{IN} (pin 3) and SET POINT (pin 2). This means that as the SET POINT is varied the dead-band is fixed at two times DELTA. Conversely as dead-band is varied, SET POINT does not move.

Freezer Alarm

Figure 8 shows a very simple configuration for a freezer alarm. Such circuits are used in industrial and home freezers as well as refrigerated trucks and rail cars. The LTC1042 is a sampled operation window comparator (for details on this device see Box Section B). The $10\text{M}-0.05\mu\text{F}$ combination sets a sample rate of 1Hz , and the bridge values program the internal window comparator for the outputs shown. For normal freezer operation, pin 1 is high and pin 6 is low. Over-temperature reverses this state and can trigger an alarm. Circuit current consumption is about $80\mu\text{A}$.

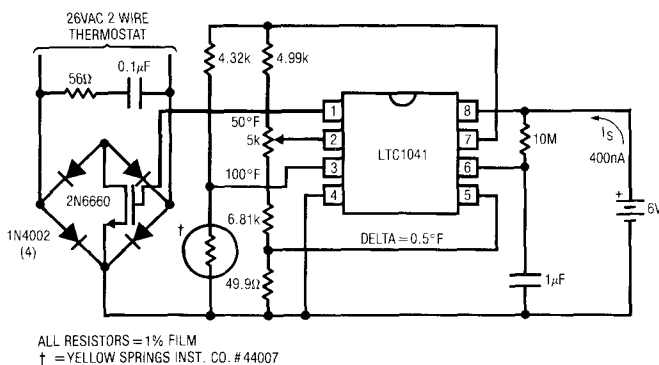


Figure 7. Wall Type Thermostat

12-Bit A-D Converter

Integrating A-D converters with low power consumption are available. Although capable of 12-bit measurements, they are quite slow, typically in the 100ms range. Higher speeds require a successive approximation (SAR) ap-

proach. No commercially produced 12-bit SAR converter features micropower (e.g., below 1mA) capability at the time of writing. Figure 9's design converts in 300 μ s, while consuming only 890 μ A.

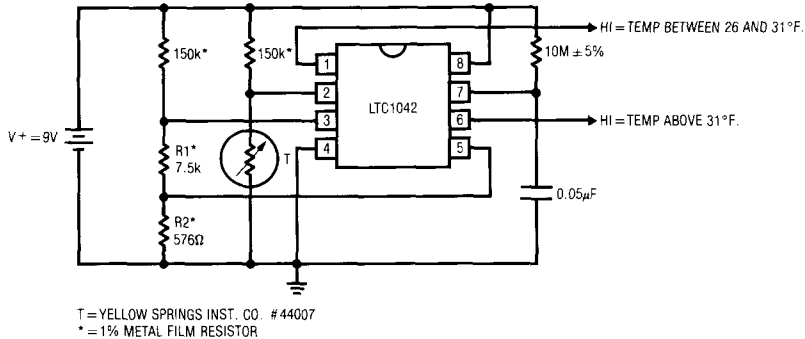


Figure 8. Freezer Alarm

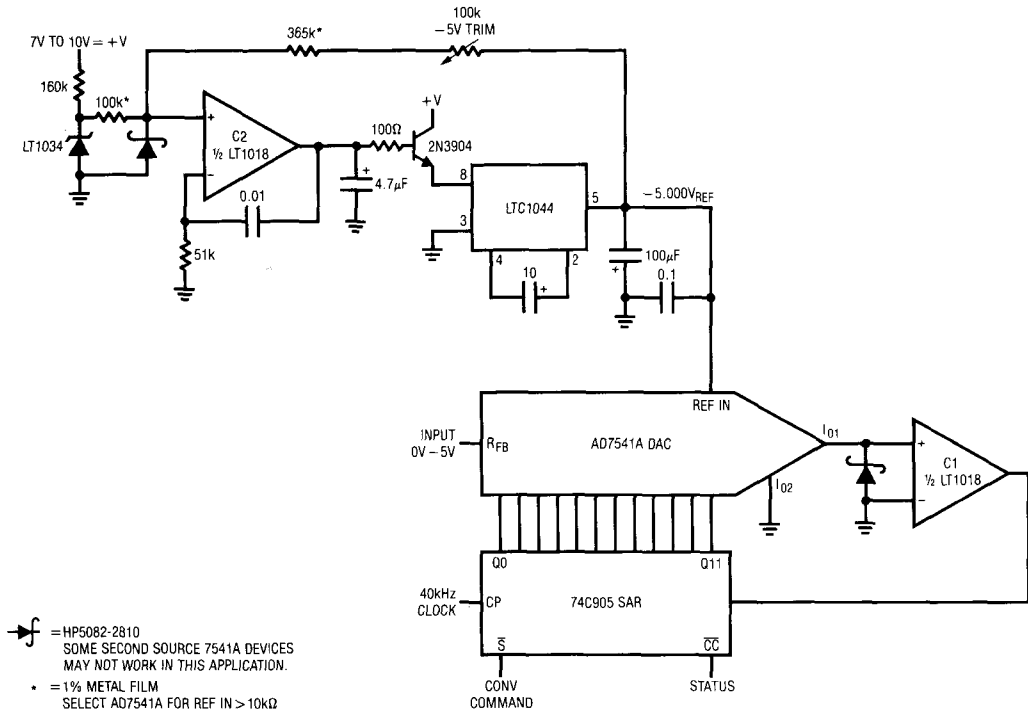


Figure 9. Micropower 12-Bit, 300 μ s A-D

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Conceptually, this design is a straightforward SAR type converter, although some special measures are needed to achieve low power operation. The SAR chip and the DAC are arranged in the standard fashion, with C1 closing a loop. Normally, CMOS DACs are not used for SAR applications because their output capacitance slows operation. In this case, the CMOS DAC's low power consumption is attractive and speed is traded away. This is not too great a penalty, because micropower comparator C1 is a good speed match for the DAC specified. A limitation with CMOS DACs is that their outputs must terminate into 0V. This mandates a current summing comparison, meaning the reference must be of opposite polarity to the input. Since most micropower systems run from single sided positive rails, it is unrealistic to expect the user to supply the A-D with a negative input. To be readily usable, the converter should accept positive inputs and derive a negative reference internally. This issue is addressed by C2 and the LTC1044 plus-to-minus voltage converter, which form a negative reference.

C2, compensated as an op amp, servo controls the LTC1044 via the boost transistor. The LTC1044's negative output is fed back to C2's input, closing a regulation loop. Scaled current summing from the output and the LT1034 forces a 5.000V output. The Schottky diode prevents possible summing point negative overdrive during start-up. The choice of 5V for a reference maintains reasonable LSB overdrive for C1, but accounts for over half the circuit's current requirement. This limitation is set by the DAC's relatively low input impedance. Dropping the reference voltage would save significant power, but would also reduce LSB size below a millivolt. This would cause comparator offset and gain to become significant error sources.

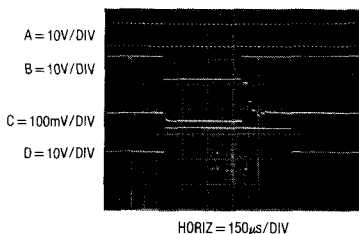


Figure 10. Micropower SAR A-D Waveforms

Although the DAC has no negative supply, it can accept the negative reference because its thin film resistors are not intrinsic to the monolithic structure. Ground referred C1 cannot accept any negative voltages, however, and is Schottky clamped.

Performance includes a typical tempco of 30ppm/°C, 300µs conversion time, 890µA current consumption and an accuracy of ± 2 LSBs. Trimming involves adjusting the 100k potentiometer for exactly -5V at V_{REF} . The DAC's internal feedback resistor serves as the input. Figure 10 shows operating waveforms. Trace A is the clock. Trace B is the convert command. The SAR is cleared on trace B's falling edge and conversion commences on the rise. During conversion, C1's input (trace C) sequentially converges towards zero. When conversion is complete, the status line (trace D) drops low.

10-Bit, 100µA A-D Converter

Figure 11's A-D has less resolution than the previous circuit, but requires only 100µA. The design consists of a current source, an integrating capacitor, a comparator and some logic elements. When a pulse is applied to the convert command input (trace A, Figure 12), the paralleled 74C906 sections reset the 0.075µF capacitor to zero (trace B). Simultaneously, 74C14 inverter A goes low, biasing the 2N3809 current source on. During this interval the current source stabilizes, delivering its output to ground via the paralleled 74C906 sections. On the falling edge of the convert command pulse the 0.075µF capacitor begins to charge linearly. When the ramp voltage equals the input, C1 switches. Inverter A goes high, shutting off the current source. A small current is bled through the 10M-diode connection to keep the ramp charging, but at a greatly reduced rate. This insures overdrive for C1, but minimizes

current source on-time, saving power. C1's output, a pulse (trace C) width, is directly dependent on the value of E_x . This pulse width gates C2's clock output via the 74C00 configuration. The 74C00's also gate out the portion of C1's output due to the convert command pulse. Thus, the clock pulse bursts appearing at the output (trace D) are proportional to E_x . For the arrangement shown, 1024 pulses appear for a 5V full-scale input. The current source scaling resistor and ramp capacitor specified provide good temperature compensation because of their opposing thermal coefficients. The circuit will typically hold ± 1 LSB accuracy over 0°C – 70°C with an additional ± 1 LSB due to the asynchronous relationship between the clock and the conversion sequence. If the conversion sequence is synchronized to the clock, the ± 1 LSB asynchronous limitation is removed, and total error falls to ± 1 LSB over 0°C – 70°C . The flip-flop shown in dashed lines permits such synchronization. Conversion rate varies

with input. At tenth scale 150Hz is possible, decreasing to 20Hz at full-scale.

Power consumption of the A–D is extremely low, due to the CMOS logic elements and the LT1017 comparator. Quiescent ($E_{IN} = 0\text{V}$) current is $100\mu\text{A}$ at $V_{SUPPLY} = 9\text{V}$, decreasing to $80\mu\text{A}$ for $V_{SUPPLY} = 7\text{V}$. Because current source on-time varies with input, power consumption also varies. For $E_{IN} = 5\text{V}$, current consumption rises to $125\mu\text{A}$ for $E_{SUPPLY} = 9\text{V}$ and $105\mu\text{A}$ at $E_{SUPPLY} = 7\text{V}$. Additional power savings are possible by shutting off the current source during capacitor reset, but accuracy suffers due to current source settling time requirements. The $0.075\mu\text{F}$ capacitor's accumulated charge is thrown away at each reset. A smaller capacitor would help, but C1's bias currents would introduce significant error.

Turning off the current source after C1 switches saves significant power. Figure 13, taken at a 25mV input, shows

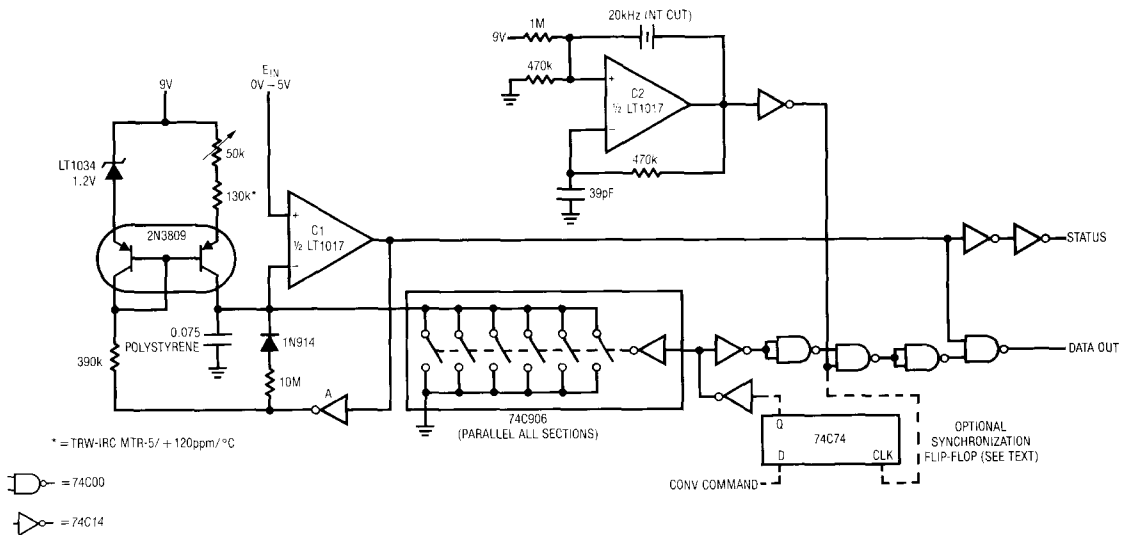


Figure 11. 10-Bit, 100 μA A–D

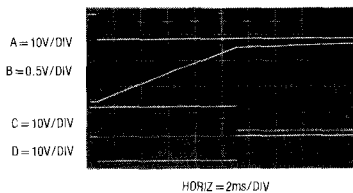


Figure 12. Waveforms for the 100 μA A–D

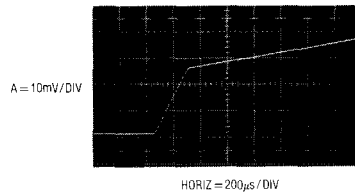


Figure 13. Detail of the Switched Slope Capacitor Charging

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the ramp zero reset and the clean switching. When the current source switches off, the ramp slope decreases but continues to move upward, insuring overdrive. The 10M-diode pair provides the charge, but less than a microampere is lost.

20µs Sample-Hold

Figure 14 is a companion sample-hold for the SAR A-D. Acquisition time is 20µs, with low power operation (see Figure 14 table). This circuit takes full advantage of the programming pin on the LT1006 op amp to maximize speed-power performance. When the sample command (trace A, Figure 15) is given, the CD4066 switches close. S1 and S2 allow A1's output (trace B) to charge the capacitor (trace C is capacitor current). Simultaneously S3 and S4 close, raising the op amp's internal bias network. This

puts both amplifiers into hyperdrive, boosting slew rate to speed acquisition time. A2 (trace D) is seen to settle cleanly to 1mV in 20µs. When the sample command goes low, all switches go off, A2 follows the voltage stored on the capacitor, and supply current drops by a factor of five (see Figure 14 table). In normal operation, sample time is short compared to hold and current consumption is low. The 360k resistors set the circuit's hold mode quiescent current at the value noted in the table.

10kHz Voltage-to-Frequency Converter

Figure 16, another data converter, is a voltage-to-frequency converter. A 0V-5V input produces a 0kHz-10kHz output, with a linearity of 0.02%. Gain drift is 40ppm/°C. Maximum current consumption is only 145µA, far below currently available units.

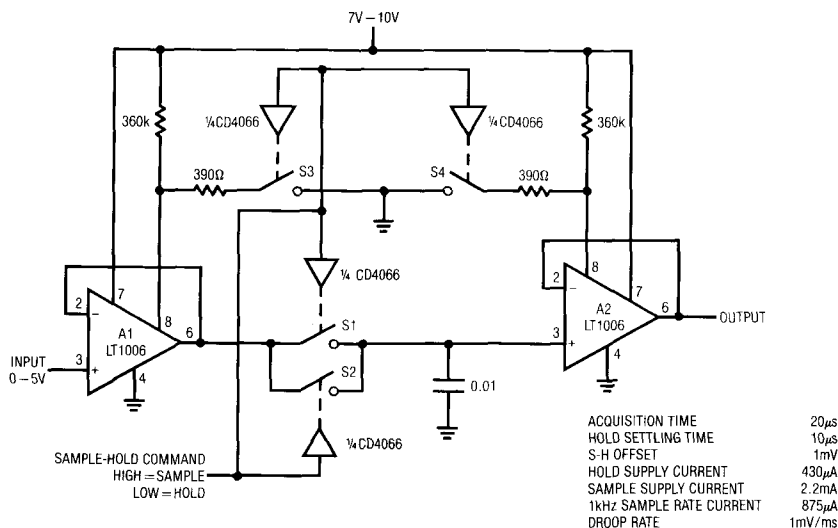


Figure 14. Micropower Sample-Hold

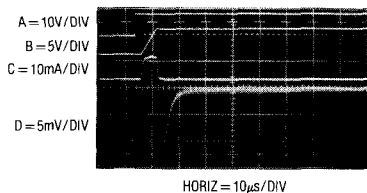


Figure 15. Figure 14's Waveforms

The evolution of this circuit is described in Box Section A, "Some Guidelines for Micropower Design and an Example". To understand circuit operation, assume C1's positive input is slightly below its negative input (C2's output is low). The input voltage causes a positive going ramp at C1's positive input (trace A, Figure 17). C1's output is low, biasing the CMOS inverter outputs high. This allows current to flow from Q1's emitter, through the inverter supply pin to the 0.001 μ F capacitor. The 10 μ F capacitor provides high frequency bypass, maintaining low impedance at Q1's emitter. Diode connected Q6 provides a path to ground. The voltage to which the 0.001 μ F unit charges is a

function of Q1's emitter potential and Q6's drop. When the ramp at C1's positive input goes high enough, C1's output goes high (trace B) and the inverters switch low (trace C). The Schottky clamp prevents CMOS inverter input overdrive. This action pulls current from C1's positive input capacitor via the Q5-0.001 μ F route (trace D). This current removal resets C1's positive input ramp to a potential slightly below ground, forcing C1's output to go low. The 50pF capacitor connected to the circuit output furnishes AC positive feedback, ensuring that C1's output remains positive long enough for a complete discharge of the 0.001 μ F capacitor. The Schottky diode prevents C1's input

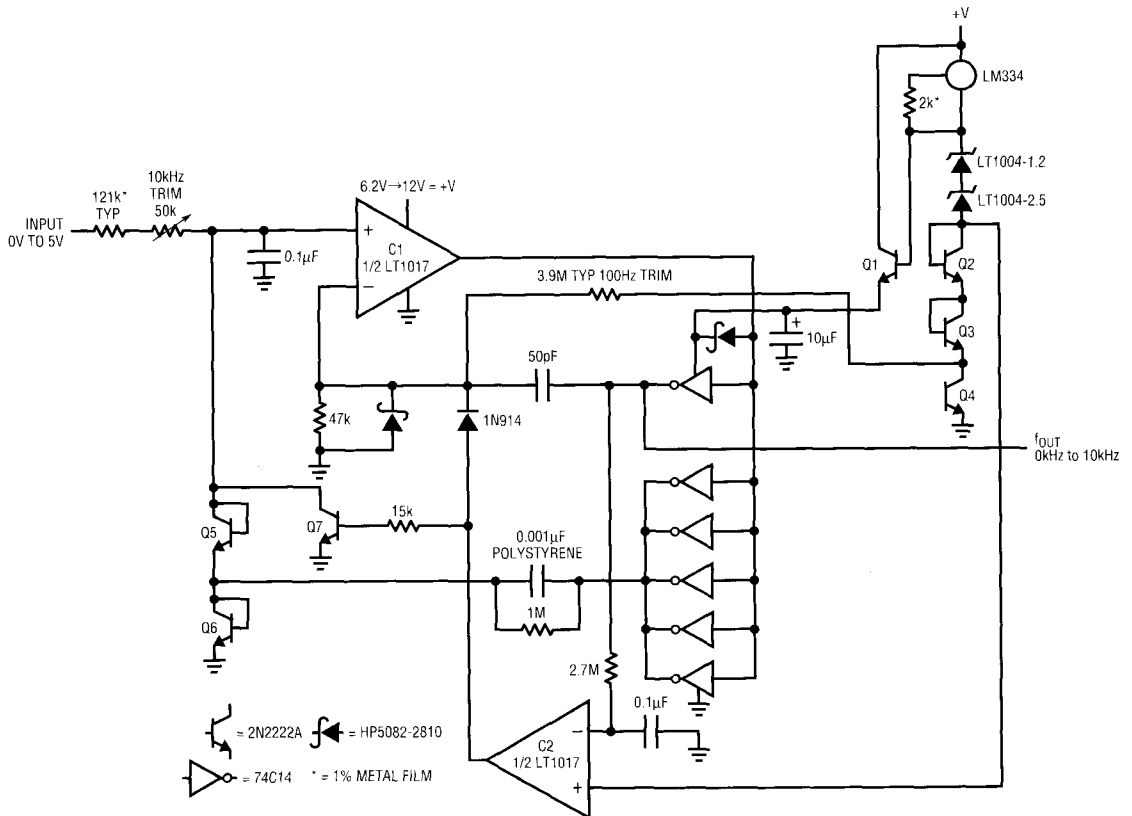


Figure 16. Micropower 10kHz V-F Converter

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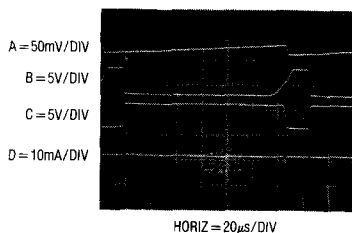


Figure 17. Figure 16's Waveforms

from being driven outside its negative common-mode limit. When the 50pF unit's feedback decays, C1 again switches low and the entire cycle repeats. The oscillation frequency depends directly on the input voltage derived current.

Q1's emitter voltage must be carefully controlled to get low drift. Q3 and Q4 temperature compensate Q5 and Q6 while Q2 compensates Q1's V_{BE} . The two LT1004s are the actual voltage reference and the LM334 current source provides 35µA bias to the stack. The current drive provides excellent supply immunity (better than 40ppm/V) and also aids circuit temperature coefficient. It does this by utilizing the LM334's 0.3%/°C tempco to slightly temperature modulate the voltage drop in the Q2-Q4 trio. This correction's sign and magnitude directly oppose that of the -120ppm/°C 0.001µF polystyrene capacitor, aiding overall circuit stability.

The Q1 emitter-follower delivers charge to the 0.001µF capacitor efficiently. Both base and collector current end up in the capacitor. The paralleled CMOS inverters provide low loss SPDT reference switching without significant drive losses. The 0.001µF capacitor, as small as accuracy

permits, draws only small transient currents during its charge and discharge cycles. The 50pF-47k positive feedback combination draws insignificantly small switching currents. Figure 18, a plot of supply current vs. operating frequency, reflects the low power design. At zero frequency, the LT1017's quiescent current and the 35µA reference stack bias accounts for all current drain. There are no other paths for loss. As frequency scales up, the charge-discharge cycle of the 0.001µF capacitor introduces the 7µA/kHz increase shown. A smaller value capacitor would cut power, but the effects of stray capacitance, charge imbalance in the 74C14, and LT1017 bias currents would introduce accuracy errors.

Circuit startup or overdrive can cause the circuit's AC-coupled feedback to latch. If this occurs, C1's output goes high. C2, detecting this via the inverters and the 2.7M-0.1µF lag, also goes high. This lifts C1's negative input and grounds the positive input with Q7, initiating normal circuit action.

Because the charge pump is directly coupled to C1's output, response is fast. Figure 19 shows the output (trace B) settling within one cycle for a fast input step (trace A).

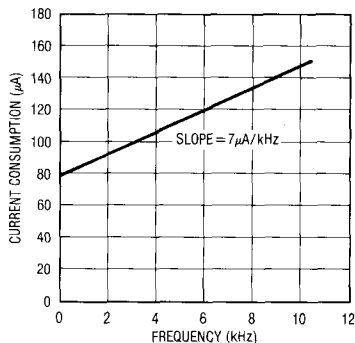


Figure 18. Current Consumption vs. Frequency for Figure 16

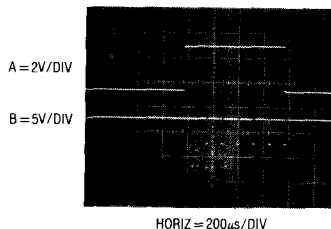


Figure 19. Figure 16's Step Response

To calibrate this circuit, apply 50mV and select the value at C1's input for a 100Hz output. Then, apply 5V and trim the input potentiometer for a 10kHz output.

An evolutionary history of this design appears in Box Section A, "Some Guidelines for Micropower Design and an Example".

A nice day at the San Francisco Zoo with Celia Moreno M.D., instrumental in arriving at the final configuration, is happily acknowledged.

1MHz Voltage-to-Frequency Converter

Figure 20 is also a V→F converter, but runs at 1MHz full-scale. Quiescent current is 90μA, ascending linearly to

360μA at 1MHz output. Obtaining higher operating frequency requires trade-offs in power consumption and step response performance. Linearity is 0.02% over a 100Hz→1MHz range, drift about 50ppm/°C and step response inside 350ms to full-scale.

This circuit has similarities to Figure 16, although operation is somewhat different. An input causes A1 to swing towards ground, biasing Q8. Q8's collector ramps (trace A, Figure 21) as it charges the 3pF capacitor plus stray capacitance associated with Q7 and the 74C14 Schmitt input connected to the node. When the ramp hits the Schmitt's threshold its output (trace B) goes low, turning on diode connected Q7. Q7's path discharges the node

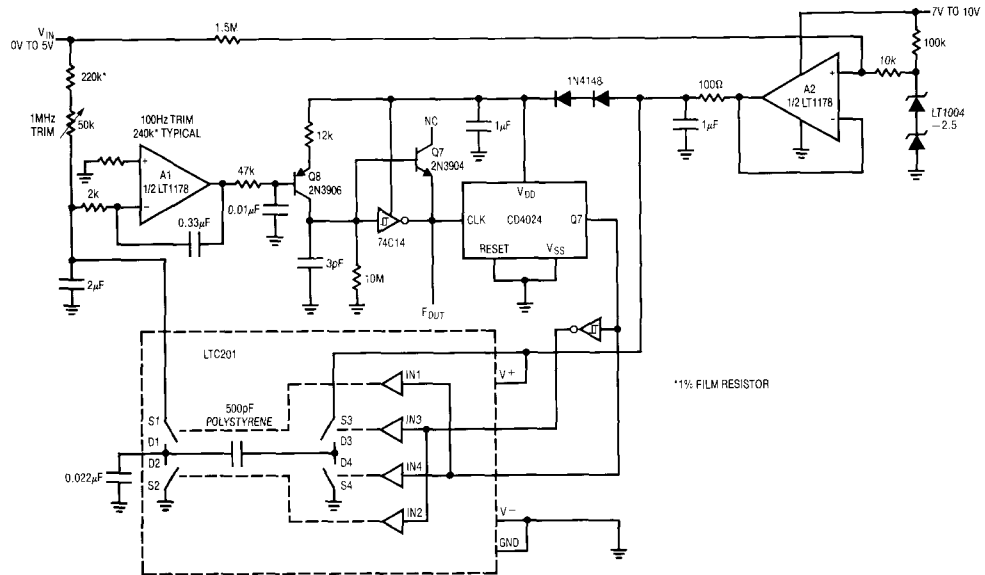


Figure 20. Micropower 1MHz V→F Converter

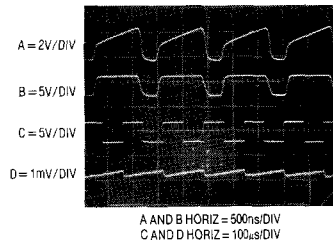


Figure 21. Figure 20's Waveforms

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capacitances, forcing ramp reset. The 74C14 returns high, and oscillation commences. The 74C14 also drives the CD4024 divider, and serves as the circuit's output. The divider's + 128 output (trace C) controls a reference-charge pump arrangement similar to Figure 16's. A2 furnishes a buffered reference. The 500pF capacitor is alternately charged and discharged by the LTC201 switch sections. The charge increments pulled through S1 continually force A1's 2 μ F capacitor to zero (trace D), balancing the input derived current. The 0.022 μ F capacitor at the D1-D2 LTC201 node eliminates excessive differentiated response, preventing spurious modes. This action closes a loop around A1, and it servo controls the Q7, Q8, 74C14 oscillator to run at whatever frequency is required to maintain its negative input at zero. This servo behavior eliminates oscillator drift and non-linearity as error terms, allowing the performance specifications noted. The 0.33 μ F capacitor at A1 stabilizes the loop. This capacitor accounts for the circuit's 350ms settling time.

The resistor from the input to A2 sums a small input related voltage to the reference, improving linearity. The 10M resistor at Q8's collector deliberately introduces leakage to ground, dominating all node leakages. This ensures low frequency operation by forcing Q8 to source current to maintain oscillations.

The circuit's current drain, while low, is larger than Figure 16's. The increase is primarily due to high frequency oscillator and divider operation. The series diodes in the oscillator-divider supply line lower supply voltage, decreasing current consumption. Oscillator current is also heavily influenced by the capacitance and swing at Q8's collector. The swing is fixed by the 74C14 thresholds. Capacitance has been chosen at the lowest possible value commensurate with desired low frequency operation.

To trim this circuit, put in 500 μ V and select the indicated value at A1's positive input for 100Hz out. Then, put in 5V and trim the 50k potentiometer for 1MHz out. Repeat this procedure until both points are fixed.

Switching Regulator

No discussion of micropower circuitry is complete without mention of switching regulators. Often, battery voltages must be efficiently converted to different potentials to meet circuit requirements. Figure 22 shows a micropower buck type switching regulator with a quiescent drain of

70 μ A and 20mA output current capability. When the output voltage drops (trace A, Figure 23) C1's negative input also falls, causing its output (trace B) to rise. This turns on the paralleled 74C907 open source buffers, and their outputs (trace C) go high. Current ramps up through the inductor, maintaining the regulator output. When output voltage rises a small amount, C1's output returns low and the cycle repeats. This action maintains regulator output despite line and load changes. The LT1004 serves as a reference and the 5pF capacitor ensures clean switching at C1. The 2810 Schottky diode prevents negative overdrives due to the 5pF unit's differentiated response; the 1N5817 is a catch diode, preventing excessive inductor caused negative voltages.

This circuit's low quiescent drain is due to the LT1017's small operating currents and the 74C907's low input drive requirements. Circuit resistor values are kept high to save current. C2 shuts down the regulator when output current exceeds 50mA. It does this by comparing the potential across the 0.2 Ω shunt to a resistively divided portion of the LT1004 reference. Excessive current drain trips C2 high, forcing C1's negative input high. This removes drive from the 74C907 buffers, shutting down the regulator.

Utilization of a CMOS buffer as a pass switch for a switching regulator is somewhat unusual, but performance is quite good. Figure 24 plots efficiency vs. output current at two input voltages. Efficiencies above 90% are possible, with output current to 20mA depending on input.

Post Regulated Micropower Switching Regulator

Figure 25 is another buck type switching regulator, but features a low loss linear post-regulator, quiescent current of 40 μ A and 50mA output capacity. The LT1020 linear regulator provides lower noise than a straight switching approach. Additionally, it offers internal current limiting and contains an auxiliary comparator which is used to form the switching regulator.

The switching loop is similar to Figure 22's circuit. A drop at the switching regulator's output (pin 3 of the LT1020 regulator; trace A, Figure 26) causes the LT1020's comparator to go high. The 74C04 inverter chain switches, biasing the P-channel MOSFET switch's grid (trace B). The MOSFET comes on (trace C), delivering current to the inductor (trace D). When the voltage at the inductor-220 μ F junction goes high enough (trace A), the comparator

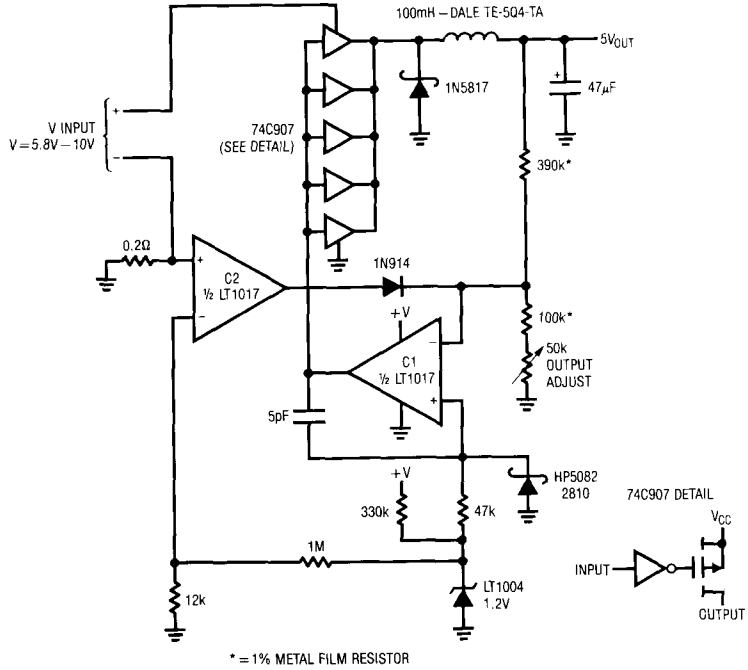


Figure 22. Micropower Switching Regulator

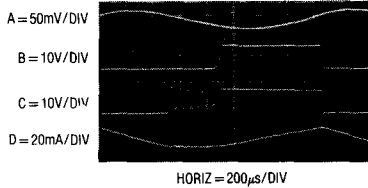


Figure 23. Figure 22's Waveforms

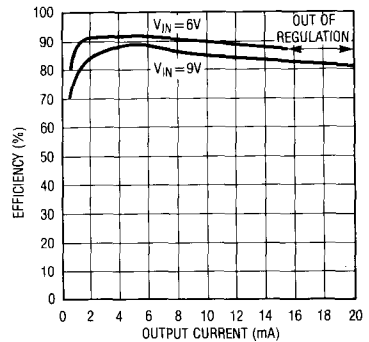


Figure 24. Figure 22's Efficiency vs. Output Current

Application Note 23

switches high, turning off MOSFET current flow. This switching loop regulates the LT1020's input pin at a value set by the resistor divider in the comparator's negative input and the LT1020's 2.5V reference. The 680pF capacitor stabilizes the loop and the 1N5817 is the catch diode. The 270pF capacitor aids comparator switching and the 2810 diode prevents negative overdrives.

The low dropout LT1020 linear regulator smooths the switched output. Output voltage is set with the feedback pin associated divider. A potential problem with this circuit is start-up. The switching loop supplies the LT1020's input but relies on the LT1020's internal comparator to function. Because of this, the circuit needs a start-up mechanism. The 74C04 inverters serve this function. When power is applied, the LT1020 sees no input, but the inverters do. The 220k path lifts the first inverter high, causing the chain to switch, biasing the MOSFET and starting the circuit. The inverter's rail-to-rail swing also provides ideal MOSFET grid drive.

Even though this circuit's 40 μ A quiescent current is lower than Figure 22's, it can source more current. The extremely small quiescent current is due to the low LT1020 drain and the MOS elements. Figure 27 plots efficiency vs. output current for two LT1020 input-output differential voltages. Efficiency exceeding 80% is possible, with outputs to 50mA available.

Figures 28 and 29 show two other LT1020 micropower regulator based circuits. In many processor based systems it is desirable to monitor or control the power down sequence. Figure 28 produces a logical "1" output when the regulator output begins to dropout (e.g., battery is low). Here, the regulator is programmed for a 5V output with the 1M Ω feedback resistors. The 0.001 μ F capacitor provides frequency compensation. The LT1020's internal comparator senses the difference between the chip's 2.5V reference and a small portion of the IC's pass transistor current (supplied at pin 13). At the edge of dropout, the

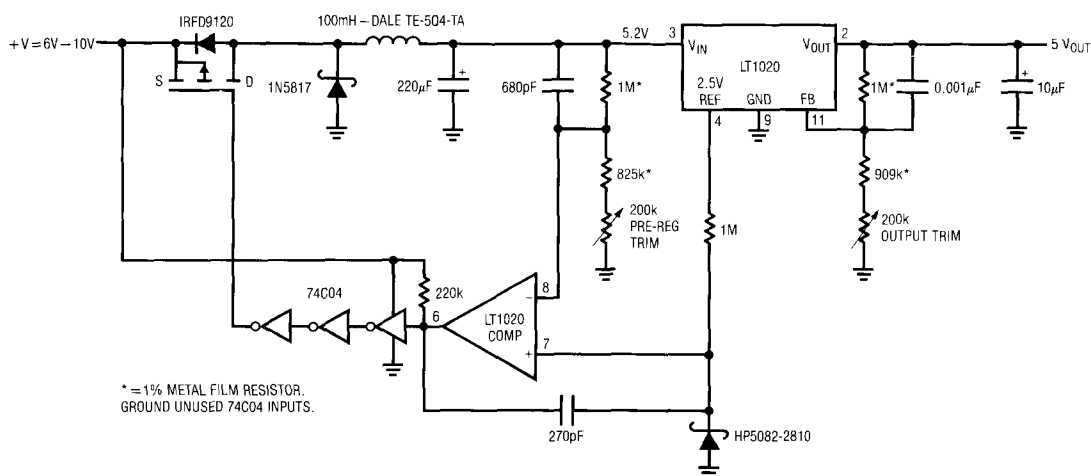


Figure 25. Micropower Post-Regulated Switching Regulator

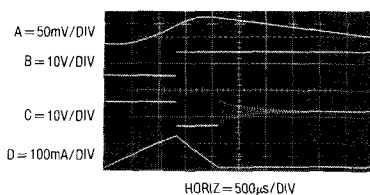


Figure 26. Figure 25's Waveforms

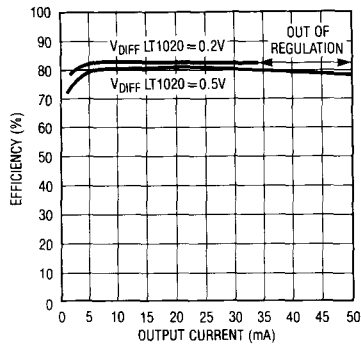


Figure 27. Figure 25's Efficiency vs. Output Current

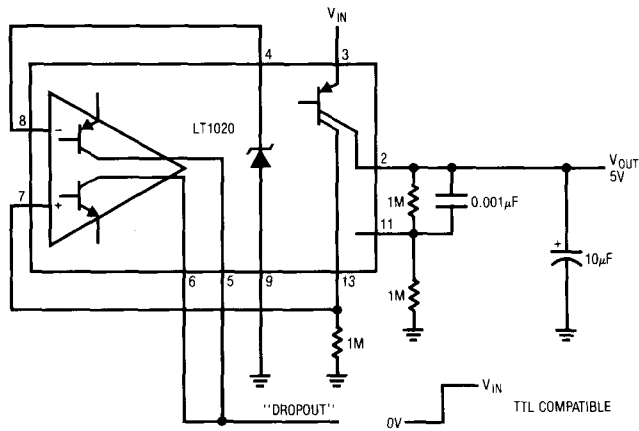


Figure 28. Regulator with Logic Output on Dropout

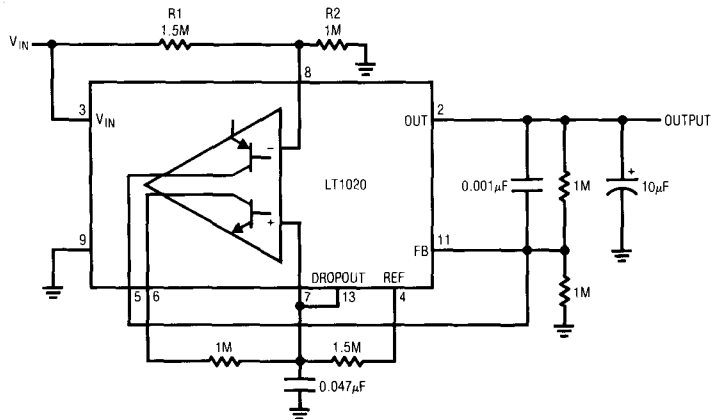


Figure 29. Regulator with Output Shutdown on Dropout

Application Note 23

LT1020's pass transistor goes towards saturation, raising pin 13's voltage. This trips the comparator, and its output goes high. This signal can be used to alert a processor that power is about to go down.

Figure 29 is similar, except that power is turned completely off when dropout begins to occur, preventing unregulated supply conditions. The comparator feedback is arranged for a hysteresis type response. Although the output turns off at dropout, it will not turn on until:

$$\text{Turn On} = \frac{V_{IN} \times R2}{R1 + R2} = 2.5V$$

This prevents battery "creep back" from causing oscillation.

Figure 30 shows a simple way to shut the LT1020 down. In this state it draws only 40 μ A. The logic signal forces the feedback pin above the internal 2.5V reference, and all drive is removed from the output transistor. Figure 31 shows a low loss way to implement a "glitchless" memory battery backup. During line powered operation, the right LT1020 does the work. The feedback string is arranged so that the left LT1020 does not conduct under line powered conditions. When the line goes down, the associated LT1020 begins to go off, allowing the battery driven regulator to turn on, maintaining the load.

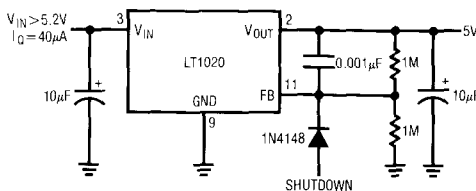


Figure 30. LT1020 Shutdown

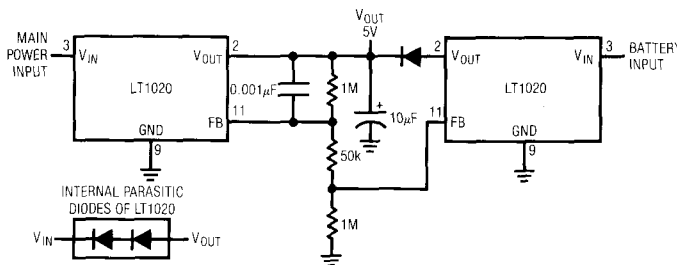


Figure 31. Battery Backup Regulator

BOX SECTION A

Some Guidelines for Micropower Design and an Example

As with all engineering, micropower circuitry requires attention to detail, awareness of trade-offs and an opportunistic bent towards achieving the design goal.

The most obvious way to save power is to choose components which require little energy. Additional savings require more effort.

Circuits should be examined in terms of current flow. Consider such flow in all DC and AC paths. For example, do DC base currents go where they can do some useful work, or are they thrown away? Try to keep AC signal swings down, particularly if capacitors (parasitic or intended) must be continually charged and discharged. Examine the circuit for areas where power strobing may be allowable.

Consider quiescent vs. dynamic power requirements of components to avoid unpleasant surprises. Datasheets usually specify quiescent power because the manufacturer doesn't know what the user's circuit conditions are. For example, everyone "knows" that "MOS devices draw no current." Unfortunately, Mother Nature dictates that as frequency and signal swings go up, the capacitances associated with MOS devices begin to require more power. It is often a mistake to automatically associate low power operation with a process technology. While it's likely that CMOS will provide lower power operation for a given function than 12AX7s, a bipolar approach may be even better. Consider individual situations on the basis of their specific requirements before committing to a technology. Very often, circuits require several technologies (e.g., CMOS, bipolar and discrete) for best results.

Usually, achieving low power operation requires performance trade-offs. Minimizing signal swings and current saves power, but moves circuit operation closer to the noise floor. Offsets, drift, bias currents and noise become increasingly significant error factors as signal amplitudes are constricted to save power. This is a fundamental trade-off and must be carefully considered. Circuits employing power strobing can sometimes get around this problem by utilizing low duty cycles. Text Figure 3 uses this technique to achieve dramatic power savings in a circuit with an on-state drain approaching 20mA (see also Box Section B, "Sampling Techniques and Components for Micropower Circuits").

Text Figure 16, a voltage-to-frequency converter, furnishes an example of the evolution of a low power design. Design goals included a 10kHz maximum output, fast step response, linearity inside 0.05% and a maximum supply current of 150 μ A. Other specifications appear in the text.

Figure A1 shows an early version of this circuit. Operation is similar to the text described for Figure 16, but a brief description follows: When the input current-derived ramp at C1's negative input crosses zero, C1's output drops low, pulling charge through C1. This forces the negative input below zero. C2 provides positive feedback, allowing a complete discharge for C1. When C2 decays, C1's output goes high, clamping at the level set by D1, D2 and V_{REF}. C1

receives charge and recycling occurs when C1's negative input again arrives at zero. The frequency of this action is related to the input voltage. Diodes D3 and D4 provide steering, and are temperature compensated by D1 and D2. C1A's sink saturation voltage is uncompensated, but small. C1B is a start-up loop.

Although the LT1017 and LT1034 have low operating currents, this circuit pulls almost 400 μ A. The AC current paths include C1's charge-discharge cycle, and C2's branch. The DC path through D2 and V_{REF} is particularly costly. C1's charging must occur quickly enough for 10kHz operation, meaning the clamp seen by C1A's output must have low impedance at this frequency. C3 helps, but significant current still must come from somewhere to keep impedance low. C1A's current limited output cannot do the job unaided, and the resistor from the supply is required. Even if C1A could supply the necessary current, V_{REF}'s settling time would be an issue. Dropping C1's value will reduce impedance requirements proportionally, and would seem to solve the problem. Unfortunately, such reduction magnifies the effects of stray capacitance at the D3-D4 junction. It also mandates increasing R_{IN}'s value to keep scale factor constant. This lowers operating currents at C1A's negative input, making bias current and offset more significant error sources.

Figure A2 shows an initial attempt at dealing with these issues. This scheme is similar to Figure A1, except that Q1 and Q2 appear. V_{REF} receives switched bias via Q1, instead of being on all the time. Q2 provides the sink path for C1. These transistors invert C1A's output, so its input pin assignments are exchanged. R1 provides a light current from the supply, improving reference settling time. This arrangement decreases supply current to about 300 μ A, a significant improvement. Several problems do exist, however. Q1's switched operation is really effective only at higher frequencies. In the lower ranges, C1A's output is low most of the time, biasing Q1 on and wasting power. Additionally, when C1A's output switches, Q1 and Q2 simultaneously conduct during the transition, effectively shunting R2 across the supply. Finally, the base currents of both transistors flow to ground and are lost. The basic temperature compensation is as before, except that Q2's saturation term replaces the comparator's.

Application Note 23

Figure A3 is better. Q1 is gone, Q2 remains but Q3, Q4 and Q5 have been added. V_{REF} and its associated diodes are biased from R1. Q3, an emitter-follower, is used to source current to C1. Q4 temperature compensates Q3's V_{BE} , and Q5 switches Q3.

This method has some distinct advantages. The V_{REF} string can operate at greatly reduced current because of Q3's current gain. Also, Figure A2's simultaneous conduction problem is largely alleviated because Q5 and Q2 are switched at the same voltage threshold out of C1A. Q3's base and emitter currents are delivered to C1. Q5's currents are wasted, although they are much smaller than Q3's. Q2's small base current is also lost. The values for C2 and R3 have been changed. The time constant is the

same, but some current reduction occurs due to R3's increase.

If C1 cannot be reduced for performance reasons, then its AC currents cannot be avoided. This leaves only the aforementioned Q5 and Q2 currents as significant wasted terms, along with R3's now smaller loss. Current drain for this circuit is about $200\mu A$ maximum. Text Figure 16's circuit is very similar, but eliminates Q5 and Q2's losses to achieve maximum operating current below $150\mu A$ with quiescent current under $80\mu A$. Some other refinements are included, but the circuit is the final iteration of the three versions shown here. A complete description of Figure 16 appears in the text.

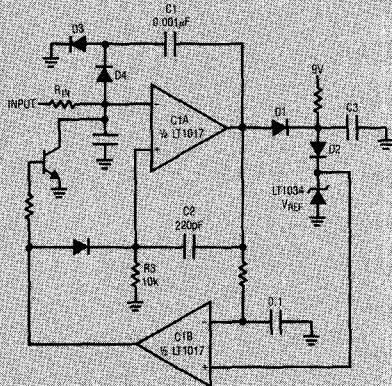


Figure A1

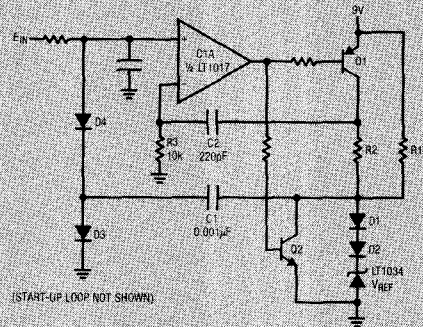


Figure A2

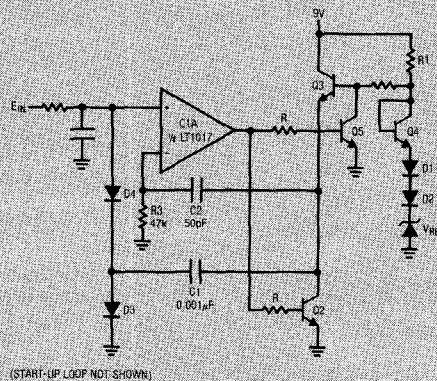


Figure A3

BOX SECTION B

Sampling Techniques and Components for Micropower Circuits

The best way to get low power circuit characteristics is to turn off the power. While there are some obvious problems with this approach, it does point a way towards minimizing power consumption. In many applications continuous circuit power is not necessary. If bandwidth requirements are low, sampling techniques offer a simple way to save power. With low duty cycles, instantaneous current can be relatively high while average drain remains low. When considering a sampled approach some issues should be examined. The required circuit bandwidth dictates the minimum sampling frequency in accordance with Nyquist criteria. The sampling interval's duration is determined by circuit settling time to the required accuracy. This settling time should be considered for all circuit elements (transducers, ICs and discrete components) singularly and together. Additionally, effects of sampled operation on component life and operating characteristics should be examined. This is particularly the case for transducers, which may be designed and tested under DC operating conditions.

Once these issues have been addressed, components can be selected. The LTC1040, LTC1041 and LTC1042 have been specifically designed for sampled operation. Figure B1 details the LTC1040, Dual Micropower Comparator. Its programmable internal oscillator sets the sampling rate with a sampling interval lasting 80 μ s. The V_{pp} output supplies power during the sampling interval, allowing drive for external circuitry or transducers. Note that the input common-mode range includes both rails. Figure B2 plots supply current vs. sampling frequency.

A related device is similar, but dedicated to "bang-bang" on-off type servo loops. The LTC1041 appears in Figure B3. Servo SET POINT and DELTA are controllable from the inputs. The associated diagram (Figure B4) graphically defines operation. Operating current is similar to the LTC1040.

A final device, the LTC1042, is also similar but is set up as a window comparator. Its internals appear in Figure B5 and the graphic operation description is shown in Figure B6. Operating current, input range and sampling characteristics are similar to the LTC1040 and LTC1041.

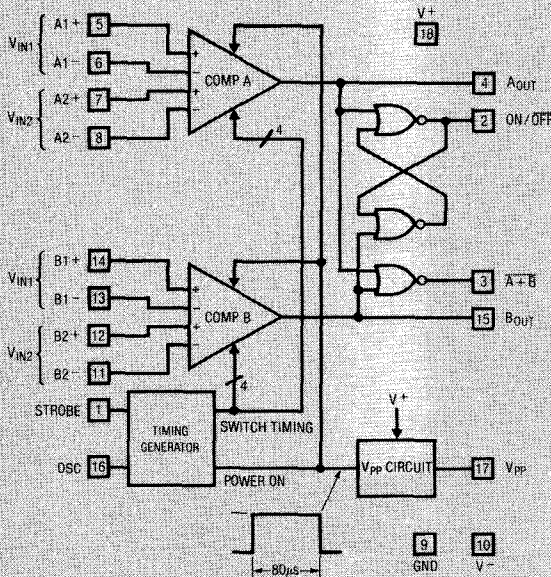


Figure B1. LTC1040 Internal Details

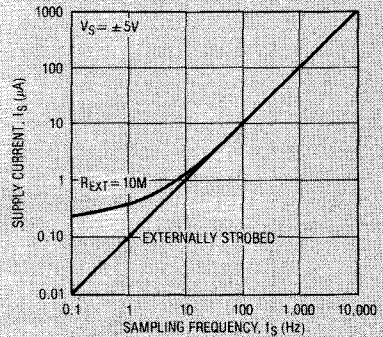


Figure B2. LTC1040 Power Consumption vs. Sampling Frequency

Application Note 23

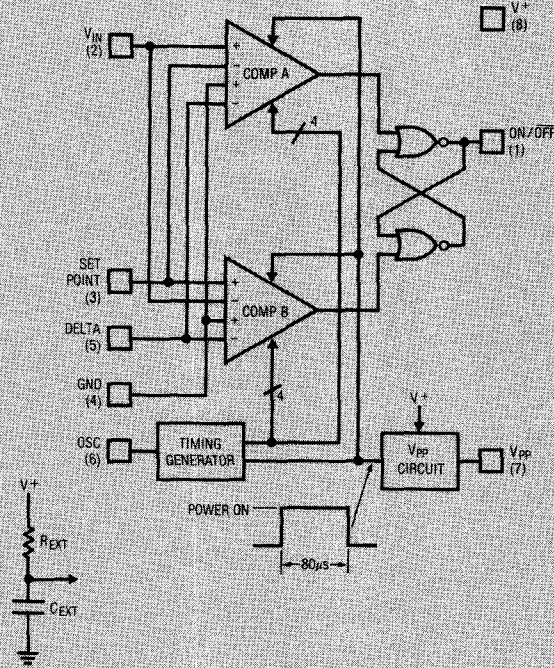


Figure B3. LTC1041 Details

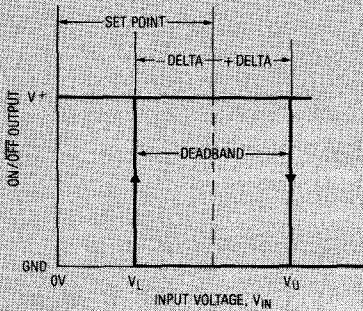


Figure B4. LTC1041 Operation Diagram

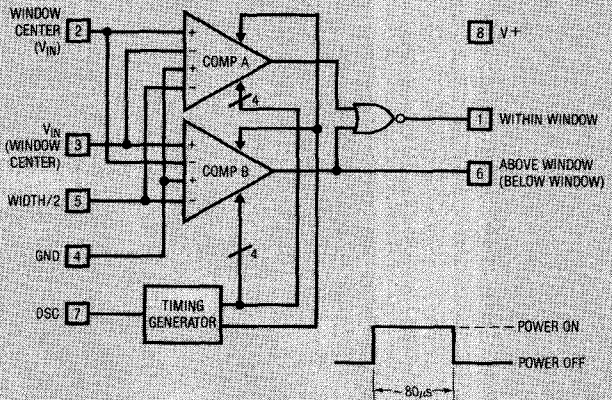


Figure B5. LTC1042 "Window" Comparator Details

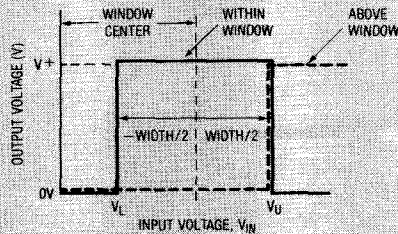


Figure B6. LTC1042 Operating Diagram

BOX SECTION C

Parasitic Effects of Test Equipment on Micropower Circuits

The energy absorbed by test equipment connections to micropower circuits can be significant. Under normal circumstances test equipment and probes have negligible power drain, but microampere level operating currents mandate care. Test instrumentation should be regarded as an integral part of the circuit. DC and AC loading and parasitic effects must be kept in mind to avoid unpleasant surprises. Such instrument connection errors can make the circuit under test look unfairly bad or good.

The DC resistance of oscilloscope probes varies from hundreds of ohms (1X types) to 10MΩ (10X), with some 10X types as low as 1MΩ. Contrary to some expectations, FET probes do not have high input resistance—some types are as low as 100kΩ, although most are about 10MΩ. The DC loading of a 10X 1M probe could introduce as much as 9μA of loss, almost 10% of Figure 11's total! The AC loading of a 10pF probe looking at Figure 11's 20kHz clock will cause apparent circuit consumption of 5μA, a significant loss in a low power circuit. 1X type probes present about 50pF of loading, with 1MΩ DC resistance when connected to the scope. This kind of probe loading can cause large errors in micropower circuits, while virtually disabling some. Such a probe, introduced at pin 6 of text Figure 7, would stop the circuit's oscillator. If placed across the supply of the same circuit it would consume 15 times the circuit's

operating current. Similarly, the probe's 50pF input capacitance connected to Figure 20 (Q8's collector) results in a 25% apparent increase in circuit current at 1MHz output.

Probe AC and DC loading are not the only effects. Some DVM's produce "charge spitting" at their inputs. Such parasitic charge, introduced into high impedance nodes, can cause substantial errors. It's also worth remembering that DVM DC loading may change with range. Lower ranges may have very high input impedance, but higher ranges are typically 10MΩ. A 10MΩ DVM reading Figure 7's supply consumes 1½ times the circuit current.

Figure C1 shows a way test equipment can make the circuit look too good, instead of too bad. If the pulse generator is adjusted more than a diode drop above the regulator's output, the bypass capacitor peak detects the charge delivered through the IC's internal diode. The regulator can't sink current, and with its output forced high it won't source anything. Under these conditions the circuit functions while the current meter reads zero....a very low power circuit indeed!*

*Practically speaking, most regulators and power supplies can sink small amounts of current. Because of this, the current meter may actually read negative.

Application Note 23

Figure C2 shows a very simple, but useful, circuit which greatly aids probe loading problems in micropower circuits. The LT1022 high speed FET op amp drives an LT1010 buffer. The LT1010's output allows DVM cable and probe driving and also biases the circuit's input shield. This bootstraps the input capacitance, reducing its effect. DC

and AC errors of this circuit are low enough for almost all work, with enough bandwidth for just about any low power circuit. Built into a small enclosure with its own power supply, it can be used ahead of a 'scope or DVM with good results. Pertinent specifications appear in the diagram.

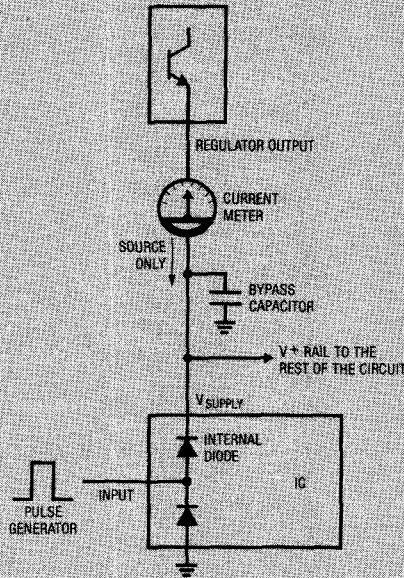


Figure C1

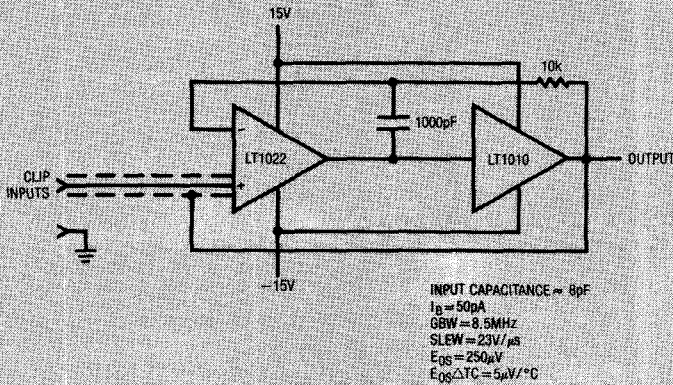


Figure C2

Unique Applications for the LTC1062 Lowpass Filter

Nello Sevastopoulos
 Philip Karantzalis

The LTC1062 As A Loop Filter

With commercially available PLLs, the loop filter is designed by the user to optimize the loop performance. For a variety of applications, a 1st or 2nd order lowpass passive or active R, C filter will do the job. When minimum output jitter and good transient response are required simultaneously, the design of the loop filter becomes more sophisticated. For instance, a fast transient response implies wide filter bandwidth and a reduced VCO output jitter implies minimum ripple at the VCO input. This is achieved by high outband attenuation of the lowpass filter. The LTC1062 provides the above requirements as well as economy and cutoff frequency programmability to be used advantageously in PLL designs.

The circuit of Figure 1 illustrates the use of the LTC1062 as a loop filter. The power supplies for the circuit are a single 5V for the PLL and $\pm 5V$ for the LTC1062. The CMOS PLL is a CD4046B. The LTC1062 can also be used with a single 5V with some additional level shifting (see AN20). Phase detector #2 drives a diode-resistor limiter combination to make the voltage at input R of the LTC1062 swing from one diode above ground to one diode below the 5V supply. Additionally, the two 5k resistors establish a maximum AC impedance to keep the LTC1062 in its operating region and to bias the VCO input at its mid point when phase detector #2 switches into a three-state mode.

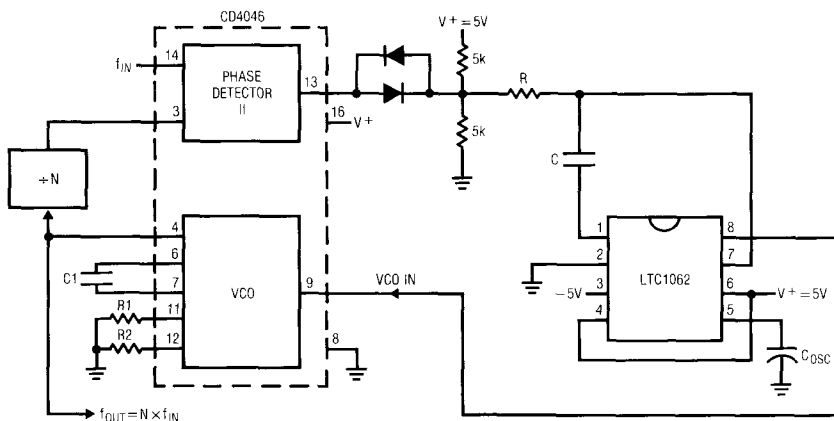


Figure 1

Application Note 24

An empirical design procedure for input frequencies less than 5kHz ($f_{IN} \leq 5\text{kHz}$, Figure 1) is illustrated below:

- Given the minimum input frequency value, the cutoff frequency, f_c , of the LTC1062 should be chosen as:

$$1/6 (f_{IN(MIN)}) \leq f_c \leq 1/4 (f_{IN(MIN)})$$

The internal (or external) clock frequency of the LTC1062 should be 150 to 250 times the desired cutoff frequency, f_c .

- The capacitor C_{OSC} setting the LTC1062's internal oscillator should be chosen by:

$$C_{OSC} = \left(\frac{130\text{kHz}}{250 \times f_c} - 1 \right) \times 33\text{pF}$$

By further decreasing the value of C_{OSC} , the internal clock frequency of the LTC1062 increases and the damping of the loop also increases.

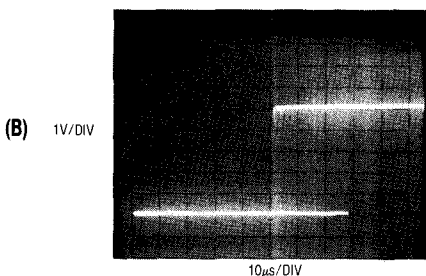
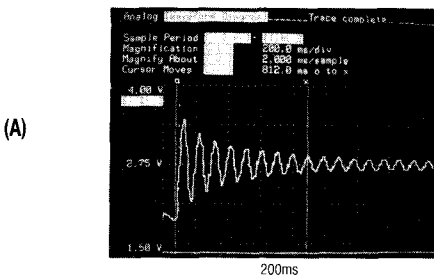
- By letting the value of $C = 0.047\mu\text{F}$, the LTC1062 input resistor R should be:

$$R = \frac{5500\text{k}\Omega}{f_c (\text{Hz})}$$

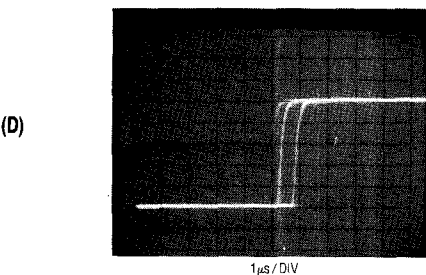
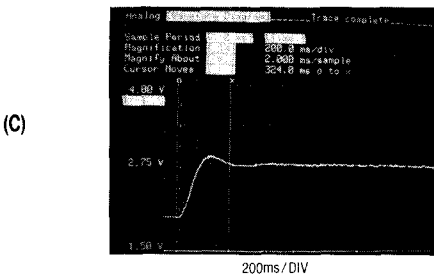
Note: For this application, the loop filter is not required to be maximum flat and, therefore, the (R, C) values of the LTC1062 can be within $\pm 5\%$ tolerance.

To illustrate the performance difference between a low-pass passive R, C loop filter and the LTC1062, the circuit of Figure 1 was tested for two different PLL input frequency ranges.

The first case is a PLL with a $60\text{Hz} \pm 10\%$ input frequency range and with $\div N = 100$. Then, the PLL's VCO output could be used to drive the clock input of a precision switched capacitor filter, such as an LTC1060A set up in a 100:1 clock to center ratio, and configured as a 60Hz sharp notch or bandpass filter. Figure 2A shows the transient response of the loop when a passive R,C loop filter, Figure 3,



Transient response (A) and jitter (B) of the PLL with a passive R, C loop filter. The output frequency of the VCO is 6kHz and the $\div N = 100$.



Transient response (C) and jitter (D) of the PLL with the LTC1062 used as a loop filter. The VCO output frequency is 6kHz and the $\div N = 100$. The jitter is reduced to the internal jitter of the VCO.

Figure 2

is used. The input frequency is shifted from 54Hz to 60Hz and the loop takes 820ms to settle within 5% of its steady state value. The corner frequency of the R, C passive filter is 22Hz. The natural frequency of the loop is approximately 10Hz and the damping factor less than 0.1. Figure 2B shows the jitter at the VCO output under the above conditions. A $30\mu\text{s}$ jitter with $f_{OUT} = 6\text{kHz}$ corresponds to 18% instantaneous frequency inaccuracy. This makes the PLL VCO output unusable as a clock generator for a tracking switched capacitor filter. A small improvement in the VCO output jitter could be achieved by further decreasing the filter's cutoff frequency; this, however, would further penalize the circuit's settling time.

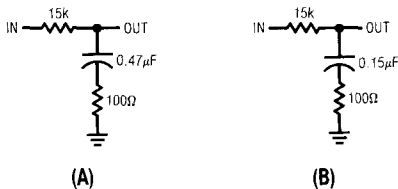
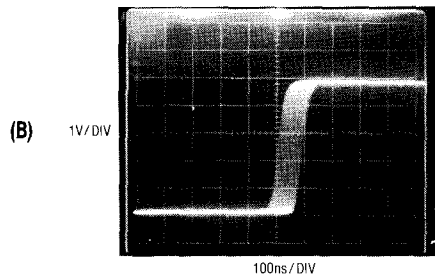
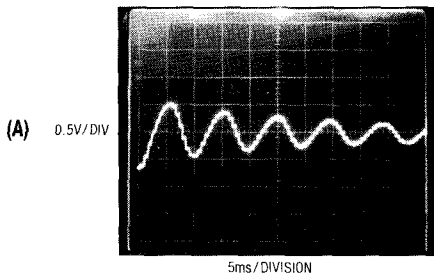


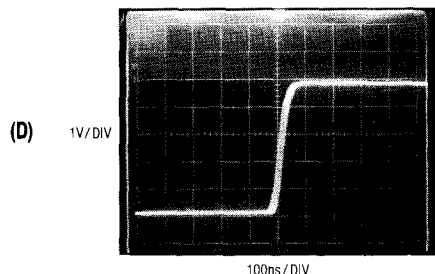
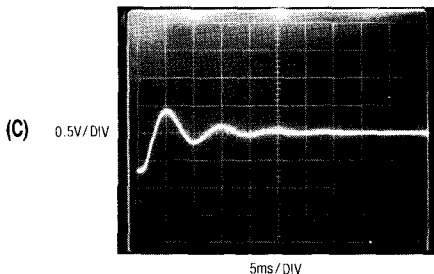
Figure 3. Lowpass R, C Filters used for the 2 PLL Examples

Figures 2C and 2D show the PLL performance when an LTC1062 is used as a loop filter. The corner frequency f_c of the LTC1062 was set at 9.5Hz ($\approx 1/6 f_{IN}$) and its internal clock was set for 2.4kHz ($\approx 252 \times f_c$). The settling time of the loop was 320ms and the damping factor was optimally set to 0.7. The $1\mu\text{s}$ VCO output jitter, $f_{OUT} = 6\text{kHz}$, was measured over 5 periods and it is attributed to the inherited jitter of the VCO internal circuitry. With the LTC1062 used as a loop filter, the circuit's jitter corresponds to 0.12% frequency error. This is quite adequate to drive the clock input of 0.3% accurate switched capacitor filters, such as LTC1059A or LTC1060A.

For the second example, the circuitry of Figure 1 was set for a PLL input of $f_{IN} = 1400\text{Hz} \pm 30\%$ and a divide by $N = 128$. The circuit's transient response, when the input shifted from 1260Hz to 1540Hz and when an R, C passive loop filter was used, is shown in Figure 4. The cutoff frequency of the R, C passive, Figure 3B, was set at 53Hz. The VCO output jitter, Figure 4B, was $\Delta t = 90\text{ns}$ and was measured over 5 periods. This yields a $\Delta t/5T \times 100\% = 0.32\%$ total phase jitter of the output frequency, $f_{OUT} = 1400 \times 128 = 179.2\text{kHz}$.



Transient response (A) and jitter (B) of the PLL with a passive R, C loop filter. the output frequency is $f_{OUT} = 179.2\text{kHz}$ and the $\div N = 128$.



Transient response (C) and jitter (D) of the PLL when an LTC1062 is used as a loop filter, the output frequency, $f_{OUT} = 179.2\text{kHz}$ and the $\div N = 128$.

Figure 4

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Figures 4C and 4D show the loop's performance when an LTC1062 replaces the R, C passive filter. The LTC1062 was set for a cutoff frequency of $f_c = 250\text{Hz}$ or $1/5$ of the $f_{IN(MIN)}$. The internal oscillator of the LTC1062 was set at 43kHz or 172 times its cutoff frequency. The VCO output jitter was $\Delta t = 30\text{ns}$ (or 0.09%) and was measured over 6 periods. Note the excellent transient response of the circuit, Figure 4C, when compared to the underdamped response, Figure 4A.

These two PLL cases demonstrate the advantages of using the LTC1062 as a loop filter in conjunction with the CD4046B phase locked loop. For a variety of low frequency inputs and high $\div N$ numbers, the LTC1062 allows the loop to simultaneously achieve good transient response and minimum output jitter. For best results, use the LTC1062 for PLL input frequencies below 5kHz and when the CD4046B operates with a single 5V supply, set 2.75V bias

at the VCO input as the center of the tracking range. The minimum and maximum locking range settings of the VCO input should then be 2.25V and 3.25V , respectively.

Clock Sweeplable Pseudo Bandpass/Notch Filters

If the feedback capacitor from pins 1 to 7 is replaced with a resistor, Figure 5, the circuit loses its lowpass characteristics and the response of the filter becomes selective like a bandpass. Also, since the two external components (R_2 , R_1) are frequency independent, *the LTC1062 can be fully swept with an external clock.*

Figure 6 shows the frequency response of Figure 5, for a clock frequency of 100kHz . Figure 7 shows the variation of the peak gain, H_{op} , and the peak frequency, f_p , of Figure 6 versus different values of the (R_1/R_2) resistor ratio.

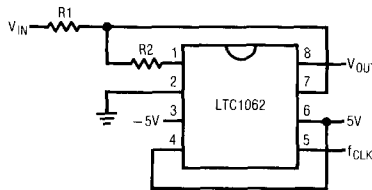


Figure 5

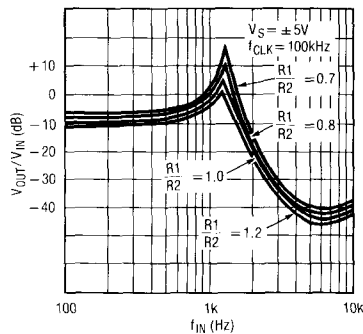


Figure 6

As can be seen from Figure 7, the resistor ratio (R_1, R_2) alters mainly the peak gain of the filter and has very little effect on the value of the peak frequency of Figures 5 or 6.

Because of this, two LTC1062s can now be stagger-tuned with a common clock, as shown in Figures 8 and 9, to produce a respectable bandpass response.

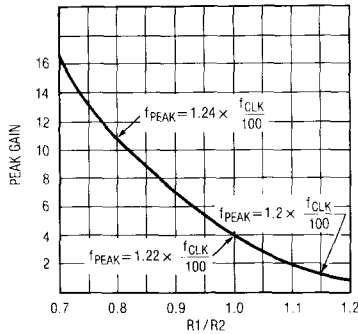


Figure 7

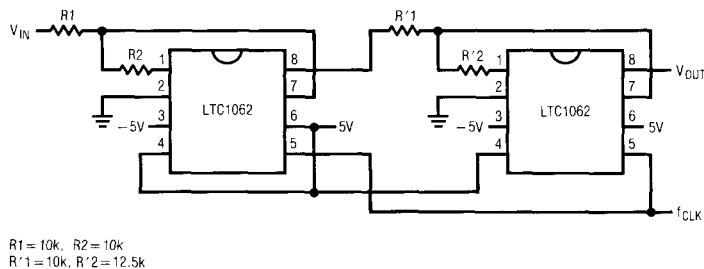


Figure 8. Cascading Two LTC1062s to Form a Very Selective Clock Sweepable Bandpass

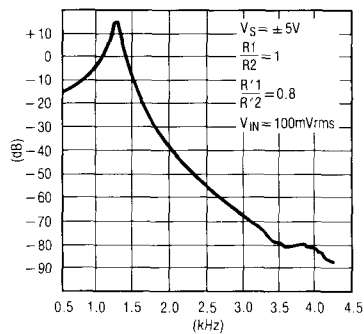


Figure 9

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In Figure 6, the -180° phase shift occurs just before the frequency of the peak. Using this property and summing the output of the bandpass filter, Figure 10, with the input voltage, a clock tunable notch response is realized, Figure 11. The clock to notch frequency ratio is 79.3:1 and it is predictable and repeatable from part to part. The

notch frequency response of Figure 11 is obtained by setting the ratio $(R1/R2)$ equal to 1.24 and by letting all the gain resistors be equal. Standard 1% value resistors will produce a 40dB deep notch. Additional notch depth can be obtained by tuning resistor R1.

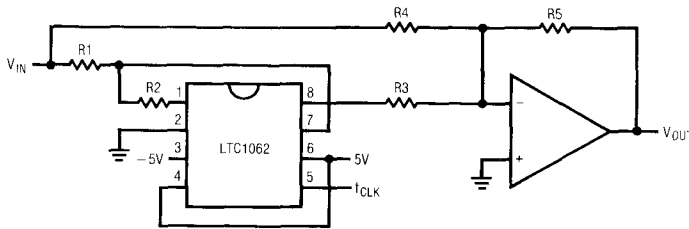


Figure 10. Clock Tunable Notch Filter
For simplicity use $R3 = R4 = R5 = 10k$;

$$\frac{R1}{R2} = 1.234, \frac{f_{CLK}}{f_{notch}} = 79.3$$

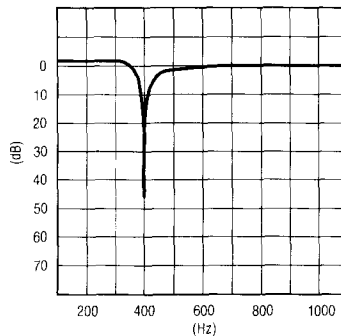


Figure 11. LTC1062 Notch Response

Accommodating High Input Voltages

High input voltages outside the input common-mode range of the LTC1062 can be divided down through a simple resistor divider, Figure 12. The DC gain of the lowpass filter is $R2/(R1 + R2)$ and for maximum passband flatness, the paralleled combination of $R1, R2$ should be chosen as:

$$\frac{1}{2\pi(R1//R2) \times C} = \frac{f_{CUTOFF}}{1.63}; R1//R2 \geq 5k\Omega$$

Note, in Figure 12, there is no need for an external op amp to buffer the divided down input voltage. The internal buffer input, pin 7, performs this function.

An obvious and often encountered application is to use this technique to interface the LTC1062 with op amps powered from $\pm 15V$ supplies, Figure 13. Two inexpensive 7V zeners limit the LTC1062 power supply voltage to $\pm 8V$; meanwhile, the output of the op amp A is divided by 2. The DC accurate output of the LTC1062 is then amplified by 2. For this application, an LT1013 precision dual op amp is recommended. The maximum DC output voltage will be $300\mu V$ if the A grade of the LT1013 is used.

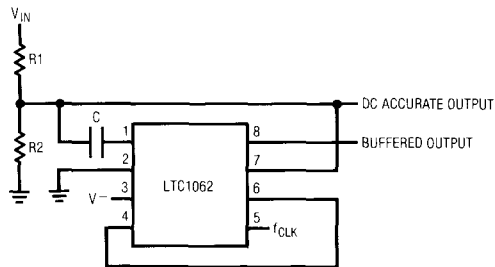


Figure 12. Using Input Resistor Divider to Accommodate High DC and/or AC Input Voltages. Pin 7 DC Buffers the Input Voltage.

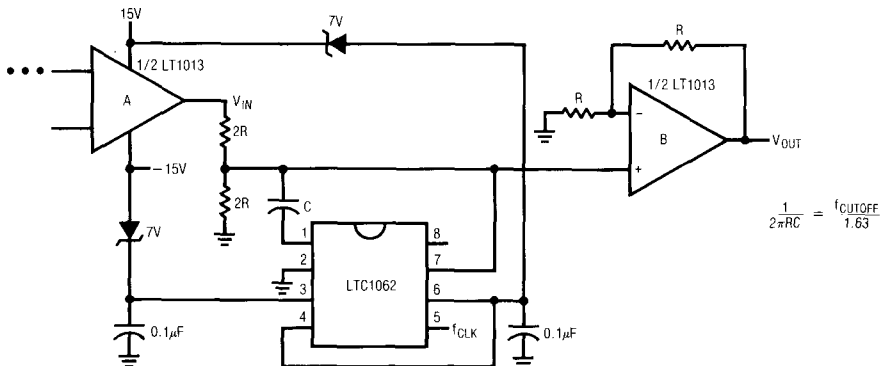


Figure 13. Using the LTC1062 in Conjunction with Precision Op Amps Operating from $\pm 15V$ Power Supply

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Programming Various Cutoff Frequencies

To obtain several cutoff frequencies with a single LTC1062, the clock frequency and the external $R \times C$ product should be simultaneously varied such as:

$$\frac{1}{2\pi RC} = \frac{f_C}{1.64} = \frac{f_{\text{CLOCK}}}{164}$$

For instance, to double the filter's cutoff frequency, we should double the clock frequency and, at the same time, divide by two the $R \times C$ product of the external resistor-capacitor combination. With a dual four channel multiplexer, we can easily obtain four different cutoff frequencies by selecting four input resistors and four clock

frequencies. In Figure 14, the clock frequencies, all of them being $\leq 50\text{kHz}$, where derived through a simple R, C oscillator.

Applying an External Clock Before the Power Supplies are ON

If the clock at pin 5 is externally applied before the power supplies turn ON, the device will latch. To avoid this, insert a 500Ω resistor or in series with pin 5. This will prevent latch up over temperature. If the power supplies exceed $\pm 6\text{V}$, the input protection resistor should be increased to 1k .

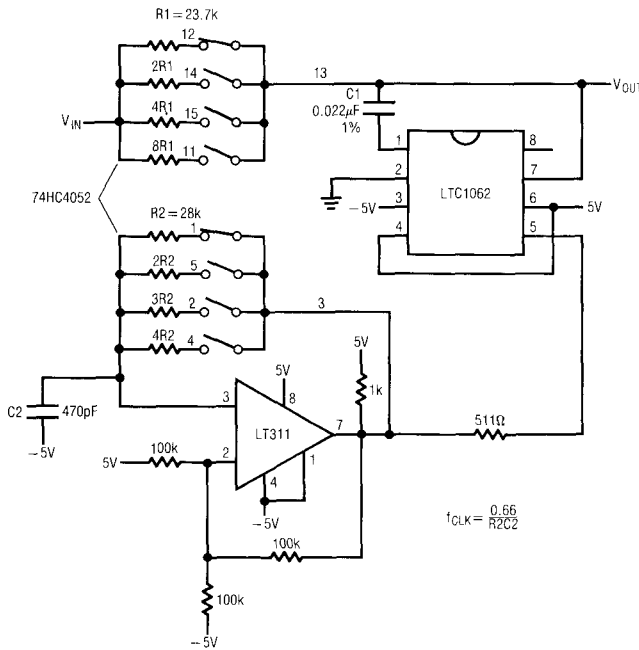


Figure 14. Using a Dual 4-Channel Multiplexer to Obtain Four Different Cutoff Frequencies (500Hz, 250Hz, 125Hz, 62.5Hz).

Switching Regulators for Poets A Gentle Guide for the Trepidatious

Jim Williams

The above title is not happenstance and was arrived at after considerable deliberation. As a linear IC manufacturer, it is our goal to encourage users to design and build switching regulators. A problem is that while everyone agrees that *working* switching regulators are a good thing, everyone also agrees that they are difficult to get working. Switching regulators, with their high efficiency and small size, are increasingly desirable as overall package sizes shrink. Unfortunately, switching regulators are also one of the most difficult linear circuits to design. Mysterious modes, sudden, seemingly inexplicable failures, peculiar regulation characteristics and just plain explosions are common occurrences. Diodes conduct the wrong way. Things get hot that shouldn't. Capacitors act like resistors, fuses don't blow and transistors do. The output is at ground, and the ground terminal shows volts of noise.

Added to this poisonous brew is the regulator's feedback loop, sampled in nature and replete with uncertain phase shifts. Everything, of course, varies with line and load conditions—and the time of day, or so it seems. In the face of such menace, what are Everyman and the poets to do?

The classic approach is to seek wisdom. Substantial expertise exists but is concentrated in a small number of corporate and academic areas. These resources are not readily accessed by Everyman and some cynics might suggest that they are deliberately protected by a self-

serving priesthood. A glance through conference proceedings and published literature yields either a storm of mathematics or absurdly coy and simple little block diagrams that make everything look just so easy. Either way, Everyman loses. And the poets don't even get to try.

Something to think about is that most people who want switching regulators don't need 98.2% efficiency or 100W/cubic inch. They aren't trying to get tenure and don't care about inventing a new type of circuit. What they want are concepts directly applicable to construction of working circuits with readily-available parts. Thus equipped, Everyman can build and sell useful products, presumably buy more components and everyone's interests (not incidentally, including ours) are served.

As author, I must confess that I am more poet than switching regulator designer, and my poetry ain't very good. Before this effort, my enthusiasm level for switchers resided somewhere between trepidation and terror. This position has changed to one of cautiously respectful optimism. Several things aided this transformation and significantly influenced this publication. The "encouragement" of the Captains of this corporation, emphasized over the last year at increasingly insistent levels, constituted one form of inspiration. Conversations with users (or people who wanted to be) provided more valuable perspective and strength in the knowledge that I was not alone in my difficulties with switchers.

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At the circuit level, a significant decision was to employ standard, off-the-shelf magnetics exclusively.* This policy was driven by the observation that the majority of problems encountered with switchers centered around inductive components. This approach almost certainly prevents precisely-optimized performance and may horrify some veteran switcher designers. It also eliminates inductor construction uncertainties, saves time and greatly increases the likelihood of getting a design running. It's much easier to work with, and get enthusiastic about, a functional circuit than the smoking carcass of a devastated breadboard. If standard inductor characteristics aren't optimal, it's easier to see the evidence on a scope than to guess why you don't see anything.

Additionally, once the circuit is running, an optimized version of the standard product can be supplied by the inductor manufacturer. It's generally easier for the inductor manufacturer to modify its standard product than to start from scratch. The process of communicating and translating circuit performance requirements into inductor construction details is tricky. Using standard product as a starting point accelerates the dialogue, minimizing the number of iterations required for satisfactory results. Often, the standard product suffices for the purpose and no further effort is required.

Strictly speaking, it makes more sense to design the inductor to meet circuit requirements than to fashion a circuit around a standard inductor. Deliberately ignoring this consideration considerably complicated the author's work, but hopefully will simplify the reader's (such is the lot of an application note writer's life). Those interested in inductor design theory are commended to LTC Application Note AN-19, "LT1070 Design Manual."

*For recommended magnetics supplier, see page 13.

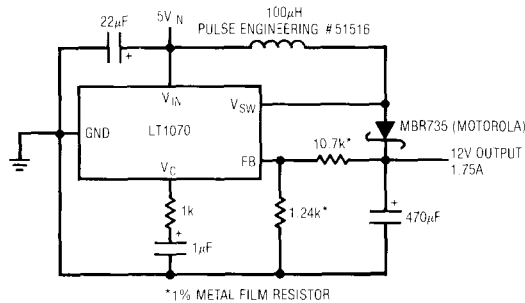


Figure 1. Flyback-Type Regulator

A final aid in achieving my new outlook on switchers was the LT1070 family. In terms of circuit construction and ease of use they really are superior switching regulator ICs. A 75V, 5A (LT1070HV) on-chip power switch, complete control loop, oscillator and only 5 pins eliminate a lot of the ambiguity of other devices. Internal details and operating features of the LT1070 family are detailed in Appendix A, "Physiology of the LT1070."

Basic Flyback Regulator

Figure 1 shows a basic flyback regulator using the LT1070. It converts a 5V input to a 12V output. Figure 2 shows the voltage (Trace A) and the current (Trace B) waveforms at the V_{SW} pin. The V_{SW} output is the collector of a common emitter NPN, so current flows when it is low. Current is pulled through the 100µH inductor and controlled to a value of which forces the 12V output to be constant. The circuit's 40kHz repetition rate is set by the LT1070's internal oscillator. During the time V_{SW} is low, current flow through the inductor causes a magnetic field to be induced into the area around the inductor. The amount of energy stored in this field is a function of the current level, how long current flows, the characteristics of the inductor and its core material. It is often useful to think of the inductor as a bucket and analogize current flow as water pouring into it. The ultimate limit on energy storage is set by the bucket's capacity, corresponding to the inductor's saturation limitations. The amount of energy that can be put into an inductor in a given time is limited by the applied voltage and the inductance. The amount of energy that can be stored without saturating the inductor is limited by the core characteristics. Size, core material, operating frequency, voltage and current influence inductor design.

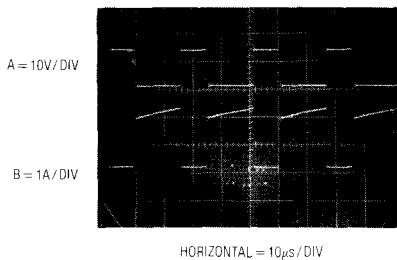


Figure 2. Flyback Regulator's Waveforms at 7W Loading

If the inductor is enclosed in a feedback-enforced loop, such as Figure 1, the energy put into it will be controlled to meet circuit output demands. Figure 3 shows what happens when output demand doubles. In this case duty cycle doesn't change much but current doubles. This requires the inductor to store more energy. If it couldn't meet the storage requirement, e.g., it saturated and could not hold any more magnetic flux, it would cease to look inductive. If this point is reached, current flow is limited only by the resistance of the wire and rapidly builds to excessive and destructive values. This behavior is exactly the opposite of a capacitor, where current diminishes upon entering saturation. Capacitors can maintain energy storage with no current flowing; inductors cannot. See Appendix C, "A Checklist for Switching Regulator Designs," for details.

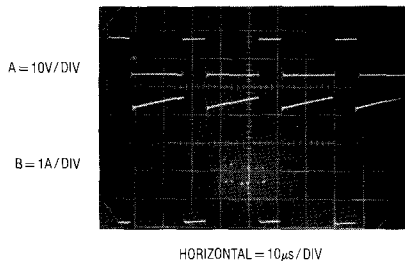


Figure 3. Flyback Regulator's Waveforms at 14W Loading

At the end of each inductor charge cycle, current flow in the inductor decays, and the magnetic field around it abruptly collapses. The V_{SW} pin is seen to rise rapidly to a voltage higher than the 5V input. This flyback action gives the regulator its voltage boost characteristics and its name. The boost characteristic is caused by the collapsing magnetic field's lines of flux cutting across the inductor's conductive wire turns. This satisfies the basic requirement for generation of a current in (and hence, a voltage across) a conductor. This moving magnetic field deposits energy into the wire in proportion to how much was stored in the core during the current charge cycle. It is worth noting that the operating characteristics shown here are similar to the Kettering ignition system used in automobiles, explaining why spark occurs when the points open.*

*Back when giants walked the earth, Real Cars used ignition points.

In this circuit the flyback is seen to clamp to a level just above the output voltage. This is so because the flyback pulse is steered through the Schottky diode to the output. The 470µF capacitor integrates the repetitive flyback events to DC, providing the circuit's output. The feedback pin (FB) samples this output via the 10.7k-1.24k divider. The LT1070 compares the feedback pin voltage to its internal 1.24V reference and controls the V_{SW} pin's duty cycle and current, closing a loop. Since the LT1070 is trying to force its feedback pin to 1.24V, output voltage may be set by varying the 10.7k or 1.24k values.

All feedback loops require some form of stability compensation (see the appended section of LTC Application Note AN-18, "The Oscillation Problem—Frequency Compensation Without Tears," for general discussion). The LT1070 is no exception. Its voltage gain characteristics, combined with the substantial phase shift of the circuit's sampled energy delivery, ensure oscillation if uncompensated. While the large output capacitor smooths the output to DC, it also teams up with the sampled energy coming into it to create phase shift. To complicate matters, the load, which may vary, also influences phase characteristics. The regulator can only source into the output capacitor. The load determines the sink time constant, influencing phase performance and overall stability.

The LT1070's internals have been designed with all this in mind and compensation is usually fairly simple. In this case the 1k-1µF combination at the compensation pin (V_C) rolls off the circuit, providing stable compensation for all operating conditions (see Appendix B, "Frequency Compensation," for details and suggestions on achieving stability in switching regulator loops).

As innocent as Figure 1 appears, it's not too difficult to get into odd and seemingly inexplicable problems. Note that the ground connection appears at the ground pin, as opposed to its customary location at the bottom of the diagram. This is deliberate and the supply and load return connections should be made there. The high speed, high current returns from the output transistor's emitter (the "other end" of the V_{SW} pin) should not be allowed to mix with the small currents of the output divider or the V_C pin.

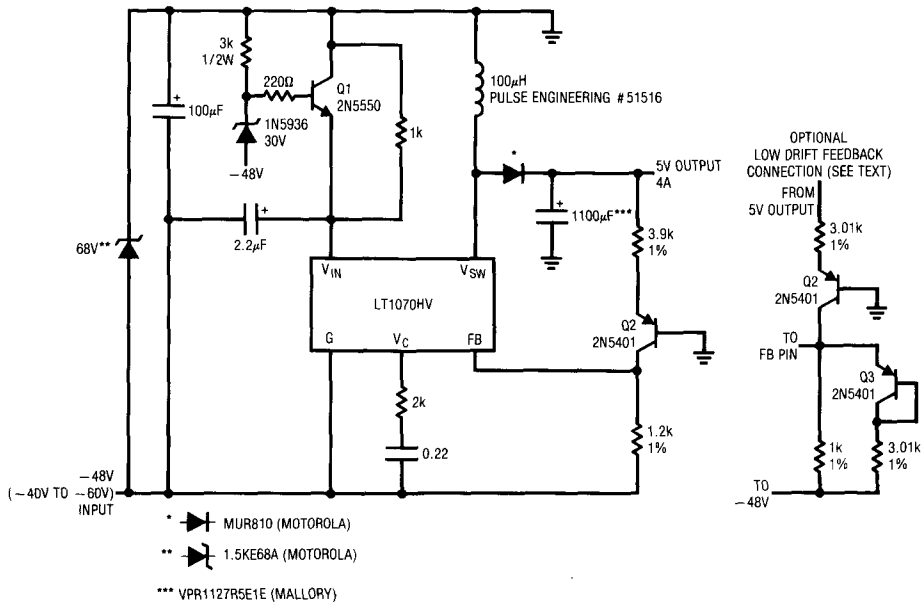


Figure 4. Non-Isolated -48V to 5V Regulator

Such mixing can promote poor regulation, unstable operation or outright oscillation. Similarly, the 22µF bypass capacitor ensures clean local power at the LT1070, even during the fast, high current drain periods when V_{SW} comes on. It should have good high frequency characteristics (tantalum or aluminum paralleled by a disc ceramic type). More discussion of these considerations appears in Appendix C.

-48V to 5V Telecom Flyback Regulator

Figure 4's circuit is operationally similar to Figure 1 but is intended for telecom applications. The raw telecom supply is nominally -48V but can vary from -40V to -60V. This range of voltages is acceptable to the V_{SW} pin but protection is required for the V_{IN} pin (V_{MAX} = 60V). Q1 and the 30V zener diode serve this purpose, dropping V_{IN}'s voltage to acceptable levels under all line conditions.

Here, the "top" of the inductor is at ground and the LT1070's ground pin at -48V. The feedback pin senses with respect to the ground pin, so a level shift is required from the 5V output. Q2 serves this purpose, introducing only -2mV/°C drift. This is normally not objectionable in a logic supply, but can be compensated with the optional appropriately scaled diode-resistor shown.

Frequency compensation is similar to Figure 1, although a low ESR (equivalent series resistance) capacitor gives less phase shift, permitting faster loop response with the reduced compensation time constant. The 68V zener is a type designed to clamp and absorb excessive line transients which might otherwise damage the LT1070 (V_{SW} maximum voltage is 75V).

Figure 5 shows operating waveforms at the V_{SW} pin. Trace A is the voltage and Trace B the current. Switching

characteristics are fast and clean. The ripples in the current trace are due to nonoptimal breadboard layout (ground as I say, not as I do). Inductor ringing on turn-off (Trace A) is characteristic of flyback configurations.

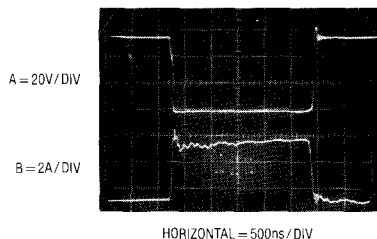


Figure 5. Non-Isolated Regulator's Waveforms

Fully-Isolated Telecom Flyback Regulator

Figure 6's circuit is another telecom regulator. Although it looks more complex, it's really a closely related extension of the previous flyback circuits. The fundamental difference is that the output is fully galvanically isolated from the input, often a requirement in equipment. This necessitates a transformer instead of a simple 2-terminal inductor. It also requires output feedback information to be transmitted to the regulator across a non-conducting path. The transformer complicates the circuit's start-up and switching characteristics while the isolated feedback requires attention to frequency compensation.

In this circuit the V_{IN} pin receives power from a transformer winding. This winding cannot supply power at start-up because the circuit is nonfunctional. Q1 through Q4 address this issue. When power is applied, Q5 cannot conduct because the LT1071 is unpowered. Q1, zener-connected Q2, and Q3 are off. Under these conditions Q4 is on, pulling the V_C pin down and strobing off the LT1071. The potential at Q1's emitter slowly rises as the 10k-100 μ F combination charges. When Q1's emitter rises high enough, it turns on. Zener-connected Q2 conducts when the voltage across it is about 7V, biasing Q3 on. Q1 sees regenerative feedback, turning Q3 on harder. Q3's turn-on cuts off Q4, allowing the V_C pin to rise and biasing up the LT1071. The rate of rise is limited by the 10 μ F-diode combination at the V_C pin. This network forces the V_C pin to come up slowly, providing a soft-start characteristic (the 100 Ω -diode string discharges the 10 μ F capacitor when circuit input power is removed). Because of this sequence,

the LT1071 cannot start up the circuit until the V_{IN} potential is well established. This prevents start-up at "starved" or unstable V_{IN} voltages which could cause erratic or destructive modes. When start-up does occur, the transformer feeds the V_{IN} pin with DC via the MUR120 diode. The 50 Ω resistor combines with the 100 μ F capacitor to give good ripple and transient filtering. This voltage is ample to run the LT1071 and reduces the current through the 10k resistor, saving power. Q1, Q2 and Q3 remain on, biasing Q4 to allow LT1071 operation.

In the previous flyback circuits, the V_{SW} pin drove the inductor directly. Here, a power MOSFET is interposed between the V_{SW} pin and the inductor. In this arrangement the inductor is a transformer and its flyback characteristics are different from a simple 2-terminal inductor. For the simple inductor, the flyback energy was clamped by and dumped directly into the output capacitor. Excessive voltages did not occur. In the transformer case, all the flyback energy does not end up in the output capacitor. Substantial flyback voltage spikes (>100V) appear across the transformer primary when the LT1071 driven MOSFET turns off.

Several measures prevent these spikes from destroying the circuit. The 0.47 μ F-2k-diode combination, a damper network, conducts during the flyback event. This loads the transformer primary, minimizing flyback amplitude. The damper values are selected empirically, with the trade-off being power dissipation in them. Very low values markedly reduce flyback potentials but cause excessive dissipation. High values permit low dissipation but allow excessive flyback voltages. The damper values should be selected under fully-loaded output conditions because flyback energy is proportionate to transformer power levels. Appendix C contains additional information on damper network considerations.

Even with the damper network, the flyback voltage is too high for the LT1071 output transistor. Q5 prevents the LT1071 from seeing the high voltage. It is connected in series with the LT1071's output transistor. This connection, sometimes called a cascode, lets Q5 stand off the high voltage and the LT1071 operates well within its breakdown limits. Development and testing of this configuration is detailed in Appendix D. Q5 has large parasitic

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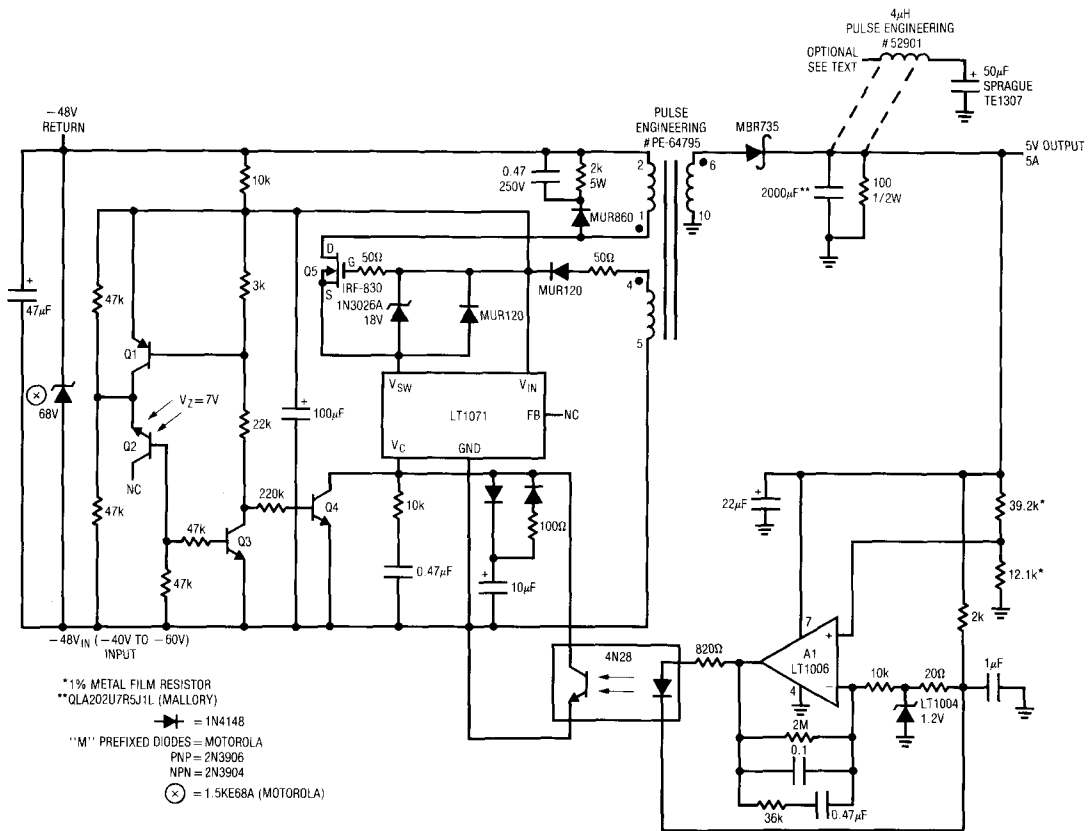


Figure 6. Fully Isolated - 48V to 5V Regulator

capacitances associated with all terminals. During switching, these capacitances can cause excessive transient voltages to appear. The 18V zener diode insures against gate-source breakdown ($V_{GSMAX} = 20V$) and the diode clamps the V_{SW} pin to the V_{IN} potential. Mention of these considerations appears in Appendix C.

The transformer's rectified and filtered secondary produces the 5V output. This output is galvanically isolated from the circuit's input. To preserve this desired feature, the feedback path must also be galvanically isolated. A1, the opto-isolator, and their associated components serve this function. A1, powered by the 5V output, compares a resistively-sampled portion of the output with the LT1004 1.2V reference. Operating at a gain of 200, it drives the

opto-isolator's LED. The opto-isolator's output transistor biases the LT1071's V_C pin, closing a regulation loop. The feedback amplifier inside the LT1071 is essentially bypassed by the A1-opto-isolator combination and is not used. Normally, the opto-isolator's drift transmission characteristics over time and temperature would result in unstable feedback. Here, A1's gain is placed ahead of the opto-isolator. This attenuates these uncertainties, providing a stable loop. This approach is not too different from inside-the-loop booster resistors and buffers used with op amps. Both schemes rely on the op amp's gain to eliminate uncertainties and drifts. Returning the opto-isolator to V_{REF} instead of ground forces the op amp to bias well above ground, minimizing saturation effects during output transients.

Frequency compensation is somewhat more involved in this circuit than the previous examples. A1 is rolled off by the $0.1\mu\text{F}$ unit. This keeps gain low at high frequency, preventing amplified ripple and noise from being fed back to the LT1071. Local compensation at the LT1071 V_C pin stabilizes the loop. The 100Ω resistor at the 5V output, a deliberate sink path, allows loop stability at light or no load. Appendix B discusses frequency compensation.

Additional transformer secondary windings could be added if desired. The input zener clips transient voltages.

Circuit waveforms appear in Figure 7. Trace A is Q5's drain voltage and Trace B the drain current. Trace A shows that the MOSFET sees about 100V due to flyback effects, but this is well within its rating. The ringing on turn-off is normal and is similar to the waveform observed in Figure 4's circuit. Trace B shows that the current flow is fast, clean and controlled. Figure 8 shows transient response for a 1A step on a 2.5A output. When Trace A goes high the step occurs. Trace B shows that output sag is corrected in about 8ms. When Trace A returns low the 1A load is removed and recovery is similar to the positive step. Broadband output noise, about 75mVp-p, may be reduced with the optional filter shown.

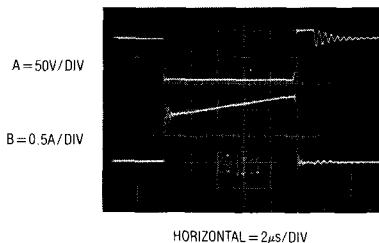


Figure 7. Fully Isolated Regulator's Waveforms

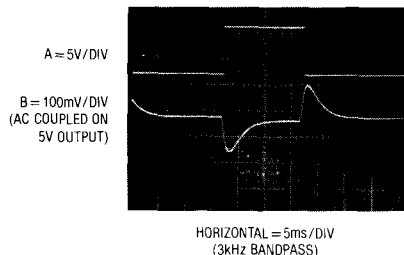


Figure 8. Fully Isolated Regulator's Transient Response for a 1A Change on a 2.5A Load

100W Off-Line Switching Regulator

One of the most desirable switching regulator circuits is also one of the most difficult to design. Figure 9's circuit has many similarities to the previous design but is powered directly from the 115VAC line. This off-line operation is desirable because it eliminates large, heavy and inefficient 60Hz magnetics and filter capacitors. The circuit provides an isolated 5V, 20A output as well as isolated $\pm 12\text{V}$, 1A outputs. Additional features include operation over a 90VAC-140VAC input range, AC line surge suppression, soft-starting and loop stability under all conditions. Efficiency exceeds 75%.

BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF THIS CIRCUIT. HIGH VOLTAGE, AC LINE-CONNECTED POTENTIALS ARE PRESENT IN THIS CIRCUIT. EXTREME CAUTION MUST BE USED IN WORKING WITH AND MAKING CONNECTIONS TO THIS CIRCUIT. REPEAT: THIS CIRCUIT CONTAINS DANGEROUS, AC LINE-CONNECTED HIGH VOLTAGE POTENTIALS. USE CAUTION.

AC line power is rectified and filtered by the diode bridge-470 μF combination. The MOV device provides surge suppression and the thermistor limits turn-on in-rush current. Start-up and soft-start circuitry is similar to Figure 6's circuit, with some changes necessitated by the higher input voltage. Erratic operation at extremely low AC line voltages (70VAC) is prevented by the 220k-1.24k divider. At very low AC line inputs, this divider forces the LT1071 feedback pin to a low state, shutting down the circuit. The high input voltage, typically 160VDC, means that the LT1071's internal current limit is set too high to protect the regulator if the circuit's output is shorted. Q6 and its associated components provide about 2A limiting. The LT1071's ground pin current flows through the 0.3Ω resistor, turning on Q6 if current is too high. The 22k-50pF RC filters noise, preventing erratic Q6 operation.

Q5, a power MOSFET, is cascoded with the LT1071 for high voltage switching. Circuit topology is similar to Figure 6, with Q5's voltage breakdown increased to 500V.

Figure 10 shows circuit waveforms at 15A output. Trace A, Q5's drain, shows the flyback pulse being damped below 300V (for a discussion of the procedures used to design the damper network and other design techniques in this circuit, see Appendix D, "Evolution of a Switching Regulator Design"). Trace B, the LT1071's V_{SW} pin, stays well within its voltage rating, despite Q5's high voltage switching. Trace C, Q5's drain current, shows that transformer current is well-controlled with no saturation effects. Trace D, damper network current, is active when Q5 goes off.

Figure 11 is a time and amplitude expansion of Q5's drain (Trace A) and transformer primary current (Trace B). Switching is clean, with residual noise due to non-ideal transformer behavior. The damper network clamps the fly-

back pulse well below Q5's 500V rating and the transformer rings off after the flyback interval. The noise on the current pulse, due to resonances in the transformer, has no significant effect on circuit operation.

Figure 12 shows output noise with the optional LC filter in use. Without the filter, noise is about 150mV. Superimposed, residual 120Hz modulation accounts for trace thickening at the peaks and could be eliminated by increasing the 470 μ F value.

Figure 13 shows transient response performance. When Trace A goes high, a 5A transient is added to a 10A steady-state load. Recovery amplitude is low and clean with a first order response. When Trace A goes low, the transient load is removed with similar results.

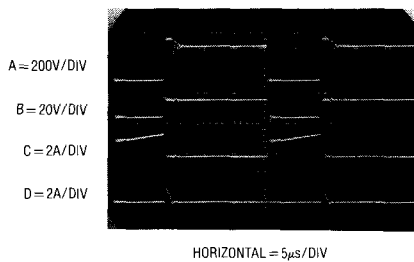


Figure 10. Off-Line Switcher's Waveforms
DANGER! Take This Measurement Only With an Isolation Transformer in Use—See Text

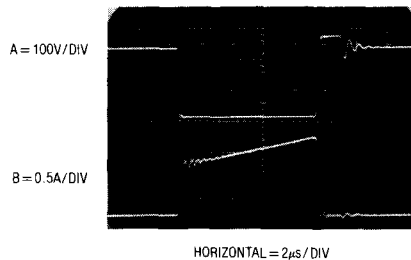


Figure 11. Detail of Off-Line Switcher's Transformer Primary Voltage and Current Waveforms
DANGER! Take This Measurement Only With an Isolation Transformer in Use—See Text

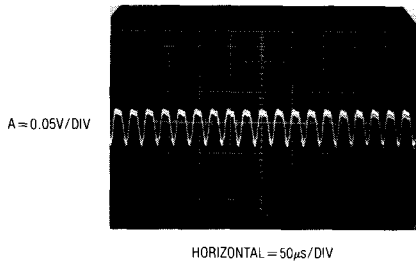


Figure 12. Figure 9's Output Ripple at 10A Output with the Optional LC Filter Added—Without the Filter, Ripple Increases to About 150mVp-p

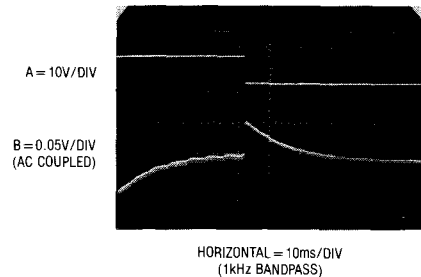


Figure 13. Figure 9's Circuit Responding to a 5A Change on a 10A Output

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Figure 14 shows response for shifts in the line. When Trace A is high, the AC line is at 140VAC. Line voltage drops to 90VAC with Trace A low. Trace B, the regulator's AC-coupled output, shows a clean recovery with small amplitude error. The ripples in the waveform, 120Hz input residue, could be reduced by increasing the 470 μ F capacitor.

Figure 15 shows the 5V output at start-up into a 20A load. Response is slightly underdamped and can be modified by adjusting the frequency compensation. The compensation shown in Figure 9 is a good compromise between transient response and turn-on characteristics. The delay on turn-on and the controlled rise time are due to the slow-start circuitry.

Figure 16 plots regulator efficiency. As would be expected, efficiency is best at high currents, where static losses are a small percentage of output power.

Switch-Controlled Motor Speed Controller

Voltage regulators are not the only switching power circuits. Figure 17 shows a motor speed regulator. The LT1070 provides simplicity and switch-mode control efficiency. Although this circuit controls a motor, it shares many considerations common to voltage regulators. When power is applied, the tachometer output is zero and the feedback pin (FB) is also at zero. This causes the LT1070 to begin pulsing its V_{SW} pin at maximum duty cycle. The

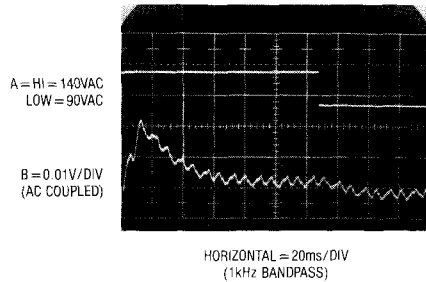


Figure 14. Figure 9 Responds to a 90VAC—140VAC Line Change—Loading is 10A—120Hz Residue in Output Could be Reduced by Increasing the 470 μ F Input Filter

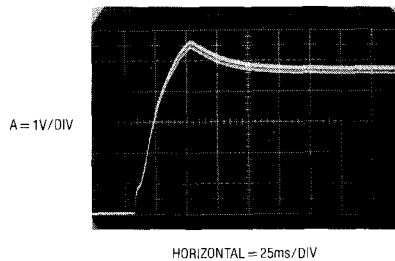


Figure 15. Start-Up for Figure 9 at 20A Loading—The 10 μ F Capacitor at the LT1070's V_C Pin Produces the Slow-Start Characteristic. If the Small Overshoot is Objectionable, Modified Frequency Compensation Can Eliminate it at Some Cost to Transient Response

motor turns, forcing tachometer output. When the FB pin arrives at the LT1070's internal voltage reference value (1.24V), the loop stabilizes. Speed is adjustable with the 25k potentiometer in the feedback string. The MUR120 damps the motor's flyback spike. The characteristics of the motor specified permit no current limiting in series

with the diode. Other motors might require this and damper network optimization should be done for any specific unit. Similarly, frequency compensation values will vary with different motor types. The diode at the tachometer output prevents transient reverse voltages due to tachometer commutator switching.

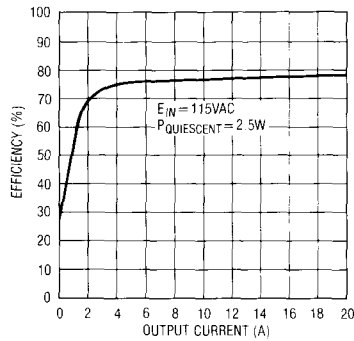


Figure 16. Figure 9's Efficiency vs Operating Point

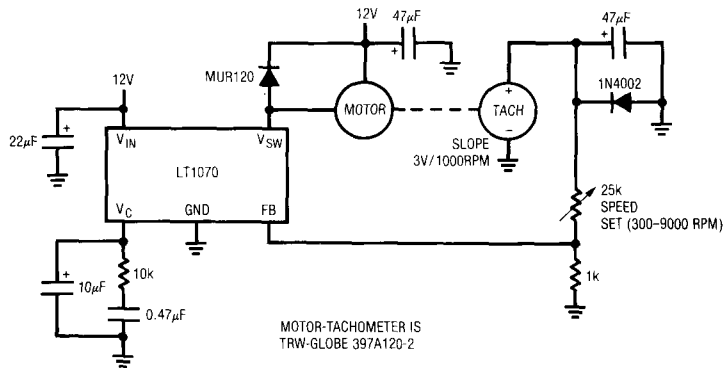


Figure 17. A Simple Motor-Tachometer Servo Loop

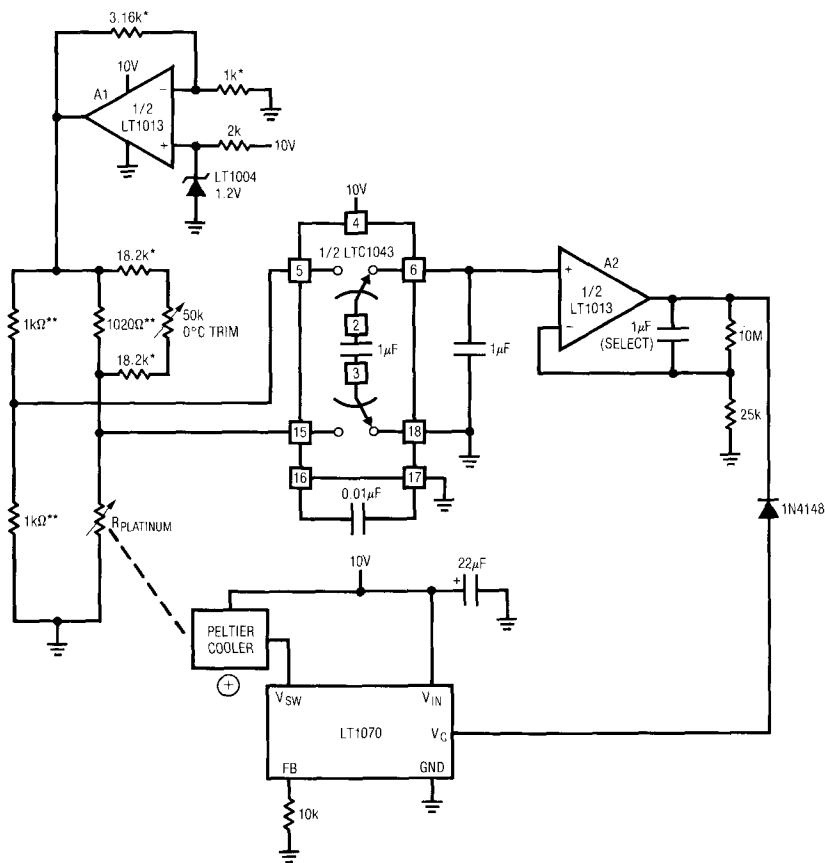
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Switch-Controlled Peltier 0°C Reference

Figure 18 is another switch-mode control circuit. Here, the LT1070 controls power to a Peltier cooler, providing a 0°C temperature reference for transducer calibration.

A platinum RTD is thermally mated to the Peltier cooler. The RTD combines with a bridge network to give a differential output. A1 provides maximum bridge drive without introducing significant heating in the RTD. The LTC1043 switched capacitor network converts this output to a single-ended signal at A2. A2, operating at a gain of

400, biases the LT1070's V_C pin. This closes a control loop around the Peltier cooler, forcing its temperature low enough to balance the bridge. The 0°C trim adjusts the servo point to precisely 0°C. A standard RTD should monitor Peltier temperature when making this trim. Alternately, the sensor specified should be supplied with a certified 0°C resistance. With the RTD and Peltier cooler tightly mated, stability is excellent. Figure 19, a plot of stability over hours in a $25^\circ\text{C} \pm 3^\circ\text{C}$ ambient, shows a 0.15°C baseline.



* 1% METAL FILM RESISTOR
 ** ULTRONIX 105A 0.1%
 R_{PLATINUM} = ROSEMOUNT # 118ME-1k at 0°C
 ⊕ = PELTIER COOLER = CAMBION # 801-2003-01-00-00

Figure 18. A Peltier-Cooled Switched-Mode 0°C Reference

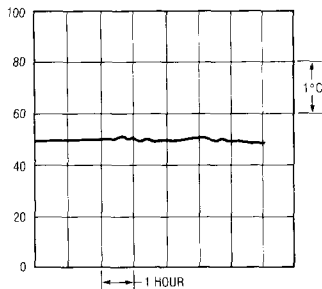


Figure 19. Stability of Figure 18's Circuit Over Many Hours with a $25^{\circ}\text{C} \pm 3^{\circ}\text{C}$ Ambient

Acknowledgements

The author acknowledges Carl Nelson's abundance of commentary, some of which was useful, during preparation of this work. Bob Dobkin's thoughts and patience are also appreciated. Ron Young made significant contributions towards Figure 6's circuit. Bill McColey and other members of the Engineering staff of Pulse Engineering, Inc.*, supplied invaluable insight and assistance on magnetics issues. As usual, our customers' requests and requirements provided the most valuable source of guidance, and they are due a special thanks.

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APPENDIX A

Physiology of the LT1070

The LT1070 is a current-mode switcher. This means that switch duty cycle is directly controlled by switch current rather than by output voltage. Referring to Figure A1, the switch is turned on at the start of each oscillator cycle. It is turned off when switch current reaches a predetermined level. Control of output voltage is obtained by using the output of a voltage-sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike ordinary switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at mid-frequencies in the energy storage inductor. This greatly simplifies closed loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short conditions. A low dropout internal regulator provides a 2.3V supply for all internal circuitry on the LT1070. This low dropout design allows input voltage to vary from 3V to 6V with virtually no change in device performance. A 40kHz oscillator is the basic clock for all internal timing. It turns on the output switch via the logic and driver circuitry. Special adaptive antisat circuitry detects onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

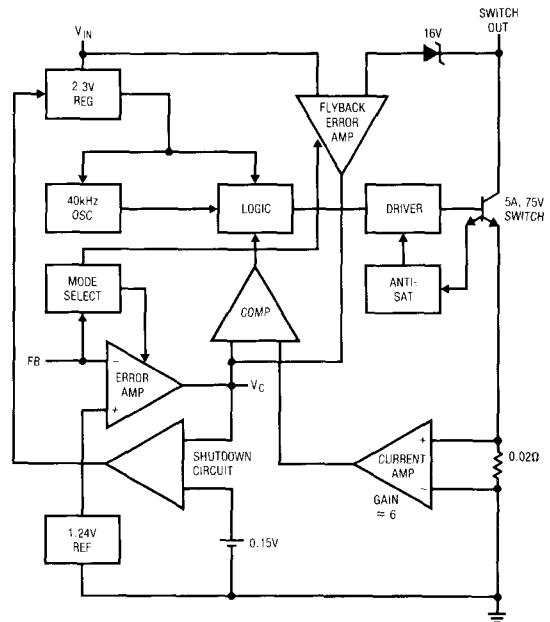


Figure A1. LT1070 Internal Details

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A 1.2V bandgap reference biases the positive input of the error amplifier. The negative input is brought out for output voltage sensing. This feedback pin has a second function; when pulled low with an external resistor, it programs the LT1070 to disconnect the main error amplifier output and connects the output of the flyback amplifier to the comparator input. The LT1070 will then regulate the value of the flyback pulse with respect to the supply voltage. This flyback pulse is directly proportional to output voltage in the traditional transformer-coupled flyback topology regulator. By regulating the amplitude of the flyback pulse the output voltage can be regulated with no direct connection between input and output. The output is fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings. A special delay network inside the LT1070 ignores the leakage inductance spike at the leading edge of the flyback pulse to improve output regulation.

The error signal developed at the comparator input is brought out externally. This pin (V_C) has four different functions. It is used for frequency compensation, current limit adjustment, soft-starting, and total regulator shutdown. During normal regulator operation this pin sits at a voltage between 0.9V (low output current) and 2.0V (high output current). The error amplifiers are current output (gm) types, so this voltage can be externally clamped for adjusting current limit. Likewise, a capacitor-coupled external clamp will provide soft-start. Switch duty cycle goes to zero if the V_C pin is pulled to ground through a diode, placing the LT1070 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown with only 50 μ A supply current for shutdown circuitry biasing. For more details, see Linear Technology Application Note AN-19, pages 4-8.

APPENDIX B

Frequency Compensation

Although the architecture of the LT1070 is simple enough to lend itself to a mathematical approach to frequency compensation, the added complications of input and/or output filters, unknown capacitor ESR, and gross operating point changes with input voltage and load current variations all suggest a more practical empirical method. Many hours spent on breadboards have shown that the simplest way to optimize the frequency compensation of the LT1070 is to use transient response techniques and an R/C box to quickly iterate toward the final compensation network.

There are many ways to inject a transient signal into a switching regulator, but the suggested method is to use an AC-coupled output load variation. This technique avoids problems of injection point loading and is general to all switching topologies. The only variation required may be an amplitude adjustment to maintain small signal conditions with adequate signal strength. Figure B1 shows the set-up.

A function of generator with 50 Ω output impedance is coupled through a 50 Ω /1000 μ F series RC network to the regulator output. Generator frequency is non-critical. A good starting point is 50Hz. Lower frequencies may cause a blinking scope display which is annoying to work with. Higher frequencies may not allow sufficient settling time for the output transient. Amplitude of the generator output is typically set at 5Vp-p to generate a 100mA-p-p load variation.

For lightly loaded output ($I_{OUT} < 100$ mA), this level may be too high for small signal response. If the positive and negative transition settling waveforms are significantly different, amplitude should be reduced. Actual amplitude is not particularly important because it is the shape of the resulting regulator output waveform that indicates loop stability.

A 2-pole oscilloscope filter with $f = 10$ kHz is used to block switching frequencies. Regulators without added LC output filters have switching frequency signals at their outputs which may have much higher amplitude than the low frequency settling waveform to be studied. The filter frequency is high enough to pass the settling waveform with no distortion.

Oscilloscope and generator connections should be made exactly as shown to prevent ground loop errors. The oscilloscope is synced by connecting the channel B probe to the generator output, with the ground clip of the second probe connected to exactly the same place as the channel A ground. The standard 50Ω BNC sync output of the generator should not be used because of ground loop errors. It may also be necessary to isolate either the generator or oscilloscope from its third wire (earth ground) connection in the power plug to prevent ground loop errors in the scope display. These ground loop errors are checked by connecting the channel A probe tip to exactly the same point as the probe ground clip. Any reading on channel A indicates a ground loop problem.

Once the proper set-up is made, finding the optimum values for the frequency compensation network is fairly straightforward. Initially, C2 is made large ($\geq 2\mu\text{F}$), and R3 is made small ($\approx 1\text{k}\Omega$). This nearly always ensures that the regulator will be stable enough to start iteration. Now, if the regulator output waveform is single-pole overdamped (see the waveforms in Figure B2), the value of C2 is reduced in steps of about 2:1 until the response becomes slightly underdamped. Next, R3 is increased in steps of 2:1 to introduce a loop "zero." This will normally improve damping and allow the value of C2 to be further reduced. Shifting back and forth between R3 and C2 variations will now allow one to quickly find optimum values.

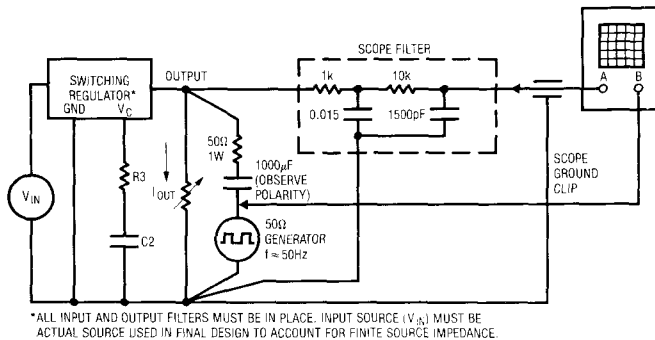


Figure B1. Testing Loop Stability

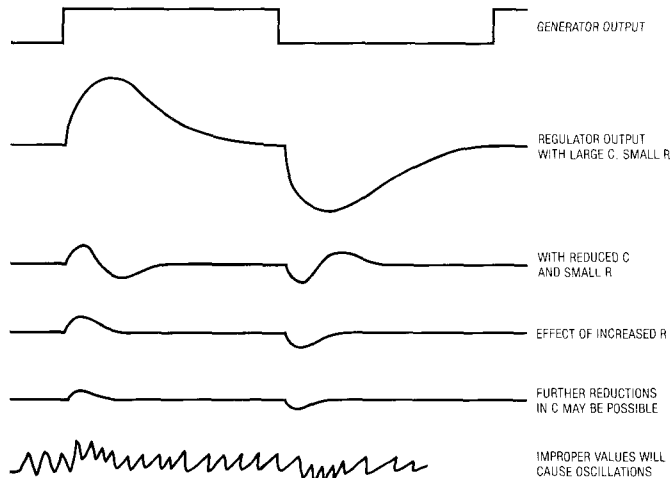


Figure B2. Output Transient Response

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If the regulator response is underdamped with the initial large value of C, R should be increased immediately before larger values of C are tried. This will normally bring about the overdamped starting condition for further iteration.

Just what is meant by "optimum values" for R3 and C2? This normally means the smallest value for C2 and the largest value for R3, which still guarantee no loop oscillations, and which result in loop settling that is as rapid as possible. The reason for this approach is that it minimizes the variations in output voltage caused by input ripple voltage and output load transients. A switching regulator which is grossly overdamped will never oscillate but it may have unacceptably large output transients following sudden changes in input voltage or output loading. It may also suffer from excessive overshoot problems on start-up or short circuit recovery.

To guarantee acceptable loop stability under all conditions, the initial values chosen for R3 and C2 should be checked under all conditions of input voltage and load current. The simplest way to accomplish this is to apply load currents of minimum, maximum, and several points in-between. At each load current, input voltage is varied from

minimum to maximum while observing the settling waveform. The additional time spent "worst-casing" in this manner is definitely necessary. Switching regulators, unlike linear regulators, have large shifts in loop gain and phase with operating conditions. If large temperature variations are expected for the regulator, stability checks should also be done at the temperature extremes. There can be significant temperature variations in several key component parameters which affect stability—in particular, input and output capacitor values and their ESRs, and inductor permeability. The LT1070 parametric variations also need some consideration. Those which affect loop stability are error amplifier gm, and the transfer function of V_C pin voltage versus switch current (listed as a transconductance under electrical specifications.) For modest temperature variations, conservative overdamping under worst-case temperature conditions is usually sufficient to guarantee adequate stability at all temperatures.

If external amplifiers or other active devices are included in the loop (e.g., Figure 6 and 9), their effects must be included in stabilizing the loop. LTC Application Note 18, pages 12-15, provides commentary that may be useful in these situations.

APPENDIX C

A Checklist for Switching Regulator Designs

1. The most common problem area in switching designs is the inductor and the most common difficulty is saturation. An inductor is saturated when it cannot hold any more magnetic flux. As an inductor arrives at saturation it begins to look more resistive and less inductive. Under these conditions the current flow through it is limited only by its DC copper resistance and the source capacity. This is why saturation often results in destructive failures. Test circuit C1 demonstrates saturation effects. The pulse generator drives Q1, forcing current into the inductor. The diode and RC combination form a typical load. Figure C2 shows results. The voltage at Q1's collector falls when it turns on (Trace A is pulse generator output, Trace B is Q1's collector). Trace C, the inductor current, ramps in controlled fashion. When Q1 goes off, current falls

and the inductor rings off. In C3, drive pulse width is longer, allowing more inductor current build-up. This requires the inductor to store more magnetic flux. Its ramp waveform is clean and controlled, indicating that it has the necessary capacity. Figure C4 brings some unpleasant surprises. Drive pulse width has been increased. Now, the inductor current departs from its ramp characteristic into a non-linear slope. The non-linear behavior starts between the third and fourth vertical divisions. This curve shows a rapidly increasing current characteristic. These conditions indicate that the inductor is entering saturation. If pulse width is increased much more, the current will rise to destructive levels. It is worth noting that some inductors saturate much more abruptly than this case.

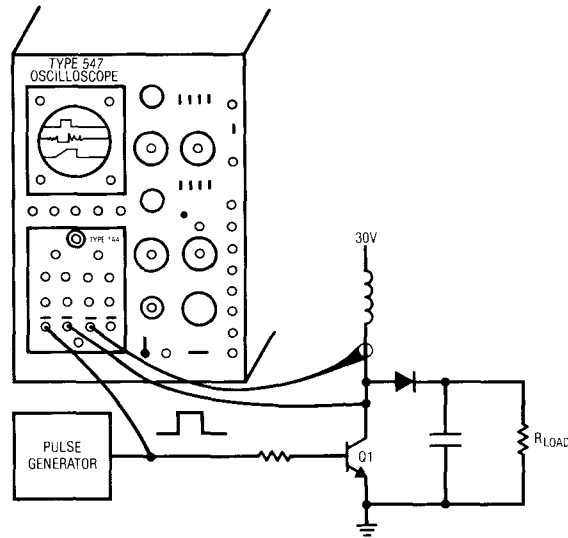


Figure C1. Inductor Saturation Test Circuit

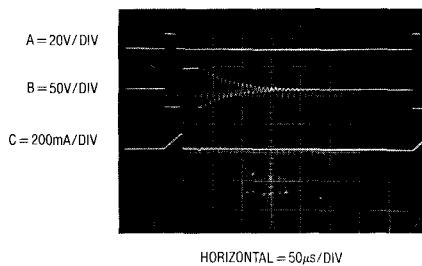


Figure C2. Normal Inductor Operation

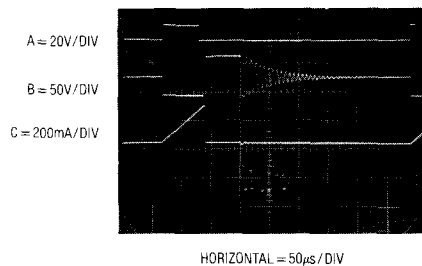


Figure C3. Normal Inductor Operation at Increased Current

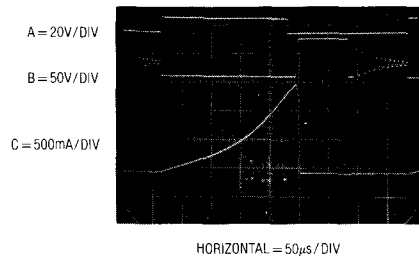


Figure C4. Inductor Being Driven into Saturation

Application Note 25

2. Always consider inductive flyback effects. Are semiconductor breakdown ratings adequate to withstand them? Is a snubber (damper) network required? Consider all possible voltages and current paths, including the transient ones via semiconductor junction capacitances, to avoid evil problems.
3. Think about requirements in capacitors. All operating conditions should be accounted for. Voltage rating is the most obvious consideration, but remember to plan for the effects of equivalent series resistance (ESR) and inductance. These specifications can have significant impact on circuit performance. In particular, an output capacitor with high ESR can make loop compensation difficult.
4. Layout is vital. Don't mix signal, frequency compensation, and feedback returns with high current returns. Arrange the grounding scheme for the best compromise between AC and DC performance. In many cases, a ground plane may help. Account for possible effects of stray inductor-generated flux on other components and plan layout accordingly.
5. Semiconductor breakdown ratings must be thought through. Account for all conditions. Transient events usually cause the most trouble, introducing stresses that are often hard to predict. Things to watch for include effects of feedthrough via semiconductor junction capacitances (note the clamping of Q5's gate in Figures 6 and 9). Such capacitances can allow excessive voltages to occur for brief durations at what is nominally a low voltage node. Study the data sheet breakdown, current capacity, and switching speed ratings carefully. Were these specifications written under the same conditions that your circuit is using the device in? If in doubt, consult the manufacturer.

"Simple" diodes furnish a good example of how carefully semiconductor operating conditions must be considered in switching regulators. Switching diodes have two important transient characteristics—reverse recovery time and forward turn-on time. Reverse recovery time occurs because the diode stores charge during its forward conducting cycle. This stored charge causes the diode to act as a low impedance conductive element for a short period

of time after reverse drive is applied. Reverse recovery time is measured by forward biasing the diode with a specified current, then forcing a second specified current backwards through the diode. The time required for the diode to change from a reverse conducting state to its normal reverse non-conducting state is reverse recovery time. Hard turn-off diodes switch abruptly from one state to the other following reverse recovery time. They therefore dissipate very little power even with moderate reverse recovery times. Soft turn-off diodes have a gradual turn-off characteristic that can cause considerable diode dissipation during the turn-off interval. Figure C5 shows typical current and voltage waveforms for several commercial diode types used in an LT1070 flyback converter with $V_{IN} = 10V$, $V_{OUT} = 20V$, 2A.

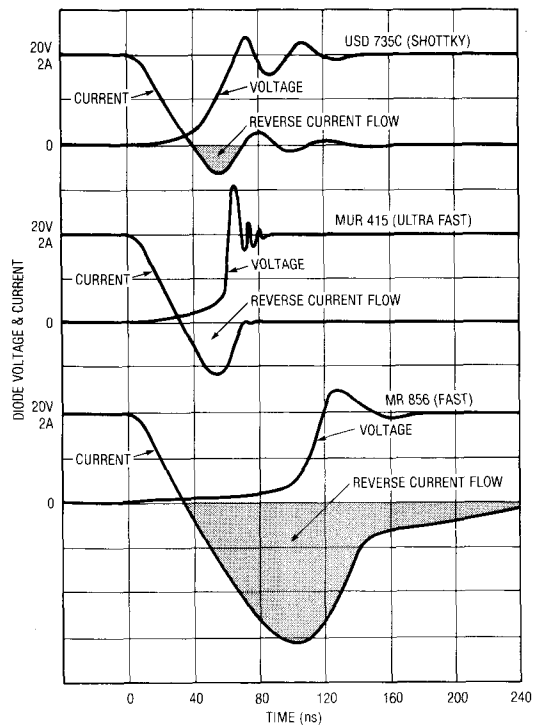


Figure C5. Diode Turn-Off Characteristics

Long reverse recovery times can cause significant extra heating in the diode or the LT1070 switch. Total power dissipated is given by:

$$P_{trr} = V \times f \times t_{RR} \times I_F$$

V = reverse diode voltage

f = LT1070 switching frequency

t_{RR} = reverse recovery time

I_F = diode forward current just prior to turn-off.

With the circuit mentioned, I_F is 4A, $V = 20V$, and $f = 40kHz$. Note that diode on current is twice output current for this particular boost configuration. A diode with $t_{rr} = 300ns$ creates a power loss of:

$$P_{trr} = (20)(40 \times 10^3)(300 \times 10^{-6})(4) = 0.96W$$

If this same diode had a forward voltage of 0.8V at 4A, its forward loss would be 2A (average current) times 0.8V equals 1.6W. Reverse recovery losses in this example are nearly as large as forward losses. It is important to realize, however, that reverse losses may not necessarily increase diode dissipation significantly. A hard turn-off diode will shift much of the power dissipation to the LT1070 switch, which will undergo a high current and high voltage condition during the duration of reverse recovery time. This has not been shown to be harmful to the LT1070, but the power loss remains.

Diode turn-on time can potentially be more harmful than reverse turn-off. It is normally assumed that the output diode clamps to the output voltage and prevents the inductor or transformer connection from rising higher than the output. A diode that turns on slowly can have a very high forward voltage for the duration of turn-on time. The problem is that this increased voltage appears across the LT1070 switch. A 20V turn-on spike superimposed on a 40V flyback mode output pushes switch voltage perilously close to the 65V limit. The graphs in Figure C6 show diode

turn-on spikes for three common diode types—fast, ultra-fast, and Schottky. The height of the spike will be dependent on rate of rise of current and the final current value, but these graphs emphasize the need for fast turn-on characteristics in applications which push the limits of switch voltage.

Fast diodes can be useless if the stray inductance is high in the diode, output capacitor or LT1070 loop. 20-gauge hook-up wire has 30nH/inch inductance. The current fall time of the LT1070 switch is $10^8 A/sec$. This generates a voltage of $(10^8)(30 \times 10^{-9}) = 3V$ per inch in stray wiring. Keep the diode, capacitor and LT1070 ground/switch lead lengths *short!*

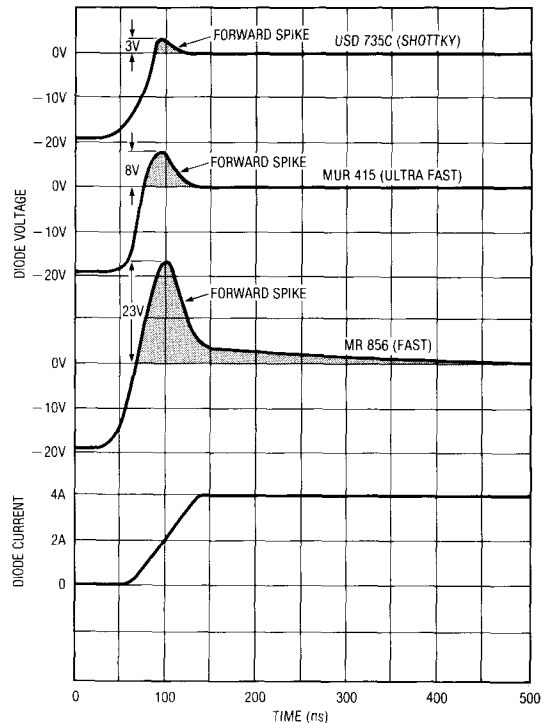


Figure C6. Diode Turn-On Spike

Application Note 25

APPENDIX D

Evolution of a Switching Regulator Design

A good way to approach designing a switching regulator is to break the problem into small tasks and then integrate everything. The combination of inductors, a sampled feedback loop, and high speed currents and voltages leaves much room for confusion. The approach used in Figure 9's design is illustrated as an example of an iterative approach in switching regulator design. This off-line circuit features high power, an isolated feedback loop and the aforementioned complexities. Any attempt to get everything working on the first try is beyond risky.

The transformer drive is the most critical part of Figure 9's design. Fast switching of over 100W at high voltage requires care. In particular, two issues must be addressed. Will the high voltage FET-LT1071 cascode connection really work? What amplitudes of flyback voltage are going to occur and what will their effects be?

Figure D1 begins the investigation. This test circuit allows checking of the high voltage cascode. To start, a resistive load is used, eliminating the possible (certain!) complications of the inductive load. Figure D2 shows waveforms. Switching is clean. Trace A is the FET drain, while Trace B is the LT1071 V_{SW} pin. Drain current appears in Trace C. Pulse width is kept deliberately low, minimizing load power dissipation. Everything appears well ordered, and the LT1071 V_{SW} pin does not see any high voltage excursions. Artifacts of the MOSFET's high voltage switching do, however, appear at the LT1071 V_{SW} pin. On the falling edge, the ringing appears, albeit at lower amplitude. The rising edge shows a slight peaking. These effects are due to the high voltage coupling through the MOSFET's junction capacitances. The diode clamps the source to 10V, but the effects of the high voltage slewing are still noticeable. This doesn't cause much trouble with the resistive load, but what will happen with the inductor's higher flyback voltages?

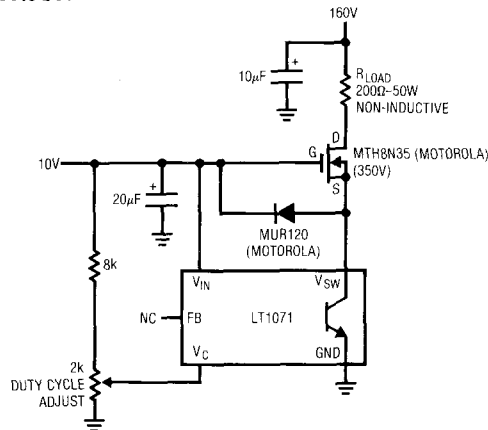


Figure D1. Test Circuit for MOSFET-LT1071 Cascode with Resistive Load

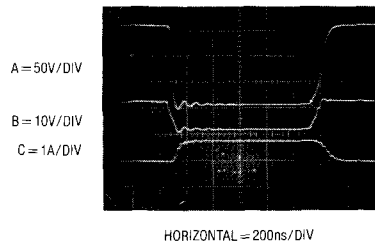


Figure D2. Testing the MOSFET-LT1071 Cascode Switch with a Resistive Load

Figure D3 shows the test circuit rearranged to accommodate the transformer load. The transformer replaces the resistor. Its terminated secondary allows it to present a significant load. The fixed 160V supply has been replaced with a 0V–200V unit, permitting voltage to be slowly and cautiously increased (“For fools rush in where angels fear to tread”—An Essay on Criticism, A. Pope). The 350V transistor is replaced with a 1000V unit, in preparation for inductive events. Figure D4 shows waveforms. As expected, the inductive flyback (Trace A) is significant, even at low supply voltage ($V_{SUPPLY}=60V$ in this photo).

Trace C, the drain current, rises with a characteristic indicating the inductive load. Trace B, the source voltage, is of greater concern. The flyback event, feeding through the MOSFET’s capacitances, causes the source (and gate) to rise above nominal clamped value. At the higher supply voltages planned, this could cause excessive gate-source voltages with resultant device destruction. Because of this, the zener diode in dashed lines is installed, clamping gate-source voltages to safe values. This component appears in Figure 9’s final design. With this correction, behavior at higher supply voltages may be investigated.

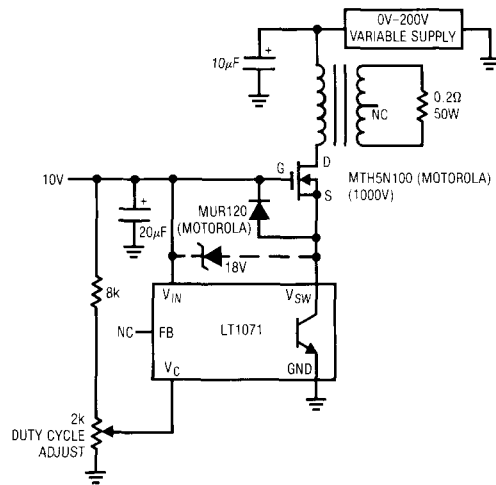


Figure D3. Test Circuit for MOSFET-LT1071 Cascode with Transformer Load

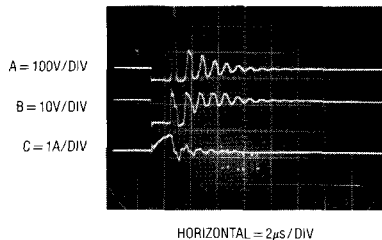
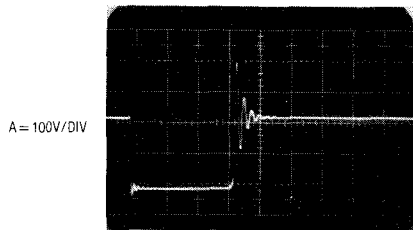


Figure D4. MOSFET-LT1071 Cascode Switching the Transformer Primary—Secondary Load is 0.2Ω

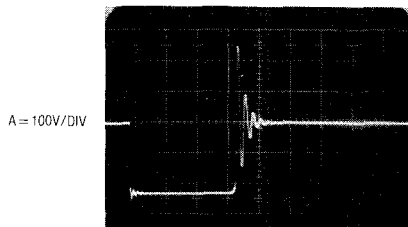
Application Note 25

Figure D5 shows the MOSFET drain at $V_{\text{SUPPLY}} = 160\text{V}$. The load draws about 2.5A. Flyback voltage rises to 400V. At 5A loading this voltage approaches 500V (Figure D6), while 10A load (Figure D7) forces almost 900V flyback. In actual regulator operation, supply voltages, switch on-time and output current can go higher, meaning flyback potentials

will exceed 1000V. This graphically mandates the need for a damper network. A simple reverse-biased diode or zener clipper will work, but will suffer from excessive dissipation. The network shown in Figure 9 is a good compromise between dissipation and reasonable flyback voltages.



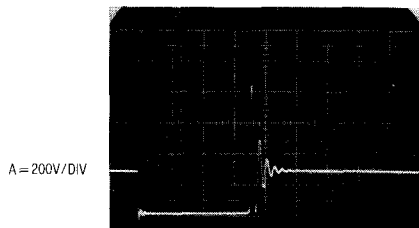
HORIZONTAL = 2.5 μ s/DIV



HORIZONTAL = 2.5 μ s/DIV

Figure D5. Undamped Regulator Flyback Pulse at 2.5A Output

Figure D6. Undamped Regulator Flyback Pulse at 5A Output



HORIZONTAL = 2.5 μ s/DIV

Figure D7. Undamped Regulator Flyback Pulse at 10A Output

Once the drive-flyback issues are settled, a feedback loop is closed around the transformer. This allows checking to see that loop stabilization is possible. Figure D8 diagrams the loop. In this configuration the regulator will function, but is unusable. The output is not galvanically isolated from the input, which ultimately must be directly AC line-driven. After this loop has been successfully closed, the isolated version is tried (Figure D9). This introduces more

phase shift, but is also found to be stable with appropriate frequency compensation. Finally, the connection between the input and output common potentials is broken, achieving the desired galvanic isolation. The start-up, soft-start and current limit features are then added and optimized. Testing involves checking performance under various line and load conditions. Details on circuit operation are covered in the text associated with Figure 9.

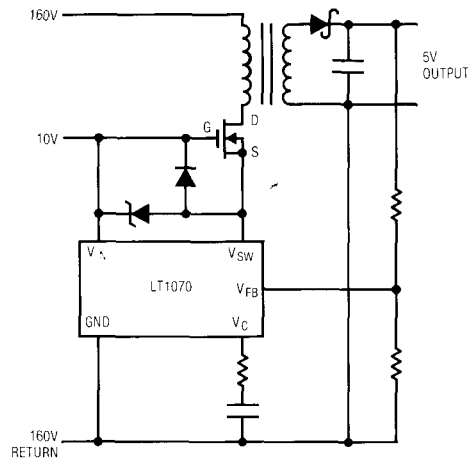


Figure D8. Developmental Version of Off-Line Switching Regulator—No Isolation is Included and the Scheme is Solely Intended to Verify that a Loop Can be Closed Around the Transformer

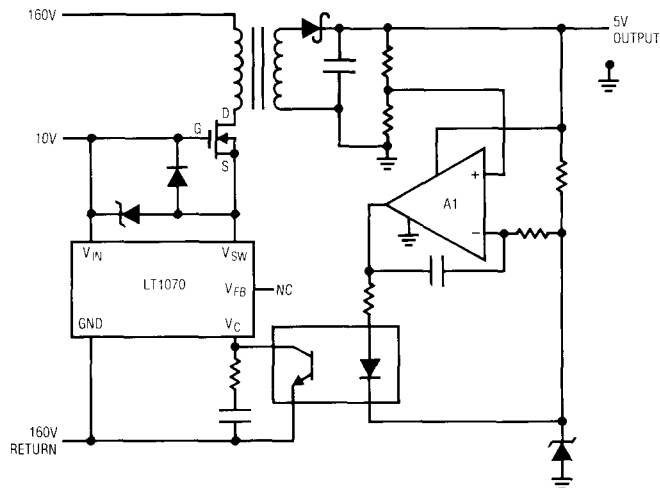
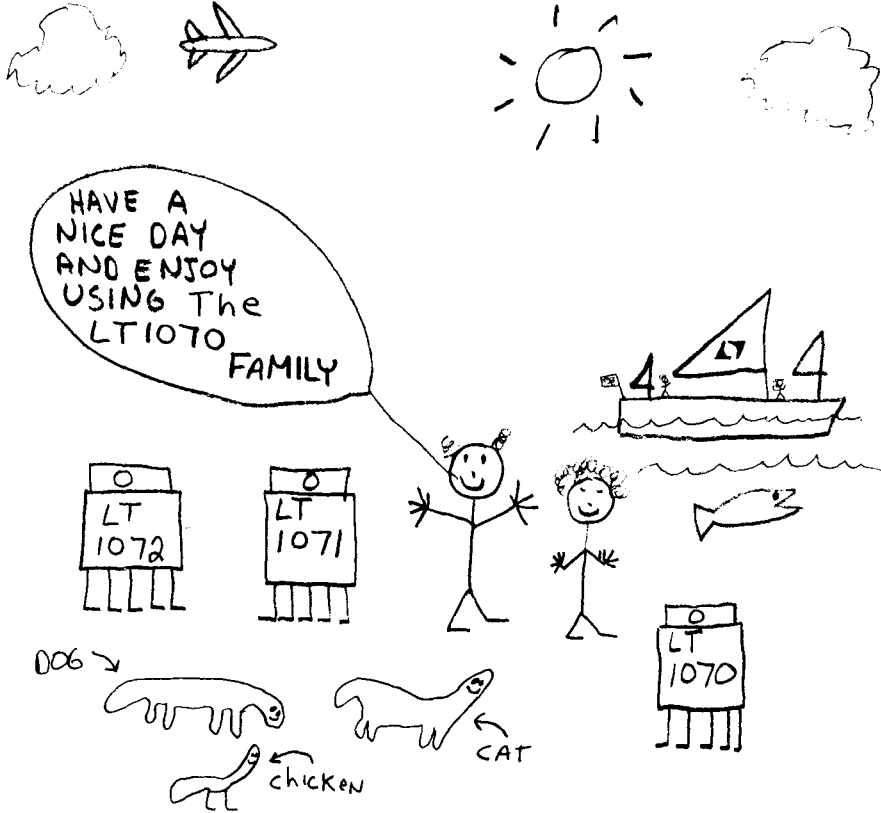


Figure D9. Developmental Version of Off-Line Regulator with Isolation—the Circuit Verifies That Loop Stability is Achievable with the Added Phase Shift of A1 and the Opto-Isolator—Start-Up, Current Limit and Soft-Start Features Must be Added to Complete the Design

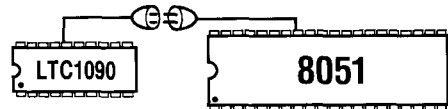


(They told me I couldn't leave the last page blank)

William

'87

Interfacing the LTC1090 to the 8051 MCU



Guy Hoover
William Rempfer

Introduction

This application note describes the hardware and software required for communication between the LTC1090 10-bit data acquisition system and the MCS-51 family of microcontrollers (e.g., 8051). The four wire interface is capable of completing a 10-bit conversion and transferring the data to the 8051 in 102 μ s. Configuration of the 8051 and the LTC1090 will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be discussed. Finally, a summary of results including data throughput rates will be provided.

Interface Details

The serial port of the 8051 does not support the synchronous, full duplex format used by the LTC1090. Therefore it is necessary for the user to construct a serial port

using four lines from one of the parallel ports available on the 8051. The lines are set or cleared using the bit manipulation features of the 8051. This provides a very flexible serial port but the data shift rate is three to four times slower than that available from microcontrollers with dedicated serial ports.

The LTC1090 has two clock lines: ACLK and SCLK. ACLK controls the A/D conversion rate while SCLK controls the data shift rate. These lines may be tied together or run separately. The 8051 provides a pin (ALE) which can be used to drive the ACLK of the LTC1090 (option 1). Alternatively, tying the clocks together saves one line that has to go between the LTC1090 and the 8051 (option 2). However, this implementation slows the data throughput rate due to additional code. The schematic of Figure 1 shows both of these options.

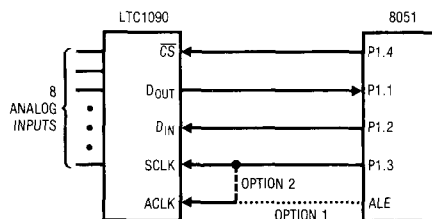


Figure 1. Schematic

Application Note 26A

Hardware Description

The 8051 was simulated and the code for this interface was developed on an Intel ICE 252 emulator.

Due to the weak pullups of the 8051, excess loading should be avoided when examining the output of the microcontroller.

The timing diagram of Figure 2 was obtained with an HP1631A logic analyzer using separate ACLK and SCLK (option 1). The 8051 clock rate was 12MHz, producing a 2.0MHz clock on the ALE pin.

The analog section of the schematic in Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1090 please see the data sheet.

Software Description

The software simulates a serial port through bit manipulation instructions of the 8051. Additionally, the software generates a delay during which time the A/D conversion takes place.

The code sets up bit one of port one as an input by setting it high. (Due to the weak pullup of the 8051, the D_{OUT} pin of the LTC1090 can then drive the pin high or low.)

SCLK is initialized to a low state and \overline{CS} is initialized to a high state. A D_{IN} word of \$0D is then loaded into the ac-

cumulator. An examination of Figure 3 and the data sheet will show that this configures the LTC1090 for CH0 with respect to CH1, unipolar, MSB first and a 10-bit word length. Next \overline{CS} goes low. If the user is tying ACLK and SCLK together (option 2) it is then necessary to generate two clock pulses to meet the deglitcher requirements. With separate clocks (option 1) the NOP is necessary to allow sufficient time for the deglitcher before starting to shift the data. Data is moved from the P1.1 pin (D_{OUT} of the LTC1090) to the carry register and shifted one bit at a time into the accumulator. At the same time, the 8-bit D_{IN} word is shifted from the accumulator into the carry register and output on P1.2 (D_{IN} of the LTC1090).

After the eight MSBs have been shifted, the contents of the accumulator are stored in R2. The final two bits are then shifted into the accumulator, placed in the most significant bits and stored in R3. The data is left justified at this point with the MSBs in R2 and the LSBs in R3. \overline{CS} is then raised and time (44 ACLK cycles) for the LTC1090 to do its next conversion must be allowed before the next read can be performed. If separate clocks are being used (option 1), quite often the microcontroller will have other tasks to accomplish and this time can be used productively. Otherwise, a routine such as the one labeled DELAY can be used. With the clocks tied together (option 2), it is necessary for the 8051 to manually clock the LTC1090 44 times and this free time is then lost as shown in Figure 7. An example of this routine is labeled LOOP 1.

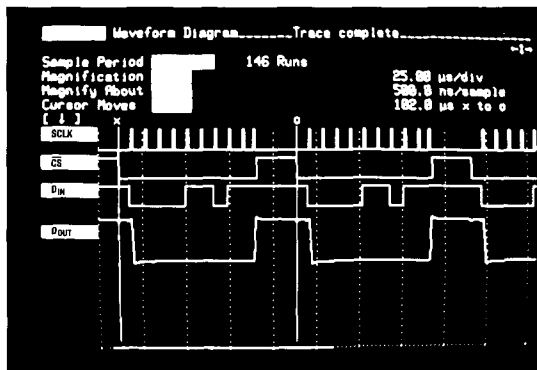


Figure 2. Timing Diagram for Option 1

If right justified data is required, the MSBF bit of the D_{IN} word could be cleared and the bits reversed (in this case producing a D_{IN} word of \$90). Also it would be necessary to swap the rotate left and rotate right instructions.

0	0	0	0	1	1	0	1
S/D	O/S	S1	S2	UNI	MSBF	WL1	WL0

Figure 3. D_{IN} Word for LTC1090

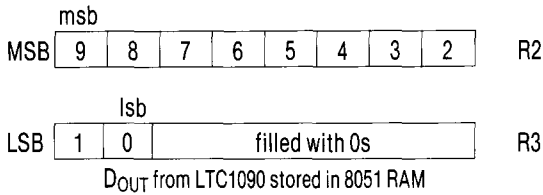


Figure 4. Memory Map

Summary

A four wire interface between the LTC1090 and the 8051 with a combined data conversion and transfer time of $102\mu s$ was demonstrated. It was shown that the ACLK of the LTC1090 can be run separately from the SCLK by tying the ACLK to the ALE of the 8051. Alternatively, the two clock pins can be tied together (saving one line at the expense of speed). The data can be either left justified or right justified in the microcontroller's memory through the proper choice of software and LTC1090 data format. The code shown applies to all MCS-51 family members. The same technique can be used on any parallel port processor.

LABEL	MNEMONIC	COMMENTS
	MOV P1, #02H	BIT 1 PORT 1 SET AS INPUT
	CLR P1.3	SCLK GOES LOW
	SETB P1.4	\overline{CS} GOES HIGH
CONT	MOV A, #0DH	D_{IN} WORD FOR LTC1090
	CLR P1.4	\overline{CS} GOES LOW
	MOV R4, #08H	LOAD COUNTER
	NOP	DELAY FOR DEGLITCHER
LOOP	MOV C, P1.1	READ DATA BIT INTO CARRY
	RLC A	ROTATE DATA BIT INTO ACC
	MOV P1.2, C	OUTPUT D_{IN} BIT TO LTC1090
	SETB P1.3	SCLK GOES HIGH
	CLR P1.3	SCLK GOES LOW
	DJNZ R4, LOOP	NEXT BIT
	MOV R2, A	STORE MSBs IN R2
	MOV C, P1.1	READ DATA BIT INTO CARRY
	CLR A	CLEAR ACC
	RLC A	ROTATE DATA BIT INTO ACC
	SETB P1.3	SCLK GOES HIGH
	CLR P1.3	SCLK GOES LOW
	MOV C, P1.1	READ DATA BIT INTO CARRY
	RRC A	ROTATE RIGHT INTO ACC
	RRC A	ROTATE RIGHT INTO ACC
	MOV R3, A	STORE LSBs IN R3
	SETB P1.3	SCLK GOES HIGH
	CLR P1.3	SCLK GOES LOW
	SETB P1.4	\overline{CS} GOES HIGH
	MOV R5, #07H	LOAD COUNTER
DELAY	DJNZ R5, DELAY	GO TO DELAY IF NOT DONE

Figure 5. 8051 Code for Option 1 (ACLK Tied to ALE)

Application Note 26A

LABEL	MNEMONIC	COMMENTS
	MOV P1, #02H	BIT 1 PORT 1 SET AS INPUT
	CLR P1.3	SCLK GOES LOW
	SETB P1.4	CS GOES HIGH
CONT	MOV A, #0DH	D _{IN} WORD FOR LTC1090
	CLR P1.4	CS GOES LOW
	SETB P1.3	SCLK GOES HIGH
	CLR P1.3	SCLK GOES LOW
	SETB P1.3	SCLK GOES HIGH
	CLR P1.3	SCLK GOES LOW
	MOV R4, #08H	LOAD COUNTER
LOOP	MOV C, P1.1	READ DATA BIT INTO CARRY
	RLC A	ROTATE DATA BIT INTO ACC
	MOV P1.2, C	OUTPUT D _{IN} BIT TO LTC1090
	SETB P1.3	SCLK GOES HIGH
	CLR P1.3	SCLK GOES LOW
	DJNZ R4, LOOP	NEXT BIT
	MOV R2, A	STORE MSBs IN R2
	MOV C, P1.1	READ DATA BIT INTO CARRY
	CLR A	CLEAR ACC
	RLC A	ROTATE DATA BIT INTO ACC
	SETB P1.3	SCLK GOES HIGH
	CLR P1.3	SCLK GOES LOW
	MOV C, P1.1	READ DATA BIT INTO CARRY
	RRC A	ROTATE RIGHT INTO ACC
	RRC A	ROTATE RIGHT INTO ACC
	MOV R3, A	STORE LSBs IN R3
	SETB P1.3	SCLK GOES HIGH
	CLR P1.3	SCLK GOES LOW
	SETB P1.4	CS GOES HIGH
LOOP1	MOV R4, #2CH	LOAD COUNTER
	SETB P1.3	SCLK GOES HIGH
	CLR P1.3	SCLK GOES LOW
	DJNZ R4, LOOP1	GO TO LOOP1 IF NOT DONE

Figure 6. 8051 Code for Option 2 (ACLK Tied to SCLK)

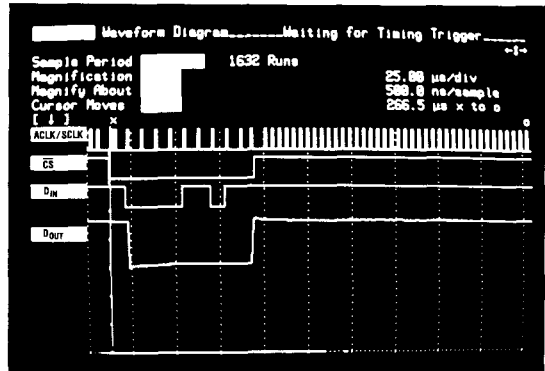
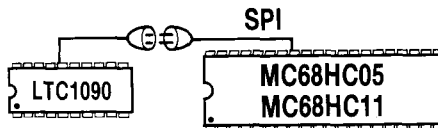


Figure 7. Timing Diagram for Option 2

Interfacing the LTC1090 to the MC68HC05 MCU

Guy Hoover
 William Rempfer



Introduction

This application note describes an interface between the LTC1090 10-bit data acquisition system and the Motorola SPI family of single chip microcomputers (e.g., 68HC05). The simple four wire interface is capable of completing a 10-bit conversion and shifting the data to the 68HC05 in 49 μ s. Configuration of the LTC1090 and the 68HC05 will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be shown. Finally, a summary of the key points of this interface will be given, including data throughput rates.

Interface Details

The LTC1090 has two clock lines: ACLK and SCLK. ACLK controls the A/D conversion rate while SCLK controls the data shift rate. Data is transferred in a synchronous, full duplex format over D_{IN} and D_{OUT}.

The Motorola Serial Peripheral Interface (SPI) is a synchronous, full duplex, serial port built into the 68HC05 that allows the user to construct a simple communication path to the LTC1090. SPI provides clock, data in and data out lines that are compatible with the LTC1090. The only additional line required is one programmable output pin (CO) to control CS on the LTC1090. The schematic of Figure 1 shows how the two devices are connected.

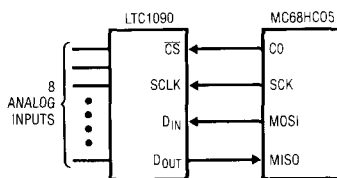


Figure 1. Schematic

Hardware Description

The 68HC05 was emulated and the code for this interface was developed on a Motorola M68HC05 EVM.

\overline{SS} (Pin 34) of the 68HC05 must be held high to enable the SPI properly for this interface.

The timing diagram of Figure 2 was obtained with an HP1631A logic analyzer using a 2MHz ACLK. The 68HC05 clock was 4MHz.

The analog section of the schematic in Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1090 please see the data sheet.

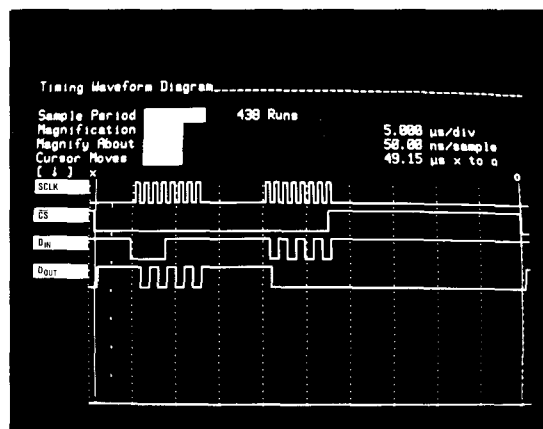


Figure 2. Timing Diagram

Application Note 26B

Software Description

The software configures and controls the SPI of the 68HC05. Additionally, the software manipulates CO (\overline{CS} of the LTC1090) and generates a delay during which time the LTC1090 performs a conversion.

The code first configures the Serial Peripheral Control Register (SPCR) of the SPI. The SPI interrupt is disabled. The SPI outputs are enabled. The SPI is configured as a master. Finally, the SPI clock is set to normally low, for data transfer on the rising edge and for a frequency equal to half the internal processor clock (one fourth the crystal frequency).

Port C is configured as all outputs by placing ones in the data direction register of port C. A D_{IN} word that configures the LTC1090 for CH0 with respect to CH1, unipolar, MSB first and a 16-bit word length is stored in \$50. Figure 3 shows how the D_{IN} word is composed.

CO is made to go low. D_{IN} for the LTC1090 is loaded into the SPI data register. Storing D_{IN} in the data register causes the transfer to begin. After waiting for the first eight bits to be transferred (8 NOPs) the status register of the SPI is examined. This clears the SPIF bit of the status register and allows the data register to be read, which is the next step. The first eight bits containing the MSBs from the LTC1090 are then stored in \$61 of the 68HC05 as shown in Figure 4. The LSBs are transferred in the same manner and stored in \$62 of the 68HC05. Notice in Figure 5

0	0	0	0	1	1	1	1
S/D	O/S	S1	S2	UNI	MSBF	WL1	WL0

Figure 3. D_{IN} Word for LTC1090

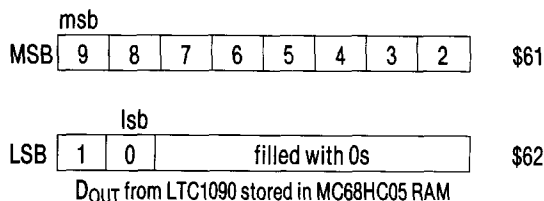


Figure 4. Memory Map

that only 6 NOPs are used in transferring the LSBs. This is because after 6 NOPs, time is consumed by the BSET command which sets the CO pin of the 68HC05. The data at this point is left justified.

At this time 44 ACLK cycles must be allowed for the A/D to perform its next conversion. Usually the processor will have other tasks to perform during this time. If this is not the case a string of NOPs or a simple delay loop can be used to generate this delay.

The code was written for the 68HC05. By changing the addresses of the special function registers however, the code should run on all of Motorola's SPI processors including the 68HC11.

Summary

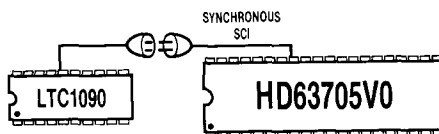
A four wire interface between the LTC1090 and the 68HC05 with a combined data conversion and transfer time of 49 μ s was demonstrated. The interface used the serial (SPI) port of the 68HC05. The 10 data bits of the LTC1090 are shifted MSB first in two eight bit transfers. The data is stored left justified in the 68HC05's internal RAM.

LABEL	MNEMONIC	COMMENTS
	LDA #50	CONFIGURATION DATA FOR SPCR
	STA \$0A	LOAD DATA INTO SPCR (\$0A)
	LDA #5FF	CONFIG. DATA FOR PORT C DDR
	STA \$06	LOAD DATA INTO PORT C DDR
	LDA #50F	LOAD LTC1090 D_{IN} DATA INTO ACC
	STA \$50	LOAD LTC1090 D_{IN} DATA INTO \$50
START	BCLR 0,\$02	CO GOES LOW (\overline{CS} GOES LOW)
	LDA \$50	LOAD D_{IN} INTO ACC FROM \$50
	STA \$0C	LOAD D_{IN} INTO SPI. START SCK
	NOP	8 NOPs FOR TIMING
	LDA \$0B	CHECK SPI STATUS REG
	LDA \$0C	LOAD LTC1090 MSBs INTO ACC
	STA \$61	STORE MSBs IN \$61
	STA \$0C	START NEXT SPI CYCLE
	NOP	6 NOPs FOR TIMING
	BSET 0,\$02	CO GOES HIGH (\overline{CS} GOES HIGH)
	LDA \$0B	CHECK SPI STATUS REGISTER
	LDA \$0C	LOAD LTC1090 LSBs INTO ACC
	STA \$62	STORE LSBs IN \$62

Figure 5. 68HC05 Code

Interfacing the LTC1090 to the HD63705V0 MCU

Guy Hoover
William Rempfer



Introduction

This application note describes an interface between the LTC1090 10-bit data acquisition system and the Hitachi 63705 microcomputer. The simple four wire interface is capable of completing a 10-bit conversion and shifting the data to the 63705 in 45 μ s. Configuration of the LTC1090 and the 63705 will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be shown. Finally, a summary of the key points of this interface will be given including data throughput rates.

Interface Details

The LTC1090 has two clock lines: ACLK and SCLK. ACLK controls the A/D conversion rate while SCLK controls the data shift rate. Data is transferred in a full duplex format over D_{IN} and D_{OUT} .

The Hitachi Serial Communication Interface (SCI) is a synchronous, full duplex, serial port built into the 63705 that allows the user to construct a simple communication path to the LTC1090. SCI provides clock, transmit and receive lines that are compatible with the LTC1090. The only

additional line required is one programmable output pin (CO) to control \overline{CS} on the LTC1090. The schematic of Figure 1 shows how the two devices are connected.

Hardware Description

The 63705 was emulated and the code for this interface was developed on a Hitachi H35MIX3 emulator.

The timing diagram of Figure 2 was obtained using an HP1631A logic analyzer. ACLK of the LTC1090 was 2 MHz and the 63705 clock was 4 MHz.

The analog section of the schematic of Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1090 please see the data sheet.

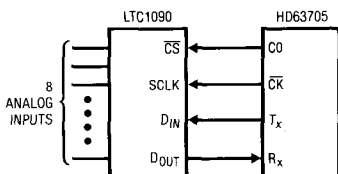


Figure 1. Schematic

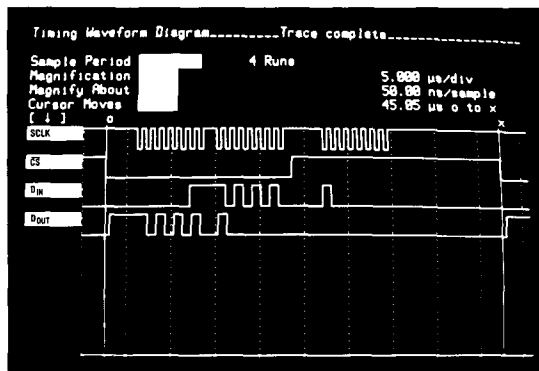


Figure 2. Timing Diagram

Application Note 26C

Software Description

The software configures and controls the SCI of the 63705. Additionally, the software manipulates C0 (\overline{CS} of the LTC1090) and generates a delay during which time the LTC1090 performs a conversion.

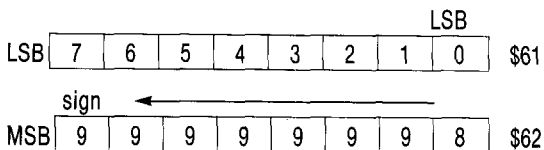
The code first configures the SCI control register (SCR). D3 and D4 are set as the SCI output and input respectively. D5 is selected as a clock output with a frequency one fourth the crystal frequency. Next, the SCI status register (SSR) is configured so that the interrupts are disabled. Data is transmitted on the falling edge of the clock and received on the rising edge of the clock.

Port C is configured as all outputs by setting the data direction register (address \$06). A D_{IN} word that configures the LTC1090 for CH0 with respect to CH1, bipolar, LSB first and a 16-bit word length is stored in \$50. Figure 3 shows how the D_{IN} word is composed. Note, that for LSB first format the D_{IN} word must be constructed opposite from MSB first format. This is so that each bit of the D_{IN} word is always shifted into the LTC1090 in the same order.

C0 is made to go low. D_{IN} for the LTC1090 is loaded into the SCI data register (SDR). Storing D_{IN} in the SDR causes the transfer to begin. After waiting for the first eight bits to be transferred (6 NOPs) the data containing the LSBs from the LTC1090 is loaded into the accumulator and then stored in \$61 of the 63705 RAM. The act of reading the LSBs into the ACC causes the next SCI transfer to begin. C0 is set and the MSBs from the LTC1090 are loaded into the ACC and then stored in \$62 of the 63705 RAM.

1	1	0	0	0	0	0	0	\$50
WLO	WL1	MSBF	UNI	S2	S1	O/S	S/D	

Figure 3. D_{IN} Word for LTC1090 Stored in 63705 RAM



OUT from LTC1090 stored in 63705 RAM

Figure 4. Memory Map

LABEL	MNEMONIC	COMMENTS
	LDA #5E0	CONFIGURATION DATA FOR SCR
	STA \$10	LOAD DATA INTO SCR (\$10)
	LDA #330	CONFIGURATION DATA FOR SSR
	STA \$11	LOAD DATA INTO SSR (\$11)
	LDA #5FF	CONFIG. DATA FOR PORT C DDR
	STA \$06	LOAD DATA INTO PORT C DDR
	LDA #5C0	LOAD LTC1090 D_{IN} DATA INTO ACC
	STA \$50	LOAD LTC1090 D_{IN} DATA INTO \$50
START	LDA \$50	LOAD D_{IN} INTO ACC FROM \$50
	BCLR 0,\$02	C0 GOES LOW (\overline{CS} GOES LOW)
	STA \$12	LOAD D_{IN} INTO SDR. START SCK
	NOP	6 NOPs FOR TIMING
	LDA \$12	LOAD LSBs. START NEXT CYCLE
	STA \$61	STORE LSBs IN \$61
	NOP	1 NOP FOR TIMING
	BSET 0,\$02	C0 GOES HIGH (\overline{CS} GOES HIGH)
	LDA \$12	LOAD MSBs
	STA \$62	STORE MSBs IN \$62

Figure 5. 63705 Code

The data at this point is right justified with the sign bit (B9) being extended into B1-B7 of \$62 as shown in Figure 4.

At this time 44 ACLK cycles must be allowed for the A/D to perform its next conversion. Usually the processor will have other tasks to perform during this time (you have to do something with the data once the processor has it). If this is not the case, a string of NOPs or a simple delay loop can be used to generate this delay.

Summary

A four wire interface between the LTC1090 and the Hitachi 63705 with a combined data conversion and transfer time of $45\mu s$ was demonstrated. The interface used the serial (SCI) port of the 63705. Because the SCI port transfers data LSB first, care must be taken to properly construct the D_{IN} word so that the bits are transmitted in the proper order to the LTC1090. The 10 data bits of the LTC1090 are shifted LSB first in two eight bit transfers. The data is stored right justified in the 63705s internal RAM.

Interfacing the LTC1090 to the COP820C MCU

Guy Hoover
 William Rempfer

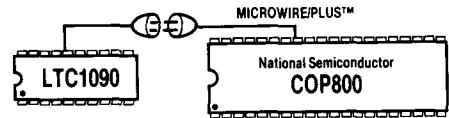
Introduction

This application note describes the hardware and software required for communication between the LTC1090 10-bit data acquisition system and the National Semiconductor COP800 microcontroller family which uses the MICROWIRE/PLUS serial interface. The simple four wire interface is capable of completing a 10-bit conversion and shifting the data in $56\mu\text{s}$. Configuration of the LTC1090 and the COP820C will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be shown. Finally, a summary of the key points of this interface will be given including data throughput rates.

Interface Details

The LTC1090 has two clock lines: ACLK and SCLK. ACLK controls the A/D conversion rate while SCLK controls the data shift rate. Data is transferred in a full duplex format over D_{IN} and D_{OUT} .

The National Semiconductor MICROWIRE/PLUS is a synchronous, full duplex, serial port built into the COP800 family that allows easy interface to the LTC1090. MICROWIRE/PLUS provides clock, data in and data out lines that are compatible with the LTC1090. One additional



line (G1) is required to control the \overline{CS} pin on the LTC1090. The schematic of Figure 1 shows how the two devices are connected.

Hardware Description

The actual interface was done using the COP820C, a member of the COP800 family. All code shown here should work with any of the COP800 family.

The code for this interface was developed on a COP820 evaluation board operated in the emulation mode.

The timing diagram of Figure 2 was obtained with an HP1631A logic analyzer using a 2MHz ACLK. The COP820C clock was 5MHz. To obtain a $56\mu\text{s}$ transfer time it is necessary to run the COP820C at 20MHz which requires a high speed version of the part.

The analog section of the schematic in Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1090 please see the data sheet.

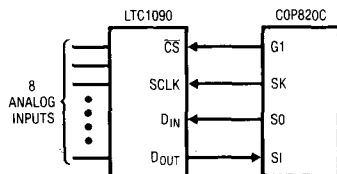


Figure 1. Schematic

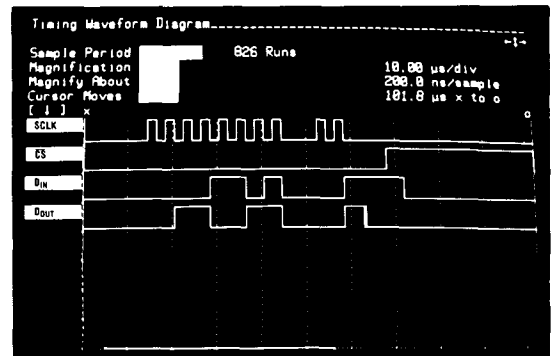


Figure 2. Timing Diagram

Application Note 26D

Software Description

The software configures and controls the MICROWIRE/PLUS serial interface of the COP820C. Additionally, the software manipulates G1 (\overline{CS} of the LTC1090) and generates a delay during which time the LTC1090 performs a conversion.

The code first loads the LTC1090 D_{IN} word into memory location. \$F0. This D_{IN} word configures the LTC1090 for CH0 with respect to CH1, MSB first, unipolar and 10 bits as shown in Figure 3. Next port G is configured for MICROWIRE™ master mode and G1 is configured as an output. The control register is initialized so that SO and SK are outputs. The port G data register address is loaded into the B register. At this point the COP820C is initialized and the data transfer process is ready to begin.

The D_{IN} word for the LTC1090 is then loaded into the ACC from location \$F0. G1 (\overline{CS}) is cleared and D_{IN} is transferred into the MICROWIRE shift register. The BUSY bit of the PSW register is set which starts the transfer of the first eight bits. A delay consisting of 15 NOPs waits for the data shift to finish at which time the D_{OUT} word from the LTC1090 is loaded into the ACC. The busy bit is set again which causes the transfer to continue. Then, the D_{OUT} word in the ACC is stored in location \$F3. The busy bit is cleared which halts the transfer. Two more bits have been shifted at this point. G1 (\overline{CS}) is set and the contents of the

0	0	0	0	1	1	0	1
S/D	O/S	S1	S2	UNI	MSBF	WL1	WLO

Figure 3. D_{IN} Word for LTC1090

		MSB								
MSB		9	8	7	6	5	4	3	2	F3
		LSB								
LSB		1	0	X	X	X	X	X	X	F4

D_{OUT} from LTC1090 stored in COP820C RAM

Figure 4. Memory Map

LABEL	MNEMONIC	COMMENTS
	LD (F0)–0D	LOAD 0D INTO F0 (D_{IN})
	LD (D5)–32	CONFIGURE PORT G
	LD (EE)–8	CONFIGURE CONTROL REG.
	LD (B)–D4	PORT G DATA REG. INTO B
LOOP	LD (A)–(F0)	LOAD D_{IN} INTO ACC
	RBIT 1	G1 RESET (\overline{CS} GOES LOW)
	X (A)––(E9)	LOAD D_{IN} INTO SHIFT REG.
	LD (B)–EF	LOAD PSW REG ADDR IN B
	SBIT 2	TRANSFER BEGINS
	NOP	15 NOPs FOR TIMING
	X (A)––(E9)	LOAD D_{OUT} INTO ACC
	SBIT 2	TRANSFER CONTINUES
	X (A)––(F3)	LOAD D_{OUT} IN ADDR F3
	RBIT 2	STOP TRANSFER
	LD (B)–D4	PUT PORT G ADDR IN B
	SBIT 1	G1 SET (\overline{CS} GOES HIGH)
	X (A)––(E9)	LOAD D_{OUT} INTO ACC
	RC	CLEAR CARRY
	RRCA	SHIFT RIGHT THRU CARRY
	RRCA	SHIFT RIGHT THRU CARRY
	RRCA	SHIFT RIGHT THRU CARRY
	X (A)––(F4)	LOAD D_{OUT} IN ADDR F4

Figure 5. COP820C Code

MICROWIRE shift register are swapped with those of the ACC. The carry is cleared and the data in the ACC is shifted right, through the carry bit three times. This puts the two LSBs of the D_{OUT} word in the MSBs of the ACC. The contents of the ACC are then stored in \$F4. The data at this point is left justified as shown in Figure 4.

44 ACLK cycles must be allowed between transfers for the A/D to perform its next conversion. The instructions, after G1 is set, take enough time so that no additional delay is required by this program.

Summary

A four wire interface between the LTC1090 and the COP820C with a combined data conversion and transfer time of 56 μ s was demonstrated. The interface used the MICROWIRE/PLUS serial port of the COP820C. The 10 data bits of the LTC1090 are shifted MSB first in one eight bit and one two bit transfer. The data is stored left justified in the COP820C's internal RAM.

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Interfacing the LTC1090 to the TMS7742 MCU

Guy Hoover
William Rempfer

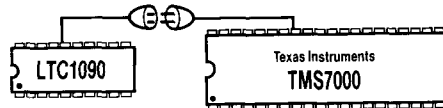
Introduction

This application note describes an interface between the LTC1090 10-bit data acquisition system and the TMS7000 family of microcomputers (e.g., TMS7742). The simple four wire interface is capable of completing a 10-bit conversion and shifting the data to the TMS7742 in 103 μ s. Configuration of the LTC1090 and the TMS7742 will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be shown. Finally, a summary of the key points of this interface will be given including data throughput rates.

Interface Details

The LTC1090 has two clock lines: ACLK and SCLK. ACLK controls the A/D conversion rate while SCLK controls the data shift rate. Data is transferred in a full duplex format over D_{IN} and D_{OUT}.

The TMS7742 contains a synchronous, full duplex, serial port that allows the user to construct a simple communication path to the LTC1090. The serial port provides clock, transmit and receive lines that are compatible with the LTC1090. The only additional line required is one pro-



grammable output pin (A0) to control \overline{CS} on the LTC1090. The schematic of Figure 1 shows how the two devices are connected.

Hardware Description

The TMS7742 was chosen because it contains 4k of EPROM which can be programmed using a standard EPROM programmer. Any member of the TMS7000 family which contains a serial port should be able to use this code with only modifications to the peripheral register numbers.

The timing diagram of Figure 2 was obtained using an HP1631A logic analyzer. ACLK of the LTC1090 was 2 MHz and the TMS7742 clock was 5 MHz.

The analog section of the schematic of Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1090 please see the data sheet.

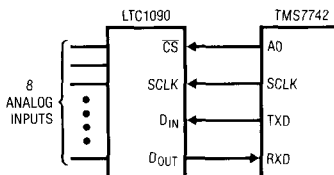


Figure 1. Schematic

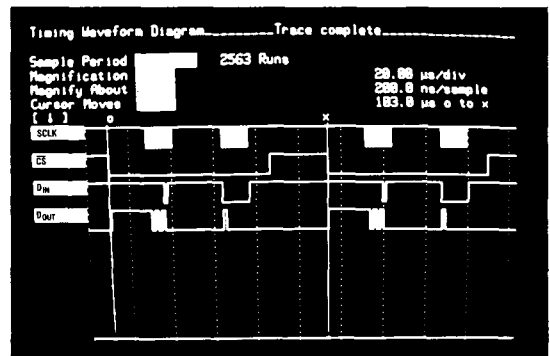


Figure 2. Timing Diagram

Application Note 26E

Software Description

The software configures and controls the serial port of the TMS7742. Additionally, the software manipulates A0 (\overline{CS} of the LTC1090) and generates a delay during which time the LTC1090 performs a conversion.

The code first disables all interrupts and initializes the stack. Next the serial port is configured. Tx is enabled, the serial port is reset, and the SMODE register is configured for 8 bits, no parity, and one stop bit. The SCLK rate is set to the processor clock frequency divided by 4. The D_{IN} word of the LTC1090 is next loaded into the ACC. This D_{IN} word (\$DF) configures the LTC1090 for CH7 with respect to COM, unipolar mode, LSB first and a 16-bit word length. Examine Figure 3 to see how this is constructed keeping in mind that the TMS7742 transmits data LSB first.

A subroutine SXTNBIT is called next. This is a routine that does the actual data shifting. A0 (\overline{CS}) is cleared. Then, the LTC1090 D_{IN} word is placed into the transmit buffer. The serial port is turned on and the data is shifted while the processor idles in a loop. The first eight bits containing the LSBs are then placed in the B register. The procedure is repeated for the next eight bits which contain the two MSBs and the result is placed in the A register. A0 (\overline{CS}) is then set and the subroutine returns to the original program. The data in the A and B registers is then stored in R5 and R6.

At this time 44 ACLK cycles must be allowed for the A/D to perform its next conversion. Enough time is consumed by this program however that no additional delay for the conversion is required.

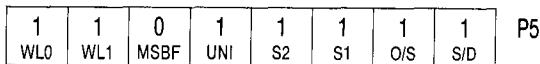


Figure 3. D_{IN} Word for LTC1090 Stored in TMS7742 RAM

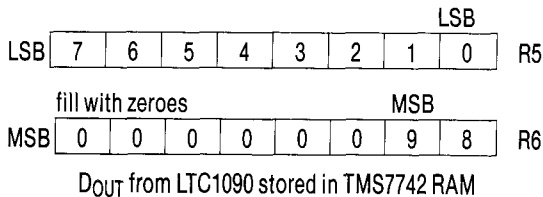


Figure 4. Memory Map

LABEL	MNEMONIC	COMMENTS
START	DINT	DISABLES ALL INTERRUPTS
	MOVP	% > 2A, P0
	MOVP	% > 02, P16
	MOV	% > 60, B
	LDSP	PUT ADDRESS INTO POINTER
	MOVP	% > DF, P5
	MOVP	% > 08, P6
	MOVP	% > 00, P17
	MOVP	% > 40, P17
	MOVP	% > 0C, P17
	MOVP	% > 00, P21
	MOVP	% > 00, P17
	MOVP	% > 00, P20
	MOVP	% > C0, P21
LOOP	MOV	% > DF, A
	CALL	SXTNBIT
	MOV	B, R5
	MOV	A, R6
SXTNBIT	ANDP	% > FE, P4
	MOVP	A, P23
	MOVP	% > 40, P21
	MOVP	% > 17, P17
	MOVP	% > C0, P21
	MOVP	% > 14, P17
	MOV	% > 02, A
WAIT1	DJNZ	A, WAIT1
	NOP	
	MOVP	P22, B
	MOVP	A, P23
	MOVP	% > 40, P21
	MOVP	% > 17, P17
	MOVP	% > C0, P21
	MOVP	% > 14, P17
	MOV	% > 02, A
WAIT2	DJNZ	A, WAIT2
	NOP	
	MOVP	P22, A
	ORP	% > 01, P4
	RETS	

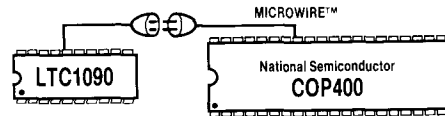
Figure 5. TMS7742 Code

Summary

A four wire interface between the LTC1090 and the TMS7742 with a combined data conversion and transfer time of $103\mu\text{s}$ was demonstrated. The interface used the serial port of the TMS7742. Because the serial port transfers data LSB first, care must be taken to properly construct the D_{IN} word so that the bits are transmitted in the proper order to the LTC1090. The 10 data bits of the LTC1090 are shifted LSB first in two eight bit transfers. The data is stored right justified in the TMS7742's internal RAM.

Interfacing the LTC1090 to the COP402N MCU

Guy Hoover
William Rempfer



Introduction

This application note describes the hardware and software required for communication between the LTC1090 10-bit data acquisition system and the National Semiconductor COP400 microcontroller family which uses the MICROWIRE serial interface. The simple four wire interface is capable of completing a 10-bit conversion and shifting the data in 100 μ s. Configuration of the LTC1090 and the COP402N will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be shown. Finally, a summary of the key points of this interface will be given including data throughput rates.

Interface Details

The LTC1090 has two clock lines: ACLK and SCLK. ACLK controls the A/D conversion rate while SCLK controls the data shift rate. Data is transferred in a full duplex format over D_{IN} and D_{OUT}.

The National Semiconductor MICROWIRE interface is a synchronous, full duplex, serial port built into the COP400 family that allows the user to easily interface to the LTC1090. MICROWIRE provides clock, data in and data out lines that are compatible with the LTC1090. One addi-

tional line (G0) is required to control the CS pin on the LTC1090. The schematic of Figure 1 shows how the two devices are connected.

Hardware Description

The actual interface will involve using the COP402N, a member of the COP400 family. All code shown here should work with any of the COP400 family.

The code for this interface was developed on a COP400 evaluation board which allows an external EPROM to be used in place of the internal processor ROM.

The timing diagram of Figure 2 was obtained with an HP1631A logic analyzer using a 2MHz ACLK. The COP402N clock was 4MHz.

The analog section of the schematic in Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1090 please see the data sheet.

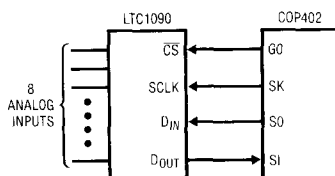


Figure 1. Schematic

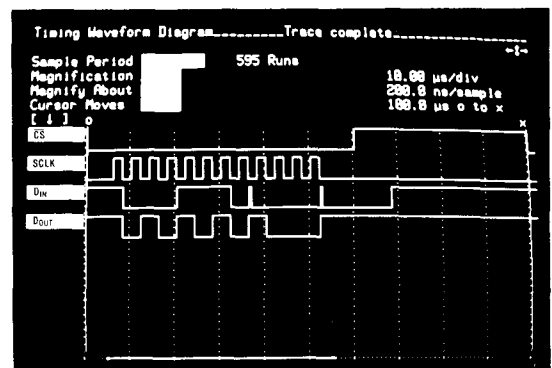


Figure 2. Timing Diagram

Application Note 26F

Software Description

The software configures and controls the MICROWIRE serial interface of the COP402N. Additionally, the software manipulates G0 (\overline{CS} of the LTC1090) and generates a delay during which time the LTC1090 performs a conversion.

The code first initializes the B register and then loads the LTC1090 D_{IN} word into the RAM of the COP402 one nibble at a time. As shown in Figure 3 the D_{IN} word configures the LTC1090 for CH0 with respect to COM, unipolar, MSB first, and 12 bits. SO is configured as an output. The carry is set so that when an XAS instruction is generated the shift clock (SK) will begin clocking data.

The first nibble of the D_{IN} word is loaded into the ACC and G0 (\overline{CS}) is cleared. The D_{IN} nibble is loaded into the shift register and the data begins to shift. The second nibble of the D_{IN} word is loaded into the ACC. One NOP is allowed for timing and then the contents of the ACC are swapped with those of the shift register. The MSBs of the LTC1090 D_{OUT} word are now in the ACC. This data is then stored in memory location \$13. The ACC is loaded with null data from RAM and another swap between the ACC and the shift register is executed. The next D_{OUT} nibble is stored in \$14. The carry is cleared so that on the next XAS instruction the shift clock will stop. The XAS instruction is executed and the final nibble of the LTC1090 D_{OUT} word containing the two LSBs and two zeroes is loaded into the

\$10				\$11			
1	0	0	0	1	1	1	0
S/D	O/S	S1	S2	UNI	MSBF	WL1	WLO

Figure 3. D_{IN} Word for LTC1090

MSB				
B9	B8	B7	B6	\$13
B5	B4	B3	B2	\$14
LSB				
B1	B0	0	0	\$15

D_{OUT} from LTC1090 stored in COP402 RAM

Figure 4. Memory Map

LABEL	MNEMONIC	COMMENTS
	CLRA	MUST BE FIRST INSTRUCTION
	LBI 1,0	BR = 1 BD = 0 INITIALIZE B REG.
	STII 8	FIRST D_{IN} NIBBLE IN \$10
	STII E	SECOND D_{IN} NIBBLE IN \$11
	STII 0	NULL DATA IN \$12, B = \$13
	LEI C	SET EN TO (1100) BIN
LOOP	SC	CARRY SET
	LDD 1,0	LOAD FIRST D_{IN} NIBBLE IN ACC
	OGI 50	G0 (\overline{CS}) CLEARED
	XAS	ACC TO SHIFT REG. BEGIN SHIFT
	LDD 1,1	LOAD NEXT D_{IN} NIBBLE IN ACC
	NOP	TIMING
	XAS	NEXT NIBBLE, SHIFT CONTINUES
	XIS 0	FIRST NIBBLE D_{OUT} TO \$13
	LDD 1,2	PUT NULL DATA IN ACC
	XAS	SHIFT CONTINUES, D_{OUT} TO ACC
	XIS 0	NEXT NIBBLE D_{OUT} TO \$14
	RC	CLEAR CARRY
	CLRA	CLEAR ACC
	XAS	THIRD NIBBLE D_{OUT} TO ACC
	OGI 51	G0 (\overline{CS}) SET
	XIS 0	THIRD NIBBLE D_{OUT} TO \$15
	LBI 1,3	SET B REG. FOR NEXT LOOP

Figure 5. COP402 Code

ACC. G0 (\overline{CS}) is taken high and the A/D begins its next conversion cycle. The third D_{OUT} nibble is stored in location \$15. The B register is then reinitialized so that when the loop is run again the data will always be stored in the same memory locations. The D_{OUT} data from the LTC1090 is now in a left justified format as shown in Figure 4.

44 ACLK cycles must be allowed between transfers for the A/D to perform its next conversion. The instructions, after G0 is set, take enough time so that no additional delay is required by this program.

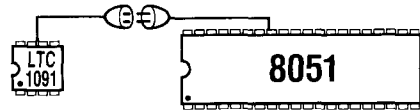
Summary

A four wire interface between the LTC1090 and the COP402N with a combined data conversion and transfer time of 100 μ s was demonstrated. The interface used the MICROWIRE serial port of the COP402N. The 10 data bits of the LTC1090 are shifted MSB first in three four bit transfers with the last two bits filled with zeroes. The data is stored left justified in the COP402N's internal RAM. The code demonstrated will work on any member of the COP400 family.

MICROWIRE is a trademark of National Semiconductor Corp.

Interfacing the LTC1091 to the 8051 MCU

Guy Hoover
 William Rempfer



Introduction

This application note describes the hardware and software required for communication between the LTC1091 10-bit data acquisition system and the MCS-51 family of microcontrollers (e.g., 8051). The three wire interface is capable of completing a 10-bit conversion and transferring the data to the 8051 in 57 μ s. Configuration of the 8051 and the LTC1091 will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be discussed. Finally, a summary of results including data throughput rates will be provided.

Interface Details

The serial port of the 8051 does not support the synchronous, half duplex format used by the LTC1091. Therefore it is necessary for the user to construct a serial port using three lines from one of the parallel ports available on the 8051. The lines are set or cleared using the bit manipulation features of the 8051. This provides a very flexible serial port.

The data lines (D_{IN} and D_{OUT}) of the LTC1091 can be tied together as shown in Figure 1. This can be done because

the I/O pins on the 8051 can be configured as either inputs or outputs independently of one another during the data transfer.

Hardware Description

The 8051 was simulated and the code for this interface was developed on an Intel ICE252 emulator.

Due to the weak pullups of the 8051, excess loading should be avoided when examining the output of the microcontroller.

The timing diagram of Figure 2 was obtained with an HP1631A logic analyzer. The 8051 clock rate was 2MHz. The clock could be run as high as 12MHz yielding the minimum conversion and transfer time of 57 μ s.

The analog section of the schematic in Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1091 please see the data sheet.

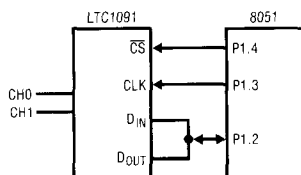


Figure 1. Schematic

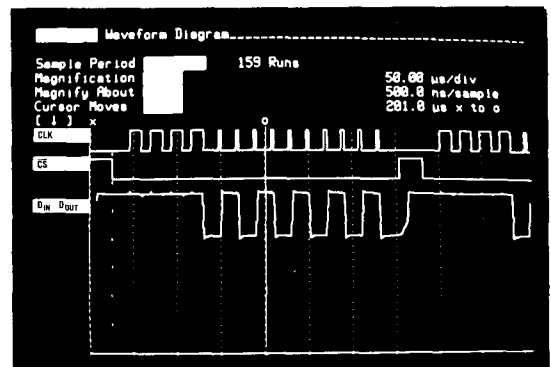


Figure 2. Timing Diagram

Application Note 26G

Software Description

The software simulates a serial port through bit manipulation instructions of the 8051.

\overline{CS} is initialized by setting it high. Next the D_{IN} word for the LTC1091 is loaded into the accumulator. The LTC1091 is configured for MSB first and CH1 with respect to ground. Note that only the first four most significant bits of the byte loaded into the accumulator are sent to the LTC1091. The four LSBs of the D_{IN} word are don't cares.

\overline{CS} is then cleared and a counter is set to four (the number of bits in the D_{IN} word). For each of the four D_{IN} bits the accumulator is shifted left with the MSB going into the carry bit. SCLK is cleared. The carry bit is output to D_{IN} and SCLK is set. The counter is decremented and checked and if all four bits have been output, P1.2 (D_{IN} and D_{OUT}) is set. This allows the pin to be used as an input now, to read the data in from the LTC1091.

SCLK is then cleared and the counter is set to nine (the first bit shifted out from the LTC1091 is a dummy, so nine shifts are required to fill the first byte.). The eight MSBs are read in the same manner as the D_{IN} word was output. The eight MSBs are stored in R2 and the remaining two LSBs are read into the accumulator. The LSBs are shifted into the MSBs of the accumulator and the remainder of the accumulator is masked to zeroes. The LSBs are then stored in R3 as shown in Figure 4. \overline{CS} is then set and the process is completed. At this point the data is left justified.

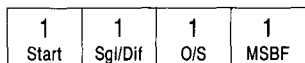


Figure 3. D_{IN} Word for LTC1091

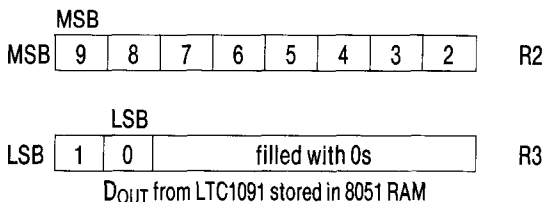


Figure 4. Memory Map

LABEL	MNEMONIC	COMMENTS
BEGIN	SETB P1.4	\overline{CS} GOES HIGH
AGAIN	MOV A, #FFH	D_{IN} WORD FOR LTC1091
	CLR P1.4	\overline{CS} GOES LOW
	MOV R4, #04H	LOAD COUNTER
LOOP1	RLC A	ROTATE D_{IN} BIT INTO CARRY
	CLR P1.3	SCLK GOES LOW
	MOV P1.2, C	OUTPUT D_{IN} BIT TO LTC1091
	SETB P1.3	SCLK GOES HIGH
	DJNZ R4, LOOP1	NEXT BIT
	MOV P1, #04H	BIT 2 BECOMES AN INPUT
	CLR P1.3	SCLK GOES LOW
	MOV R4, #09H	LOAD COUNTER
LOOP	MOV C, P1.2	READ DATA BIT INTO CARRY
	RLC A	ROTATE DATA BIT INTO CARRY
	SETB P1.3	SCLK GOES HIGH
	CLR P1.3	SCLK GOES LOW
	DJNZ R4, LOOP	NEXT BIT
	MOV R2, A	STORE MSBs IN R2
	MOV C, P1.2	READ DATA BIT INTO CARRY
	SETB P1.3	SCLK GOES HIGH
	CLR P1.3	SCLK GOES LOW
	CLR A	CLEAR ACC
	RLC A	ROTATE DATA BIT TO ACC
	MOV C, P1.2	READ DATA BIT INTO CARRY
	RRC A	ROTATE RIGHT INTO ACC
	RRC A	ROTATE RIGHT INTO ACC
	ANL A, #C0H	MASK UNUSED BITS
	MOV R3, A	STORE LSBs IN R3
	SETB P1.4	\overline{CS} GOES HIGH

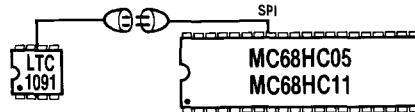
Figure 5. Code

Summary

A three wire interface between the LTC1091 and the 8051 with a combined data conversion and transfer time of 57 μ s was demonstrated. The data is transferred MSB first and resides in two bytes of the 8051 RAM in a left justified format. The code shown applies to all MCS-51 family members. The same technique can be used on any parallel port processor which allows individual bits to be programmed as inputs or outputs.

Interfacing the LTC1091 to the MC68HC05 MCU

Guy Hoover
 William Rempfer



Introduction

This application note describes an interface between the LTC1091 10-bit data acquisition system and the Motorola SPI family of single chip microcomputers (e.g., 68HC05). The simple four wire interface is capable of completing a 10-bit conversion and shifting the data to the 68HC05 in 58 μ s. Configuration of the LTC1091 and the 68HC05 will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be shown. Finally, a summary of the key points of this interface will be given, including data throughput rates.

Interface Details

The LTC1091 has one clock line which controls the A/D conversion rate and the data shift rate. Data is transferred in a half duplex, synchronous format over D_{IN} and D_{OUT}.

The Motorola Serial Peripheral Interface (SPI) is a synchronous, full duplex, serial port built into the 68HC05 that allows the user to construct a simple communication path to the LTC1091. SPI provides clock, data in and data out lines that are compatible with the LTC1091. The only

additional line required is one programmable output pin (C0) to control \overline{CS} on the LTC1091. The schematic of Figure 1 shows how the two devices are connected.

Hardware Description

The 68HC05 was emulated and the code for this interface was developed on a Motorola M68HC05 EVM.

\overline{SS} (Pin 34) of the 68HC05 must be held high to enable the SPI properly for this interface.

The timing diagram of Figure 2 was obtained with an HP1631A logic analyzer using a 4MHz clock for the 68HC05.

The analog section of the schematic in Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1091 please see the data sheet.

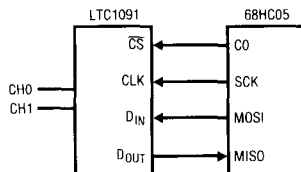


Figure 1. Schematic

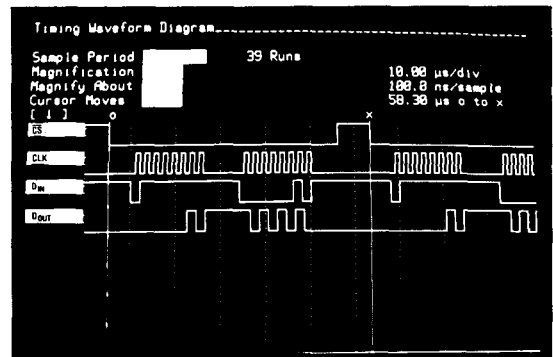


Figure 2. Timing Diagram

Application Note 26H

Software Description

The software configures and controls the SPI of the 68HC05. Additionally, the software manipulates C0 (CS of the LTC1091).

The code first configures the Serial Peripheral Control Register (SPCR) of the SPI. The SPI interrupt is disabled. The SPI outputs are enabled. The SPI is configured as a master. Finally, the SPI clock is set to normally low, for data transfer on the rising edge and for a frequency equal to one fourth the internal processor clock (one eighth the crystal frequency).

Port C is configured as all outputs by placing ones in the data direction register of port C. A D_{IN} word that configures the LTC1091 for CH1 with respect to ground and MSB first is stored in \$50. Figure 3 shows how the D_{IN} word is composed. Leading zeroes in the D_{IN} word are ignored. This makes it easy to position the D_{OUT} word on exact byte boundaries so that shifting the data to right justify it is not necessary.

C0 is made to go low. D_{IN} for the LTC1091 is loaded into the SPI data register. Storing D_{IN} in the data register causes the transfer to begin. The status register of the SPI is tested until the SPIF bit is set which indicates the transfer is finished. Reading the SPI status register clears the SPIF bit and allows the data register to be read, which is the next step. The first eight bits containing the MSBs from the LTC1091 are then stored in \$60 of the 68HC05 as shown in Figure 4. The LSBs are transferred in the same manner and stored in \$61 of the 68HC05.

0	1	1	1	1	1	1	1
Ignore	Start	S/D	O/S	MSBF	don't care	don't care	don't care

Figure 3. 4-Bit D_{IN} Word for LTC1091 in \$50

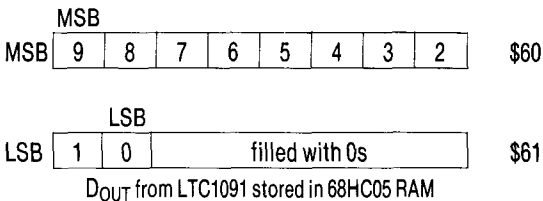


Figure 4. Memory Map

LABEL	MNEMONIC	COMMENTS	
	LDA	#\$51	DATA FOR SPCR
	STA	\$0A	LOAD DATA INTO SPCR
	LDA	#\$FF	DATA FOR DDR
	STA	\$06	CONFIGURE PORT C DDR
	LDA	#\$7F	D _{IN} WORD FOR LTC1091
	STA	\$50	PUT D _{IN} WORD IN \$50
START	BCLR	0, \$02	C0 (CS) GOES LOW
	LDA	\$50	PUT D _{IN} WORD IN ACC
	STA	\$0C	START TRANSFER
TEST	TST	\$0B	TEST IF DONE
	BPL	TEST	IF NOT TRY AGAIN
	LDA	\$0C	LOAD MSBs IN ACC
	STA	\$0C	START NEXT TRANSFER
	AND	#\$03	MASK UNUSED BITS
	STA	\$60	STORE MSBs IN \$60
TEST1	TST	\$0B	TEST IF DONE
	BPL	TEST1	IF NOT TRY AGAIN
	BSET	0, \$02	C0 (CS) GOES HIGH
	LDA	\$0C	PUT LSBs IN ACC
	STA	\$61	PUT LSBs IN \$61

Figure 5. 68HC05 Code

The code was written for the 68HC05. By changing the addresses of the special function registers however, the code should run on all of Motorola's SPI processors including the 68HC11.

Summary

A four wire interface between the LTC1091 and the 68HC05 with a combined data conversion and transfer time of 58μs was demonstrated. The interface used the serial (SPI) port of the 68HC05. The 10 data bits of the LTC1091 are shifted MSB first in two eight bit transfers. The data is stored left justified in the 68HC05's internal RAM.

Interfacing the LTC1091 to the COP820C MCU

Guy Hoover
 William Rempfer

Introduction

This application note describes the hardware and software required for communication between the LTC1091 10-bit data acquisition system and the National Semiconductor COP800 microcontroller family which uses the MICROWIRE/PLUS serial interface. The simple four wire interface is capable of completing a 10-bit conversion and shifting the data in $45\mu\text{s}$. Configuration of the LTC1091 and the COP820C will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be shown. Finally, a summary of the key points of this interface will be given including data throughput rates.

Interface Details

The LTC1091 clock line controls the A/D conversion rate and the data shift rate. Data is transferred in a half duplex, synchronous, format over D_{IN} and D_{OUT} .

The National Semiconductor MICROWIRE/PLUS is a synchronous, full duplex, serial port built into the COP800 family that allows easy interface to the LTC1091. MICROWIRE/PLUS provides clock, data in and data out lines that are compatible with the LTC1091. One additional line (G1) is required to control the \overline{CS} pin on the LTC1091. The schematic of Figure 1 shows how the two devices are connected.

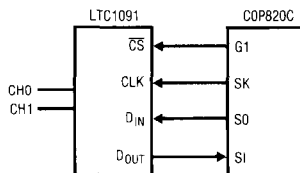
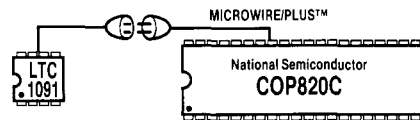


Figure 1. Schematic



Hardware Description

The actual interface was done using the COP820C, a member of the COP800 family. All code shown here should work with any of the COP800 family.

The code for this interface was developed on a COP820 evaluation board operated in the emulation mode.

The timing diagram of Figure 2 was obtained with an HP1631A logic analyzer. A 5MHz COP820C clock ($2\mu\text{s}$ instruction cycle) was used. By operating the MCU with a $1\mu\text{s}$ instruction cycle (high speed option) the minimum conversion and transfer time of $45\mu\text{s}$ is achieved.

The analog section of the schematic in Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1091 please see the data sheet.

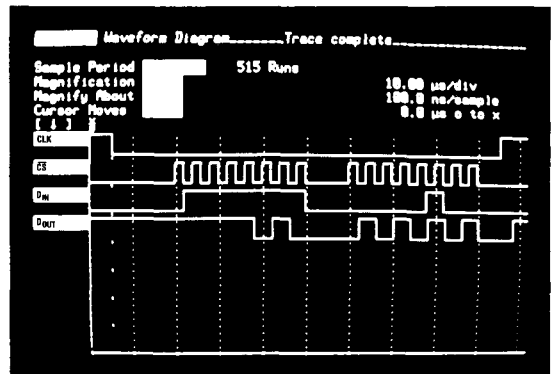


Figure 2. Timing Diagram

Application Note 261

Software Description

The software configures and controls the MICROWIRE/PLUS serial interface of the COP820C. Additionally, the software manipulates G1 (\overline{CS} of the LTC1091).

The code first loads the D_{IN} word of the LTC1091 into the memory address \$F0. The D_{IN} word (\$7F) contains a leading zero which is ignored, followed by a start bit. The next two bits configure the LTC1091 for CH1 with respect to ground. The fifth bit configures the A/D for MSB first mode and the remaining three LSBs are ignored as shown in Figure 3.

Next port G is configured such that pin G1 is an output and the MICROWIRE/PLUS serial port is a master. The control register is configured to enable SO and SK. Also the SK divide by is set up in such a way that the SK clock rate is equal to the crystal frequency divided by 20. The address of the port G data register is put into the B register so that the individual bits of port G can be manipulated. G1 (\overline{CS}) is then initialized by setting it high.

The D_{IN} word is then loaded into the accumulator. G1 is cleared and the LTC1091 D_{IN} word is loaded into the MICROWIRE™ shift register. The busy bit is set which begins the data transfer. 16 NOPs are used as a timer to allow the transfer to be completed. After the transfer is complete the D_{OUT} information is loaded into the accumulator and the next eight bits start to shift. The six MSBs in the accumulator are set to zeroes and the result is stored in \$F3. Nine NOPs are then used to wait until the second eight bits have been shifted. G1 (\overline{CS}) is then set and the

0	1	1	1	1	1	1	1
Ignore	Start	S/D	O/S	MSBF	don't care	don't care	don't care

Figure 3. 4-Bit D_{IN} Word for LTC1091 in \$F0

MSB								
filled with zeroes						9	8	F3
LSB								
7	6	5	4	3	2	1	0	F4

D_{OUT} from LTC1091 stored in COP820C RAM

Figure 4. Memory Map

LABEL	MNEMONIC	COMMENTS
	LD (F0) — \$7F	LOAD D_{IN} WORD INTO \$F0
	LD (D5) — \$32	G1 IS OUT, MICROWIRE MASTER
	LD (EE) — \$08	ENABLE SO, SK
	LD (B) — \$D4	PORT G DATA ADDR INTO B
	SBIT 1	G1 SET (CS GOES HIGH)
LOOP	LD (A) — (F0)	PUT LTC1091 D_{IN} WORD IN ACC
	RBIT 1	G1 CLEARED (CS GOES LOW)
	X (A) — — (E9)	D_{IN} IN MICROWIRE SHIFT REG.
	LD (B) — \$EF	PUT PSW REG. ADDR. INTO B
	SBIT 2	BUSY BIT SET TRANSFER START
	NOP	16 NOPs FOR TIMING
	X (A) — — (E9)	LOAD D_{OUT} INTO ACC
	SBIT 2	BUSY BIT SET TRANSFER START
	AND #03	MASK OUT UNUSED BITS
	X (A) — — (F3)	LOAD D_{OUT} INTO ADDR F3
	NOP	
	LD (B) — \$D4	PORT G DATA REG. ADDR. IN B
	SBIT 1	G1 SET (CS GOES HIGH)
	X (A) — — (E9)	LOAD D_{OUT} INTO ACC
	X (A) — — (F4)	LOAD LSB INTO ADDR. F4

Figure 5. Code

data is loaded into the accumulator. The LSBs are then loaded into memory location \$F4. The data at this point is right justified. With the appropriate shift routine the data can be easily left justified.

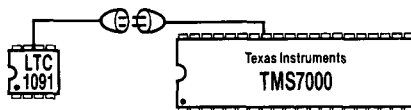
Summary

A four wire interface between the LTC1091 and the COP820C with a combined data conversion and transfer time of 45 μ s was demonstrated. The interface used the MICROWIRE/PLUS serial port of the COP820C. The 10 data bits of the LTC1091 are shifted MSB first in two eight bit transfers. The data is stored right justified in the COP820C's internal RAM.

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Interfacing the LTC1091 to the TMS7742 MCU

Guy Hoover



Introduction

This application note describes an interface between the LTC1091 10-bit data acquisition system and the TMS7000 family of microcomputers (e.g., TMS7742). The simple four wire interface is capable of completing a 10-bit conversion and shifting the data to the TMS7742 in 99 μ s. Configuration of the LTC1091 and the TMS7742 will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be shown. Finally, a summary of the key points of this interface will be given including data throughput rates.

Interface Details

The LTC1091 clock line controls the A/D conversion rate and the data shift rate. Data is transferred in a synchronous, half duplex format over D_{IN} and D_{OUT} .

The TMS7742 contains a synchronous, full duplex, serial port that allows the user to construct a simple communication path to the LTC1091. The serial port provides clock, transmit and receive lines that are compatible with the LTC1091. The only additional line required is one programmable output pin (A0) to control \overline{CS} on the LTC1091.

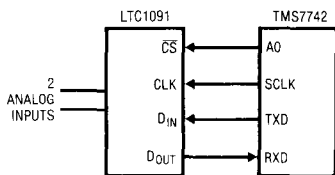


Figure 1. Schematic

The schematic of Figure 1 shows how the two devices are connected.

Hardware Description

The TMS7742 was chosen because it contains 4k of EPROM which can be programmed using a standard EPROM programmer. Any member of the TMS7000 family which contains a serial port should be able to use this code with only modifications to the peripheral register numbers.

The timing diagram of Figure 2 was obtained using an HP1631A logic analyzer. The TMS7742 clock was 5 MHz.

The analog section of the schematic of Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1091 please see the data sheet.

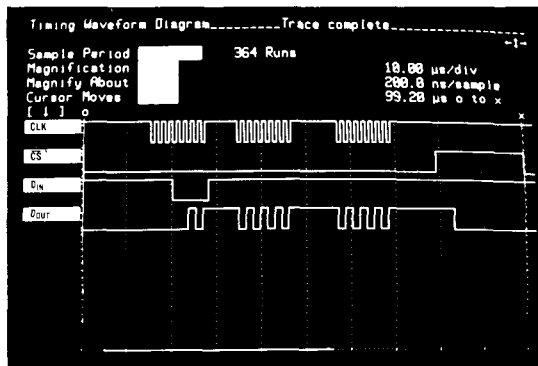


Figure 2. Timing Diagram

Application Note 26J

Software Description

The software configures and controls the serial port of the TMS7742. Additionally, the software manipulates A0 (\overline{CS} of the LTC1091).

The code first disables all interrupts and initializes the stack. The data direction register for the A port then sets A5 (RXD) as an input and all other bits including A0 (\overline{CS}) as outputs. Next the serial port is configured. Tx is enabled, the serial port is reset, and the SMODE register is configured for 8 bits, no parity, and one stop bit. The SCLK rate is set to the processor clock frequency divided by 4.

The SCLK is turned off and A0 (\overline{CS}) is cleared. The D_{IN} word of the LTC1091 is loaded into the TXBUF. This D_{IN} word (07) configures the LTC1091 for CH1 with respect to ground and LSB first. Examine Figure 3 to see how this is constructed keeping in mind that the TMS7742 transmits data LSB first. The serial port and SCLK are turned on and the data is shifted while the processor idles in a loop. The first eight bits contain the D_{IN} word and the first three MSBs of the D_{OUT} word. (The LTC1091 clocks out the data MSB first and then LSB first when in the LSB first mode.) The serial port is turned on again and the next eight bits containing the rest of the MSB first data and the first two bits of the LSB first data are shifted while the processor idles in a loop. The data containing the LSBs is then placed in the B register. The procedure is repeated for the next eight bits which contain the MSBs and the result is placed in the A register. A0 (\overline{CS}) is then set. The data in the B register is stored in R5. If desired the lowest six bits of the B register can be cleared by adding them with \$C0. The data in the A register is stored in R6. The data is now stored left justified as shown in Figure 4.

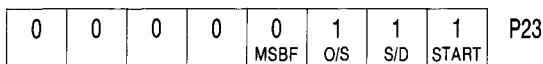


Figure 3. D_{IN} Word for LTC1091 Stored in TMS7742 TXBUF

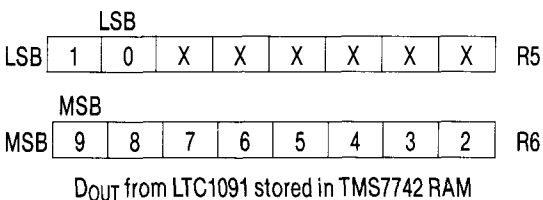


Figure 4. Memory Map

LABEL	MNEMONIC	COMMENTS
START	DINT	DISABLES ALL INTERRUPTS
	MOVP % > 2A, P0	DISABLE INTERRUPT FLAGS
	MOVP % > 02, P16	DISABLE INTERRUPT FLAGS
	MOV % > 60, B	ADDRESS OF STACK
	LDSP	PUT ADDRESS INTO POINTER
	MOVP % > DF, P5	CONFIGURE PORT A
	MOVP % > 08, P6	ENABLE Tx BY SETTING B3 = 1
	MOVP % > 00, P17	P17 POINTS TO SCTL0
	MOVP % > 40, P17	RESET THE SERIAL PORT
	MOVP % > 0C, P17	CONFIGURE THE SERIAL PORT
	MOVP % > 00, P21	TURN START BIT OFF
	MOVP % > 00, P17	ENABLE THE SERIAL PORT
	MOVP % > 00, P20	SET SCLK RATE (TIMER 3)
LOOP	MOVP % > 40, P21	SCLK OFF
	ANDP % > FE, P4	A0 CLEARED (\overline{CS} GOES LOW)
	MOVP % > 07, P23	PUT LTC1091 D_{IN} INTO TXBUF
	MOVP % > 17, P17	ENABLE SERIAL PORT
	MOVP % > C0, P21	SCLK ON (TRANSFER BEGINS)
	MOVP % > 14, P17	TXEN GOES LOW
	MOV % > 02, A	LOAD COUNTER
WAIT	DJNZ A, WAIT	LOOP WHILE SHIFT OCCURS
	NOP	MORE DELAY
	MOVP % > 17, P17	ENABLE SERIAL PORT
	MOVP % > 14, P17	TXEN GOES LOW
	MOV % > 02, A	LOAD COUNTER
WAIT1	DJNZ A, WAIT1	LOOP WHILE SHIFT OCCURS
	NOP	DELAY
	MOVP P22, B	PUT D_{OUT} FROM LTC1091 IN B
	MOVP % > 17, P17	ENABLE SERIAL PORT
	MOVP % > 14, P17	TXEN GOES LOW
	MOV % > 02, A	LOAD COUNTER
WAIT2	DJNZ A, WAIT2	LOOP WHILE SHIFT OCCURS
	NOP	DELAY
	MOVP P22, A	PUT D_{OUT} FROM LTC1091 IN A
	ORP % > 01, P4	A0 SET (\overline{CS} GOES HIGH)
	MOV B, R5	PUT FIRST 2 LSBs IN R5
	MOV A, R6	PUT MSBs IN R6

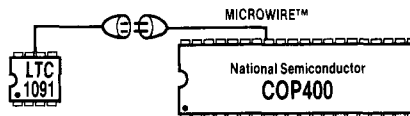
Figure 5. TMS7742 Code

Summary

A four wire interface between the LTC1091 and the TMS7742 with a combined data conversion and transfer time of 99 μ s was demonstrated. The interface used the serial port of the TMS7742. Because the serial port transfers data LSB first, care must be taken to properly construct the D_{IN} word so that the bits are transmitted in the proper order to the LTC1091. The 10 data bits of the LTC1091 are shifted LSB first in three eight bit transfers. The data is stored left justified in the TMS7742's internal RAM.

Interfacing the LTC1091 to the COP402N MCU

Guy Hoover



Introduction

This application note describes the hardware and software required for communication between the LTC1091 10-bit data acquisition system and the National Semiconductor COP400 microcontroller family which uses the MICROWIRE serial interface. The simple four wire interface is capable of completing a 10-bit conversion and shifting the data in 116 μ s. Configuration of the LTC1091 and the COP402N will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be shown. Finally, a summary of the key points of this interface will be given including data throughput rates.

Interface Details

The LTC1091 clock line controls the A/D conversion rate and the data shift rate. Data is transferred in a half duplex format over D_{IN} and D_{OUT}.

The National Semiconductor MICROWIRE interface is a synchronous, full duplex, serial port built into the COP400 family that allows the user to easily interface to the LTC1091. MICROWIRE provides clock, data in and data out lines that are compatible with the LTC1091. One addi-

tional line (G0) is required to control the \overline{CS} pin on the LTC1091. The schematic of Figure 1 shows how the two devices are connected.

Hardware Description

The actual interface will involve using the COP402N, a member of the COP400 family. All code shown here should work with any of the COP400 family.

The code for this interface was developed on a COP400 evaluation board which allows an external EPROM to be used in place of the internal processor ROM.

The timing diagram of Figure 2 was obtained with an HP1631A logic analyzer. The COP402N clock was 4MHz.

The analog section of the schematic in Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1091 please see the data sheet.

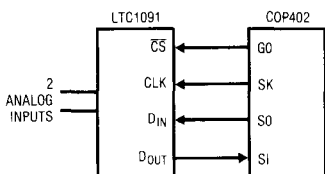


Figure 1. Schematic

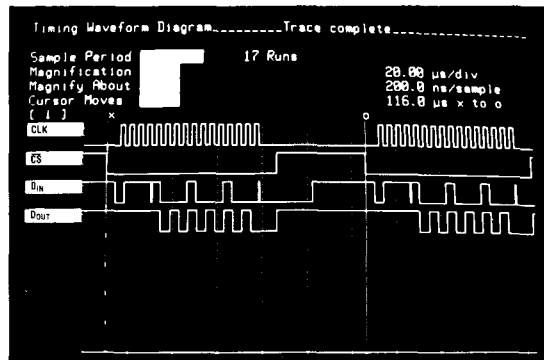


Figure 2. Timing Diagram

Application Note 26K

Software Description

The software configures and controls the MICROWIRE serial interface of the COP402N. Additionally, the software manipulates G0 (\overline{CS} of the LTC1091).

The code first initializes the B register and then loads the LTC1091 D_{IN} word into the RAM of the COP402 one nibble at a time. As shown in Figure 3 the D_{IN} word configures the LTC1091 for CH1 with respect to GND and MSB first. SO is configured as an output. The carry is set so that when an XAS instruction is generated the shift clock (SK) will begin clocking data.

The first nibble of the D_{IN} word is loaded into the ACC and G0 (\overline{CS}) is cleared. The D_{IN} nibble is loaded into the shift register and the data begins to shift. The second nibble of the D_{IN} word is loaded into the ACC. One NOP is allowed for timing and then the contents of the ACC are swapped with those of the shift register. The transfer continues. One NOP is allowed for timing. The second D_{IN} nibble is loaded into the ACC again and the contents of the ACC are swapped with those of the shift register. The MSBs of the LTC1091 D_{OUT} word are now in the ACC. This data is then stored in memory location \$13. The ACC is loaded with the second D_{IN} nibble from RAM and another swap

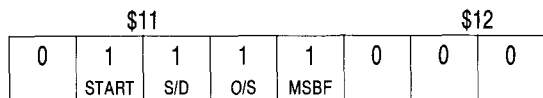
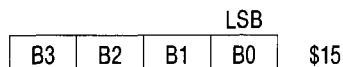
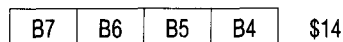
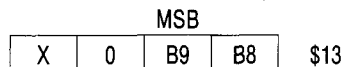


Figure 3. D_{IN} Word for LTC1090



D_{OUT} from LTC1091 stored in COP402 RAM

Figure 4. Memory Map

LABEL	MNEMONIC	COMMENTS
	CLRA	MUST BE FIRST INSTRUCTION
LBI	1,1	BR = 1 BD = 1 INITIALIZE B REG.
STII	7	FIRST D_{IN} NIBBLE IN \$11
STII	8	SECOND D_{IN} NIBBLE IN \$12
LEI	8	SET EN TO (1000) BIN
SC		CARRY SET
LDD	1,1	LOAD FIRST D_{IN} NIBBLE IN ACC
OGI	50	GO (\overline{CS}) CLEARED
XAS		ACC TO SHIFT REG. BEGIN SHIFT
LDD	1,2	LOAD NEXT D_{IN} NIBBLE IN ACC
NOP		TIMING
XAS		NEXT NIBBLE, SHIFT CONTINUES
NOP		TIMING
LDD	1,2	LOAD NULL DATA IN ACC
XAS		NEXT NIBBLE, SHIFT CONTINUES
XIS	0	FIRST NIBBLE D_{OUT} TO \$13
LDD	1,2	LOAD NULL DATA IN ACC
XAS		SHIFT CONTINUES, D_{OUT} - ACC
XIS	0	NEXT NIBBLE D_{OUT} TO \$14
RC		CLEAR CARRY
CLRA		CLEAR ACC
XAS		THIRD NIBBLE D_{OUT} TO ACC
OGI	51	GO (\overline{CS}) SET
XIS	0	THIRD NIBBLE D_{OUT} TO \$15
LBI	1,3	SET B REG. FOR NEXT LOOP

Figure 5. COP402 Code

between the ACC and the shift register is executed. The next D_{OUT} nibble is stored in \$14. The carry is cleared so that on the next XAS instruction the shift clock will stop. The XAS instruction is executed and the final nibble of the LTC1091 D_{OUT} word containing the LSBs is loaded into the ACC. G0 (\overline{CS}) is taken high. The third D_{OUT} nibble is stored in location \$15. The B register is then reinitialized so that when the loop is run again the data will always be stored in the same memory locations. The D_{OUT} data from the LTC1091 is now in a right justified format as shown in Figure 4.

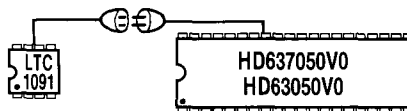
Summary

A four wire interface between the LTC1091 and the COP402N with a combined data conversion and transfer time of 116 μ s was demonstrated. The interface used the MICROWIRE serial port of the COP402N. The 10 data bits of the LTC1091 are shifted MSB first in four four bit transfers. The data is stored right justified in the COP402N's internal RAM. The code demonstrated will work on any member of the COP400 family.

MICROWIRE is a trademark of National Semiconductor Corp.

Interfacing the LTC 1091 to the HD637050 MCU

Guy Hoover
William Rempfer



Introduction

This application note describes an interface between the LTC1091 10-bit data acquisition system and the Hitachi 63705 microcomputer. The simple four wire interface is capable of completing a 10-bit conversion and shifting the data to the 63705 in 84 μ s. Configuration of the LTC1091 and the 63705 will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be shown. Finally, a summary of the key points of this interface will be given including data throughput rates.

Interface Details

The LTC1091 clock line controls the A/D conversion rate and the data shift rate. Data is transferred in a half duplex synchronous format over D_{IN} and D_{OUT}.

The Hitachi Serial Communication Interface (SCI) is a synchronous, full duplex, serial port built into the 63705 that allows the user to construct a simple communication path to the LTC1091. SCI provides clock, transmit and receive lines that are compatible with the LTC1091. The only additional line required is one programmable output pin

(C0) to control \overline{CS} on the LTC1091. The schematic of Figure 1 shows how the two devices are connected.

Hardware Description

The 63705VOC was chosen for this application because it contains 4k bytes of EPROM which can be programmed by a 27256 EPROM programmer. The code shown will work on the 6305VO without modification.

The timing diagram of Figure 2 was obtained using an HP1631A logic analyzer. The 63705 clock was 4 MHz.

The analog section of the schematic of Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1091 please see the data sheet.

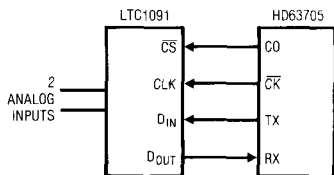


Figure 1. Schematic

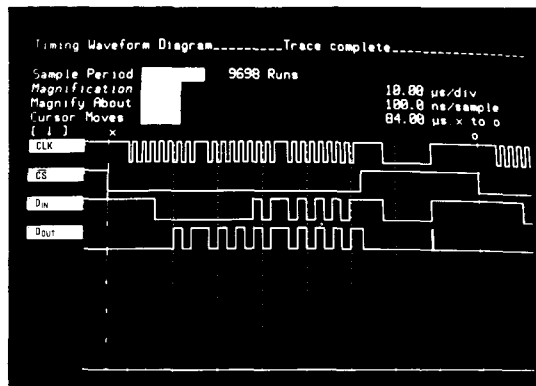


Figure 2. Timing Diagram

Application Note 26L

Software Description

The software configures and controls the SCI of the 63705. Additionally, the software manipulates C0 (\overline{CS} of the LTC1091).

The code first configures the SCI control register (SCR). D3 and D4 are set as the SCI output and input respectively. D5 is selected as a clock output with a frequency one eighth the crystal frequency. Next, the SCI status register (SSR) is configured so that the interrupts are disabled. Data is transmitted on the falling edge of the clock and received on the rising edge of the clock.

Bit 0 of Port C is configured as an output by setting the first bit of the data direction register (address \$06) to one. A D_{IN} word that configures the LTC1091 for CH1 with respect to ground and LSB first is stored in \$50. Figure 3 shows how the D_{IN} word is composed. Note, that for LSB first format the D_{IN} word must be constructed opposite from MSB first format.

C0 is made to go low. D_{IN} for the LTC1091 is loaded into the SCI data register (SDR). Storing D_{IN} in the SDR causes the transfer to begin. When LSB first is selected, the LTC1091 first clocks out the data MSB first and then clocks out the data LSB first. After waiting for the first eight bits to be transferred the data containing the MSBs is loaded into the ACC. This starts the next transfer. The next eight bits are then shifted out and the first two LSBs from the LTC1091 are loaded into the accumulator and then stored in \$61 of the 63705 RAM. The act of reading the

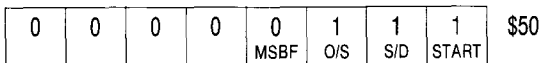


Figure 3. D_{IN} Word for LTC1091 Stored in 63705 RAM

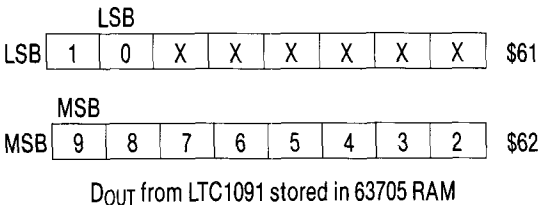


Figure 4. Memory Map

LABEL	MNEMONIC	COMMENTS	
LDA	#\$E1	CONFIGURATION DATA FOR SCR	
STA	\$10	LOAD DATA INTO SCR (\$10)	
LDA	#\$30	CONFIGURATION DATA FOR SSR	
STA	\$11	LOAD DATA INTO SSR (\$11)	
LDA	#\$01	CONFIG. DATA FOR PORT C DDR	
STA	\$06	LOAD DATA INTO PORT C DDR	
LDA	#\$07	LOAD LTC1091 D_{IN} DATA INTO ACC	
STA	\$50	LOAD LTC1091 D_{IN} DATA INTO \$50	
LOOP	LDA	\$50	LOAD D_{IN} INTO ACC FROM \$50
	BCLR	0,\$02	C0 GOES LOW (\overline{CS} GOES LOW)
	STA	\$12	LOAD D_{IN} INTO SDR. START SCK
	BCLR	1,\$06	FOR TIMING
	BCLR	1,\$06	FOR TIMING
	BCLR	1,\$06	FOR TIMING
	LDA	\$12	LOAD DATA START NEXT CYCLE
	BCLR	1,\$06	FOR TIMING
	BCLR	1,\$06	FOR TIMING
	BCLR	1,\$06	FOR TIMING
	LDA	\$12	LOAD LSBs START NEXT CYCLE
	STA	\$61	STORE LSBs IN \$61
	BCLR	1,\$06	FOR TIMING
	BCLR	1,\$06	FOR TIMING
	BSET	0,\$02	C0 GOES HIGH. (\overline{CS} GOES HIGH)
	LDA	#\$00	CONFIGURATION DATA FOR SCR
	STA	\$10	DISABLE SCI
	LDA	\$12	LOAD MSBs
	STA	\$62	STORE MSBs IN \$62
	LDA	#\$E1	CONFIGURATION DATA FOR SCR
	STA	\$10	TURN SCI ON

Figure 5. 63705 Code

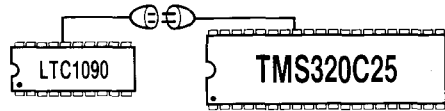
LSBs into the ACC causes the next SCI transfer to begin. After the next eight bits are transferred, then C0 is set and the SCI port is disabled. The MSBs from the LTC1091 are loaded into the ACC and then stored in \$62 of the 63705 RAM. The SCI port is then enabled. The data at this point is left justified as shown in Figure 4.

Summary

A four wire interface between the LTC1091 and the Hitachi 63705 with a combined data conversion and transfer time of $84\mu s$ was demonstrated. The interface used the serial (SCI) port of the 63705. Because the SCI port transfers data LSB first, care must be taken to properly construct the D_{IN} word so that the bits are transmitted in the proper order to the LTC1091. The 10 data bits of the LTC1091 are shifted MSB first and then LSB first in three eight bit transfers. The data is stored left justified in the 63705's internal RAM.

Interfacing the LTC1090 to the TMS320C25 DSP

Guy Hoover



Introduction

This application note describes the hardware and software required for communication between the LTC1090 10-bit data acquisition system and the TMS320C25 digital signal processor (DSP). In particular two interfaces will be demonstrated. The first interface requires only one inverter in addition to the LTC1090 and the TMS320C25. The second interface, which is optimized for speed of transfer and minimum processor supervision, can complete a conversion and shift the data in only 32 μ s. Configuration of the TMS320C25 and LTC1090 will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be presented. Finally, a summary of results including data throughput rates will be provided.

Interface Details

The LTC1090 has two clock lines: ACLK and SCLK. ACLK controls the A/D conversion rate while SCLK controls the data shift rate. Data is transferred in a synchronous, full duplex format over D_{IN} and D_{OUT}.

The serial port of the TMS320C25 is not directly compatible with that of the LTC1090. The data shift clock lines

(CLKR, CLKX) are inputs only. Therefore the data shift clock must be externally generated. Inverting the shift clock is also necessary because the LTC1090 and the TMS320C25 clock data on opposite edges. This prevents a race condition. The framing pulse width of the TMS320C25 is not long enough to be used as a chip select for the A/D directly. It must somehow be stretched. This can be done with additional hardware or through software control of the shift clock which controls the framing pulse timing.

The schematic of Figure 1 has the shift clock generated by the XF pin of the TMS320C25. The signal is inverted with a 74HC04 and fed into the SCLK pin of the LTC1090. The framing pulse is properly generated by delaying the SCLK edge which causes FSX to fall until the A/D conversion is finished. This method results in the simplest hardware configuration but has the drawbacks of requiring more processor supervision and a slower data shift time.

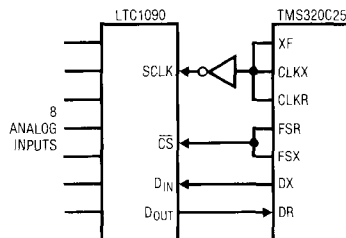
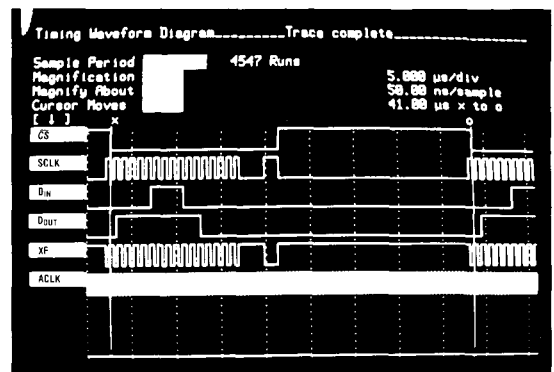


Figure 1. Circuit 1: Minimum Hardware Interface


 Figure 2. Timing for Circuit 1 Shows 41 μ s Throughput Rate

Application Note 26M

The schematic of Figure 7 has the shift clock generated by dividing down the processor clock with a 74HC163 counter. The signal is inverted with a 74HC04 and fed into the CLKX and CLKR pins of the TMS320C25. The \overline{CS} signal is generated with another 74HC163 and two inverters. The obvious disadvantage of this method is that it requires considerably more hardware to implement but it provides a faster data shift rate and requires less processor supervision.

Hardware Description

The DSP was emulated and the code for this interface was developed on a TMS320C25 Software Development System (SWDS). The SWDS requires a PC compatible computer to run.

The timing diagram of Figure 2 was obtained using the circuit of Figure 1. The timing diagram of Figure 8 was obtained using the circuit of Figure 7. Both pictures were taken with an HP1631 logic analyzer. ACLK was 2.5MHz and SCLK was 1.25MHz. The TMS320C25 clock rate was 40MHz.

The analog sections of the schematics of Figure 2 and Figure 7 are omitted for clarity. For a complete discussion of analog considerations involved in using the LTC1090 please see the data sheet.

B14				B7			
0	0	0	0	1	1	1	1
S/D	O/S	S1	S2	UNI	MSBF	WL1	WLO

Figure 3. D_{IN} Word in ACC of TMS320C25 for Circuit 1

MSB									LSB		
9	8	7	6	5	4	3	2	1	0	filled with 0s	>200

D_{OUT} from LTC1090 stored in TMS320C25 RAM

Figure 4. Memory Map for Circuit 1

LABEL	MNEMONIC	COMMENTS
AORG	0	ON RST CODE STARTS AT 0
B	INIT	BRANCH TO INIT ROUTINE
AORG	>26	ADDRESS OF RINT VECTOR
B	RINT	BRANCH TO RINT ROUTINE
AORG	>32	MAIN PROGRAM ADDRESS
INIT	DINT	DISABLE INTERRUPTS
	LDPK	DATA PAGE POINTER IS 0
	LARP	AUX. REG. POINTER IS 1
	LRLK	AUX. REG. 1 = >200
	LACK	CONFIG. WORD FOR IMR
	SACL	PUT CONFIG. WORD IN IMR
	STXM	CONFIGURE FSX AS OUTPUT
	FORT	SET SERIAL PORT TO 16 BITS
TXRX	RXF	RESET XF
	STC	SET TC BIT (FIRST TIME FLG)
	LACK	>F0 LOAD D_{IN} WORD INTO ACC
	SFSM	FSX STARTS ON XSR LOAD
	RPTK	2 REPEAT 3 TIMES
	SFL	SHIFT D_{IN} TO LEFT
	SACL	>1 D_{IN} PUT IN TX REGISTER
	EINT	ENABLE INTERRUPTS
TIMER	RXF	RESET XF (\overline{SCLK})
	RPTK	2 REPEAT 3 TIMES
	NOP	TIMING
	SXF	SET XF (\overline{SCLK})
	BBZ	TIMER SCLKS UNTIL RINT
	RPTK	>D0 DELAY FOR CONVERSION
	NOP	
	RTC	RESET TC (NOT FIRST TIME)
	B	TIMER NEXT SCLK
RINT	ZALS	>0 STORE D_{OUT} WORD IN ACC
	SFL	SHIFT ACC LEFT 1 BIT
	SACL	*0 STORE ACC IN >200
	B	TXRX GO TO TXRX ROUTINE
	END	

Figure 5. TMS320C25 Code for Circuit 1

Software Description

The software configures and controls the serial port of the TMS320C25. Additionally, the software generates a delay during which time the LTC1090 performs a conversion.

The first 13 lines of code are the same for circuit 1 and circuit 2. The code first sets up the interrupt and reset vectors. On reset the TMS320C25 starts executing code at the label INIT. Upon completion of a 16-bit data transfer, an interrupt is generated and the DSP will begin executing code at the label RINT.

Next, the code initializes registers in the TMS320C25 that will be used in the transfer routine. The interrupts are temporarily disabled. The data memory page pointer register is set to zero. The auxiliary register pointer is loaded with one and auxiliary register one is loaded with the value 200 hexadecimal. This is the data memory location where the data from the LTC1090 will be stored. The interrupt mask register (IMR) is configured to recognize the RINT interrupt, which is generated after receiving the last of 16 bits on the serial port. This interrupt is still disabled at this time however. The transmit framing synchronization pin (FSX) is configured to be an output. The F0 bit of the status register ST1, is initialized to zero which sets up the serial port to operate in the 16-bit mode.

The code for transmitting and receiving data is different for the two circuits. For circuit 1 the XF bit is first initialized to 0. The TC bit is set (TC is used as a flag to determine whether the processor is waiting for the A/D to perform a conversion, TC set, or whether the processor is shifting data, TC cleared). Next, the D_{IN} word is loaded into the ACC and shifted left three times so that it appears as in Figure 3. This D_{IN} word configures the LTC1090 for CH0 with respect to CH1, unipolar, MSB first, and 16-bit length. The D_{IN} word is then put in the transmit register and the RINT interrupt is enabled. For circuit 2 the code is similar except that XF and TC are not used. Also the D_{IN} word for circuit 2 configures the LTC1090 for 10 bits instead of 16 bits (Figure 6) because the additional hardware of circuit 2 allows fewer bits to be shifted which speeds up the transfer process. The circuit 1 code then causes the DSP to put out one SCLK cycle on the XF pin. This causes

the FSX pin (\overline{CS}) to go high. The FSX pin stays high until the DSP goes through 208 NOPs during which time the LTC1090 performs a conversion. The XF bit is then reset and set with a $0.8\mu s$ period until the RINT interrupt is generated. For the circuit 2 code the timer consists of only one instruction that loops upon itself until the RINT interrupt is generated. All clocking and \overline{CS} functions are performed by the hardware. This time could be used to do some simple processing of the data.

For circuit 1 once RINT is generated the code begins execution at the label RINT. This code stores the D_{OUT} word from the LTC1090 in the ACC, shifts it left one bit to position it properly and then stores it in location 200 hex. The data appears in location 200 hex left justified as shown in Figure 4. The code is set up to continually loop, so at this point the code jumps to label TXRX and repeats from there. The circuit 2 code handles the RINT interrupt in a similar fashion except that the data is shifted right five bits and is stored right justified as shown in Figure 10. Also the circuit 2 code has the delay for the LTC1090 in the RINT routine instead of during the TIMER routine.

Summary

Two interfaces between the LTC1090 10-bit data acquisition and the TMS320C25 DSP were demonstrated. The first interface required only one inverter in addition to the A/D and the DSP. The combined data conversion and transfer time of this interface was $41\mu s$. The data was placed in the internal RAM of the TMS320C25 in a left justified format. The second circuit, which required two counters and three inverters to implement, was able to perform a conversion and shift the data to the processor in only $32\mu s$. The data also was placed in the RAM of the TMS320C25 except that it was in a right justified format.

B14						B7	
0	0	0	0	1	1	0	1
S/D	O/S	S1	S2	UNI	MSBF	WL1	WL0

Figure 6. D_{IN} Word in ACC of TMS320C25 for Circuit 2

Application Note 26M

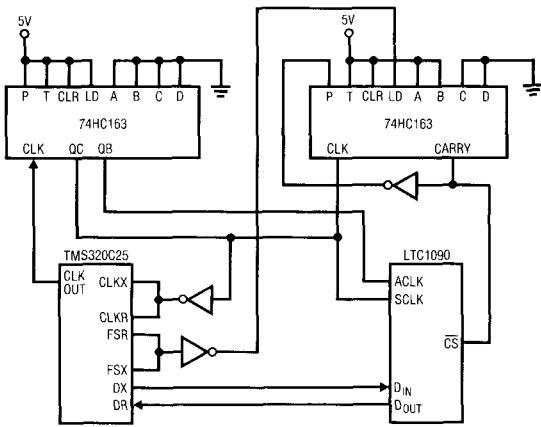


Figure 7. Circuit 2: Minimum Software Interface

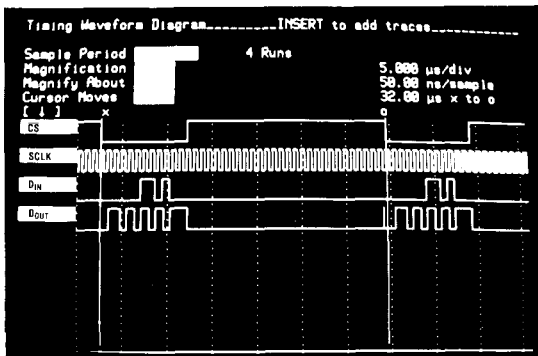
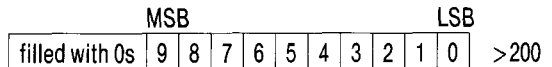


Figure 8. Timing for Circuit 2 shows 32µs Throughput Rate

LABEL	MNEMONIC	COMMENTS
AORG	0	ON RST CODE STARTS AT 0
B	INIT	BRANCH TO INIT ROUTINE
AORG	>26	ADDRESS OF RINT VECTOR
B	RINT	BRANCH TO RINT ROUTINE
INIT	AORG >32	MAIN PROGRAM ADDRESS
	DINT	DISABLE INTERRUPTS
	LDPK >0	DATA PAGE POINTER IS 0
	LARP >1	AUX. REG. POINTER IS 1
	LRLK AR1, >200	AUX. REG. 1 = >200
	LACK >10	CONFIG. WORD FOR IMR
	SACL >4	PUT CONFIG. WORD IN IMR
	STXM	CONFIGURE FSX AS OUTPUT
	FORT 0	SET SERIAL PORT TO 16 BITS
TXRX	LACK >D0	LOAD D _{IN} WORD INTO ACC
	SFSM	FSX STARTS ON XSR LOAD
	RPTK 2	REPEAT 3 TIMES
	SFL	SHIFT D _{IN} TO LEFT
	SACL >1	D _{IN} PUT IN TX REGISTER
	EINT	ENABLE INTERRUPTS
TIMER	B	TIMER
		LOOP UNTIL FINISHED
RINT	ZALS >0	STORE D _{OUT} WORD IN ACC
	RPTK >4	REPEAT 5 TIMES
	SFR	SHIFT ACC RIGHT 1 BIT
	SACL *,0	STORE ACC IN >200
	RPTK 127	DELAY
	NOP	22µS FOR
	RPTK 3	NEXT
	NOP	CONVERSION
	B	TXRX
		GO TO TXRX ROUTINE
	END	

Figure 9. TMS320C25 Code for Circuit 2

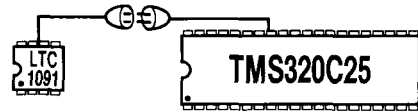


D_{OUT} from LTC1090 stored in TMS320C25 RAM

Figure 10. Memory Map for Circuit 2

Interfacing the LTC1091/92 to the TMS320C25 DSP

Guy Hoover



Introduction

This application note describes the hardware and software required for communication between the LTC1091 10-bit data acquisition system and the TMS320C25 digital signal processor (DSP). In particular two interfaces will be demonstrated. The first interface requires only one inverter in addition to the LTC1091 and the TMS320C25. The second interface, which is optimized for speed of transfer and minimum processor supervision, can complete a conversion and shift the data in only 32 μ s. Configuration of the TMS320C25 and LTC1091 will be discussed as it applies to this interface as well as the minor modifications required for the interface to work with the LTC1092. Schematics, code, and timing diagrams will be presented. Finally, a summary of results including data throughput rates will be provided.

Interface Details

The LTC1091 clock line controls the A/D conversion rate and the data shift rate. Data is transferred in a syn-

chronous, half duplex format over D_{IN} and D_{OUT} . The serial port of the TMS320C25 is not directly compatible with that of the LTC1091. The data shift clock lines (CLKR, CLKX) are inputs only. Therefore the data shift clock must be externally generated. Inverting the shift clock is also necessary because the LTC1091 and the TMS320C25 clock data on opposite edges. This prevents a race condition.

The schematic of Figure 1 has the shift clock generated by the XF pin of the TMS320C25. The signal is inverted with a 74HC04 and fed into the CLK pin of the LCT1091. The framing pulse of the TMS320C25 is fed directly to the \overline{CS} of the LTC1091. DX and DR are tied directly to D_{IN} and D_{OUT} respectively. This method results in the simplest hardware configuration but has the drawbacks of requiring more processor supervision and a slower data shift time.

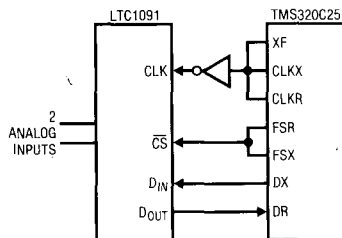


Figure 1. Circuit 1: Minimum Hardware Interface

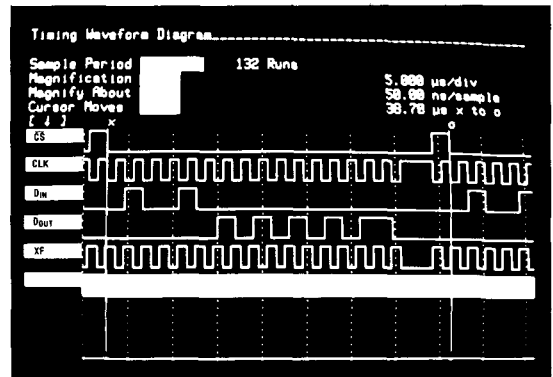


Figure 2. Timing for Circuit 1 Shows 39 μ s Throughput Rate

Application Note 26N

The schematic of Figure 6 has the clock generated by dividing down the CLK OUT pin by a factor of 16 with a 74HC163 counter. The signal is inverted with a 74HC04 and fed into the CLK pin of the LTC1091. The \overline{CS} signal is generated directly from the FSX pin of the TMS320C25. The obvious disadvantage of this method is that it requires considerably more hardware to implement but it provides a faster data shift rate and requires less processor supervision.

Hardware Description

The DSP was emulated and the code for this interface was developed on a TMS320C25 Software Development System (SWDS). The SWDS requires a PC compatible computer to run.

The timing diagram of Figure 2 was obtained using the circuit of Figure 1. The timing diagram of Figure 7 was obtained using the circuit of Figure 6. Both pictures were taken with an HP1631 logic analyzer. The CLK was 500kHz for the timing diagram of Figure 2 and 625kHz for the timing diagram of Figure 7. The TMS320C25 clock rate was 40MHz.

The analog sections of the schematics of Figure 1 and Figure 6 are omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1091 please see the data sheet.

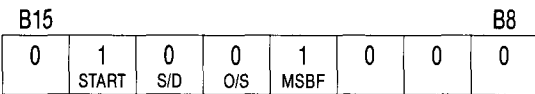
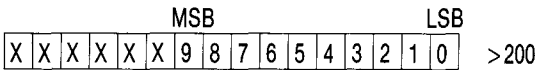


Figure 3. D_{IN} Word in ACC of TMS320C25 for Circuits 1 and 2



D_{OUT} from LTC1091 stored in TMS320C25 RAM

Figure 4. Memory Map for Circuits 1 and 2

LABEL	MNEMONIC	COMMENTS
	AORG 0	ON RST CODE STARTS AT 0
	B INIT	BRANCH TO INIT ROUTINE
	AORG >26	ADDRESS OF RINT VECTOR
	B RINT	BRANCH TO RINT ROUTINE
INIT	AORG >32	MAIN PROGRAM ADDRESS
	DINT	DISABLE INTERRUPTS
	LDPK >0	DATA PAGE POINTER IS 0
	LARP >1	AUX. REG. POINTER IS 1
	LRLK AR1, >200	AUX. REG. 1 = >200
	LACK >10	CONFIG. WORD FOR IMR
	SACL >4	PUT CONFIG. WORD IN IMR
	STXM	CONFIGURE FSX AS OUTPUT
	FORT 0	SET SERIAL PORT TO 16 BITS
	RXF	RESET XF
TXRX	LACK >48	LOAD D_{IN} WORD INTO ACC
	SFSM	FSX STARTS ON XSR LOAD
	RPTK 7	REPEAT 8 TIMES
	SFL	SHIFT D_{IN} TO LEFT
	SACL >1	D_{IN} PUT IN TX REGISTER
TIMER	EINT	ENABLE INTERRUPTS
	SXF	SET XF (\overline{CLK})
	RPTK 5	REPEAT 6 TIMES
	NOP	TIMING
	RXF	RESET XF (\overline{CLK})
	RPTK 3	REPEAT 4 TIMES
	NOP	NOP FOR TIMING
B TIMER	CLKS UNTIL RINT	
RINT	ZALS >0	STORE D_{OUT} WORD IN ACC
	SACL *, 0	STORE ACC IN >200
	B TXRX	GO TO TXRX ROUTINE
	END	

Figure 5. TMS320C25 Code for Circuit 1

Software Description

The software configures and controls the serial port of the TMS320C25.

The first 13 lines of code are the same for circuit 1 and circuit 2. The code first sets up the interrupt and reset vectors. On reset the TMS320C25 starts executing code at the label INIT. Upon completion of a 16-bit data transfer, an interrupt is generated and the DSP will begin executing code at the label RINT.

Next, the code initializes registers in the TMS320C25 that will be used in the transfer routine. The interrupts are temporarily disabled. The data memory page pointer register is set to zero. The auxiliary register pointer is loaded with one and auxiliary register one is loaded with the value 200 hexadecimal. This is the data memory location where the data from the LTC1091 will be stored. The interrupt mask register (IMR) is configured to recognize the RINT interrupt, which is generated after receiving the last of 16 bits on the serial port. This interrupt is still disabled at this time however. The transmit framing synchronization pin (FSX) is configured to be an output. The F0 bit of the status register ST1, is initialized to zero which sets up the serial port to operate in the 16-bit mode. For circuit 1 the XF bit is first initialized to zero.

The code for transmitting and receiving data is the same for the two circuits except for the section of code labelled TIMER. The D_{IN} word is loaded into the ACC and shifted left eight times so that it appears as in Figure 3. This D_{IN} word configures the LTC1091 for CH0 with respect to CH1 and MSB first. The D_{IN} word is then put in the transmit register and the RINT interrupt is enabled. For circuit 1 the XF bit is set which causes the FSX pin to generate a \overline{CS} signal which is fed into the \overline{CS} pin of the LTC1091 and the FSR pin of the TMS320C25.

The XF bit is then reset and set with a $2.0\mu s$ period until the RINT interrupt is generated. For the circuit 2 code the timer consists of only one instruction that loops upon itself until the RINT interrupt is generated. All clocking and \overline{CS} functions are performed by the hardware. This time could be used to do some simple processing of the data.

Once RINT is generated the code begins execution at the label RINT. This code stores the D_{OUT} word from the LTC1091 in the ACC and then stores it in location 200 hex. The data appears in location 200 hex right justified as shown in Figure 4. The code is set up to continually loop, so at this point the code jumps to label TXRX and repeats from there.

The code for circuits 1 and 2 can be made to work with the LTC1092 as well with only minor modifications. It is not necessary to use a D_{IN} word for the LTC1092, which reduces the number of lines required by the interface. After the data has been shifted into the TMS320C25 it must be shifted twice to the left for left justified data or shifted four times to the right for right justified data.

Summary

Two interfaces between the LTC1091 10-bit data acquisition and the TMS320C25 DSP were demonstrated. The first interface required only one inverter in addition to the A/D and the DSP. The combined data conversion and transfer time of this interface was $39\mu s$. The data was placed in the internal RAM of the TMS320C25 in a right justified format. The second circuit, which required a counter and an inverter to implement, was able to perform a conversion and shift the data to the processor in only $32\mu s$. The data again was placed in the RAM of the TMS320C25 in a right justified format. With only minor modifications these interfaces can also be used with the LTC1092.

Application Note 26N

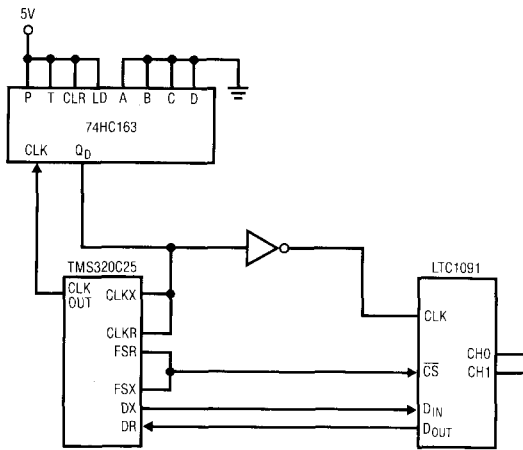


Figure 6. Circuit 2: Minimum Software Interface

LABEL	MNEMONIC	COMMENTS
AORG	0	ON RST CODE STARTS AT 0
B	INIT	BRANCH TO INIT ROUTINE
AORG	>26	ADDRESS OF RINT VECTOR
B	RINT	BRANCH TO RINT ROUTINE
INIT	AORG >32	MAIN PROGRAM ADDRESS
	DINT	DISABLE INTERRUPTS
	LDPK >0	DATA PAGE POINTER IS 0
	LARP >1	AUX. REG. POINTER IS 1
	LRLK AR1, >200	AUX. REG. 1 = >200
	LACK >10	CONFIG. WORD FOR IMR
	SACL >4	PUT CONFIG. WORD IN IMR
	STXM	CONFIGURE FSX AS OUTPUT
	FORT 0	SET SERIAL PORT TO 16 BITS
TXRX	LACK >48	LOAD D _{IN} WORD INTO ACC
	SFSM	FSX STARTS ON XSR LOAD
	RPTK 7	REPEAT 8 TIMES
	SFL	SHIFT D _{IN} TO LEFT
	SACL >1	D _{IN} PUT IN TX REGISTER
	EINT	ENABLE INTERRUPTS
TIMER	B	TIMER
		LOOP UNTIL FINISHED
RINT	ZALS >0	STORE D _{OUT} WORD IN ACC
	SACL *, 0	STORE ACC IN >200
	B	GO TO TXRX ROUTINE
	END	

Figure 8. TMS320C25 Code for Circuit 2

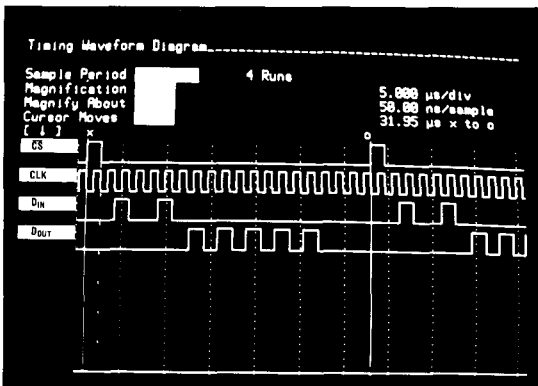


Figure 7. Timing for Circuit 2 Shows 32μs Throughput Rate

Interfacing the LTC1090 to the Z-80 MPU

Guy Hoover

Introduction

This application note describes an interface between the LTC1090 10-bit data acquisition system and the Z-80 microcomputer. The interface is capable of completing a 10-bit conversion and shifting the data to Z-80 in $288\mu\text{s}$. Configuration of the LTC1090 and the Z-80 will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be shown. Finally, a summary of the key points of this interface will be given, including data throughput rates.

Interface Details

The LTC1090 has two clock lines: ACLK and SCLK. ACLK controls the A/D conversion rate while SCLK controls the data shift rate. Data is transferred serially in a synchronous, full duplex format over D_{IN} and D_{OUT} .

The Z-80 does not have a serial port. Therefore it is necessary for the user to construct a serial port with TTL gates as shown in the schematic of Figure 1.

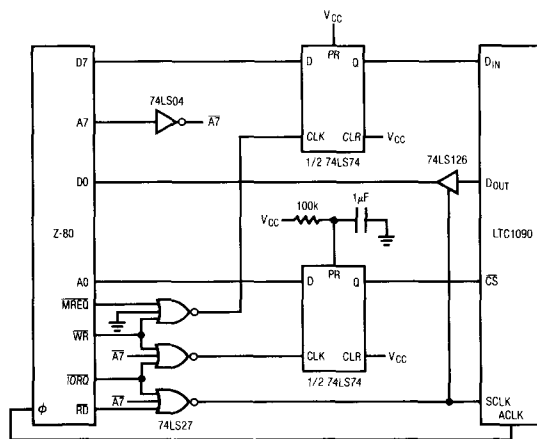
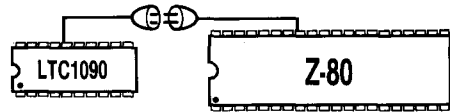


Figure 1. Serial Interface Requires Four 74LS Chips



Hardware Description

\overline{CS} is set or cleared by placing a 1 or a 0 on address line A0 and writing to an I/O port that has an even address of 128 or higher. The LTC1090 SCLK is generated by reading from an I/O port that has an address greater than 128. Data is clocked into the LTC1090 one bit at a time by placing the desired bit on D7 of the Z-80 and writing to any memory location. The serial data output of the LTC1090 is fed into D0 of the Z-80 through the 74LS126. The 74LS126 prevents the LTC1090 from writing to the data bus of the Z-80 except when the microprocessor requires data from the A/D. The ACLK of the LTC1090 is also the clock for the Z-80.

The code for this interface was developed on a Multitech MPF-1 single board development system.

The timing diagram of Figure 2 was obtained with an HP1631A logic analyzer. The Z-80 clock rate was 1.79MHz. Using a Z-80B and running it at a 6MHz clock rate, it is possible to reduce this time to approximately $100\mu\text{s}$. This would require generating ACLK externally or dividing down the ϕ signal.

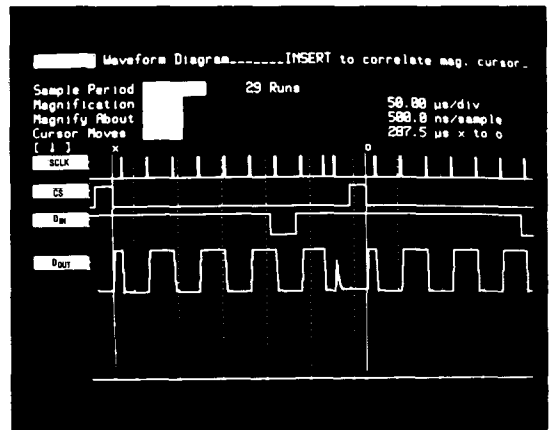


Figure 2. Throughput Time is Limited by the Z-80 MPU. A 10 Bit Conversion Result is Transmitted Every $288\mu\text{s}$.

Application Note 260

The analog section of the schematic of Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1090 please see the data sheet.

Software Description

The software serially shifts the D_{IN} configuration word to the LTC1090 while simultaneously reading the previous data back. Additionally, the software waits while the LTC1090 performs its next conversion before attempting the next data exchange cycle.

The code, Figure 5, first clears the C register. Next the E register, which is used as a counter, is loaded with the value 8. The D register is loaded with the D_{IN} word for the LTC1090. This word as shown in Figure 3 configures the LTC1090 for channel 7 with respect to common. D_{IN} also sets up the LTC1090 for unipolar mode, MSB first and tells the A/D to shift out 10 bits of data. \overline{CS} is brought low by writing to I/O port 128 (80H). The MSB of the D register containing the D_{IN} word is then output on bit 7 of the data bus of the Z-80. The first bit of the LTC1090 D_{OUT} word is then read into the A register. The act of reading this bit also generates an SCLK pulse. The D_{OUT} bit is then shifted into the carry bit and from there it is rotated into the LSB of the

B register. The next bit of the D_{IN} word is shifted into the MSB of the D register. The E register counter is decremented. At this point a test is made to determine if the first eight bits have been shifted. If not, another D_{IN} bit is output and D_{OUT} bit is read until eight bits have been shifted. The two LSBs of the D_{OUT} word are similarly shifted into the C register. These two bits are then shifted right through the carry until they are in the two MSB positions of the C register. \overline{CS} is then brought high. The 10 bit LTC1090 D_{OUT} word is stored left justified in the Z-80 at this time as shown in Figure 4.

After the last SCLK pulse is ended 44 ACLK cycles must be allowed for the LTC1090 to perform the desired A/D conversion. During this time \overline{CS} is taken high. The software must ensure that this occurs.

Summary

An interface between the LTC1090 10 bit data acquisition system and the Z-80 microprocessor with a combined data conversion and transfer time of $288\mu s$ was demonstrated. The interface used four 74LS chips to interface the two devices. The 10 data bits of the LTC1090 are shifted MSB first one bit at a time. The data is stored left justified in the Z-80's internal registers.

1	1	1	1	1	1	0	1
S/D	O/S	S1	S2	UNI	MSBF	WL1	WL0

Figure 3. D_{IN} Word for LTC1090 Stored in D Register of Z-80

MSB								
9	8	7	6	5	4	3	2	REG B
LSB								
1	0	FILLED WITH 0's						REG C

D_{OUT} from LTC1090 stored in Z-80 registers

Figure 4. Memory Map of Z-80

LABEL	MNEMONIC	COMMENTS
BEGIN	LD C,00H	INITIALIZE REG C
	LD E,08H	INITIALIZE REG E
	LD D,FDH	PUT D_{IN} IN REG D
	OUT (80H),A	\overline{CS} GOES LOW
LOOP	LD (HL),D	OUTPUT D_{IN} BIT
	IN A,(80H)	READ D_{OUT} BIT
	RRA	SHIFT DATA TO CARRY
	RL	SHIFT DATA TO REG B
	RLC	SHIFT D_{IN} WORD LEFT
	DEC E	DECREMENT COUNTER
	JP NZ,LOOP	GET NEXT BIT IF NOT 0
	IN A,(80H)	READ BIT 1 OF D_{OUT}
	RRA	SHIFT BIT INTO CARRY
	RL	SHIFT DATA TO REG C
	IN A,(80H)	READ BIT 0 OF D_{OUT}
	RRA	SHIFT BIT INTO CARRY
	RR	REG C SHIFTS RIGHT
	RR	REG C SHIFTS RIGHT
	OUT (81H),A	\overline{CS} GOES HIGH

Figure 5. Z-80 Code

Interfacing the LTC1090 to the HD64180

Guy Hoover
William Rempfer

Introduction

This application note describes an interface between the LTC1090 10-bit data acquisition system and the Hitachi 64180 microprocessor. The simple four wire interface is capable of completing a 10-bit conversion and shifting the data to the 64180 in $96\mu\text{s}$. Configuration of the LTC1090 and the 64180 will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be shown. Finally, a summary of the key points of this interface will be given including data throughput rates.

Interface Details

The LTC1090 has two clock lines: ACLK and SCLK. ACLK controls the A/D conversion rate while SCLK controls the data shift rate. Data is transferred in a synchronous full duplex format over D_{IN} and D_{OUT} .

The 64180 has a clocked serial I/O port (CSIO) that allows the user to construct a simple communication path to the LTC1090. The serial port provides clock, transmit and receive lines that are compatible with the LTC1090. The only additional line required is one programmable output pin (RTSO) to control \overline{CS} on the LTC1090. The schematic of Figure 1 shows how the two devices are connected.

Hardware Description

The timing diagram of Figure 2 was obtained using an HP1631A logic analyzer. ACLK of the LTC1090 was 2MHz and the 64180 crystal frequency was 4MHz. This produced

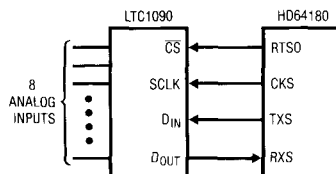
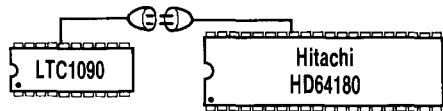


Figure 1. LTC1090 Transmits Data to HD64180 Using 4 Wires



a transfer time of $479\mu\text{s}$. A version of the 64180 can be run at a 20MHz crystal frequency so the times shown can be reduced by a factor of five yielding a total transfer time of $96\mu\text{s}$.

At crystal frequencies up to 4MHz ACLK can be generated directly from the ϕ pin of the 64180. Above 4MHz a divider must be used to generate ACLK or it must be externally generated to ensure it remains below 2MHz.

The analog section of the schematic of Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1090 please see the data sheet.

Software Description

The software configures and controls the CSIO of the 64180. Additionally, the software manipulates RTSO (\overline{CS} of the LTC1090) and generates a delay during which time the LTC1090 performs a conversion. Because the CSIO of the 64180 communicates in a half duplex format it is necessary for the software to first write a configuration word to

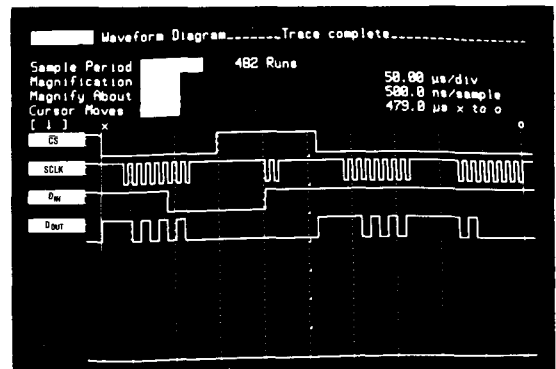


Figure 2. Timing Diagram. Transfer Times as Short as $96\mu\text{s}$ are Possible.

Application Note 26P

the LTC1090 and then read back the data. Normally with the LTC1090 the D_{IN} and D_{OUT} words are transferred simultaneously.

The software first disables all interrupts and enables the receive (RXS) pin. The D_{IN} word is loaded into the Transmit Receive Data Register. The D_{IN} word programs the LTC1090 for channel 7 with respect to common, LSB first, unipolar and eight bits as shown in Figure 3. Note, that for LSB first format processors the D_{IN} word must be constructed opposite from MSB first format. This is because the bits forming the D_{IN} word of the LTC1090 must always be shifted in the same order regardless of whether MSB first or LSB first is chosen. B4 of CNTLA0 is cleared which causes \overline{CS} of the LTC1090 to go low. B4 of the CSIO control register is set which causes the D_{IN} word for the LTC1090 to begin transmitting. B7 of the CSIO control register is polled until a 1 is detected. B4 of CNTLA0 is then set which causes \overline{CS} to go high.

Forty-four ACLK cycles must pass before \overline{CS} can be taken low so that the A/D can perform a conversion. During this time a transmit is started and stopped so that the TXS line will stop high. The transmit is not allowed to finish to save time. It is desirable to have the TXS line high so that the proper word length will be clocked into the LTC1090 when D_{OUT} is read.

\overline{CS} of the LTC1090 is again cleared. The CSIO control register is set up to receive this time. The transmit line is held high so that all ones are clocked into the LTC1090 D_{IN} pin while the LSBs of D_{OUT} are being clocked into the 64180. The same polling method is used as before. After the first eight bits are received the data is stored in Register L. The two MSBs are then clocked in and placed in

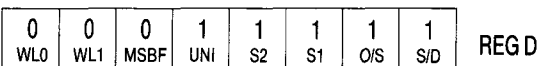


Figure 3. D_{IN} Word for LTC1090 Stored in Reverse Order in 64180 Internal Registers

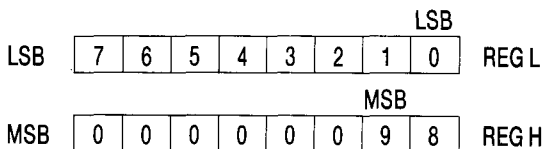


Figure 4. D_{OUT} from LTC1090 Stored in 64180 Internal Registers

Register H. The data at this point is right justified with the unused bits being set to 0s as shown in Figure 4. \overline{CS} of the LTC1090 is then set again.

Because the D_{IN} word received by the LTC1090 was a dummy word, it is not necessary to wait 44 ACLK cycles again at this point. The \overline{CS} line can be brought low immediately and another cycle begun at this time.

Summary

A four wire interface between the LTC1090 and the Hitachi 64180 with a combined data conversion and transfer time of $96\mu s$ was demonstrated. The interface used the CSIO port of the 64180. Because the CSIO port transfers data LSB first care must be taken in constructing the D_{IN} word so that the bits are transmitted in the proper order to the LTC1090. A configuration word is written to the LTC1090 in one eight bit transfer and then the 10 data bits of the LTC1090 are shifted LSB first to the 64180 in two eight bit transfers. The data is stored right justified in the 64180's internal registers.

ADDR	LABEL	CODE	MNEMONIC	COMMENTS
0	BEGIN	F3	DI	DISABLE INTERRUPTS
1		1E 00	LD E, 00H	DATA FOR ASCII STATUS REG
3		ED 19 05	OUT0 (05H), E	ENABLE RXS
6	LOOP	16 1F	LD D, 1FH	LOAD D_{IN} IN REG D
8		ED 11 0B	OUT0 (0BH), D	LOAD D_{IN} IN TRDR
B		1E 00	LD E, 00H	DATA FOR CNTLA0
D		ED 19 00	OUT0 (00H), E	DATA IN CNTLA0. \overline{CS} RESET
10		1E 10	LD E, 10H	DATA FOR CSIO CONTROL REG
12		ED 19 0A	OUT0 (0AH), E	START TRANSMIT OF D_{IN}
15		0E 0A	LD C, 0AH	ADDR OF CSIO CONTROL REG
17	TX1	ED 74 80	TSTIO 80H	
1A		28 FB	JR Z TX1	WAIT FOR TRANSFER TO END
1C		1E 10	LD E, 10H	DATA FOR CNTLA0
1E		ED 19 00	OUT0 (00H), E	DATA IN CNTLA0. \overline{CS} SET
21		16 FF	LD D, FFH	DUMMY DATA WORD
23		ED 11 0B	OUT0 (0BH), D	LOAD DUMMY IN TRDR
26		1E 10	LD E, 10H	DATA FOR CSIO CONTROL REG
28		ED 19 0A	OUT0 (0AH), E	START TRANSMIT OF DUMMY
2B		1E 00	LD E, 00H	DATA FOR CSIO CONTROL REG
2D		ED 19 0A	OUT0 (0AH), E	STOP TRANSMIT OF DUMMY
30		ED 20 0B	INO H, (0BH)	CLEAR EF OF CSIO CNTRL REG
33		1E 00	LD E, 00H	DATA FOR CNTLA0
35		ED 19 00	OUT0 (00H), E	DATA IN CNTLA0. \overline{CS} RESET
38		1E 20	LD E, 20H	DATA FOR CSIO CNTRL REG
3A		ED 19 0A	OUT0 (0AH), E	RECEIVE D_{OUT} LSBs
3D	RX1	ED 74 80	TSTIO 80H	
40		28 FB	JR Z RX1	WAIT FOR TRANSFER TO END
42		ED 28 0B	INO L, (0BH)	PUT LSBs IN REG L
45		ED 19 0A	OUT0 (0AH), E	RECEIVE D_{OUT} MSBs
48	RX2	ED 74 80	TSTIO 80H	
4B		28 FB	JR Z RX2	WAIT FOR TRANSFER TO END
4D		ED 20 0B	INO H, (0BH)	PUT MSBs IN REG H
50		1E 10	LD E, 10H	DATA FOR CNTLA0
52		ED 19 00	OUT0 (00H), E	DATA IN CNTLA0. \overline{CS} SET
55		C3 06 00	JP LOOP	DO NEXT CONVERSION

Figure 5. HD64180 Code Transfers Data to and from the LTC1090

Interfacing the LTC1091 to the HD64180

Guy Hoover
 William Rempfer

Introduction

This application note describes an interface between the LTC1091 10-bit data acquisition system and the Hitachi 64180 microprocessor. The simple four wire interface is capable of completing a 10-bit conversion and shifting the data to the 64180 in 91 μ s. Configuration of the LTC1091 and the 64180 will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be shown. Finally, a summary of the key points of this interface will be given including data throughput rates.

Interface Details

The LTC1091 clock line controls the A/D conversion rate and the data shift rate. Data is transferred in a synchronous half duplex format over D_{IN} and D_{OUT} .

The 64180 has a clocked serial I/O port (CSIO) that allows the user to construct a simple communication path to the LTC1091. The serial port provides clock, transmit and receive lines that are compatible with the LTC1091. The only additional line required is one programmable output pin (RTSO) to control \overline{CS} on the LTC1091. The schematic of Figure 1 shows how the two devices are connected.

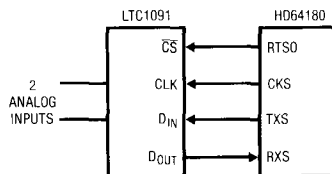
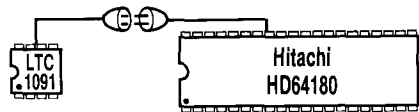


Figure 1. LTC1091 Transmits Data to HD64180 Using 4 Wires



Hardware Description

The timing diagram of Figure 2 was obtained using an HP1631A logic analyzer. The 64180 crystal frequency was 4MHz. This produced a transfer time of 455 μ s. A version of the 64180 can be run at 20MHz crystal frequency so the times shown can be reduced by a factor of five yielding a total transfer time of 91 μ s.

The analog section of the schematic of Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1091 please see the data sheet.

Software Description

The software configures and controls the CSIO of the 64180. Additionally, the software manipulates RTS0 (\overline{CS}) of the LTC1091).

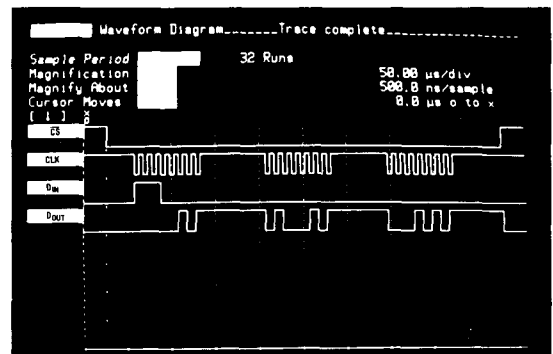


Figure 2. Timing Diagram. Throughput Times as Short as 91 μ s are Possible.

Application Note 26Q

The software first disables all interrupts and enables the receive (RXS) pin. The D_{IN} word is loaded into the Transmit Receive Data Register. The D_{IN} word programs the LTC1091 for channel 1 with respect to ground and LSB first as shown in Figure 3. Note, that for LSB first format processors the D_{IN} word must be constructed opposite from MSB first format. This is because the bits forming the D_{IN} word into the LTC1091 must always be shifted in the same order regardless of whether MSB first or LSB first is chosen. B4 of CNTLA0 is cleared which causes \overline{CS} of the LTC1091 to go low. B4 of the CSIO control register is set which causes the D_{IN} word for the LTC1091 to begin transmitting. After receiving the start bit, channel information, and LSB first format data the LTC1091 starts transmitting the results of the conversion back to the 64180 in MSB first format. The first three bits of this data are ignored by the 64180 because it is still in the transmit mode. B7 of the CSIO control register is polled until a 1 is detected signifying the end of the transfer.

The CSIO control register is set up to receive this time. The same polling method is used as before. After the first eight bits are received the data is stored in Register A. The last two bits received were transmitted in LSB first format. These two bits end up in the two MSBs of REG A, where they are ANDed with C0H to clear the LSBs of REG A. The D_{OUT} LSBs in REG A are then stored in the L register. The eight MSBs of D_{OUT} are then clocked in and placed in Register H. The data at this point is left justified as shown in Figure 4. \overline{CS} of the LTC1091 is then set again. The \overline{CS} line can be brought low immediately and another cycle begun at this time.

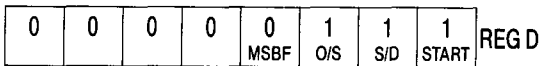


Figure 3. D_{IN} Word for LTC1091 Stored in Reverse Order in 64180 Internal Registers

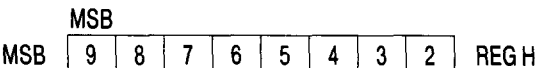


Figure 4. D_{OUT} from LTC1091 Stored in 64180 Internal Registers

Summary

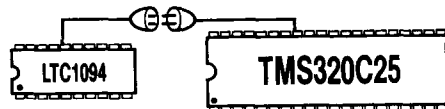
A four wire interface between the LTC1091 and the Hitachi 64180 with a combined data conversion and transfer time of $91\mu s$ was demonstrated. The interface used the CSIO port of the 64180. Because the CSIO port transfers data LSB first care must be taken in constructing the D_{IN} word so that the bits are transmitted in the proper order to the LTC1091. A configuration word is written to the LTC1091 in one eight bit transfer and then the 10 data bits of the LTC1091 are shifted LSB first to the 64180 in two eight bit transfers. The data is stored left justified in the 64180's internal registers.

ADDR	LABEL	CODE	MNEMONIC	COMMENTS
0	BEGIN	F3	DI	DISABLE INTERRUPTS
		1E 00	LD E, 00H	DATA FOR ASCII STATUS REG
3		ED 19 05	OUT0 (05H), E	ENABLE RXS
6	LOOP	16 07	LD D, 07H	LOAD D_{IN} IN REG D
8		ED 11 0B	OUT0 (0BH), D	LOAD D_{IN} IN TRDR
B		1E 00	LD E, 00H	DATA FOR CNTLA0
D		ED 19 00	OUT0 (00H), E	DATA IN CNTLA0. \overline{CS} RESET
10		1E 10	LD E, 10H	DATA FOR CSIO CONTROL REG
12		ED 19 0A	OUT0 (0AH), E	START TRANSMIT OF D_{IN}
15		0E 0A	LD C, 0AH	ADDR OF CSIO CONTROL REG
17	TX1	ED 74 80	TSTIO 80H	
1A		28 FB	JR ZTX1	WAIT FOR TRANSFER TO END
1C		ED 20 0B	IN0 H, (0BH)	CLEAR EF OF CSIO CNTRL REG
1F		1E 20	LD E, 20H	DATA FOR CSIO CNTRL REG
21		ED 19 0A	OUT0 (0AH), E	RECEIVE D_{OUT} LSBs
24	RX1	ED 74 80	TSTIO 80H	
27		28 FB	JR ZRX1	WAIT FOR TRANSFER TO END
29		ED 38 0B	IN0 A, (0BH)	PUT LSBs IN REG A
2C		E6 C0	AND C0H	MASK OUT LSBs
2E		6F	LD L, A	PUT D_{OUT} IN REG L
2F		ED 19 0A	OUT0 (0AH), E	RECEIVE D_{OUT} MSBs
32	RX2	ED 74 80	TSTIO 80H	
35		28 FB	JR ZRX2	WAIT FOR TRANSFER TO END
37		ED 20 0B	IN0 H, (0BH)	PUT MSBs IN REG H
3A		1E 10	LD E, 10H	DATA FOR CNTLA0
3C		ED 19 00	OUT0 (00H), E	DATA IN CNTLA0. \overline{CS} SET

Figure 5. HD64180 Code Transfers Data to and from the LTC1091

Interfacing the LTC1094 to a Parallel Bus

Guy Hoover
William Rempfer



Introduction

This application note describes the hardware and software required to interface the LTC1094 10-bit data acquisition system to the TMS320C25 digital signal processor. The circuitry shown can be used to interface any member of the LTC1090 family to the bus of virtually any processor with only minor modifications. The software provided is specific to the TMS320 family. The interface shown can be either interrupt driven or polled by the processor after a convert command has been given to the LTC1094. The interface is capable of completing a 10-bit conversion and transferring the data to the TMS320C25 in 40 μ s. Configuration of the LTC1094 and the TMS320C25 will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be discussed. Finally, a summary of results will be provided.

Interface Details

The LTC1094 is a serial 10-bit data acquisition system. It uses a half duplex synchronous serial interface. It uses a D_{IN} word to configure the A/D for channel number, unipolar or bipolar, and MSB first or LSB first. Data is shifted out on the D_{OUT} line. Both D_{IN} and D_{OUT} are synchronous with the CLK line.

Many processors do not have a compatible serial port. It then becomes necessary to construct an interface circuit that will allow the LTC1094 to hang directly on the data bus of the processor. The circuit of Figure 1 interfaces directly to the TMS320C25 bus. It latches the D_{IN} word pro-

vided by the processor and then shifts it to the LTC1094. The LTC1094 then clocks out the D_{OUT} word to a shift register where the data is latched and the conversion complete signal is sent to the processor. When the processor requests the D_{OUT} word the interface circuit comes out of tri-state and the data is present on the bus. The circuit generates the clock for the LTC1094 and automatically shuts it off after the conversion has been done. The processor must provide chip select, read/write and interrupt lines as well as a 16-bit data bus. (For an 8-bit data bus a two byte read would be required.) When the read/write line is LOW and the chip select line is LOW the D_{IN} word is latched into the 74LS165. When the read/write line is HIGH and the chip select line is LOW the D_{OUT} word is read from the 74LS365 tri-state buffers.

Hardware Description

The DSP was emulated and the code for this interface was developed on a TMS320C25 Software Development System (SWDS).

The timing diagram of Figure 2 was obtained with an HP1631 logic analyzer with an LTC1094 CLK frequency of 500kHz.

The analog section of the schematic in Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1094 please see the data sheet.

Application Note 26R

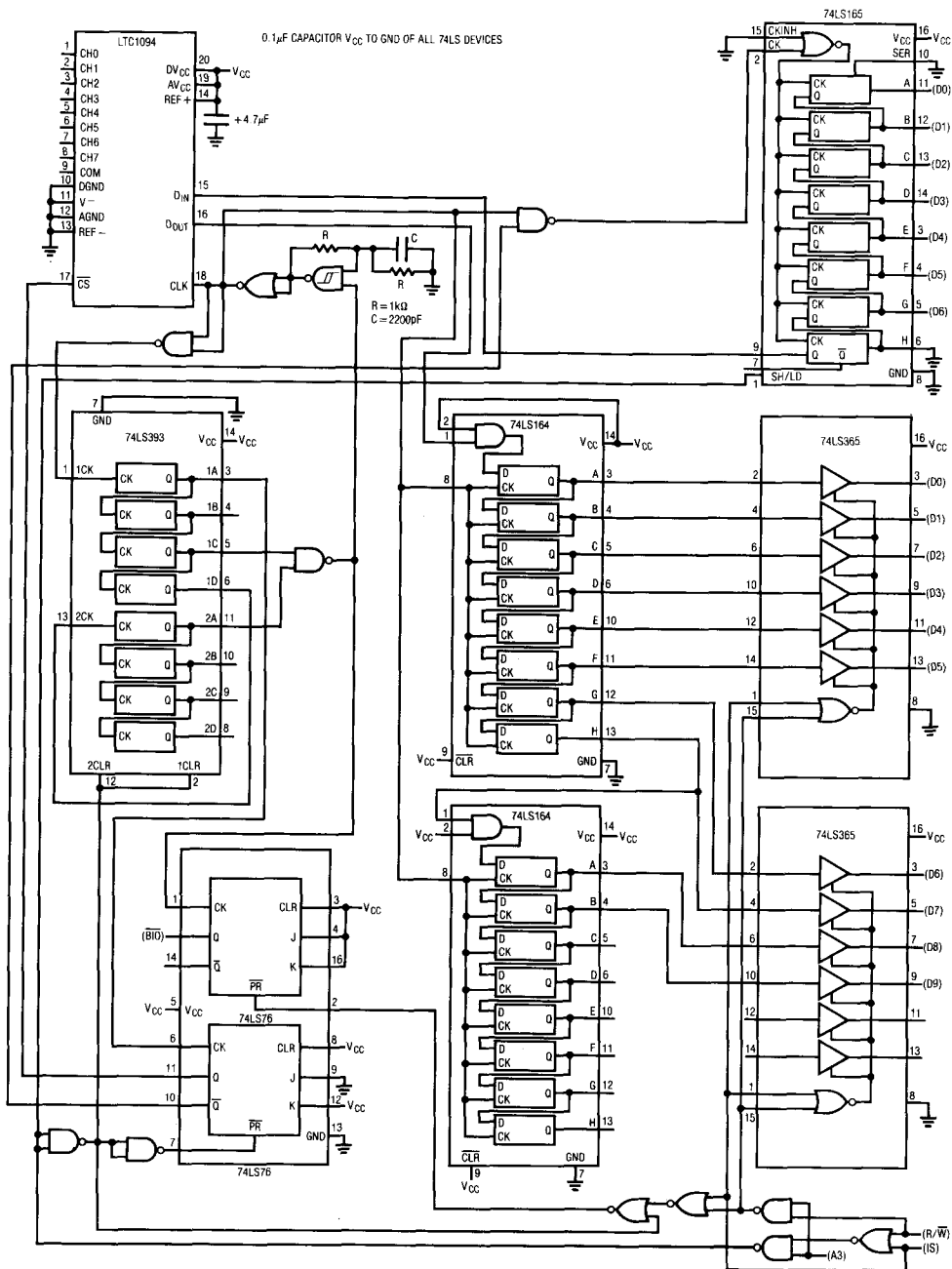


Figure 1. Circuit Allows LTC1094 to Interface Directly with the TMS320C25 Data Bus

Software Description

The software outputs a D_{IN} word from the TMS320C25 to the interface and when informed by the interface that the resulting data is present reads in the D_{OUT} word of the LTC1094.

The code of Figure 5 first disables all interrupts. Next, a D_{IN} word is placed in >60 of the TMS320C25 as shown in Figure 3. This D_{IN} word configures the LTC1094 for CH7 with respect to COM, unipolar, and MSB first. This D_{IN} word is then output to Port 8 of the TMS320C25. The software then polls the BIO pin until the interface pulls it LOW indicating that the conversion is complete and that the data is ready to be received by the TMS320C25. (The interface could just as easily connect to one of the maskable interrupt pins so that the processor could be performing some task while waiting for the conversion to be completed.) The data is then read into the TMS320C25 and placed into >61 . The data at this point is right justified as shown in Figure 4.

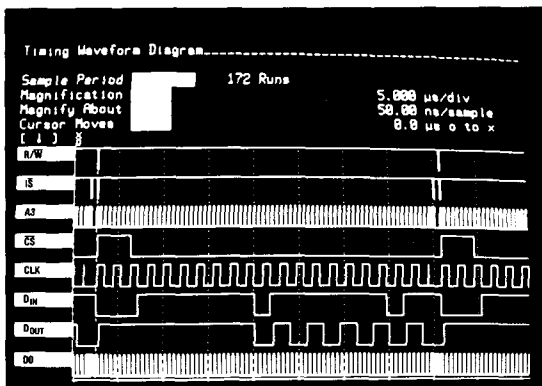


Figure 2. Timing Diagram Shows 25kHz Throughput Rate

Summary

An interface between the LTC1094 and the TMS320C25 with a combined data conversion and transfer rate of $40\mu s$ was demonstrated. This inexpensive interface (about \$2.00 in production quantities) uses ten 74LS chips to allow the LTC1094 to hang directly on the data bus of the TMS320C25. The circuit shown here should work with any 16-bit processor (an 8-bit processor would require two reads per conversion) that has a read/write line, and external interrupt capability.

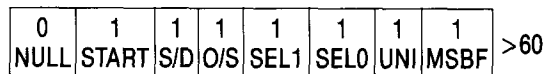


Figure 3. D_{IN} Word for LTC1094

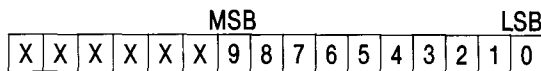


Figure 4. D_{OUT} of LTC1094 Stored in >61 of TMS320C25

LABEL	CODE	MNEMONIC	COMMENTS
		AORG >20	
START	CE01	DINT	DISABLE INTERRUPTS
LOOP	CAFF	LACK >7F	D_{IN} FOR LTC1094
	6060	SACL >60	PUT D_{IN} IN >60
	E860	OUT >60.8	OUTPUT D_{IN} TO PORT 8
WAIT1	FA80005F	BIOZ READ	IF DONE GO TO READ
	FF800024	B WAIT1	IF NOT DONE GO TO WAIT1
		AORG >5F	
READ	8861	IN >61.8	PUT D_{OUT} IN >61

Figure 5. TMS320C25 Code for Interfacing to LTC1094

Application Note 26R

A Simple Method of Designing Multiple Order All Pole Bandpass Filters by Cascading 2nd Order Sections

Nello Sevastopoulos
 Richard Markell

INTRODUCTION

Filter design, be it active, passive, or switched capacitor, is traditionally a mathematically intensive pursuit. There are many architectures and design methods to choose from. Two methods of high order bandpass filter design are discussed herein. These methods allow the filter designer to simplify the mathematical design process and allow LTC's switched capacitor filters (LTC1059, 60, 61, 64) to be utilized as high quality bandpass filters.

The first method consists of the traditional cascading of non-identical 2nd order bandpass sections to form the familiar Butterworth and Chebyshev bandpass filters. The second method consists of cascading identical 2nd order bandpass sections. This approach, although "non-text-book," enables the hardware to be simple and the mathematics to be straightforward. Both methods will be described here.

AN27A is the first of a series of application notes from LTC concerning our universal filter family. Additional notes in the series will discuss notch, lowpass and highpass filters implemented with the universal switched capacitor filter. An addition to this note will extend the treatment of bandpass filters to the elliptic or Cauer forms.

This note will first present a finished design example and proceed to present the design methodology which relies on tabular simplification of traditional filter design techniques.

DESIGNING BANDPASS FILTERS

Table 1 was developed to enable *anyone* to design Butterworth bandpass filters. We will discuss the tables in more detail later in this paper, but let's first design a filter.

EXAMPLE 1 — DESIGN

A 4th order 2kHz Butterworth bandpass filter with a -3dB bandwidth equal to 200Hz is required as shown in Figure 1.

Noting that $(f_{\text{BP}}/\text{BW}) = 10/1$ we can go directly to Table 1 for our normalized center frequencies. From Table 1 under 4th order Butterworth bandpass filters, we go to $(f_{\text{BP}}/\text{BW}) = 10$.

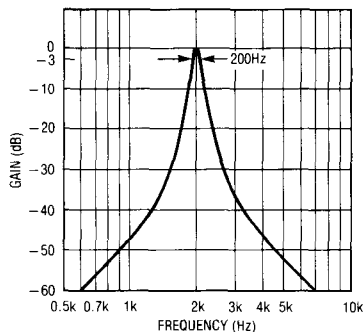


Figure 1. 4th Order Butterworth BP Filter, $f_{\text{BP}} = 2\text{kHz}$

Application Note 27A

We find $f_{o1} = 0.965$ and $f_{o2} = 1.036$ (both normalized to $f_{oBP} = 1$). To find our desired actual center frequencies, we must multiply by $f_{oBP} = 2\text{kHz}$ to obtain $f_{o1} = 1.930\text{kHz}$ and $f_{o2} = 2.072\text{kHz}$.

The Q's are $Q_1 = Q_2 = 14.2$ which is read directly from Table 1. Also available from the table is K which is the product of each individual bandpass gain H_{oBP} . To put it another way, the value of K is the gain required to make the gain, H, of the overall filter equal to 1 at f_{oBP} . Our filter parameters are highlighted in the following table:

f_{oBP}	f_{o1}	f_{o2}	Q's	K
2kHz	1.93kHz	2.072kHz	$Q_1 = Q_2 = 14.2$	2.03

HARDWARE IMPLEMENTATION

Universal switched capacitor filters are simple to implement. A bandpass filter can be built from the traditional state-variable filter topology. Figure 2 shows this topology for both switched capacitor and active operational amplifier implementations. Our example requires four resistors for each 2nd order section. So eight resistors are required to build our filter.

We start with two 2nd order sections (1 LTC1060, 2/3 LTC1061 or 1/2 LTC1064), Figure 3.

We associate resistors as belonging to 2nd order sections, so R1x belongs to the x section. Thus R12, R22,

R33 and R42 all belong to the second of two 2nd order sections in our example.

Our requirements are shown in the following table:

SECTION 1	SECTION 2
$f_{o1} = 1.93\text{kHz}$	$f_{o2} = 2.072\text{kHz}$
$Q_1 = 14.2$	$Q_2 = 14.2$
$H_{oBP1} = 1$	$H_{oBP2} = 2.03$

Note that $H_{oBP1} \times H_{oBP2} = K$ and this is the reason for choosing $H_{oBP2} = 2.03$.

For this example we choose the $f_o = \frac{f_{CLK}}{50} \sqrt{\frac{R_2}{R_4}}$ mode,

so we will tie the 50/100/Hold pin on the SCF chip to $V+$, generally (5V to 7V). We choose 100kHz as our clock and calculate resistor values. Choosing the nearest 1% resistor values we can implement the filter using Figure 3's topology and the resistor values listed below.

- R11 = 147k
- R12 = 71.5k
- R21 = 10k
- R22 = 10.7k
- R31 = 147k
- R32 = 147k
- R41 = 10.7k
- R42 = 10k

Our design is now complete. We have only to generate a TTL or CMOS compatible clock at 100kHz which we feed to the clock pin of the switched capacitor filter and we should be "on the air."

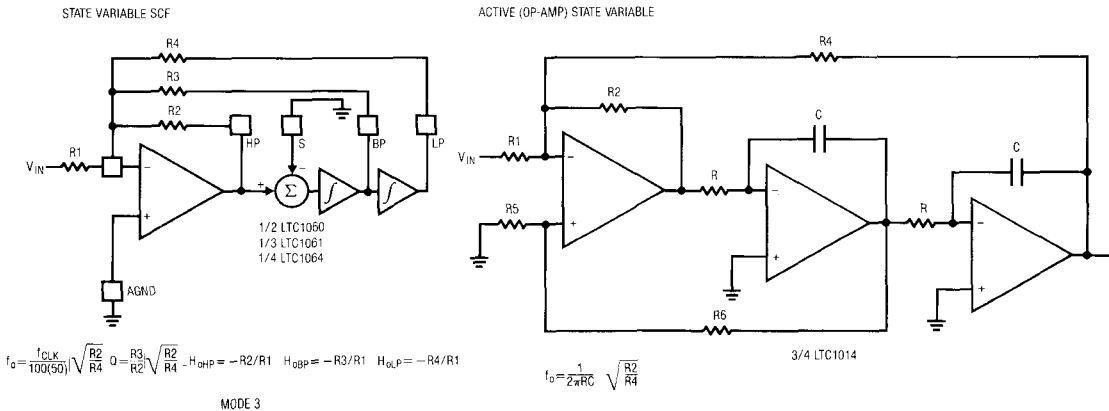


Figure 2. Switched Capacitor vs Active RC State Variable Topology

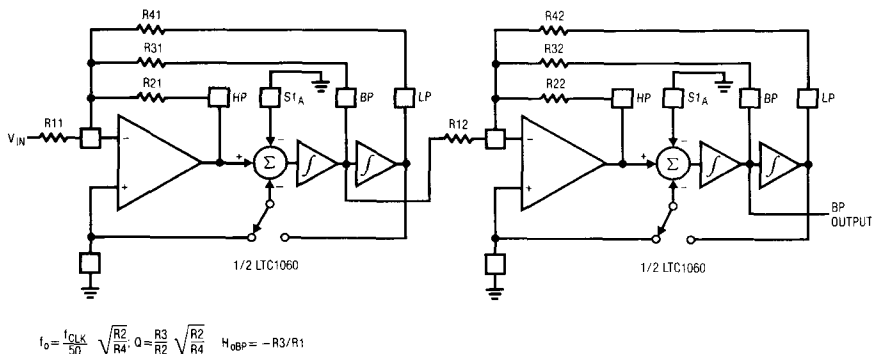


Figure 3. Two 2nd Order Sections Cascaded to Form 4th Order BP Filter

DESIGNING BANDPASS FILTERS — THEORY BEHIND THE DESIGN

Traditionally, bandpass filters have been designed by laborious calculations requiring some time to complete. At the present time programs for various personal or laboratory computers are often used. In either case, no small amount of time and/or money is involved to evaluate, and later test, a filter design.

Many designers have inquired as to the feasibility of cascading 2nd order bandpass sections of relatively low Q to obtain more selective, higher Q, filters. This approach is ideally suited to the LTC family of switched capacitor filters (LTC1059, 1060, 1061 and 1064). The clock to center frequency ratio accuracy of a typical "Mode 1" design with non "A" parts is better than 1% in a design that simply requires three resistors of 1% tolerance or better. Also, no expensive high precision film capacitors are required as in the active op-amp state variable design.

We present here an approach for designing bandpass filters using the LTC1059, 1060, 1061 or the 1064 which many designers have "on the air" in days instead of weeks.

CASCADING IDENTICAL 2ND ORDER BANDPASS SECTIONS

When we want to detect single frequency tones and simultaneously reject signals in close proximity, simple 2nd order bandpass filters often do the job. However, there are cases where a 2nd order section cannot be implemented

with the required characteristics (generally the Q's are too high). We wish to explore here the use of cascaded identical 2nd order sections for building high Q bandpass filters.

For a 2nd order bandpass filter:

$$Q = \frac{\sqrt{1-G^2}}{G} \times \frac{f/f_0}{|1-(f/f_0)^2|} \quad (1)$$

Where Q is the required filter quality factor

f is the frequency where the filter should have gain, G, expressed in Volts/V.

f₀ is the filter center frequency. Unity gain is assumed at f₀.

EXAMPLE 2 — DESIGN

We wish to design a 2nd order BP filter to pass 150Hz and to attenuate 60Hz by 50dB. The required Q may be calculated from Equation (1):

$$\text{So, } Q = \frac{\sqrt{1-(3.162 \times 10^{-3})^2}}{3.162 \times 10^{-3}} \times \frac{60/150}{|1-(60/150)^2|} = 150.7$$

This very high Q dictates a -3dB bandwidth of 1Hz.

Although the universal switched capacitor filters can realize such high Q's, their guaranteed center frequency accuracy of ±0.3%, although impressive, is not enough to

Application Note 27A

pass the 150Hz signal without gain error. According to the previous equation, the gain at 150Hz will be $1 \pm 26\%$; the rejection, however, at 60Hz will remain at -50dB . The gain inaccuracy can be corrected by tuning resistor $R4$ when mode 3, Figure 2, is used. Also, if only detection of the signal is sought, the gain inaccuracy could be acceptable.

This high Q problem can be solved by cascading two identical 2nd order bandpass sections. To achieve a gain, G , at frequency f the required Q of each 2nd order section is:

$$Q = \frac{\sqrt{1-G}}{\sqrt{G}} \times \frac{f/f_0}{|1-(f/f_0)^2|} \quad (2)$$

The gain at each bandpass section is assumed unity.

In order to obtain 50dB attenuation at 60Hz, and still pass 150Hz, we will use two identical 2nd order sections.

We can calculate the required Q for each of two 2nd order sections from Equation (2):

$$\text{So, } Q = \frac{\sqrt{1-3.162 \times 10^{-3}}}{\sqrt{3.162 \times 10^{-3}}} \times \frac{60/150}{|1-(60/150)^2|} = 8.5!!$$

With two identical 2nd order sections each with a potential error in center frequency, f_0 , of $\pm 0.3\%$ the gain error at 150Hz is $1 \pm 0.26\%$. If lower cost (non "A" versions of LTC1060 and LTC1064) 2nd order bandpass sections are used with an f_0 tolerance of $\pm 0.8\%$, the gain error at 150Hz is $1 \pm 1.8\%$! The benefits of lower Q sections are therefore obvious.

HARDWARE IMPLEMENTATION

Mode 1 Operation of LTC1060, 1061, 1064

As previously discussed, we associate resistors with each 2nd order section, so $R1x$ belongs to x section. Thus $R12$, $R22$ and $R23$ belong to the second of the two 2nd order sections, Figure 4.

Each section has the same requirements as shown:

$$\begin{aligned} f_{o1} &= f_{o2} = 150\text{Hz} \\ Q_1 &= Q = 8.5 \\ H_{oBP1} &= H_{oBP2} = 1 \end{aligned}$$

Note that we could get gain out of our BP filter structure by letting the product of the H_{oBP} terms be > 1 (within the performance limits of the filter itself).

For our example using the LTC1060 we will use $f_{o1} = f_{o2} = f_{CLK}/100$. So we input a 15kHz clock and tie the 50/100/Hold pin to mid-supplies (ground for $\pm 5\text{V}$ supplies).

We can implement this filter using the two sections of an LTC1060 filter operated in mode 1. Mode 1 is the fastest operating mode of the switched capacitor filters. It provides Lowpass, Bandpass and Notch outputs.

Each 2nd order section will perform approximately as shown in Figure 5, curve (a).

Implementation in mode 1 is simple as only three resistors are required per section. Since we are cascading *identical* sections, the calculations are also simple.

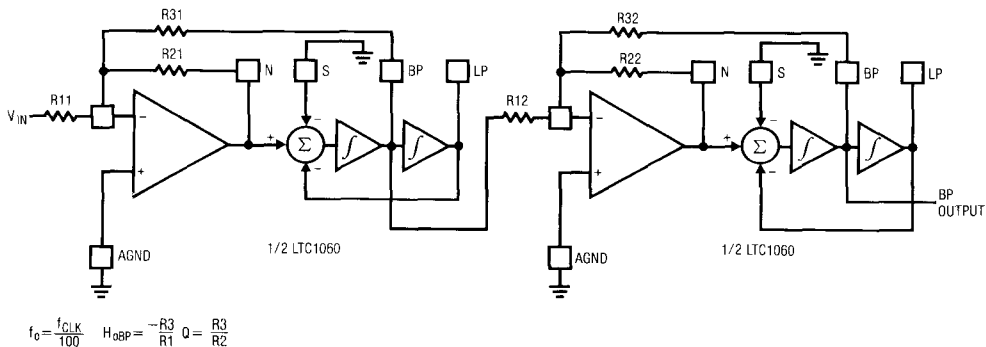


Figure 4. LTC1060 as BP Filter Operating in Mode 1

We can calculate the resistor values from the indicated formulas and then choose 1% values. (Note that we let our minimum value be 20k.) The required values are:

$$\begin{aligned} R_{11} &= R_{12} = 169k \\ R_{21} &= R_{22} = 20k \\ R_{31} &= R_{32} = 169k \end{aligned}$$

Our design is complete. The performance of two 2nd order sections cascaded versus one 2nd order section is shown in Figure 5, curve (b). We must, however, generate a TTL or CMOS clock at 15kHz to operate the filter.

Mode 2 Operation of LTC1060 Family

Suppose that we have no 15kHz clock source readily available. We can use what is referred to as mode 2, which allows the input clock frequency to be less than 50:1 or 100:1

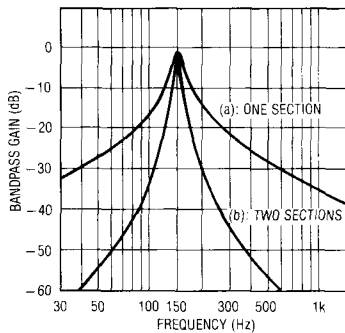


Figure 5. Cascading Two 2nd Order BP Sections for Higher Q Response

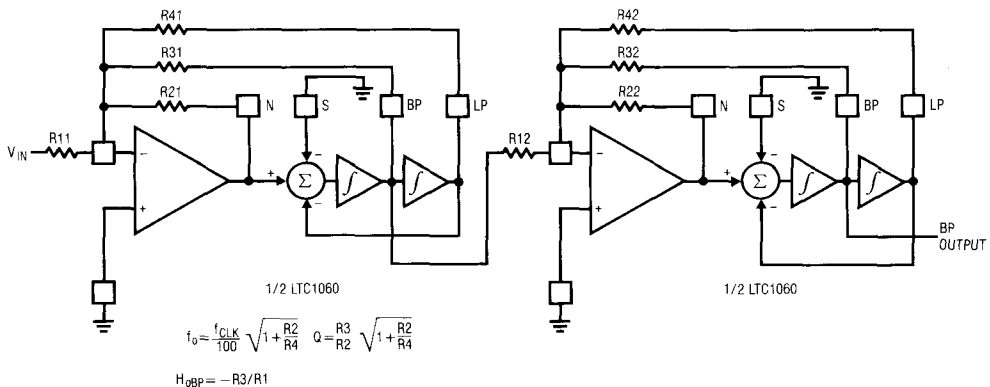


Figure 6. LTC1060 as BP Filter Operating in Mode 2

$[f_{CLK}/f_0 = 50 \text{ or } 100]$. This still depends on the connection of the 50/100/Hold pin.

If we wish to operate our previous filter from a television crystal at 14.318MHz we could divide this frequency by 1000 to give us a clock of 14.318kHz. We could then set up our mode 2 filter as shown in Figure 6.

We can calculate the resistor values from the formulas shown and then choose 1% values. The required values are:

$$\begin{aligned} R_{11}, R_{12} &= 162k \\ R_{21}, R_{22} &= 20k \\ R_{31}, R_{32} &= 162k \\ R_{41}, R_{42} &= 205k \end{aligned}$$

CASCADING MORE THAN TWO IDENTICAL 2ND ORDER BP SECTIONS

If more than two identical bandpass sections (2nd order) are cascaded, the required Q of each section may be shown to be:

$$Q = \frac{\sqrt{1 - G^{2/n}}}{G^{1/n}} \times \frac{(f/f_0)}{|1 - (f/f_0)^2|} \quad (3)$$

where Q, G, f and f_0 are as previously defined and n = the number of cascaded 2nd order sections.

Application Note 27A

The equivalent Q of the overall bandpass filter is then:

$$Q_{\text{equiv}} = \frac{Q(\text{identical section})}{\sqrt{(2^{1/n}) - 1}} \quad (4)$$

Figure 7 shows the passband curves for Q=2 cascaded bandpass sections where n is the number of 2nd order sections cascaded.

The benefits can be seen for two and three cascaded sections. Cascading four or more sections increases the Q, but not as rapidly. Nevertheless for designers requiring high Q bandpass filters cascading identical sections is a very real option considering the simplicity.

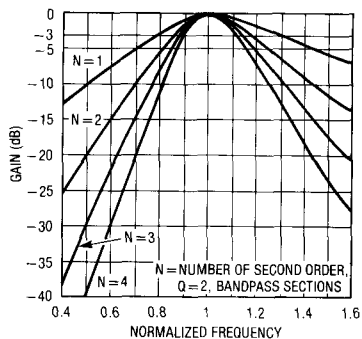


Figure 7. Frequency Response of n Cascaded Identical 2nd Order Bandpass Sections

SIMPLE 2ND ORDER BANDPASS FILTERS

Gain and Phase Relations

The bandpass output of each 2nd order filter section of the LTC1059, 60, 61, 64, closely approximates the gain and phase response of an ideal "textbook" filter.

$$G = \frac{(H_{\text{OBP}}) \times (f_0/Q)}{[(f_0^2 - f^2)^2 + (ff_0/Q)^2]^{1/2}}$$

G = filter gain in Volts/V

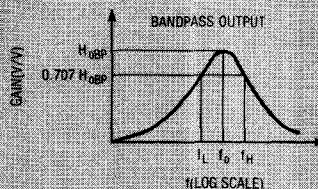
f_0 = the filter's center frequency

Q = the quality coefficient of the filter

H_{OBP} = the maximum voltage gain of the filter occurring at f_0

$\frac{f_0}{Q}$ = the -3dB bandwidth of the filter

Figure 8 illustrates the above definitions. Figure 9 illustrates the bandpass gain, G, for various values of Q. This figure is very useful for estimating the filter attenuation when several identical 2nd order bandpass filters are cascaded. High Q's make the filter more selective, and at the same time, more noisy and more difficult to realize. Q's in excess of 100 can be easily realized with the universal switched capacitor filters, LTC1059, 60, 61, 64, and still maintain low center frequency and Q drift, but for system considerations, this may not be practical.



$$Q = \frac{f_0}{f_H - f_L}, \quad f_0 = \sqrt{f_L f_H}$$

$$f_L = f_0 \left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1} \right)$$

$$f_H = f_0 \left(\frac{1}{2Q} - \sqrt{\left(\frac{1}{2Q}\right)^2 + 1} \right)$$

Figure 8. Bandpass Filter Parameters

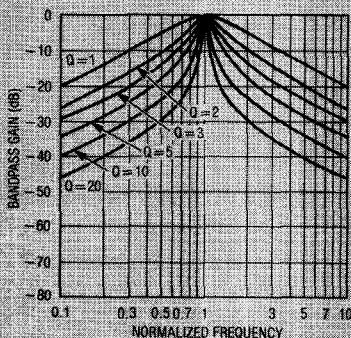


Figure 9. Bandpass Gain as a Function of Q

The phase shift, ϕ , of a 2nd order bandpass filter is:

$$\phi = -\arctan \left[\left(\frac{f_0^2 - f^2}{ff_0} \right) \times Q \right]$$

The phase shift at f_0 is 0° or, if the filter is inverting, it is -180° . All the bandpass outputs of the LTC1059, 60, 61 and LTC1064 universal filters are inverting. The phase shift, especially in the vicinity of f_0 , depends on the value of Q , see Figure 10. By the same argument, the phase shift at a given frequency varies from device to device due to the f_0 tolerance. This is true especially for high Q 's and in the vicinity of f_0 . For instance, a LTC1059A, 2nd order universal filter, has a guaranteed initial center frequency tolerance of $\pm 0.3\%$. The ideal phase shift at the ideal f_0 should be -180° . With a Q of 20, and without trimming, the worst case phase shift at the ideal f_0 will be $-180^\circ \pm 6.8^\circ$. With a Q of 5 the phase shift tolerance becomes $-180^\circ \pm 1.7^\circ$. These are important considerations when bandpass filters are used in multichannel systems where

phase matching is required. By way of comparison, a state variable active bandpass filter built with 1% resistors and 1% capacitors may have center frequency variation of $\pm 2\%$ resulting in phase variations of $\pm 38.8^\circ$ for $Q=20$ and $\pm 11.4^\circ$ for $Q=5$.

Constant Q vs. Constant BW

The bandpass outputs of the universal filters are "constant Q ." For instance, a 2nd order bandpass filter operating in mode 1 with a 100kHz clock (see LTC1060 data sheet) ideally has a 1kHz or 2kHz center frequency, and a -3dB bandwidth equal to (f_0/Q) . When the clock frequency varies, the center frequency *and* bandwidth will vary at the same rate. In a constant bandwidth filter, when the center frequency varies, the Q varies accordingly to maintain a constant (f_0/Q) ratio. A constant bandwidth BP filter could be implemented using 2nd order switched capacitor filters but this is beyond the scope of this paper.

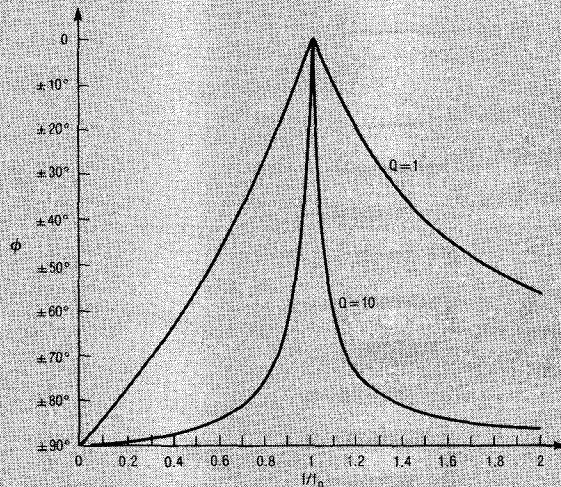


Figure 10. Phase Shift, ϕ , of a 2nd Order BP Filter Section (LTC1059, 1/2 LTC1060, 1/3 LTC1061)

Application Note 27A

Using The Tables

Tables 1 through 4 were derived from textbook filter theory. They can be easily applied to the LTC filter family (LTC1059, 1060, 1061 and 1064) if the Q's are kept relatively low (<20) and the tuning resistors are at least 1% tolerance. These lower Q designs provide almost textbook BP filter performance using LTC's switched capacitor filters. For higher Q implementations, tuning should be avoided and the "A" versions of the LTC1059, 1060, 1061 or 1064 should be specified. Also, resistor tolerances of better than 1% are a necessity.

Table 1 may be used to find pole positions and Q's for Butterworth bandpass filters. It should be noted that the bandpass filters in these tables are geometrically symmetrical about their center frequencies, f_{oBP} . Any frequency, f_3 , as shown in Figure 11 has its geometrical counterpart f_4 such that:

$$f_4 = \frac{f_{oBP}^2}{f_3}$$

Additionally, Table 1 illustrates the attenuation at the frequencies f_3 , f_5 , f_7 and f_9 which correspond to bandwidths 2, 3, 4 and 5 times the passband (see Figure 11). These values allow the user to get a good estimate of filter selectivity.

An important approximation can be made for not only the Butterworth filters in Table 1, but also for the Chebyshev filter Tables 2, 3 and 4. Treating Figure 11 (or Figure 12) as a generalized bandpass filter, the two corner frequencies f_2 and f_1 can be seen to be nearly arithmetically symmetrical with respect to f_{oBP} provided that:

$$\frac{f_{oBP}}{BW} \gg \frac{1}{2}, \quad BW = f_2 - f_1$$

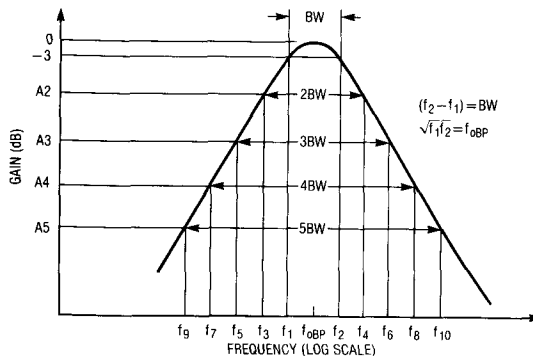
Under this condition, for either Butterworth or Chebyshev bandpass filters:

$$f_{oBP} \cong \frac{f_3 - f_4}{2} + f_3$$

$$f_{oBP} \cong \frac{f_5 - f_6}{2} + f_5$$

•
•
•

This is true for any bandwidth, BW, and any set of frequencies. The tables can now be arithmetically scaled as illustrated.

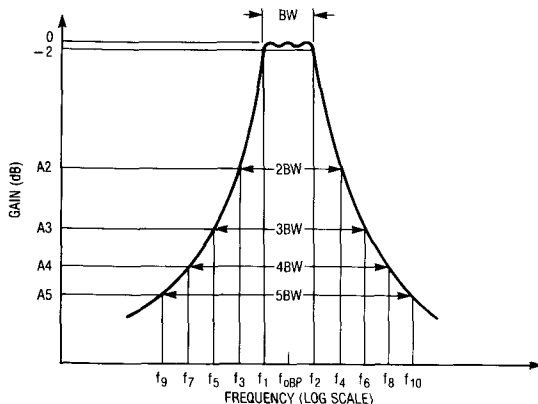


$$(f_1, f_2) = \frac{\pm BW + \sqrt{(BW)^2 + 4(f_{oBP})^2}}{2}$$

$$\text{MORE GENERALLY } (f_x, f_{x+1}) = \frac{\pm nBW + \sqrt{(nBW)^2 + 4(f_{oBP})^2}}{2}$$

(VALID FOR ANY f_x, f_{x+1} PAIR, ANY BW)

Figure 11. Generalized Bandpass Butterworth Response, (See Table 1)



$$\sqrt{A_{MAX}} = f_{oBP}$$

$$(f_4, f_3) = \frac{\pm 2BW + \sqrt{(2BW)^2 + 4(f_{oBP})^2}}{2}$$

FOR ANY (f_x, f_{x+1}) PAIR AND ANY CORRESPONDING BANDWIDTH (2BW, 3BW, ETC.)

FOR EXAMPLE:

$$(f_6, f_5) = \frac{\pm 3BW + \sqrt{(3BW)^2 + 4(f_{oBP})^2}}{2}$$

Figure 12. Generalized 4th, 6th, & 8th Order Chebyshev Bandpass Filter with 2dB Passband Ripple (A_{MAX})

Table 1. Butterworth Bandpass Filters Normalized to $f_{0BP} = 1$

f_{0BP} (Hz)	f_{0BP} (BW) (Hz)	f_{01} (Hz)	f_{02} (Hz)	f_{03} (Hz)	f_{04} (Hz)	f_{-3dB} (Hz)	f_{+3dB} (Hz)	Q1 = Q2	K	f_1 (Hz)	f_3 (Hz)	GAIN AT f_3 (dB)-A2	f_5 (Hz)	GAIN AT f_5 (dB)-A3	f_7 (Hz)	GAIN AT f_7 (dB)-A4	f_9 (Hz)	GAIN AT f_9 (dB)-A5	
4th Order Butterworth Bandpass Filter Normalized to its Center Frequency, $f_{0BP} = 1$, and -3dB Bandwidth (BW)																			
1	1	0.693	1.442			0.500	2.000	1.5	2.28	0.500	0.414	-12.3	0.303	-19.1	0.236	-24.0	0.193	-28.0	
1	2	0.836	1.195			0.781	1.281	2.9	2.07	0.781	0.618	-12.3	0.500	-19.1	0.414	-24.0	0.351	-28.0	
1	3	0.885	1.125			0.847	1.180	4.3	2.07	0.847	0.721	-12.3	0.618	-19.1	0.535	-24.0	0.469	-28.0	
1	5	0.932	1.073			0.905	1.105	7.1	2.04	0.905	0.820	-12.3	0.744	-19.1	0.677	-24.0	0.618	-28.0	
1	10	0.985	1.036			0.951	1.051	14.2	2.03	0.951	0.905	-12.3	0.861	-19.1	0.820	-24.0	0.781	-28.0	
1	20	0.992	1.018			0.975	1.025	28.3	2.03	0.975	0.951	-12.3	0.928	-19.1	0.905	-24.0	0.883	-28.0	
6th Order Butterworth Bandpass Filter Normalized to its Center Frequency, $f_{0BP} = 1$, and -3dB Bandwidth (BW)																			
Q3																			
1	1	0.650	1.539	1.000		0.500	2.000	2.2	4.79	0.500	0.414	-18.2	0.303	-28.6	0.236	-36.1	0.193	-41.9	
1	2	0.805	1.242	1.000		0.781	1.281	4.1	4.18	0.781	0.618	-18.2	0.500	-28.6	0.414	-36.1	0.351	-41.9	
1	3	0.856	1.155	1.000		0.847	1.180	6.1	3.0	0.847	0.721	-18.2	0.618	-28.6	0.535	-36.1	0.469	-41.9	
1	5	0.917	1.091	1.000		0.905	1.105	10.0	5.0	0.905	0.820	-18.2	0.744	-28.6	0.677	-36.1	0.618	-41.9	
1	10	0.958	1.044	1.000		0.951	1.051	20.0	4.01	0.951	0.905	-18.2	0.861	-28.6	0.820	-36.1	0.781	-41.9	
1	20	0.979	1.022	1.000		0.975	1.025	40.0	4.00	0.975	0.951	-18.2	0.928	-28.6	0.905	-36.1	0.883	-41.9	
8th Order Butterworth Bandpass Filter Normalized to its Center Frequency, $f_{0BP} = 1$, and -3dB Bandwidth (BW)																			
Q3 = Q4																			
1	1	0.809	1.237	0.636	1.574	0.500	2.000	1.1	2.9	10.14	0.500	0.414	-24.0	0.303	-38.0	0.236	-48.1	0.193	-55.8
1	2	0.907	1.103	0.795	1.259	0.781	1.281	2.2	5.4	8.48	0.781	0.618	-24.0	0.500	-38.0	0.414	-48.1	0.351	-55.8
1	3	0.938	1.066	0.858	1.166	0.847	1.180	3.3	7.9	8.15	0.847	0.721	-24.0	0.618	-38.0	0.535	-48.1	0.469	-55.8
1	5	0.962	1.039	0.912	1.097	0.905	1.105	5.4	13.1	8.05	0.905	0.820	-24.0	0.744	-38.0	0.677	-48.1	0.618	-55.8
1	10	0.981	1.019	0.955	1.047	0.951	1.051	10.8	26.2	8.00	0.951	0.905	-24.0	0.861	-38.0	0.820	-48.1	0.781	-55.8
1	20	0.990	1.010	0.977	1.023	0.975	1.025	21.6	52.3	8.00	0.975	0.951	-24.0	0.928	-38.0	0.905	-48.1	0.883	-55.8

Table 2. 4th Order Chebyshev Bandpass Filter Normalized to its Center Frequency $f_{0BP} = 1$

f_{0BP} (Hz)	f_{0BP}/BW_1 (Hz)	f_{01} (Hz)	f_{02} (Hz)	f_{0BP}/BW_2 (Hz)	f_{-3dB} (Hz)	f_{-3dB} (Hz)	$Q1 = Q2$	K	f_1 (Hz)	f_2 (Hz)	GAIN AT f_2 (dB)-A2	f_3 (Hz)	GAIN AT f_3 (dB)-A3	f_4 (Hz)	GAIN AT f_4 (dB)-A4	GAIN AT f_5 (dB)-A5
Passband Ripple, $A_{MAX} = 0.1dB$																
1	1	0.488	2.050	0.52	0.423	2.364	1.1	3.81	0.500	0.414	-3.2	0.303	-0.87	0.236	-13.6	0.193
1	2	0.703	1.422	1.03	0.626	1.597	1.8	2.66	0.781	0.618	-3.2	0.500	-0.87	0.414	-13.6	0.351
1	3	0.793	1.261	1.54	0.727	1.375	2.6	2.48	0.847	0.721	-3.2	0.618	-0.87	0.535	-13.6	0.469
1	5	0.871	1.148	2.58	0.825	1.213	4.3	2.38	0.905	0.820	-3.2	0.744	-0.87	0.677	-13.6	0.618
1	10	0.933	1.071	5.15	0.908	1.102	8.5	2.38	0.951	0.905	-3.2	0.861	-0.87	0.820	-13.6	0.781
1	20	0.966	1.035	10.31	0.953	1.050	16.9	2.37	0.975	0.951	-3.2	0.928	-0.87	0.905	-13.6	0.883
Passband Ripple, $A_{MAX} = 0.5dB$																
1	1	0.602	1.660	0.72	0.523	1.912	1.6	3.80	0.500	0.414	-7.9	0.303	-15.0	0.236	-20.2	0.193
1	2	0.777	1.287	1.44	0.711	1.406	2.9	3.17	0.781	0.618	-7.9	0.500	-15.0	0.414	-20.2	0.351
1	3	0.845	1.182	2.16	0.795	1.258	4.3	3.07	0.847	0.721	-7.9	0.618	-15.0	0.535	-20.2	0.469
1	5	0.904	1.106	3.60	0.871	1.149	7.1	3.03	0.905	0.820	-7.9	0.744	-15.0	0.677	-20.2	0.618
1	10	0.951	1.051	7.19	0.933	1.072	14.1	2.98	0.951	0.905	-7.9	0.861	-15.0	0.820	-20.2	0.781
1	20	0.975	1.025	14.49	0.966	1.035	28.1	2.97	0.975	0.951	-7.9	0.928	-15.0	0.905	-20.2	0.883
Passband Ripple, $A_{MAX} = 1.0dB$																
1	1	0.539	1.564	0.82	0.562	1.779	2.0	4.42	0.500	0.414	-10.3	0.303	-17.7	0.236	-23.0	0.193
1	2	0.789	1.251	1.64	0.741	1.349	3.7	3.85	0.781	0.618	-10.3	0.500	-17.7	0.414	-23.0	0.351
1	3	0.861	1.161	2.47	0.818	1.223	5.5	3.76	0.847	0.721	-10.3	0.618	-17.7	0.535	-23.0	0.469
1	5	0.914	1.094	4.12	0.886	1.129	9.2	3.71	0.905	0.820	-10.3	0.744	-17.7	0.677	-23.0	0.618
1	10	0.956	1.046	8.20	0.941	1.063	18.2	3.70	0.951	0.905	-10.3	0.861	-17.7	0.820	-23.0	0.781
1	20	0.978	1.022	16.39	0.970	1.031	36.5	3.63	0.975	0.951	-10.3	0.928	-17.7	0.905	-23.0	0.883
Passband Ripple, $A_{MAX} = 2.0dB$																
1	1	0.688	1.496	0.93	0.596	1.672	2.7	6.00	0.500	0.414	-12.7	0.303	-20.3	0.236	-25.5	0.193
1	2	0.816	1.225	1.86	0.767	1.304	5.1	5.30	0.781	0.618	-12.7	0.500	-20.3	0.414	-25.5	0.351
1	3	0.873	1.145	2.79	0.837	1.195	7.5	5.22	0.847	0.721	-12.7	0.618	-20.3	0.535	-25.5	0.469
1	5	0.922	1.065	4.65	0.898	1.113	12.5	5.13	0.905	0.820	-12.7	0.744	-20.3	0.677	-25.5	0.618
1	10	0.960	1.041	9.35	0.946	1.065	24.9	5.13	0.951	0.905	-12.7	0.861	-20.3	0.820	-25.5	0.781
1	20	0.980	1.021	18.87	0.974	1.027	49.8	5.07	0.975	0.951	-12.7	0.928	-20.3	0.905	-25.5	0.883

* f_{0BP}/BW_1 - This is the ratio of the bandpass filter center frequency to the ripple bandwidth of the filter.

** f_{0BP}/BW_2 - This is the ratio of the bandpass filter center frequency to the -30dB filter bandwidth.

Table 3. 6th Order Chebyshev Bandpass Filter Normalized to its Center Frequency $f_{op} = 1$

f_{op} (Hz)	$f_{op}BW_1$ (Hz)	f_{c1} (Hz)	f_{c2} (Hz)	f_{c3} (Hz)	$f_{op}BW_2$ (Hz)	f_{-3dB} (Hz)	f_{-3dB} (Hz)	Q = 3	K	f_1 (Hz)	f_3 (Hz)	GAIN AT f_3 (dB)-A2	f_5 (Hz)	GAIN AT f_5 (dB)-A3	f_7 (Hz)	GAIN AT f_7 (dB)-A4	f_9 (Hz)	GAIN AT f_9 (dB)-A5	
Passband Ripple, $A_{MAX} = 0.1dB$																			
1	1	0.658	1.791	1.000	0.72	0.523	1.912	2.4	1.0	9.9	0.500	0.414	-12.2	0.303	-23.6	0.236	-31.4	0.193	-37.3
1	2	0.711	1.349	1.000	1.44	0.711	1.406	4.3	2.1	7.9	0.781	0.618	-12.2	0.500	-23.6	0.414	-31.4	0.351	-37.3
1	3	0.818	1.222	1.000	2.16	0.795	1.258	6.3	3.1	7.5	0.847	0.721	-12.2	0.618	-23.6	0.535	-31.4	0.469	-37.3
1	5	0.886	1.128	1.000	3.60	0.871	1.149	10.4	5.2	7.4	0.905	0.820	-12.2	0.744	-23.6	0.677	-31.4	0.618	-37.3
1	10	0.941	1.062	1.000	7.19	0.933	1.072	20.6	10.3	7.3	0.951	0.905	-12.2	0.861	-23.6	0.820	-31.4	0.781	-37.3
1	20	0.970	1.030	1.000	14.49	0.966	1.035	41.3	20.6	7.3	0.975	0.951	-12.2	0.928	-23.6	0.905	-31.4	0.883	-37.3
Passband Ripple, $A_{MAX} = 0.5dB$																			
1	1	0.689	1.641	1.000	0.86	0.574	1.741	3.6	1.6	14.8	0.500	0.414	-19.2	0.303	-30.8	0.236	-38.6	0.193	-44.5
1	2	0.776	1.288	1.000	1.72	0.750	1.333	6.6	3.2	12.5	0.781	0.618	-19.2	0.500	-30.8	0.414	-38.6	0.351	-44.5
1	3	0.844	1.185	1.000	2.57	0.824	1.213	9.7	4.8	12.0	0.847	0.721	-19.2	0.618	-30.8	0.535	-38.6	0.469	-44.5
1	5	0.903	1.107	1.000	4.29	0.890	1.123	16.1	8.0	11.8	0.905	0.820	-19.2	0.744	-30.8	0.677	-38.6	0.618	-44.5
1	10	0.950	1.052	1.000	8.55	0.943	1.060	32.0	16.0	11.8	0.951	0.905	-19.2	0.861	-30.8	0.820	-38.6	0.781	-44.5
1	20	0.975	1.026	1.000	16.95	0.971	1.030	63.8	32.0	11.4	0.975	0.951	-19.2	0.928	-30.8	0.905	-38.6	0.883	-44.5
Passband Ripple, $A_{MAX} = 1.0dB$																			
1	1	0.626	1.598	1.000	0.91	0.593	1.687	4.5	2.0	20.1	0.500	0.414	-22.5	0.303	-34.0	0.236	-41.9	0.193	-47.8
1	2	0.787	1.271	1.000	1.83	0.763	1.310	8.3	4.1	17.1	0.781	0.618	-22.5	0.500	-34.0	0.414	-41.9	0.351	-47.8
1	3	0.852	1.174	1.000	2.74	0.834	1.199	12.3	6.1	16.7	0.847	0.721	-22.5	0.618	-34.0	0.535	-41.9	0.469	-47.8
1	5	0.908	1.101	1.000	4.59	0.897	1.115	20.3	10.1	16.4	0.905	0.820	-22.5	0.744	-34.0	0.677	-41.9	0.618	-47.8
1	10	0.953	1.050	1.000	9.17	0.947	1.066	40.5	20.2	16.4	0.951	0.905	-22.5	0.861	-34.0	0.820	-41.9	0.781	-47.8
1	20	0.976	1.024	1.000	18.18	0.973	1.028	81.0	40.5	16.4	0.975	0.951	-22.5	0.928	-34.0	0.905	-41.9	0.883	-47.8
Passband Ripple, $A_{MAX} = 2.0dB$																			
1	1	0.639	1.565	1.000	0.97	0.609	1.642	6.0	2.7	31.7	0.500	0.414	-26.0	0.303	-37.5	0.236	-45.4	0.193	-51.3
1	2	0.795	1.257	1.000	1.94	0.775	1.291	11.1	5.4	27.4	0.781	0.618	-26.0	0.500	-37.5	0.414	-45.4	0.351	-51.3
1	3	0.858	1.165	1.000	2.91	0.843	1.187	16.5	8.1	26.7	0.847	0.721	-26.0	0.618	-37.5	0.535	-45.4	0.469	-51.3
1	5	0.912	1.096	1.000	4.83	0.902	1.109	27.2	13.6	26.2	0.905	0.820	-26.0	0.744	-37.5	0.677	-45.4	0.618	-51.3
1	10	0.955	1.047	1.000	9.71	0.950	1.053	54.3	27.1	26.0	0.951	0.905	-26.0	0.861	-37.5	0.820	-45.4	0.781	-51.3
1	20	0.977	1.023	1.000	19.61	0.975	1.026	108.5	54.2	26.0	0.975	0.951	-26.0	0.928	-37.5	0.905	-45.4	0.883	-51.3

* $f_{op}BW_1$ - This is the ratio of the bandpass filter center frequency to the ripple bandwidth of the filter.

** $f_{op}BW_2$ - This is the ratio of the bandpass filter center frequency to the $-3dB$ filter bandwidth.



Table 4. 8th Order Chebyshev Bandpass Filter Normalized to its Center Frequency $f_{opp} = 1$

f_{opp} (Hz)	f_{opp}/BW_1 (Hz)	f_{o1} (Hz)	f_{z2} (Hz)	f_{z3} (Hz)	f_{z4} (Hz)	f_{opp}/BW_2 (Hz)	f_{-3dB} (Hz)	f_{-3dB} (Hz)	Q1=02	Q3=04	K	f_1 (Hz)	f_3 (Hz)	GAIN AT f_3 (dB)-A2	f_5 (Hz)	GAIN AT f_5 (dB)-A3	f_7 (Hz)	GAIN AT f_7 (dB)-A4	f_9 (Hz)	GAIN AT f_9 (dB)-A5	
Passband Ripple, $A_{MAX} = 0.1dB$																					
1	1	0.785	1.274	0.584	1.713	0.82	1.776	1.6	1.6	4.4	40.6	0.500	0.414	-23.4	0.303	-38.8	0.236	-49.3	0.193	-57.1	
1	2	0.889	1.125	0.757	1.320	1.65	0.742	1.348	3.2	7.9	32.1	0.781	0.618	-23.4	0.500	-38.8	0.414	-49.3	0.351	-57.1	
1	3	0.925	1.081	0.830	1.204	2.48	0.818	1.222	4.7	11.6	30.5	0.847	0.721	-23.4	0.618	-38.8	0.535	-49.3	0.469	-57.1	
1	5	0.954	1.048	0.894	1.118	4.12	0.886	1.129	7.9	19.1	29.9	0.905	0.820	-23.4	0.744	-38.8	0.677	-49.3	0.618	-57.1	
1	10	0.977	1.023	0.945	1.058	8.20	0.941	1.063	15.7	37.9	29.8	0.951	0.905	-23.4	0.861	-38.8	0.820	-49.3	0.781	-57.1	
1	20	0.988	1.012	0.972	1.028	16.39	0.970	1.031	31.4	75.7	29.8	0.975	0.951	-23.4	0.928	-38.8	0.905	-49.3	0.883	-57.1	
Passband Ripple, $A_{MAX} = 0.5dB$																					
1	1	0.808	1.238	0.613	1.632	0.91	1.686	2.4	2.4	6.4	90.1	0.500	0.414	-30.2	0.303	-45.5	0.236	-56.0	0.193	-63.9	
1	2	0.900	1.111	0.777	1.286	1.83	0.763	1.310	4.8	11.8	74.3	0.781	0.618	-30.2	0.500	-45.5	0.414	-56.0	0.351	-63.9	
1	3	0.932	1.073	0.845	1.183	2.74	0.834	1.199	7.1	17.4	71.5	0.847	0.721	-30.2	0.618	-45.5	0.535	-56.0	0.469	-63.9	
1	5	0.959	1.043	0.903	1.107	4.59	0.897	1.115	11.8	28.7	70.0	0.905	0.820	-30.2	0.744	-45.5	0.677	-56.0	0.618	-63.9	
1	10	0.979	1.021	0.950	1.052	9.17	0.947	1.056	23.6	57.1	70.0	0.951	0.905	-30.2	0.861	-45.5	0.820	-56.0	0.781	-63.9	
1	20	0.989	1.010	0.975	1.026	18.18	0.973	1.028	47.2	114.0	70.0	0.975	0.951	-30.2	0.928	-45.5	0.905	-56.0	0.883	-63.9	
Passband Ripple, $A_{MAX} = 1.0dB$																					
1	1	0.814	1.228	0.622	1.607	0.95	1.656	3.0	3.0	8.0	162.8	0.500	0.414	-32.0	0.303	-48.3	0.236	-58.8	0.193	-66.6	
1	2	0.903	1.107	0.784	1.275	1.90	0.771	1.297	6.0	14.8	133.2	0.781	0.618	-32.0	0.500	-48.3	0.414	-58.8	0.351	-66.6	
1	3	0.934	1.070	0.850	1.177	2.85	0.840	1.191	8.9	21.8	128.1	0.847	0.721	-32.0	0.618	-48.3	0.535	-58.8	0.469	-66.6	
1	5	0.960	1.041	0.906	1.103	4.74	0.900	1.111	14.9	36.0	127.7	0.905	0.820	-32.0	0.744	-48.3	0.677	-58.8	0.618	-66.6	
1	10	0.980	1.020	0.952	1.050	9.52	0.949	1.054	29.7	71.7	124.0	0.951	0.905	-32.0	0.861	-48.3	0.820	-58.8	0.781	-66.6	
1	20	0.990	1.010	0.976	1.025	18.87	0.974	1.027	59.4	143.0	120.0	0.975	0.951	-32.0	0.928	-48.3	0.905	-58.8	0.883	-66.6	
Passband Ripple, $A_{MAX} = 2.0dB$																					
1	1	0.820	1.220	0.629	1.588	0.98	1.631	4.0	4.0	10.6	374.8	0.500	0.414	-35.4	0.303	-50.8	0.236	-61.3	0.193	-89.2	
1	2	0.905	1.104	0.789	1.268	1.96	0.777	1.287	7.9	19.6	312.6	0.781	0.618	-35.4	0.500	-50.8	0.414	-61.3	0.351	-89.2	
1	3	0.936	1.066	0.853	1.172	2.95	0.845	1.184	11.9	29.0	302.0	0.847	0.721	-35.4	0.618	-50.8	0.535	-61.3	0.469	-89.2	
1	5	0.961	1.040	0.909	1.100	4.90	0.903	1.107	19.7	47.9	302.0	0.905	0.820	-35.4	0.744	-50.8	0.677	-61.3	0.618	-89.2	
1	10	0.980	1.020	0.953	1.049	9.80	0.950	1.052	39.5	95.4	302.0	0.951	0.905	-35.4	0.861	-50.8	0.820	-61.3	0.781	-89.2	
1	20	0.990	1.010	0.976	1.024	19.61	0.975	1.026	79.0	190.0	302.0	0.975	0.951	-35.4	0.928	-50.8	0.905	-61.3	0.883	-89.2	

* f_{opp}/BW_1 - This is the ratio of the bandpass filter center frequency to the ripple bandwidth of the filter.

** f_{opp}/BW_2 - This is the ratio of the bandpass filter center frequency to the -3dB filter bandwidth.

Chebyshev or Butterworth — A System Designers Confusion

The filter designer/mathematician is familiar with terms such as:

$$K_C = \tanh A$$

$$A = \frac{1}{n} \cosh^{-1} \frac{1}{\epsilon}$$

$$\text{Ripple bandwidth} = 1/\cosh A$$

$$\text{and } A_{dB} = 10 \log [1 + \epsilon^2 (C_n^2(\Omega))]$$

This is all gobbledeygook (not to be confused with flooby-dust) to the system designer. The system designer is accustomed to -3dB bandwidths and may be tempted to use only Butterworth filters because they have the cherished -3dB bandwidths. But specs. are specs. and Butterworth bandpass filters are only so good. Chebyshev bandpass filters trade off ripple in the passband for somewhat steeper rolloff to the stopband. More ripple translates to a higher "Q" filter. The pain of the filter designer is sometimes tolerable to the system designer.

Tables 1 through 4 are unique (we think) in that they present -3dB bandwidths for Chebyshev filters for use by system designers. Nevertheless we would be amiss to Mr. Chebyshev if we did not, at least, explain ripple bandwidth.

Figure 13 shows the Chebyshev bandpass filter at frequencies near the passband.

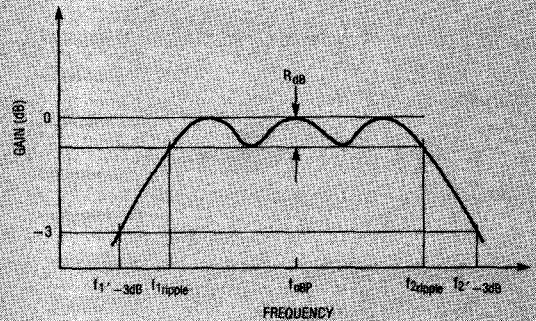


Figure 13. Typical Chebyshev BP Filter — Close-up of Passband

It can be clearly seen that the ripple bandwidth ($f_{1\text{ripple}} - f_{2\text{ripple}}$) is the band of passband frequencies where the ripple is less than or equal to a specific value (R_{dB}). The -3dB bandwidth is seen to be greater than the ripple bandwidth and that is the subject of much confusion on the part of the system designer.

Tables 1 through 4 allow the system designer to use -3dB bandwidths to specify Chebyshev BP filters. The Chebyshev approximation to the ideal BP filter has many benefits over the Butterworth filter near the cutoff frequency.

YOU CAN DESIGN WITH CHEBYSHEV FILTERS!!!

EXAMPLE 3 — DESIGN

Use Table 4 to design an 8th order all pole Chebyshev bandpass filter centered at $f_{0BP} = 10.2\text{kHz}$ with a -3dB bandwidth equal to 800Hz as shown in Figure 14.

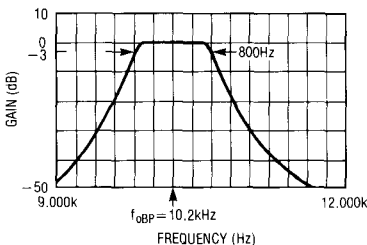


Figure 14. Example 3 — 8th Order Chebyshev BP Filter
 $f_{0BP} = 10.2\text{kHz}$, $BW = 800\text{Hz}$

We choose $A_{MAX} = 0.1\text{dB}$. Now we calculate:

$$\frac{f_{0BP}}{f_{BW(-3dB)}} = \frac{10.2\text{kHz}}{800\text{Hz}} = 12.75$$

We can now extract from Table 4 the following line:

f_{0BP}	f_{0BP}/BW_1	$f_{01}(\text{Hz})$	$f_{02}(\text{Hz})$	$f_{03}(\text{Hz})$	$f_{04}(\text{Hz})$	f_{0BP}/BW_2	$Q_1 = Q_2$	$Q_3 = Q_4$	K
1	10	0.977	1.023	0.945	1.058	8.20	15.7	37.9	29.8

Since our bandwidth ratio f_{0BP}/BW_2 is not exactly on a chart line, but between two lines, we must arithmetically scale to obtain our design parameters. Our f_{0BP}/BW_2 ratio lies between 8.2 and 16.39. (Remember, this is -3dB BW!)

Application Note 27A

For a symmetrical bandpass filter the poles are symmetrical about f_{oBP} . Then:

$$(f_{o2} - f_{o1}) = (1.023 - 0.977) \times 10.2\text{kHz} \times \left(\frac{8.2}{12.75}\right) = 302\text{Hz}$$

Note: $\left(\frac{8.2}{12.75}\right) = \frac{f_{oBP}}{BW}$ Scaling Factor

So our first two poles lie symmetrically about f_o (10.2kHz) and are 302Hz apart:

$$f_{o2} = 10200\text{Hz} + 302\text{Hz}/2 = 10351\text{Hz}$$

$$f_{o1} = 10200\text{Hz} - 302\text{Hz}/2 = 10049\text{Hz}$$

The Q of these two poles is equal and is also scaled:

$$Q_1 = Q_2 = 15.7 \times \frac{12.75}{8.2} = 24.4$$

We next calculate the two additional poles:

$$(f_{o4} - f_{o3}) = (1.058 - 0.945) \times 10.2\text{kHz} \times \frac{8.2}{12.75} = 741\text{Hz}$$

$$f_{o3} = 10200\text{Hz} - 741\text{Hz}/2 = 9830\text{Hz}$$

$$f_{o4} = 10200\text{Hz} + 741\text{Hz}/2 = 10571\text{Hz}$$

The Q's are:

$$Q_3 = Q_4 = 37.9 \times \frac{12.75}{8.2} = 58.9$$

Q's of this magnitude are difficult to realize no matter how the filter is realized. The filter designer should strive for Q's no greater than 20 and perhaps no greater than 10 at frequencies above 20kHz. K, for this example, is not scaled and will be equal to 29.8 from Table 4.

Example 3 — Frequency Response Estimation

Table 4 (and also Tables 1, 2 and 3) may be used by the filter designer to obtain a good approximation to the overall shape of the bandpass filter. Referring to Figure 12 for Chebyshev filters, we may use the charts to find f_3, f_5, f_7, \dots . These frequencies define the band edges at 2, 3, 4,.....times the ripple bandwidth of the Chebyshev Filter.

Example 3 specified a 10.2kHz bandpass filter with an 800Hz – 3dB bandwidth. Our task, if we choose to accept

it, is to convert our – 3dB bandwidth to the ripple bandwidth of the filter so that we may use the tables.

Recalling that:

$$\frac{f_{oBP}}{BW_{2(-3dB)}} = 12.75 \quad \text{and that } f_{oBP} = 1,$$

(Because all the tables are normalized), we calculate $BW_{2(-3dB)} = .0784$

Comparing the Table 4 values for $A_{MAX} = 0.1\text{dB}$ we note that:

$$\frac{f_{oBP}}{BW_{1(\text{ripple})}} \cong \frac{f_{oBP}}{BW_{2(-3dB)}} \times (\text{Scaling Factor})$$

For $A_{MAX} = 0.1\text{dB}$, 8th order Chebyshev, this factor is approximately 0.82. For other order filters and/or different values of A_{MAX} we can examine the corresponding chart values to find our scaling factor.

So our ripple BW is:

$$BW_{2(-3dB)} \times (\text{Scaling Factor}) = BW_{1(\text{ripple})}$$

$$.0784 \times 0.82 = .0643$$

Now we can calculate f_3, f_5, f_7, \dots . Notice that once we find f_3, f_5, f_7, \dots it does not matter where on the table our filter falls. The filter bandwidth determines f_3, f_5, f_7, \dots and once we know these frequencies we can directly get our gains at these frequencies.

By formula:

$$(f_x, f_{x+1}) = \frac{\pm nBW + \sqrt{(nBW)^2 + 4(f_{oBP})^2}}{2}$$

for our case $f_{oBP} = 1$

Calculating:

$$2BW = .1286 \quad \frac{\pm 2BW + \sqrt{(.1286)^2 + 4}}{2} = 1.0664, 0.9378$$

$$3BW = .1929 \quad \frac{\pm 3BW + \sqrt{(.1929)^2 + 4}}{2} = 1.1011, 0.9082$$

Then we can denormalize to find points for our Bode plot:

$$(f_3, f_4) = 0.9378 \times f_{0BP} = 0.9378 \times 10.2\text{kHz} = 9.566\text{kHz}$$

$$1.0664 \times f_{0BP} = 1.0664 \times 10.2\text{kHz} = 10.877\text{kHz}$$

Gain = -23.4dB both f_3 and f_4

$$(f_5, f_6) = 0.9082 \times f_{0BP} = 0.9082 \times 10.2\text{kHz} = 9.264\text{kHz}$$

$$1.1011 \times f_{0BP} = 1.1011 \times 10.2\text{kHz} = 11.231\text{kHz}$$

Gain = -38.8dB both f_5 and f_6

Example 3 — Implementation

The 10.2kHz (f_{0BP}), 8th order bandpass filter can be implemented with an LTC1064A using three sections in mode 2 and one section in mode 3. The implementation is shown briefly in Figures 15 and 16. The calculations are not shown here, but are similar to the previous hardware implementations of example 1 and 2.

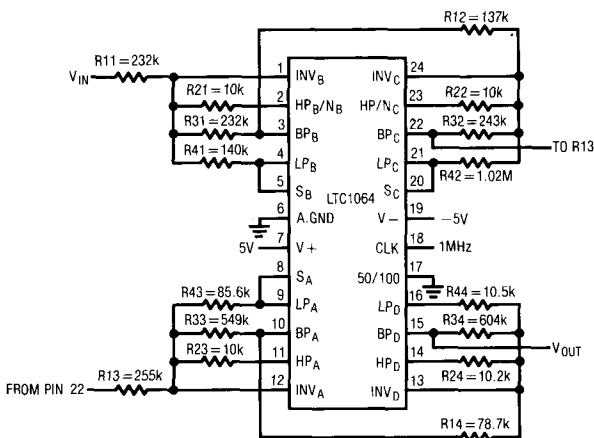


Figure 15. LTC1064 Implementation Pinout — 10.2kHz 8th Order BPF

Application Note 27A

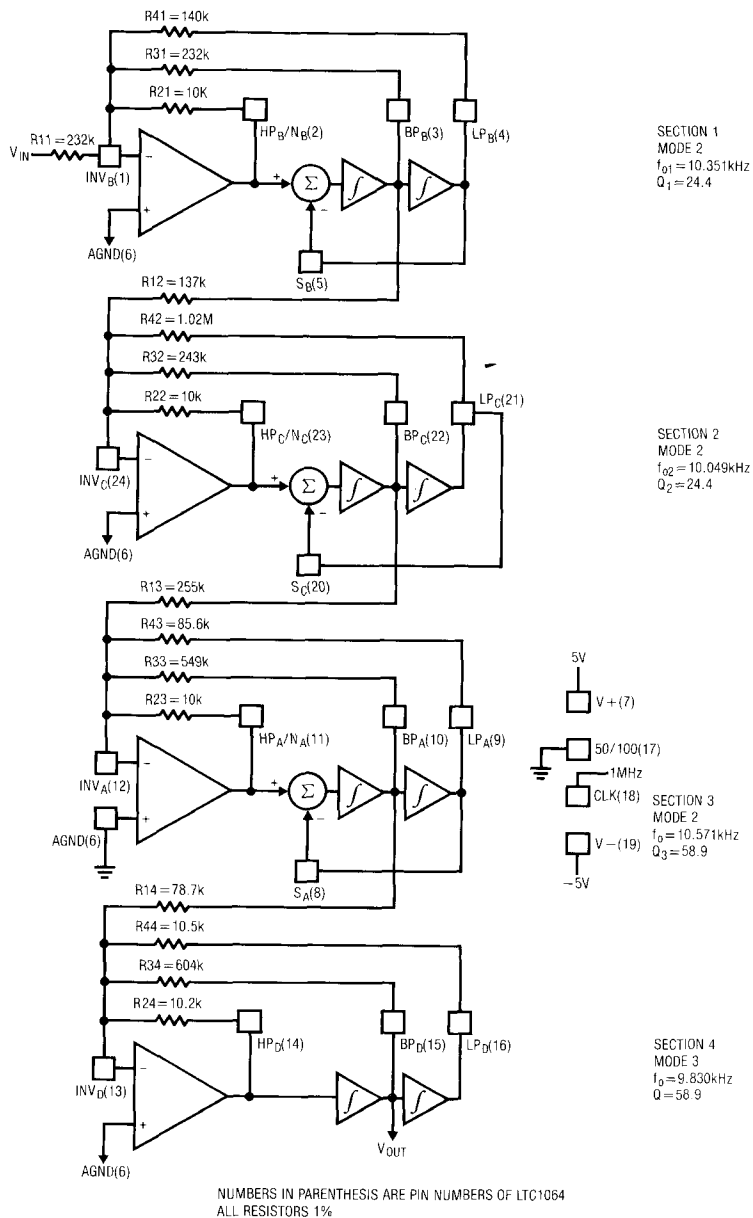


Figure 16. Implementation of 10.2kHz 8th Order BPF – Section by Section For LTC1064

Thermocouple Measurement

Jim Williams

Introduction

In 1822, Thomas Seebeck, an Estonian physician, accidentally joined semicircular pieces of bismuth and copper (Figure 1) while studying thermal effects on galvanic arrangements. A nearby compass indicated a magnetic disturbance. Seebeck experimented repeatedly with different metal combinations at various temperatures, noting relative magnetic field strengths. Curiously, he did not believe that electric current was flowing, and preferred to describe the effect as "thermo-magnetism." He published his results in a paper, "Magnetische Polarisation der Metalle und Erze durch Temperatur-Differenz" (see references).

Subsequent investigation has shown the "Seebeck Effect" to be fundamentally electrical in nature, repeatable, and quite useful. Thermocouples, by far the most common transducer, are Seebeck's descendants.

Thermocouples in Perspective

Temperature is easily the most commonly measured physical parameter. A number of transducers serve temperature measuring needs and each has advantages and considerations. Before discussing thermocouple based measurement it is worthwhile putting these sensors in perspective. Figure 2's chart shows some common contact temperature sensors and lists characteristics. Study reveals thermocouple strengths and weaknesses compared to other sensors. In general, thermocouples are inexpensive, wide range sensors. Their small size makes them fast and their low output impedance is a benefit. The inherent voltage output eliminates the need for excitation.

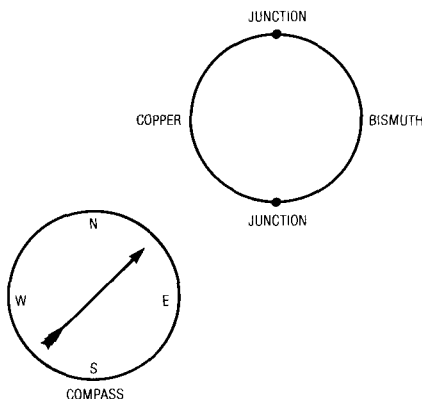


Figure 1. The Arrangement for Dr. Seebeck's Accidental Discovery of "Thermo-Magnetism"

Application Note 28

TYPE	RANGE OF OPERATION	SENSITIVITY AT +25°C	ACCURACY	LINEARITY	SPEED IN STIRRED OIL	SIZE	PACKAGE	COST	COMMENTS
Thermocouples (All Types)	-270°C to +1800°C	Typically less than 50 μ V/°C	\pm 0.5°C with Reference	Poor over wide range, better over \approx 100°C	Typically 1 Sec. Some Types are Faster	0.02 In. Bead Typical, 0.0005 In. Units are Available	Metallic Bead, Variety of Probes Available.	\$1 to \$50 Depending on Type, Specifications and Package.	Requires Reference, Low Level Output Requires Stable Signal Conditioning Components.
Thermistors and Thermistor Composites	-100°C to +450°C	\approx 5%/°C for Thermistors. \approx 0.5%/°C for Linearized Units.	\pm 0.1°C Standard from -40°C to +100°C; \pm 0.01°C from 0°C to +60°C Available.	\pm 0.2°C for Linearized Composite Units over 100°C Ranges	1 to 10 Sec is Standard; 3 to 100ms Types are Available	Beads Can be as Small as 0.005 In., But 0.04 to 0.1 In. is Typical. "Flake" Types are Only 0.001 In. Thick.	Glass, Epoxy, Teflon Encapsulated, Metal Housing, etc.	\$2 to \$10 for Standard Units. \$10 to \$350 for High Precision Types and Specials	Highest Temperature Sensitivity of Any Common Sensor. Special Units Required for Long Term Stability Above +100°C.
Platinum Resistance Wire	-250°C to +900°C	Approximately +0.5%/°C	\pm 0.1°C Readily Available. \pm 0.01°C in Precision Standards — Lab Units	Nearly Linear Over Large Spans; Typically Within 1° Over 200°C Ranges	Typically Several Seconds	1/8 to 1/4 In. Typical, Smaller Sizes Available	Glass, Epoxy, Ceramic, Teflon, Metal, Etc.	\$25 to \$1000 Depending on Specs; Most Industrial Types Below \$100	Sets Standard for Stability Over Long Term. Has Wider Temp. Range Than Thermistor, but Lower Sensitivity.
Diodes and Transistors	-270°C to +175°C	-2.2 mV/°C (Approx. 0.33%/°C)	\pm 2°C to \pm 5°C Over -55°C to +125°C	Within 2° Over Operating Range	1 to 10 Sec. is Standard. Small Diode Packages Permit Speeds in ms Range	Standard Diode and Transistor Case Sizes. Glass Passivated Chips Permit Extremely Small Sizes.	Glass, Metal	Below 50¢. Cryogenic Units More Expensive	Require Individual Calibration. Must be Driven from Current Source for Optimum Performance. Extremely Inexpensive. Calibrated Cryogenic Types Available.
Integrated Circuit	-85°C to +125°C Typical	0.4%/°C Typical	Over -55°C to +125°C	Within 1° (0.2° From 0°C to +70°C) Typical	Several Seconds	TO-18 Transistor Package Size. Also MiniDIP	Metal, Plastic	\$1 to \$10	Current and Voltage Outputs Available

Figure 2. Characteristics of Some Contact Temperature Sensors (Chart Adapted from Reference 2)

JUNCTION MATERIALS	APPROXIMATE SENSITIVITY IN $\mu\text{V}/^\circ\text{C}$ AT 25°C	USEFUL TEMPERATURE RANGE ($^\circ\text{C}$)	APPROXIMATE VOLTAGE SWING OVER RANGE	LETTER DESIGNATION
Copper — Constantan	40.6	-270 to + 600	25.0mV	T
Iron — Constantan	51.70	-270 to +1000	60.0mV	J
Chromel — Alumel	40.6	-270 to +1300	55.0mV	K
Chromel — Constantan	60.9	-270 to +1000	75.0mV	E
Platinum 10% — Rhodium/Platinum	6.0	0 to +1550	16.0mV	S
Platinum 13% — Rhodium/Platinum	6.0	0 to +1600	19.0mV	R

Figure 3. Temperature vs Output for Some Thermocouple Types

Signal Conditioning Issues

Potential problems with thermocouples include low level outputs, poor sensitivity and non-linearity (see Figures 3 and 4). The low level output requires stable signal conditioning components and makes system accuracy difficult to achieve. Connections (see Appendix A) in thermocouple systems must be made with great care to get good accuracy. Unintended thermocouple effects (e.g., solder and copper create a $3\mu\text{V}/^\circ\text{C}$ thermocouple) in system connections make "end-to-end" system accuracies better than 0.5°C difficult to achieve.

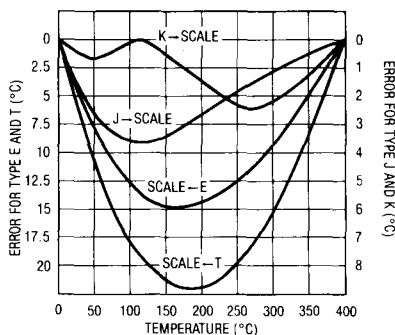


Figure 4. Thermocouple Nonlinearity for Types J, K, E and T Over 0°C - 400°C . Error Increases Over Wider Temperature Ranges.

Cold Junction Compensation

The unintended, unwanted and unavoidable parasitic thermocouples require some form of temperature reference for absolute accuracy. (See Appendix A for a discussion on minimizing these effects). In a typical system, a "cold junction" is used to provide a temperature reference

(Figure 5). The term "cold junction" derives from the historical practice of maintaining the reference junction at 0°C in an ice bath. Ice baths, while inherently accurate, are impractical in most applications. Another approach servo controls a Peltier cooler, usually at 0°C , to electronically simulate the ice bath (Figure 6). This approach* eliminates ice bath maintenance, but is too complex and bulky for most applications.

*A practical example of this technique appears in LTC Application Note AN-25, "Switching Regulators for Poets."

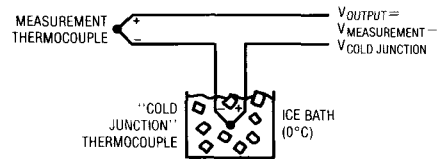


Figure 5. Ice Bath Based Cold Junction Compensator

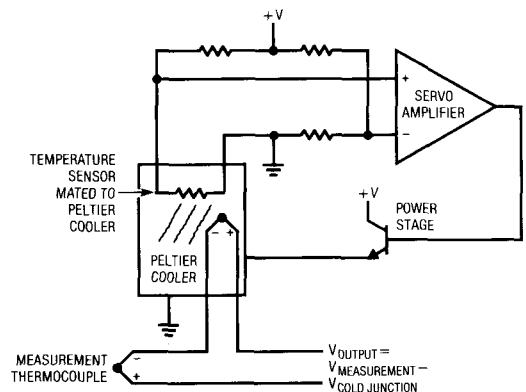


Figure 6. A 0°C Reference Based on Feedback Control of a Peltier Cooler (Sensor is Typically a Platinum RTD)

Application Note 28

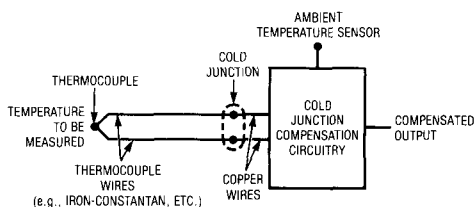


Figure 7. Typical Cold Junction Compensation Arrangement.
Cold Junction and Compensation Circuitry must be Isothermal

Figure 7 conveniently deals with the cold junction requirement. Here, the cold junction compensator circuitry does not maintain a stable temperature but tracks the cold junction. This temperature tracking, subtractive term has the same effect as maintaining the cold junction at constant temperature, but is simpler to implement. It is designed to produce 0V output at 0°C and have a slope equal to the thermocouple output (Seebeck coefficient) over the expected range of cold junction temperatures. For proper operation, the compensator must be at the same temperature as the cold junction.

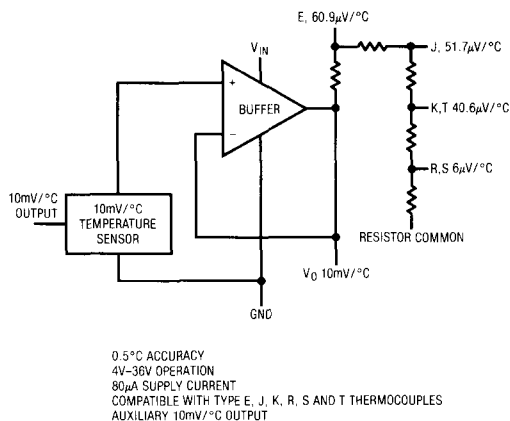


Figure 8. LT1025 Thermocouple Cold Junction Compensator

Figure 8 shows a monolithic cold junction compensator IC, the LT1025. This device measures ambient (e.g., cold junction) temperature and puts out a voltage scaled for use with the desired thermocouple. The low supply current minimizes self-heating, ensuring isothermal operation with the cold junction. It also permits battery or low power operation. The 0.5°C accuracy is compatible with overall achievable thermocouple system performance. Various compensated outputs allow one part to be used with many thermocouple types. Figure 9 uses an LT1025 and an amplifier to provide a scaled, cold junction compensated output. The amplifier provides gain for the difference between the LT1025 output and the type J thermocouple. C1 and C2 provide filtering, and R5 trims gain. R6 is a typical value, and may require selection to accommodate R5's trim range. Alternately, R6 may be re-scaled, and R5 enlarged, at some penalty in trim resolution. Figure 10 is similar, except that the type K thermocouple subtracts from the LT1025 in series-opposed fashion, with the residue fed to the amplifier. The optional pull down resistor allows readings below 0°C.

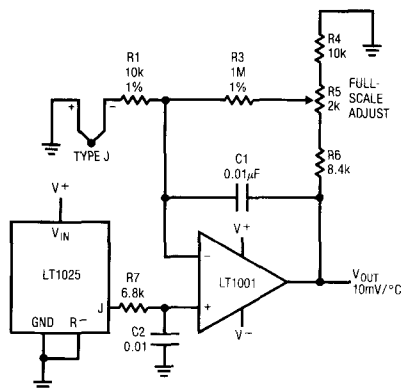


Figure 9. LT1025 Cold Junction Compensates a Type J Thermocouple. The Op Amp Provides the Amplified Difference Between the Thermocouple and the LT1025 Cold Junction Output.

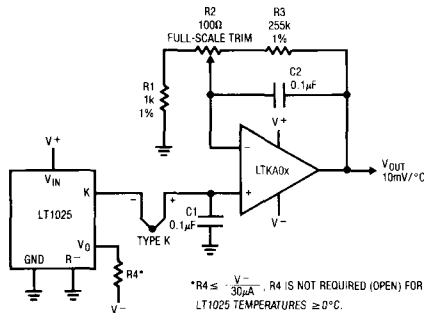


Figure 10. LT1025 Compensates a Type K Thermocouple. The Amplifier Provides Gain for the LT1025-Thermocouple Difference.

Amplifier Selection

The operation of these circuits is fairly straightforward, although amplifier selection requires care.

Thermocouple amplifiers need very low offset voltage and drift, and fairly low bias current if an input filter is used. The best precision bipolar amplifiers should be used for type J, K, E, and T thermocouples which have Seebeck coefficients of 40–60µV/°C. In particularly critical applications, or for R and S thermocouples (6–15µV/°C), a chopper-stabilized amplifier is required. Linear Technology offers two amplifiers specifically tailored for thermocouple applications. The LTKA0x is a bipolar design with extremely low offset (30µV), low drift (1.5µV/°C), very low bias current (1nA), and almost negligible warm-up drift (supply current is 400µA).

For the most demanding applications, the LTC1052 CMOS chopper-stabilized amplifier offers 5µV offset and 0.05µV/°C drift. Input bias current is 30pA, and gain is typically 30 million. This amplifier should be used for R and S thermocouples, especially if no offset adjustments can be tolerated, or where a large ambient temperature swing is expected. Alternatively, the LTC1050, which has similar drift and slightly higher noise can be used. If board space is at a premium, the LTC1050 has the capacitors internally.

Regardless of amplifier type, for best possible performance dual-in-line (DIP) packages should be used to avoid thermocouple effects in the kovar leads of TO-5 metal can packages. This is particularly true if amplifier supply current exceeds 500µA. These leads can generate both DC and AC offset terms in the presence of thermal gradients in the package and/or external air motion.

In many situations, thermocouples are used in high noise environments, and some sort of input filter is required. To reject 60Hz pick-up with reasonable capacitor values, input resistors in the 10k–100k range are needed. Under these conditions, bias current for the amplifier needs to be less than 1nA to avoid offset and drift effects.

To avoid gain error, high open loop gain is necessary for single-stage thermocouple amplifiers with 10mV/°C or higher outputs. A type K amplifier, for instance, with 100mV/°C output, needs a closed loop gain of 2,500. An ordinary op amp with a minimum loop of 50,000 would have an initial gain error of (2,500)/(50,000) = 5%! Although closed loop gain is commonly trimmed, temperature drift of open loop gain will have a deleterious effect on output accuracy. Minimum suggested loop gain for type E, J, K, and T thermocouples is 250,000. This gain is adequate for type R and S if output scaling is 10mV/°C or less.

Additional Circuit Considerations

Other circuit considerations involve protection and common-mode voltage and noise. Thermocouple lines are often exposed to static and accidental high voltages, necessitating circuit protection. Figure 11 shows two suggested approaches. These examples are designed to prevent excessive overloads from damaging circuitry. The added series resistance can serve as part of a filter. Effects of the added components on overall accuracy should be evaluated. Diode clamping to supply lines is effective, but leakage should be noted, particularly when large current limiting resistors are used. Similarly, IC bias currents combined with high value protection resistors can generate apparent measurement errors. Usually, a favorable compromise is possible, but sometimes the circuit configuration will be dictated by protection or noise rejection requirements.

Differential Thermocouple Amplifiers

Figure 12A shows a way to combine filtering and full differential sensing. This circuit features 120dB DC common-mode rejection if all signals remain within the LTC1043 supply voltage range. The LTC1043, a switched capacitor building block, transfers charge between the input "flying" capacitor and the output capacitor. The LTC1043's commutating frequency, which is settable, controls rate of charge

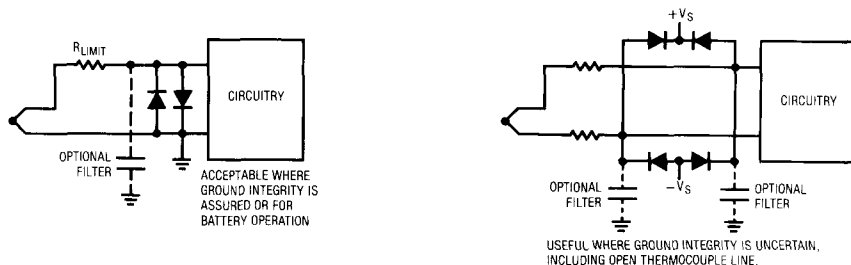


Figure 11. Input Protection Schemes

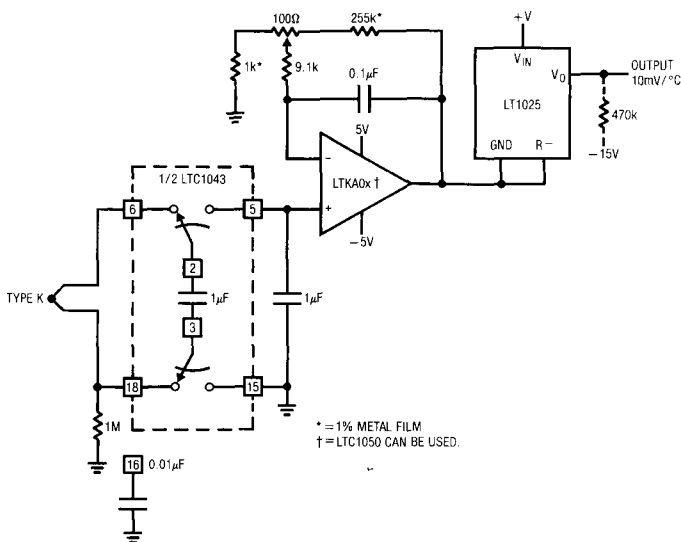


Figure 12A. Full Differential Input Thermocouple Amplifiers

transfer, and hence overall bandwidth. The differential inputs reject noise and common-mode voltages inside the LTC1043's supply rails. Excursions outside these limits require protection networks, as previously discussed. As in Figure 9, an optional resistor pull-down permits negative readings. The 1M resistor provides a bias path for the LTC1043's floating inputs. Figure 12B, for use with grounded thermocouples, subtracts sensor output from the LT1025.

Isolated Thermocouple Amplifiers

In many cases, protection networks and differential operation are inadequate. Some applications require continu-

ous operation at high common-mode voltages with severe noise problems. This is particularly true in industrial environments, where ground potential differences of 100V are common. Under these conditions the thermocouple and signal conditioning circuitry must be completely galvanically isolated from ground. This requires a fully isolated power source and an isolated signal transmission path to the ground referred output. Thermocouple work allows bandwidth to be traded for DC accuracy. With careful design, a single path can transfer floating power and isolated signals. The output may be either analog or digital, depending on requirements.

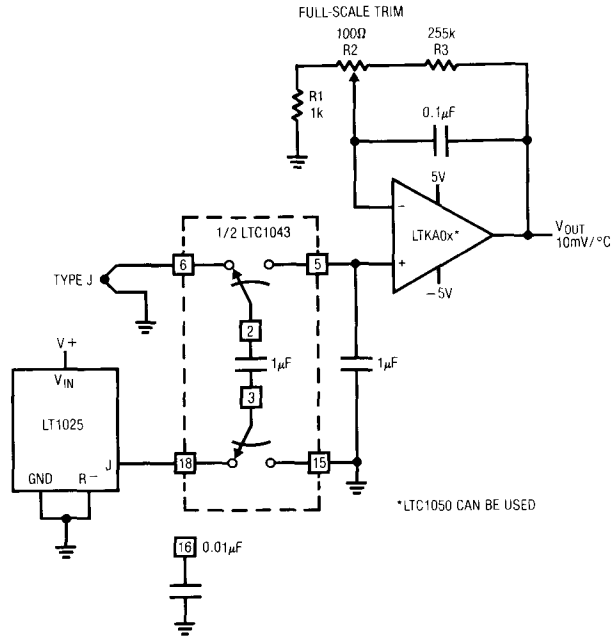


Figure 12B.

Figure 13 shows an isolated thermocouple signal conditioner which provides 0.25% accuracy at 175V common-mode. A single transformer transmits isolated power and data. 74C14 inverter I1 forms a clock (trace A, Figure 14). I2, I3 and associated components deliver a stretched pulse to the 2.2k resistor (trace B). The amplitude of this pulse is stabilized because A1's fixed output supplies 74C14 power. The resultant current through the 2.2k resistor drives L1's primary (trace E). A pulse appears at L1's secondary (trace F, Q2's emitter). A2 compares this amplitude with A5's signal conditioned thermocouple voltage. To close its loop, A2's output (trace G) drives Q2's base to force L1's secondary (pins 3-6) to clamp at A5's output value. Q2 operates in inverted mode, permitting clamping action even for very low A5 outputs. When L1's secondary (trace F) clamps, its primary (trace E) also clamps. After A2 settles, the clamp value is stable. This stable clamp value represents A5's thermocouple related information. Inverter I4 generates a clock delayed pulse (trace C) which is

fed to A3, a sample-and-hold amplifier. A3 samples L1's primary winding clamp value. A4 provides gain scaling and the LT1004 and associated components adjust offset. When the clock pulse (trace A) goes low, sampling ceases. When trace B's stretched clock pulse goes low, the I5-I6 inverter chain output (trace D) is forced low by the 470k-75pF differentiator's action. This turns on Q1, forcing substantial energy into L1's primary (trace E). L1's secondary (trace F) sees large magnetic flux. A2's output (trace G) moves as it attempts to maintain its loop. The energy is far too great, however, and A2 rails. The excess energy is dumped into the pin 1-4 winding, placing a large current pulse (trace H) into the 22μF capacitor. This current pulse occurs with each clock pulse, and the capacitor charges to a DC voltage, furnishing the circuit's isolated supply. When the 470k-75pF differentiator times out, the I5-I6 output goes high, shutting off Q1. At the next clock pulse the entire cycle repeats.

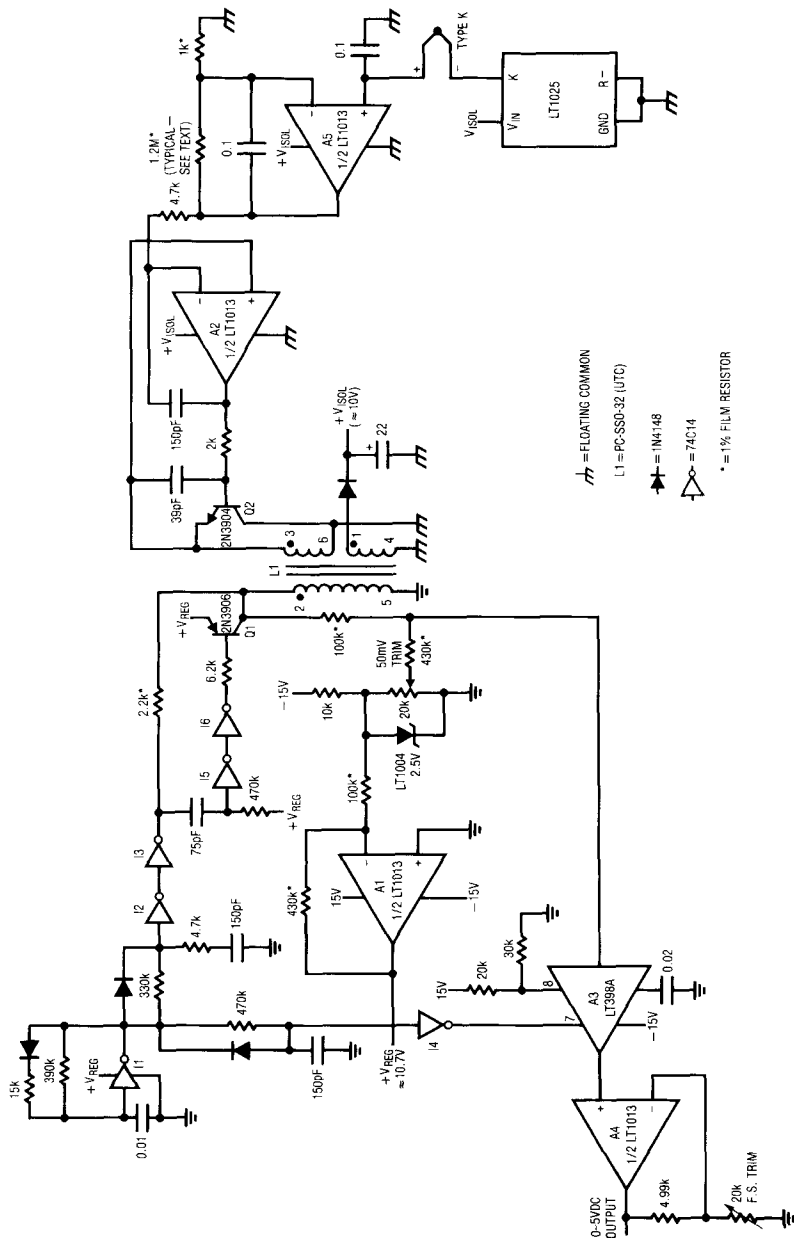


Figure 13. 0.25% Thermocouple Isolation Amplifier

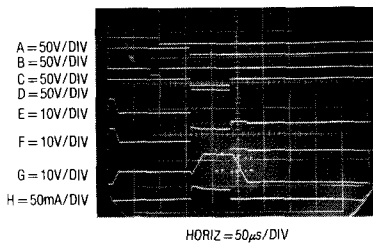


Figure 14. Waveforms for Figure 13's Thermocouple Isolation Amplifier

Proper operation of this circuit relies on several considerations. Achievable accuracy is primarily limited by transformer characteristics. Current during the clamp interval is kept extremely low relative to transformer core capacity. Additionally, the clamp period must also be short relative to core capacity. The clamping scheme relies on avoiding core saturation. This is why the power refresh pulse occurs immediately after data transfer, and not before. The transformer must completely reset before the next data transfer. A low clock frequency (350Hz) ensures adequate transformer reset time. This low clock frequency limits bandwidth, but the thermocouple data does not require any speed.

Gain slope is trimmed at A5, and will vary depending upon the desired maximum temperature and thermocouple type. The "50mV" trim should be adjusted with A5's output at 50mV. The circuit cannot read A5 outputs below 20mV (0.5% of scale) due to Q2's saturation limitations.

Drift is primarily due to the temperature dependence of L1's primary winding copper. This effect is swamped by the 2.2k series value with the 60ppm/°C residue partially compensated by I3's saturation resistance tempco. Overall tempco, including the LT1004, is about 100ppm/°C. Increased isolation voltages are possible with higher transformer breakdown ratings.

Figure 15's thermocouple isolation amplifier is somewhat more complex, but offers 0.01% accuracy and typical drift of 10ppm/°C. This level of performance is useful in servo systems or high resolution applications. As in Figure 13, a single transformer provides isolated data and power transfer. In this case the thermocouple information is width modulated across the transformer and then demodulated

back to DC. I1 generates a clock pulse (trace A, Figure 16). This pulse sets the 74C74 flip-flop (trace B) after a small delay generated by I2, I3 and associated components. Simultaneously, I4, I5 and Q1 drive L1's primary (trace C). This energy, received by L1's secondary (trace H), is stored in the 47µF capacitor and serves as the circuit's isolated supply. L1's secondary pulse also clocks a closed loop pulse width modulator composed of C1, C2, A3 and A4. A4's positive input receives A5's LT1025 based thermocouple signal. A4 servo-biases C2 to produce a pulse width each time C1 allows the 0.003µF capacitor (trace E) to receive charge via the 430kΩ resistor. C2's output width is inverted by I6 (trace F), integrated to DC by the 47k-0.68µF filter and fed back to A4's negative input. The 0.68µF capacitor compensates A4's feedback loop. A4 servo controls C2 to produce a pulse width that is a function of A5's thermocouple related output. I6's low loss MOS switching characteristics combined with A3's supply stabilization ensure precise control of pulse width by A4. Operating frequency, set by the I1 oscillator on L1's primary side, is normally a stability concern, but ratios out because it is common to the demodulation scheme, as will be shown.

I6's output width's (trace F) negative-going edge is differentiated and fed to I7. I7's output (trace G) drives Q3. Q3 puts a fast spike into L1's secondary (trace H). "Sing around" behavior by C1 is gated out by the diode at C2's positive input. Q3's spike is received at L1's primary, pins 7 and 3. Q2 serves as a clocked synchronous demodulator, pulling its collector low (trace D) only when its base is high and its emitter is low (e.g., when L1 is transferring data, not power). Q2's collector spike resets the 74C74 flip-flop. The MOS flip-flop is driven from a stable source (A1) and it is also clocked at the same frequency as the pulse width modulator. Because of this, the DC average of its Q output depends on A5's output. Variations with supply, temperature and I1 oscillator frequency have no effect. A2 and its associated components extract the DC average by simple filtering. The 100k potentiometer permits desired gain scaling. Because this scheme depends on edge timing at the flip-flop, the delay in resetting the 0.003µF capacitor causes a small offset error. This term is eliminated by matching this delay in the 74C74 "set" line with the previously mentioned I2-I3 delay network. This delay is set so that the rising edge of the flip-flop output (trace B)

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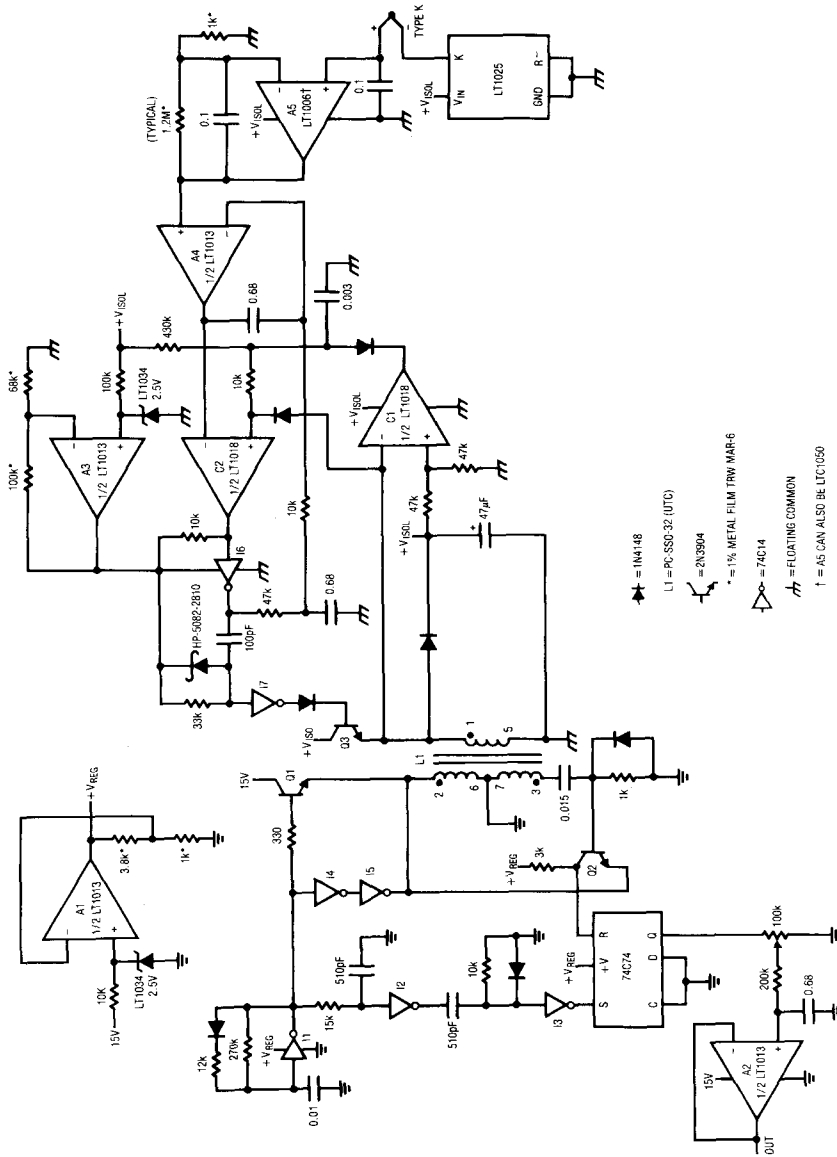


Figure 15. 0.01% Thermocouple Isolation Amplifier

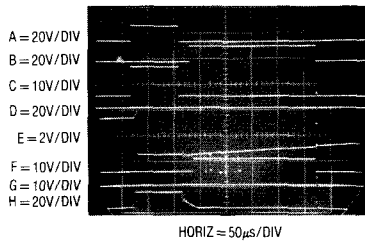


Figure 16. Pulse-Width-Modulation Based Thermocouple Isolation Amplifier Waveforms

corresponds to I6's rising edge. No such compensation is required for falling edge data because circuit elements in this path (I7, Q3, L1 and Q2) are wideband. With drift matched LT1034's and the specified resistors, overall drift is typically 10ppm/°C with 0.01% linearity.

Digital Output Thermocouple Isolator

Figure 17 shows another isolated thermocouple signal conditioner. This circuit has 0.25% accuracy and features a digital (pulse width) output. I1 produces a clock pulse (trace A, Figure 18). I2-I5 buffers this pulse and biases Q1 to drive L1. Concurrently, the 680pF-10k values provide a differentiated spike (trace B), setting the 74C74 flip-flop (trace C). L1's primary drive is received at the secondary.

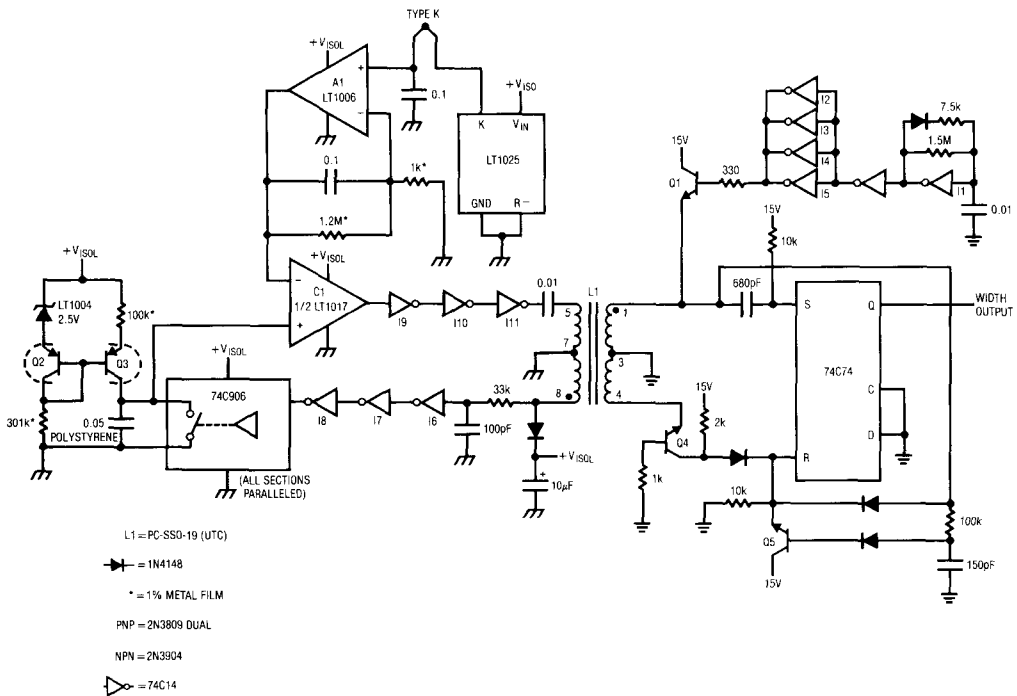


Figure 17. Digital Output Thermocouple Isolator

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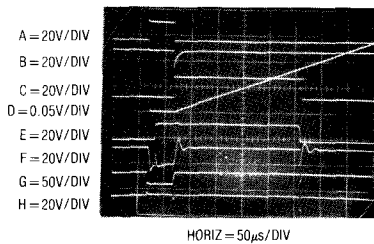


Figure 18. Waveforms for Digital-Output Thermocouple Isolator

The $10\mu\text{F}$ capacitor charges to DC, supplying isolated power. The pulse received at L1's secondary also resets the $0.05\mu\text{F}$ capacitor (trace D) via the inverters (I6, I7, I8) and the 74C906 open drain buffer. When the received pulse ends, the $0.05\mu\text{F}$ capacitor charges from the Q2-Q3 current source. When the resultant ramp crosses C1's threshold (A1's thermocouple related output voltage) C1 switches high, tripping the I9-I11 inverter chain. I11 (trace E) drives L1's secondary via the $0.01\mu\text{F}$ capacitor (trace F). The $33\text{k}-100\text{pF}$ filter prevents regenerative "sing around". The resultant negative-going spike at L1's primary biases Q4, causing its collector (trace G) to go low. Q4 and Q5 form a clocked synchronous demodulator which can pull the 74C74 reset pin low only when the clock is low. This condition occurs during data transfer, but not during power

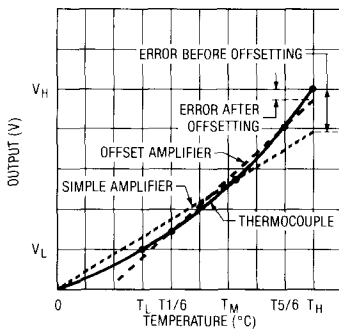


Figure 19. Offset Curve Fitting

transfer. The demodulated output (trace H) contains a single negative spike synchronous with C1's (e.g., I11's) output transition. This spike resets the flip-flop, providing the circuit output. The 74C74's width output thus varies with thermocouple temperature.

Linearization Techniques

It is often desirable to linearize a thermocouple based signal. Thermocouples' significant nonlinear response requires design effort to get good accuracy. Four techniques are useful. They include offset addition, breakpoints, analog computation, and digital correction. Offset addition schemes rely on biasing the nonlinear "bow" with a constant term. This results in the output being high at low scale and low at high scale with decreased errors between these extremes (Figure 19). This compromise reduces overall error. Typically, this approach is limited to slightly nonlinear behavior over wide ranges or larger non-linearity over narrow ranges.

Figure 20 shows a circuit utilizing offset linearization for a type S thermocouple. The LT1025 provides cold junction compensation and the LTC1052 chopper stabilized amplifier is used for low drift. The type S thermocouple output slope varies greatly with temperature. At 25°C it is

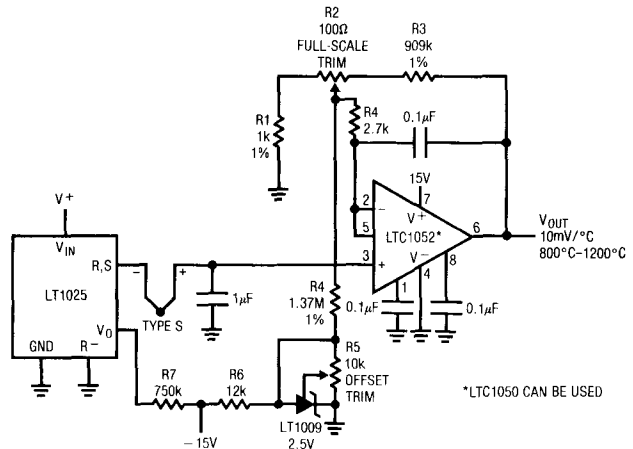


Figure 20. Offset Based Linearization

$6\mu\text{V}/^\circ\text{C}$, with an $11\mu\text{V}/^\circ\text{C}$ slope at 1000°C . This circuit gives 3°C accuracy over the indicated output range. The circuit, similar to Figure 10, is not particularly unusual except for the offset term derived from the LT1009 and applied through R4. To calibrate, trim R5 for $V_{\text{OUT}}=1.669$ at $V_{\text{IN}}=0.000\text{mV}$. Then, trim R2 for $V_{\text{OUT}}=9.998\text{V}$ at $T=1000^\circ\text{C}$ or for $V_{\text{IN}}(+\text{ input})=9.585\text{mV}$.

Figure 21, an adaption of a configuration shown by Sheingold (reference 3), uses breakpoints to change circuit gain as input varies. This method relies on scaling of the input and feedback resistors associated with A2-A6 and A7's reference output. Current summation at A8 is linear with the thermocouple's temperature. A3-A6 are the breakpoints, with the diodes providing switching when the respective summing point requires positive bias. As shown, typical accuracy of 1°C is possible over a 0°C - 650°C sensed range.

Figure 22, derived from Villanucci (reference 8), yields similar performance but uses continuous function analog computing to replace breakpoints, minimizing amplifiers and resistors. The AD538 combines with appropriate scaling to linearize response. The causality of this circuit is similar to Figure 22; the curve fit mechanism (breakpoint vs. continuous function) is the primary difference.

Digital techniques for thermocouple linearization have become quite popular. Figure 23, developed by Guy M. Hoover and William C. Rempfer, uses a microprocessor fed from a digitized thermocouple output to achieve linearization. The great advantage of digital techniques is elimination of trimming. In this scheme a large number of breakpoints are implemented in software.

The 10-bit LTC1091A A/D gives 0.5°C resolution over a 0°C to 500°C range. The LTC1052 amplifies and filters the thermocouple signal, the LT1025A provides cold junction compensation and the LT1019A provides an accurate reference. The J type thermocouple characteristic is linearized digitally inside the processor. Linear interpolation between known temperature points spaced 30°C apart introduces less than 0.1°C error. The 1024 steps provided by the LTC1091 (24 more than the required 1000) ensure 0.5°C resolution even with the thermocouple curvature.

Offset error is dominated by the LT1025 cold junction compensator which introduces 0.5°C maximum. Gain

error is 0.75°C max because of the 0.1% gain resistors and, to a lesser extent, the output voltage tolerance of the LT1019A and the gain error of the LTC1091A. It may be reduced by trimming the LT1019A or gain resistors. The LTC1091A keeps linearity better than 0.15°C . The LTC1052's $5\mu\text{V}$ offset contributes negligible error (0.1°C or less). Combined errors are typically inside 0.5°C . These errors don't include the thermocouple itself. In practice, connection and wire errors of 0.5°C to 1°C are not uncommon. With care, these errors can be kept below 0.5°C .

The 20k-10k divider on CH1 of the LTC1091 provides low supply voltage detection (the LT1019A reference requires a minimum supply of 6.5V to maintain accuracy). Remote location is possible with data transferred from the MCU to the LTC1091 via the 3-wire serial port.

Figure 24 is a complete software listing* of the code required for the 68HC05 processor. Preparing the circuit involves loading the software and applying power. No trimming is required.

*Including of a software based circuit was not without attendant conscience searching and pain on the author's part. Hopefully, the Analog Faithful will tolerate this transgression . . . I'm sorry everybody, it just works too well!

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2. Williams, J., "Designer's Guide to Temperature Sensors", EDN, May 5, 1977.
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4. "Omega Temperature Measurement Handbook", Omega Engineering, Stamford Connecticut.
5. "Practical Temperature Measurements", Hewlett-Packard Applications Note #290, Hewlett-Packard.
6. Thermocouple Reference Tables, NBS Monograph 125, National Bureau of Standards.
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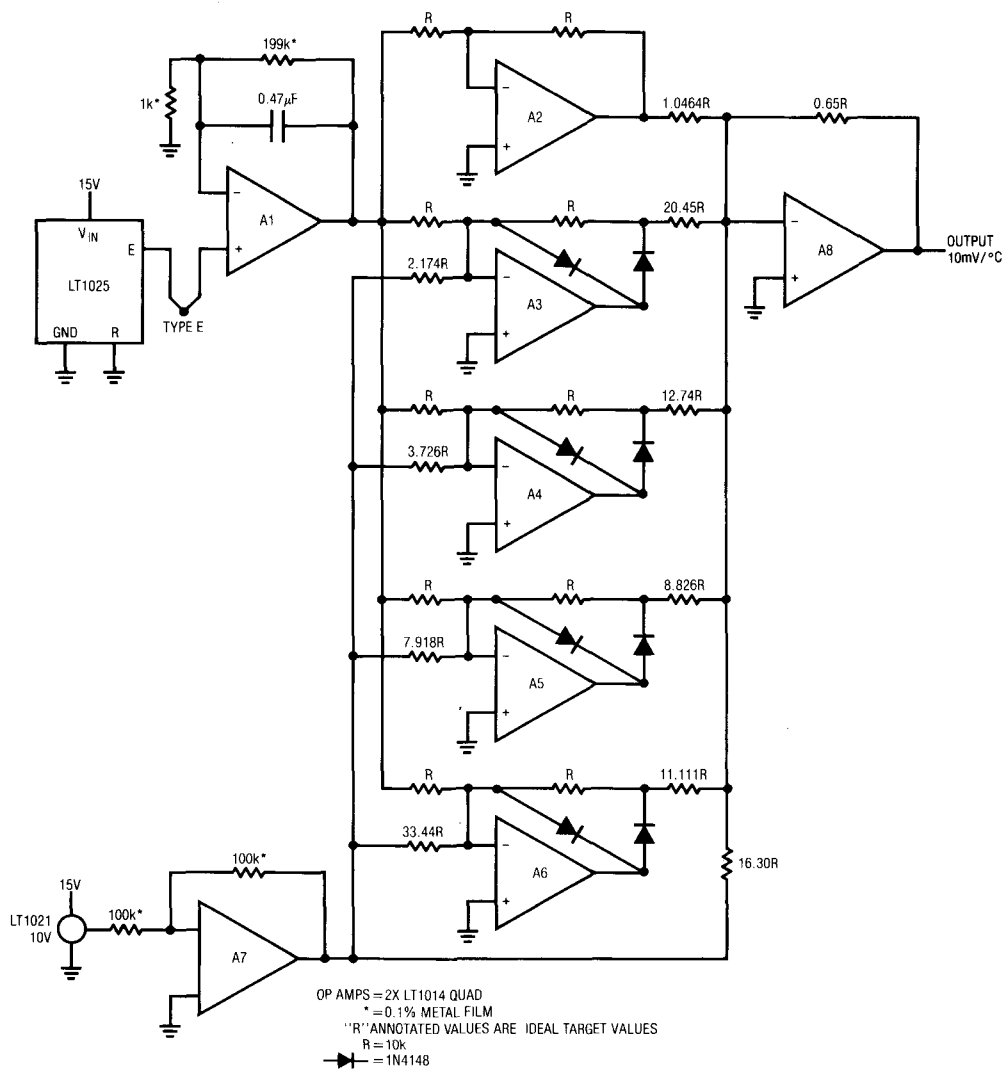


Figure 21. Breakpoint Based Linearization (see Reference 3)

THERMO-COUPLE TYPE	SEEBECK COEFFICIENT ($\mu\text{V}/^\circ\text{C}$)	IC1 PIN
E	60.9	1
J	51.7	8
K, T	40.6	7
R, S	5.95	6

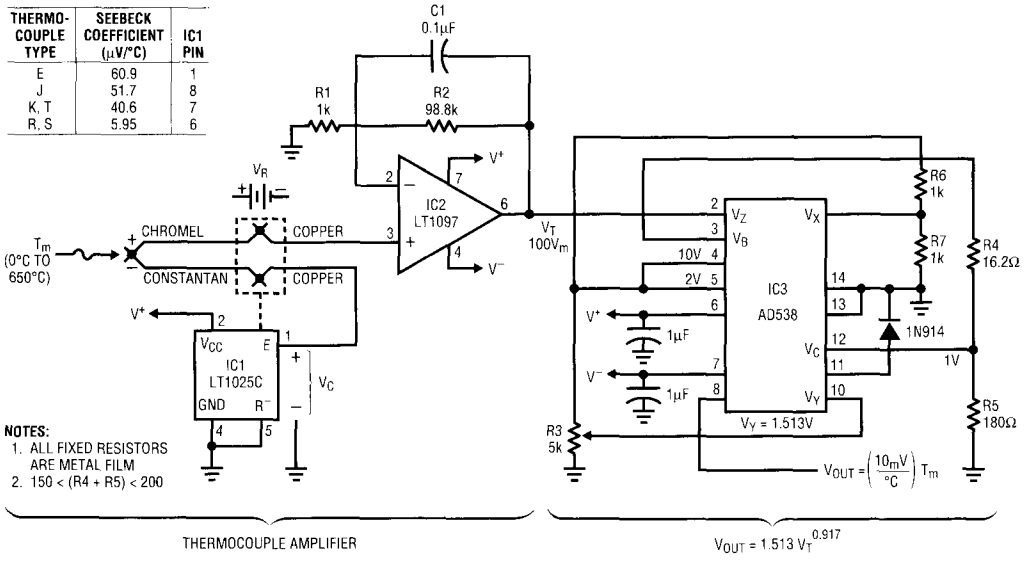


Figure 22. Continuous Function Linearization (see Reference 8)

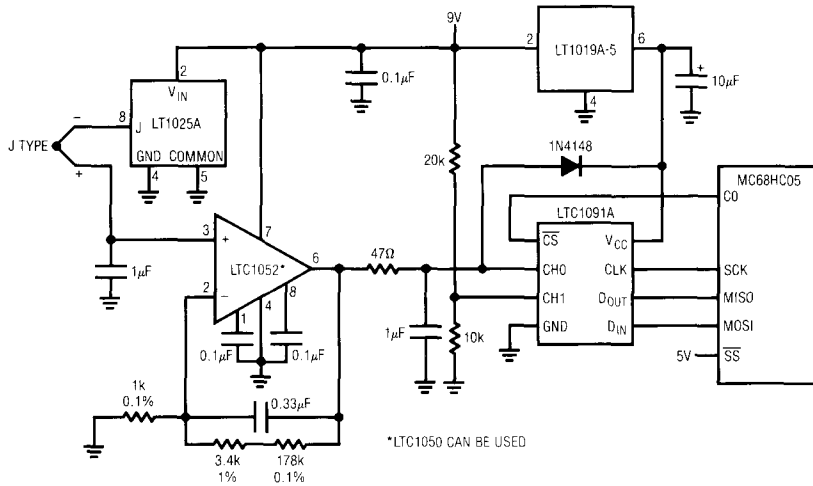


Figure 23. Processor Based Linearization

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*      TYPE J THERMOCOUPLE LINEARIZATION PROGRAM
*      WRITTEN BY GUY HOOVER LINEAR TECHNOLOGY CORPORATION
*      REV 1 10/4/87
*      N IS NUMBER OF SEGMENTS THAT THERMOCOUPLE RESPONSE IS DIVIDED INTO
*      TEMPERATURE (°C) = M * X + B
*      M IS SLOPE OF THERMOCOUPLE RESPONSE FOR A GIVEN SEGMENT
*      X IS A/D OUTPUT — SEGMENT END POINT
*      B IS SEGMENT START POINT IN DEGREES (°C * 2)

ORG      $1000
FDB      $00,$39,$74,$B0,$EE,$12B,$193,$262,$330,$397      TABLE FOR X
ORG      $1020
FDB      $85DD,$823A,$7FB4,$7DD4,$7CAF,$7BC3,$7B8A,$7C24,$7C1F,$7B3A      TABLE FOR M
ORG      $1040
FDB      $00,$3C,$78,$B4,$F0,$12C,$190,$258,$320,$384      TABLE FOR B
ORG      $10FF
FCB      $13      N * 2
ORG      $0100
OPT      ]
STA      $0A      LOAD CONFIGURATION DATA INTO $0A
LDA      #$00      CONFIGURATION DATA FOR PORT A DDR
STA      $04      LOAD CONFIGURATION DATA INTO PORT A
LDA      #$FF      CONFIGURATION DATA FOR PORT B DDR
STA      $05      LOAD CONFIGURATION DATA INTO PORT B
LDA      #$F7      CONFIGURATION DATA FOR PORT C DDR
STA      $06      LOAD CONFIGURATION DATA INTO PORT C
JSR      HOUSEKP INITIALIZE ASSORTED REGISTERS

MES92L   NOP
JSR      CHECK
LDA      #$6F      DIN WORD FOR LTC1091 CH0, W/RESPECT TO GND, MSB FIRST
STA      $50      STORE IN DIN BUFFER
JSR      READ91    READ LTC1091

LINEAR   LDX      $10FF    LOAD SEGMENT COUNTER INTO X
DOAGAIN  LDA      $1000,X  LOAD LSBs OF SEGMENT N
          STA      $55      STORE LSBs IN $55
          DECX      DECREMENT X
          LDA      $1000,X  LOAD MSBs OF SEGMENT N
          STA      $54      STORE MSBs IN $54
          JSR      SUBTRCT  SEGMENT
          BPL      ADDB
          JSR      DECBX    DECREMENT X

SEGMENT  JMP      DOAGAIN
          LDA      $1020,X  LOAD MSBs OF SLOPE
          STA      $54      STORE MSBs IN $54
          INCX      INCREMENT X
          LDA      $1020,X  LOAD LSBs OF SLOPE
          STA      $55      STORE LSBs IN $55
          JSR      TBMULT  RETURNS RESULT IN $61 AND $62
          LDA      $1040,X  LOAD LSBs OF BASE TEMP
          STA      $55      STORE LSBs IN $55
          DECX      DECREMENT X
          LDA      $1040,X  LOAD MSBs OF BASE TEMP
          STA      $54
          JSR      ADDB

CHECK    LDA      #$7F      DIN WORD FOR CH1
          STA      $50      LOAD DIN WORD INTO $50
          JSR      READ91    READ BATTERY VOLTAGE
          LDA      #$02      LOAD MSB OF MIN BATT VOLTAGE
          STA      $54      PUT IN MSB OF SUBTRACT BUFFER
          LDA      #$CC      LOAD LSB OF MIN BATT VOLTAGE
          STA      $55      PUT IN LSB OF SUBTRACT BUFFER
          JSR      SUBTRCT  COMPARE BATT VOLTAGE WITH MINIMUM
          BPL      NOPROB  IF BATT OK GOTO NOPROB

```

Figure 24. Code for Processor Based Linearization

	JSR	ADDB	
	LDA	#S01	
	STA	\$56	SET BATTERY LOW FLAG
	RTS		
NOPROB	JSR	ADDB	
	CLR	\$56	CLEAR LOW BATTERY FLAG
	RTS		
READ91	LDA	#S50	CONFIGURATION DATA FOR SPCR
	STA	\$0A	LOAD CONFIGURATION DATA
	LDA	\$50	
	BCLR	2,\$02	BIT 0 PORT C GOES LOW (\overline{CS} GOES LOW)
	STA	\$0C	LOAD D_{IN} INTO SP1 DATA REG. START TRANSFER.
BACK91	TST	\$0B	TEST STATUS OF SPIF
	BPL	BACK91	LOOP TO PREVIOUS INSTRUCTION IF NOT DONE
	LDA	\$0C	LOAD CONTENTS OF SPI DATA REG. INTO ACC
	STA	\$0C	START NEXT CYCLE
	AND	#S03	CLEAR 6 MSBs OF FIRST D_{OUT}
	STA	\$61	STORE MSBs IN \$61
BACK92	TST	\$0B	TEST STATUS OF SPIF
	BPL	BACK92	LOOP TO PREVIOUS INSTRUCTION IF NOT DONE
	BSET	2,\$02	SET BIT 0 PORT C (\overline{CS} GOES HIGH)
	LDA	\$0C	LOAD CONTENTS OF SPI DATA INTO ACC
	STA	\$62	STORE LSBs IN \$62
	RTS		
SUBTRCT	LDA	\$62	LOAD LSBs
	SUB	\$55	SUBTRACT LSBs
	STA	\$62	STORE REMAINDER
	LDA	\$61	LOAD MSBs
	SBC	\$54	SUBTRACT W/CARRY MSBs
	STA	\$61	STORE REMAINDER
	RTS		
ADDB	LDA	\$62	LOAD LSBs
	ADD	\$55	ADD LSBs
	STA	\$62	STORE SUM
	LDA	\$61	LOAD MSBs
	ADC	\$54	ADD W/CARRY MSBs
	STA	\$61	STORE SUM
	RTS		
TBMULT	CLR	\$68	
	CLR	\$69	
	CLR	\$6A	
	CLR	\$6B	
	STX	\$58	STORE CONTENTS OF X IN \$58
	LSL	\$62	MULTIPLY LSBs BY 2
	ROL	\$61	MULTIPLY MSBs BY 2
	LDA	\$62	LOAD LSBs OF LTC1091 INTO ACC
	LDX	\$55	LOAD LSBs OF M INTO X
	MUL		MULTIPLY LSBs
	STA	\$6B	STORE LSBs IN \$6B
	STX	\$6A	STORE IN \$6A
	LDA	\$62	LOAD LSBs OF LTC1091 INTO ACC
	LDX	\$54	LOAD MSBs OF M INTO X
	MUL		
	ADD	\$6A	ADD NEXT BYTE
	STA	\$6A	STORE BYTE
	TXA		TRANSFER X TO ACC
	ADC	\$69	ADD NEXT BYTE
	STA	\$69	STORE BYTE
	LDA	\$61	LOAD MSBs OF LTC1091 INTO ACC
	LDX	\$55	LOAD LSBs OF M INTO X

Figure 24. Code for Processor Based Linearization (Continued)

	MUL		
	ADD	\$6A	ADD NEXT BYTE
	STA	\$6A	STORE BYTE
	TXA		TRANSFER X TO ACC
	ADC	\$69	ADD NEXT BYTE
	STA	\$69	STORE BYTE
	LDA	\$61	LOAD MSBs OF LTC1091 INTO ACC
	LDX	\$54	LOAD MSBs OF M INTO X
	MUL		
	ADD	\$69	ADD NEXT BYTE
	STA	\$69	STORE BYTE
	TXA		TRANSFER X TO ACC
	ADC	\$68	ADD NEXT BYTE
	STA	\$68	STORE BYTE
	LDA	\$6A	LOAD CONTENTS OF \$6A INTO ACC
	BPL	NNN	
	LDA	\$69	LOAD CONTENTS OF \$69 INTO ACC
	ADD	#\$01	ADD 1 TO ACC
	STA	\$69	STORE IN \$69
	LDA	\$68	LOAD CONTENTS OF \$68 INTO ACC
	ADC	#\$00	FLOW THROUGH CARRY
	STA	\$68	STORE IN \$68
NNN	LDA	\$68	LOAD CONTENTS OF \$68 INTO ACC
	STA	\$61	STORE MSBs IN \$61
	LDA	\$69	LOAD CONTENTS OF \$69 INTO ACC
	STA	\$62	STORE IN \$62
	LDX	\$58	RESTORE X REGISTER
	RTS		RETURN
HOUSEKP	BSET	0,\$02	SET B0 PORT C
	BSET	2,\$02	SET B2 PORT C
	RTS		

Figure 24. Code for Processor Based Linearization (Continued)

APPENDIX A

Error Sources in Thermocouple Systems

Obtaining good accuracy in thermocouple systems mandates care. The small thermocouple signal voltages require careful consideration to avoid error terms when signal processing. In general, thermocouple *system* accuracy better than 0.5°C is difficult to achieve. Major error sources include connection wires, cold junction uncertainties, amplifier error and sensor placement.

Connecting wires between the thermocouple and conditioning circuitry introduce undesired junctions. These junctions form unintended thermocouples. The number of junctions and their effects should be minimized, and kept isothermal. A variety of connecting wires and accessories are available from manufacturers and their literature should be consulted (reference 4).

Thermocouple voltages are generated whenever dissimilar materials are joined. This includes the leads of IC packages, which may be kovar in TO-5 cans, alloy 42 or copper in dual-in-line packages, and a variety of other materials in plating finishes and solders. The net effect of these thermocouples is "zero" if all are at exactly the same temperature, but temperature gradients exist within IC packages and across PC boards whenever power is dissipated. For this reason, extreme care must be used to ensure that no temperature gradients exist in the vicinity of the thermocouple terminations, the cold junction compensator (e.g., LT1025) or the thermocouple amplifier. If a gradient cannot be eliminated, leads should be positioned isothermally, especially the LT1025 R⁻ and appropriate output pins, the amplifier input pins, and the gain setting resistor

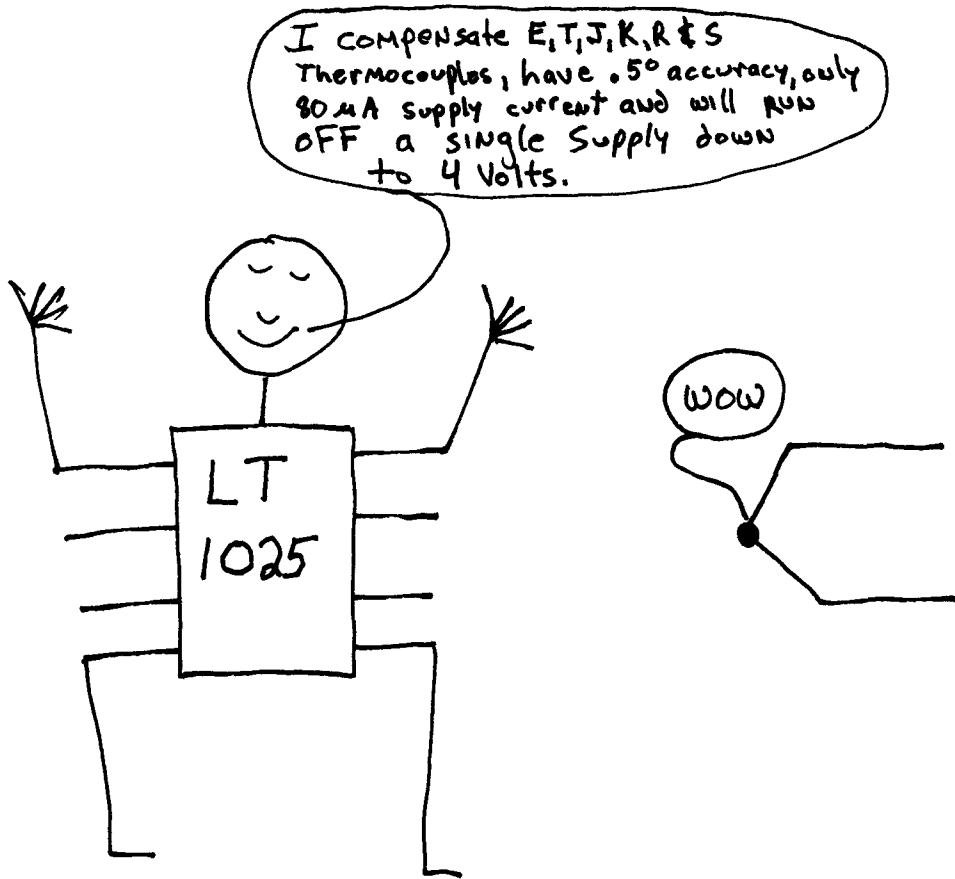
leads. An effect to watch for is amplifier offset voltage warm-up drift caused by mismatched thermocouple materials in the wire-bond/lead system of the IC package. This effect can be as high as tens of microvolts in TO-5 cans with kovar leads. It has nothing to do with the actual offset drift specification of the amplifier and can occur in amplifiers with measured "zero" drift. Warm-up drift is directly proportional to amplifier power dissipation. It can be minimized by avoiding TO-5 cans, using low supply current amplifiers, and by using the lowest possible supply voltages. Finally, it can be accommodated by calibrating and specifying the system after a five minute warm-up period.

A significant error source is the cold junction. The error takes two forms. The subtractive voltage produced by the cold junction must be correct. In a true cold junction (e.g., ice point reference) this voltage will vary with inability to maintain the desired temperature, introducing error. In a cold junction compensator like the LT1025, error occurs with inability to sense and track ambient temperature. Minimizing sensing error is the manufacturer's responsibility (we do our best!), but tracking requires user care. Every effort should be made to keep the LT1025 isothermal with the cold junction. Thermal shrouds, high thermal capacity blocks and other methods are commonly employed to ensure that the cold junction and the compensator are at the same temperature.

Amplifier offset uncertainties and, to a lesser degree, bias currents and open loop gain should be considered. Amplifier selection criteria is discussed in the text under "Amplifier Selection."

A final source of error is thermocouple placement. Remember that the thermocouple measures its own temperature. In flowing or fluid systems, remarkably large errors can be generated due to effects of laminar flow or eddy currents around the thermocouple. Even a "simple" surface measurement can be wildly inaccurate due to thermal conductivity problems. Silicone thermal grease can reduce this, but attention to sensor mounting is usually required. As much of the sensor surface as possible should be mated to the measured surface. Ideally, the sensor should be tightly mounted in a drilled recess in the surface. Keep in mind that the thermocouple leads act as heat pipes, providing a direct thermal path to the sensor. With high thermal capacity surfaces this may not be a problem, but other situations may require some thought. Often, thermally mating the lead wire to the surface or coiling the wire in the environment of interest will minimize heat piping effects.

As a general rule, skepticism is warranted, even in the most "obviously simple" situations. Experiment with several sensor positions and mounting options. If measured results agree, you're probably on the right track. If not, re-think and try again.



Waller
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Some Thoughts on DC-DC Converters

Jim Williams
Brian Huffman

INTRODUCTION

Many systems require that the primary source of DC power be converted to other voltages. Battery driven circuitry is an obvious candidate. The 6V or 12V cell in a laptop computer must be converted to different potentials needed for memory, disc drives, display and operating logic. In theory, AC line powered systems should not need DC-DC converters because the implied power transformer can be equipped with multiple secondaries. In practice, economics, noise requirements, supply bus distribution problems and other constraints often make DC-DC conversion preferable. A common example is logic dominated, 5V powered systems utilizing $\pm 15V$ driven analog components.

The range of applications for DC-DC converters is large, with many variations. Interest in converters is commensurately quite high. Increased use of single supply powered systems, stiffening performance requirements and battery operation have increased converter usage.

Historically, efficiency and size have received heavy emphasis. In fact, these parameters can be significant, but often are of secondary importance. A possible reason behind the continued and overwhelming attention to size and efficiency in converters proves surprising. Simply put, these parameters are (within limits) *relatively easy to achieve!* Size and efficiency advantages have their place, but other system-oriented problems also need treatment. Low quiescent current, wide ranges of allowable inputs, substantial reductions in wideband output noise and cost effectiveness are important issues. One very important

converter class, the 5V to $\pm 15V$ type, stresses size and efficiency with little emphasis towards parameters such as output noise. This is particularly significant because wideband output noise is a frequently encountered problem with this type of converter. In the best case, the output noise mandates careful board layout and grounding schemes. In the worst case, the noise precludes analog circuitry from achieving desired performance levels (for further discussion see Appendix A, "The 5V to $\pm 15V$ Converter — A Special Case"). The 5V to $\pm 15V$ DC-DC conversion requirement is ubiquitous, and presents a good starting point for a study of DC-DC converters.

5V TO $\pm 15V$ CONVERTER CIRCUITS

Low Noise 5V to $\pm 15V$ Converter

Figure 1's design supplies a $\pm 15V$ output from a 5V input. Wideband output noise measures 200 microvolts peak-to-peak, a 100x reduction over typical designs. Efficiency at 250mA output is 60%, about 5-10% lower than conventional types. The circuit achieves its low noise performance by minimizing high speed harmonic content in the power switching stage. This forces the efficiency trade-off noted, but the penalty is small compared to the benefit.

The 74C14 based 30kHz oscillator is divided into a 15kHz two phase clock by the 74C74 flip flop. The 74C02 gates and 10K-0.001 μ F delays condition this two phase clock

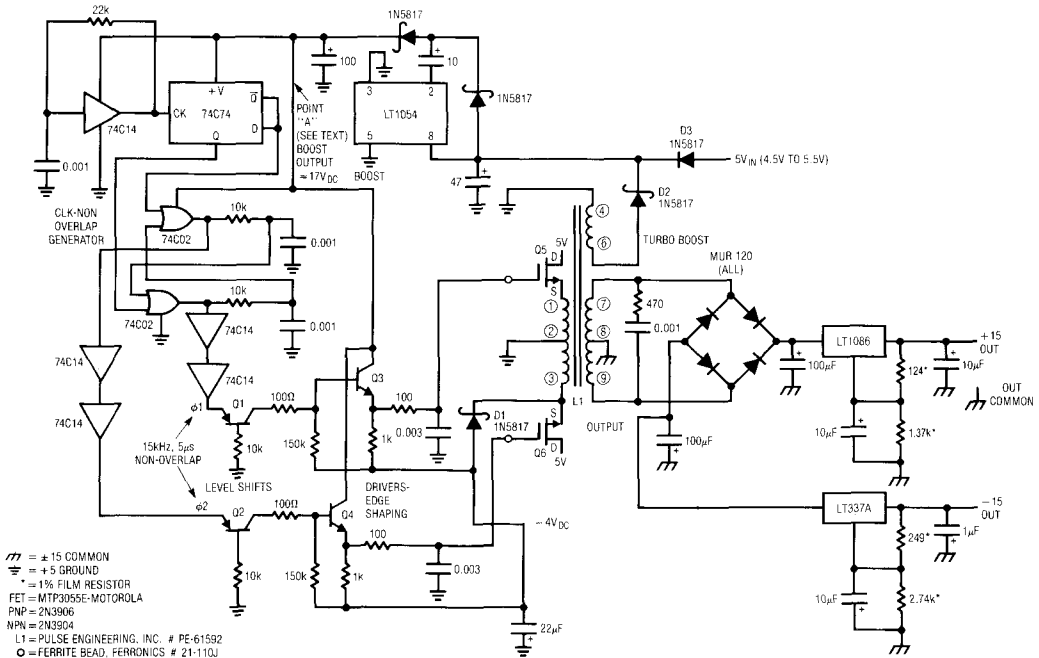


Figure 1. Low Noise 5V to ±15V Converter

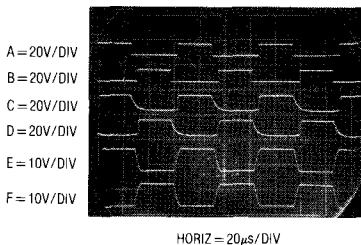


Figure 2. 5V to ±15V Low Noise Converter Waveforms

into non-overlapping, two phase drive at the emitters of Q1 and Q2 (Figure 2, traces A and B, respectively). These transistors provide level shifting to drive emitter followers Q3-Q4. The Q3-Q4 emitters see 100Ω-0.003μF filters, slowing drive to output MOSFET's Q5-Q6. The filter's effects appear at the gates of Q5 and Q6 (traces C and D, respectively). Q5 and Q6 are source followers, instead of the conventional common source connection. This limits transformer rise time to the gate terminals filtered slew rate, resulting in well controlled waveforms at the sources

of Q5 and Q6 (traces E and F, respectively). L1 sees complimentary, slew limited drive, eliminating the high speed harmonics normally associated with this type converter. L1's output is rectified, filtered and regulated to obtain the final output. The 470Ω-0.001μF damper in L1's output maintains loading during switching, aiding low noise performance. The ferrite beads in the gate leads eliminate parasitic RF oscillations associated with follower configurations.

The source follower configuration eases controlling L1's edge risetimes, but complicates gate biasing. Special provisions are required to get the MOSFET's fully turned on and off. Source follower connected Q5 and Q6 require voltage overdrive at the gates to saturate. The 5V primary supply cannot provide the specified 10V gate — channel bias required for saturation. Similarly, the gates must be pulled well below ground to turn the MOSFETs off. This is so because L1's behavior pulls the sources negative when the devices turn off. Turn-off bias is bootstrapped from the negative side of Q6's source waveform. D1 and the 22μF

capacitor produce a -4V potential for Q3 and Q4 to pull down to. Turn-on bias is generated by a two stage boost loop. The 5V supply is fed via D3 to the LT1054 switched capacitor voltage converter (switched capacitor voltage converters are discussed in Appendix B, "Switched Capacitor Voltage Converters — How They Work"). The LT1054 configuration, set up as a voltage doubler, initially provides about 9V boost to point "A" at turn-on. When the converter starts running L1 produces output ("Turbo Boost" on schematic) at windings 4-6 which is rectified by D2, raising the LT1054's input voltage. This further raises point "A" to the 17V potential noted on the schematic.

These internally generated voltages allow Q5 and Q6 to receive proper drive, minimizing losses despite their source follower connection. Figure 3, an AC coupled trace of the 15V converter output, shows $200\mu\text{V}_{\text{p-p}}$ noise at full power (250mA output). The -15V output shows nearly identical characteristics. Switching artifacts are comparable in amplitude to the linear regulators noise. Further reduction in switching based noise is possible by slowing Q5 and Q6 risetimes. This, however, necessitates reducing clock rate and increasing non-overlap time to maintain available output power and efficiency. The arrangement shown represents a favorable compromise between output noise, available output power, and efficiency.

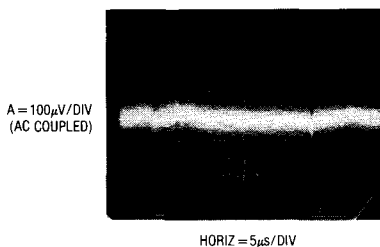


Figure 3. Output Noise of the Low Noise 5V to $\pm 15\text{V}$ Converter

Ultra-Low Noise 5V to $\pm 15\text{V}$ Converter

Residual switching components and regulator noise set Figure 1's performance limits. Analog circuitry operating at the very highest levels of resolution and sensitivity may require the lowest possible converter noise. Figure 4's converter uses sine wave transformer drive to reduce harmonics to negligible levels. The sine wave transformer drive combines with special output regulators to produce

less than $30\mu\text{V}$ of output noise. This is almost $7\times$ lower than the previous circuit and approaches a $1000\times$ improvement over conventional designs. The trade off is efficiency and complexity.

A1 is set up as a 16kHz Wien bridge oscillator. The single power supply requires biasing to prevent A1's output from saturating at the ground rail. This bias is established by returning the undriven end of the Wien network to a DC potential derived from the LT1009 reference. A1's output is a pure sine wave (Figure 5, trace A) biased off ground. A1's gain must be controlled to maintain sine wave output. A2 does this by comparing A1's rectified and filtered positive output peaks with an LT1009 derived DC reference. A2's output, biasing Q1, servo control A1's gain. The $0.22\mu\text{F}$ capacitor frequency compensates the loop, and the thermally mated diodes minimize errors due to rectifier temperature drift. These provisions fix A1's AC and DC output terms against supply and temperature changes.

A1's output is AC coupled to A3. The $2\text{k} - 820\Omega$ divider re-biases the sine wave, centering it inside A3's input common mode range even with supply shifts. A3 drives a power stage, Q2-Q5. The stages common emitter outputs and biasing permit 1V_{RMS} ($3\text{V}_{\text{p-p}}$) transformer drive, even at $V_{\text{supply}} = 4.5\text{V}$. At full converter output loading the stage delivers 3 ampere peaks but the waveform is clean (trace B), with low distortion (trace C). The $330\mu\text{F}$ coupling capacitor strips DC and L3 sees pure AC. Feedback to A3 is taken at the Q4-Q5 collectors. The $0.1\mu\text{F}$ unit at this point suppresses local oscillations. L3's secondary RC network adds additional high frequency damping.

Without control of quiescent current the power stage will encounter thermal runaway and destroy itself. A4 measures DC output current across Q5's emitter resistor and servo controls Q6 to fix quiescent current. A divided portion of the LT1009 reference sets the servo point at A4's negative input and the $0.33\mu\text{F}$ feedback capacitor stabilizes the loop.

L3's rectified and filtered outputs are applied to regulators designed for low noise. A5 and A7 amplify the LT1021's filtered 10V output up to 15V. A6 and A8 provide the -15V output. The LT1021 and amplifiers give better noise performance than three terminal regulators. The zener-resistor network clips overvoltages due to start-up transients.

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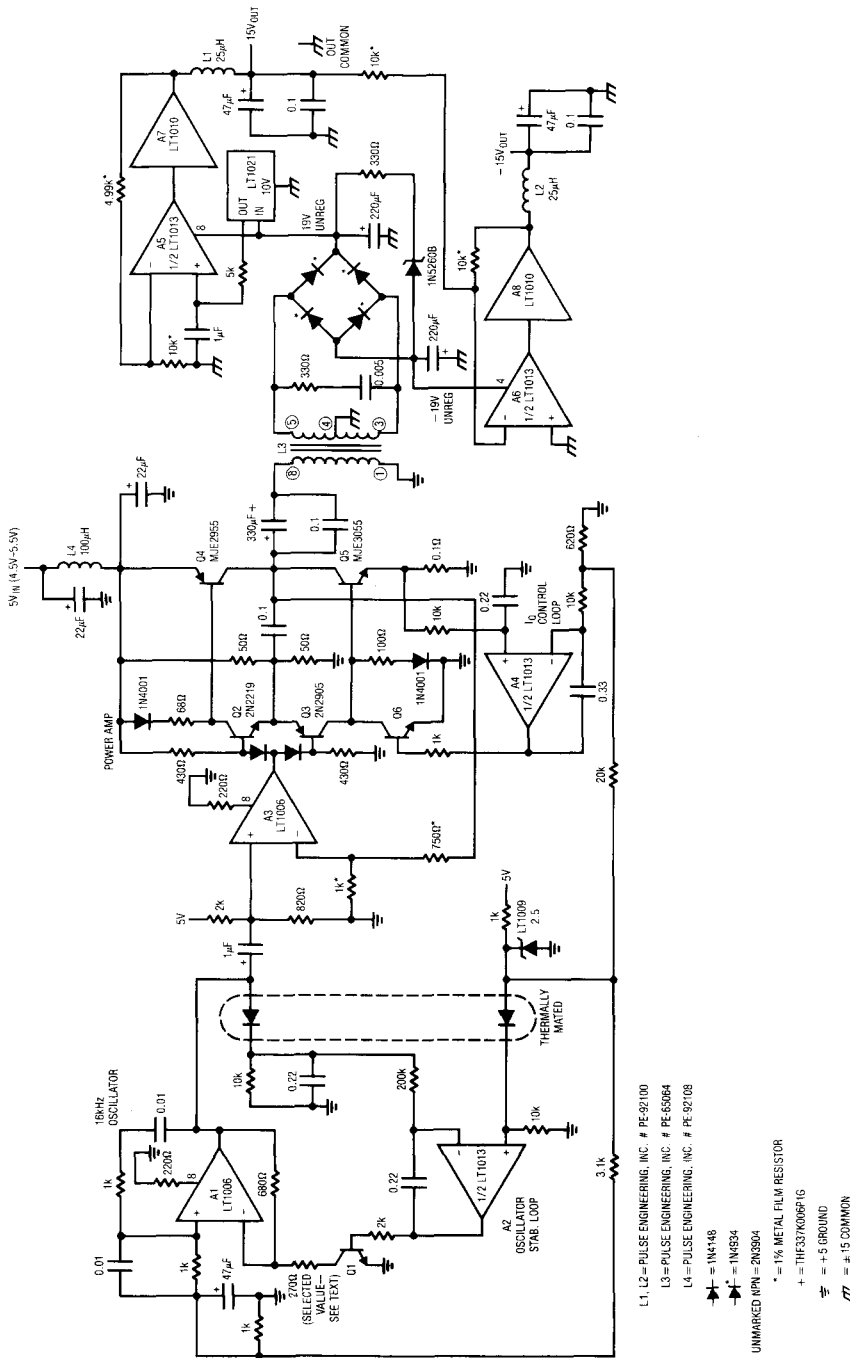


Figure 4. Ultra Low Noise Sine Wave Drive 5V to ±15V Converter

L1, L2 = PULSE ENGINEERING, INC. # PE-92100

L3 = PULSE ENGINEERING, INC. # PE-55664

L4 = PULSE ENGINEERING, INC. # PE-92108

◆ = 1N4148

◆ = 1N4534

UNMARKED NPW = 2W3804

* = 1% METAL FILM RESISTOR

+ = THF337K06P15

⊕ = +5 GROUND

⊖ = +15 COMMON

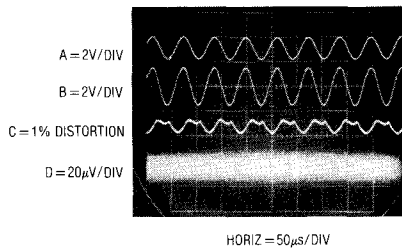


Figure 5. Waveforms for the Sine Wave Driven Converter.
Note that Output Noise (Trace D) is Only $30\mu\text{Vp-p}$.

L1 and L2 combine with their respective output capacitors to aid low noise characteristics. These inductors are outside the feedback loop, but their low copper resistance does not significantly degrade regulation. Trace D, the 15V output at full load, shows less than $30\mu\text{V}$ (2ppm) of noise. The most significant trade-off in this design is efficiency. The sine wave transformer drive forces substantial power loss. At full output (75mA), efficiency is only 30%.

Before use, the circuit should be trimmed for lowest distortion (typically 1%) in the sine wave delivered to L3. This trim is made by selecting the indicated value at A1's negative input. The 270Ω value shown is nominal, with a typical variance of $\pm 25\%$. The sine wave's 16kHz frequency is a compromise between the op amps available gain-bandwidth, magnetics size, audible noise, and minimization of wideband harmonics.

Single Inductor 5V to $\pm 15\text{V}$ Converter

Simplicity and economy are another dimension in 5V to $\pm 15\text{V}$ conversion. The transformer in these converters is usually the most expensive component. Figure 6's unusual drive scheme allows a single, two terminal inductor to replace the usual transformer at significant cost savings. Trade-offs include loss of galvanic isolation between input and output and lower power output. Additionally, the regulation technique employed causes about 50mV of clock related output ripple.

The circuit functions by periodically and alternately allowing each end of the inductor to flyback. The resultant positive and negative peaks are rectified and filtered. Regulation is obtained by controlling the number of flyback events during the respective output's flyback interval.

The leftmost logic inverter produces a 20kHz clock (trace A, Figure 7) which feeds a logic network composed of additional inverters, diodes and the 74C90 decade counter. The counter output (trace B) combines with the logic network to present alternately phased clock bursts (traces C and D) to the base resistors of Q1 and Q2. When $\phi 1$ (trace B) is unclocked it resides in its high state, biasing Q2 and Q4 on. Q4's collector effectively grounds the "bottom" of L1 (trace H). During this interval $\phi 2$ (trace A) puts clock bursts into Q1's base resistor. If the -15V output is too low servo comparator C1A's output (trace E) is high, and Q1's base can receive pulsed bias. If the converse is true the comparator will be low, and the bias gated away via Q1's base diode. When Q1 is able to bias, Q3 switches, resulting in negative going flyback events at the "top" of L1 (trace G). These events are rectified and filtered to produce the -15V output. C1A regulates by controlling the number of clock pulses that switch the Q1-Q3 pair. The LT1004 serves as a reference. Trace J, the AC coupled -15V output, shows the effect of C1A's regulating action. The output stays within a small error window set by C1A's switched control loop. As input voltage and loading conditions change C1A adjusts the number of clock pulses allowed to bias Q1-Q3, maintaining loop control.

When the $\phi 1$ and $\phi 2$ signals reverse state the operating sequence reverses. Q3's collector (trace G) is pulled high with Q2-Q4 switching controlled by C1B's servo action. Operating waveforms are similar to the previous case. Trace F is C1B's output, trace H is Q4's collector (L1's "bottom") and trace I is the AC coupled 15V output. Although the two regulating loops share the same inductor they operate independently, and asymmetrical output loading is not deleterious. The inductor sees irregularly spaced shots of current (trace K), but is unaffected by its multiplexed operation. Clamp diodes prevent reverse biasing of Q3 and Q4 during transient conditions. The circuit provides $\pm 25\text{mA}$ of regulated power at 60% efficiency.

Low Quiescent Current 5V to $\pm 15\text{V}$ Converter

A final area in 5V to $\pm 15\text{V}$ converter design is reduction of quiescent current. Typical units pull 100-150mA of quiescent current, unacceptable in many low power systems.

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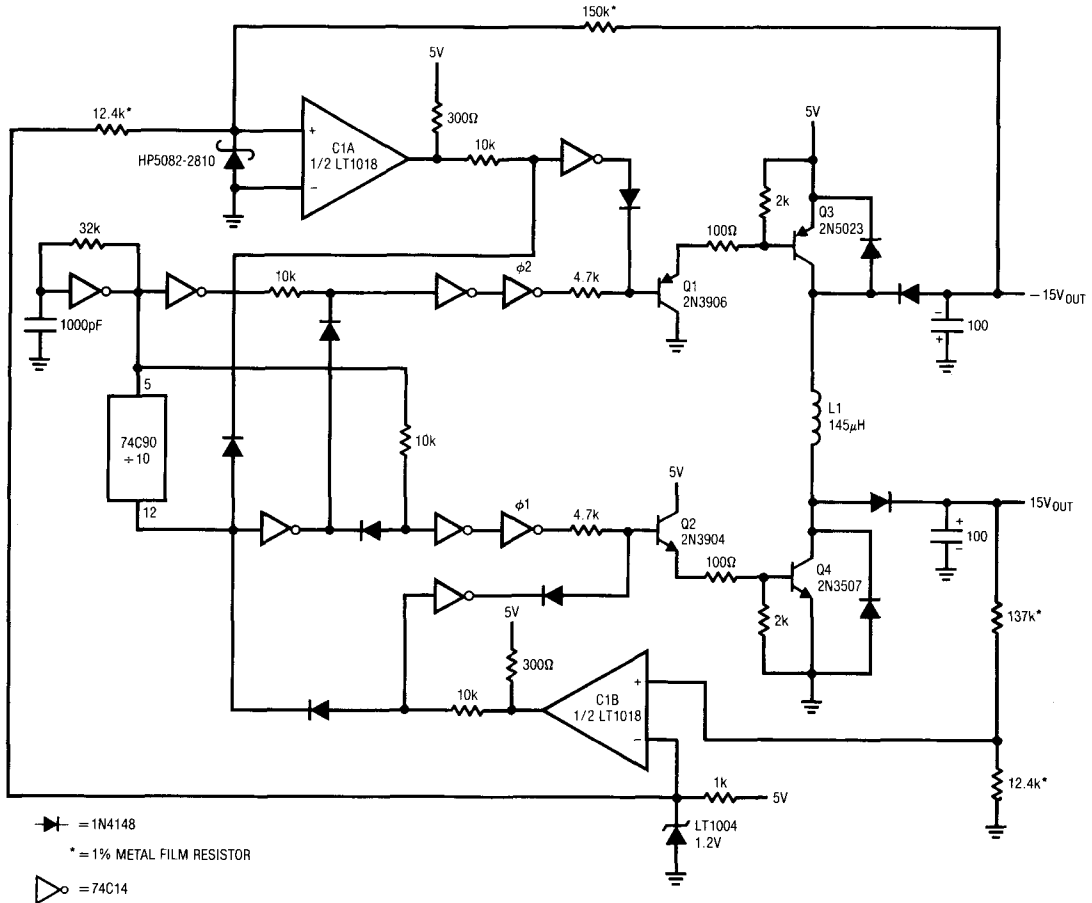


Figure 6. Single Inductor 5V to ±15V Regulated Converter

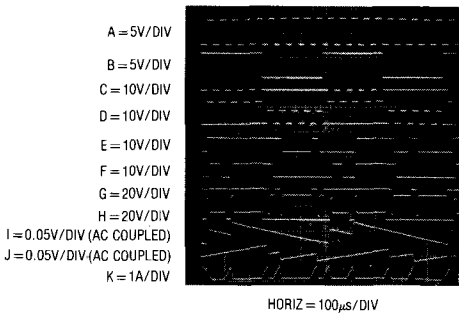


Figure 7. Waveforms for the Single Inductor, Dual-Output, Regulated Converter

Figure 8's design supplies $\pm 15\text{V}$ outputs at 100mA while consuming only 10mA quiescent current. The LT1070 switching regulator (for a complete description of this device, see Appendix C, "Physiology of the LT1070") drives L1 in flyback mode. A damper network clamps excessive flyback voltages. Flyback events at L1's secondary are half-wave rectified and filtered, producing positive and negative outputs across the 47 μF capacitors. The positive 16V output is regulated by a simple loop. Comparator C1A balances a sample of the positive output with a 2.5V reference obtained from the LT1020. When the 16V output (trace A, Figure 9) is too low, C1A switches (trace B) high, turning off the 4N46 opto-isolator. Q1 goes off, and the

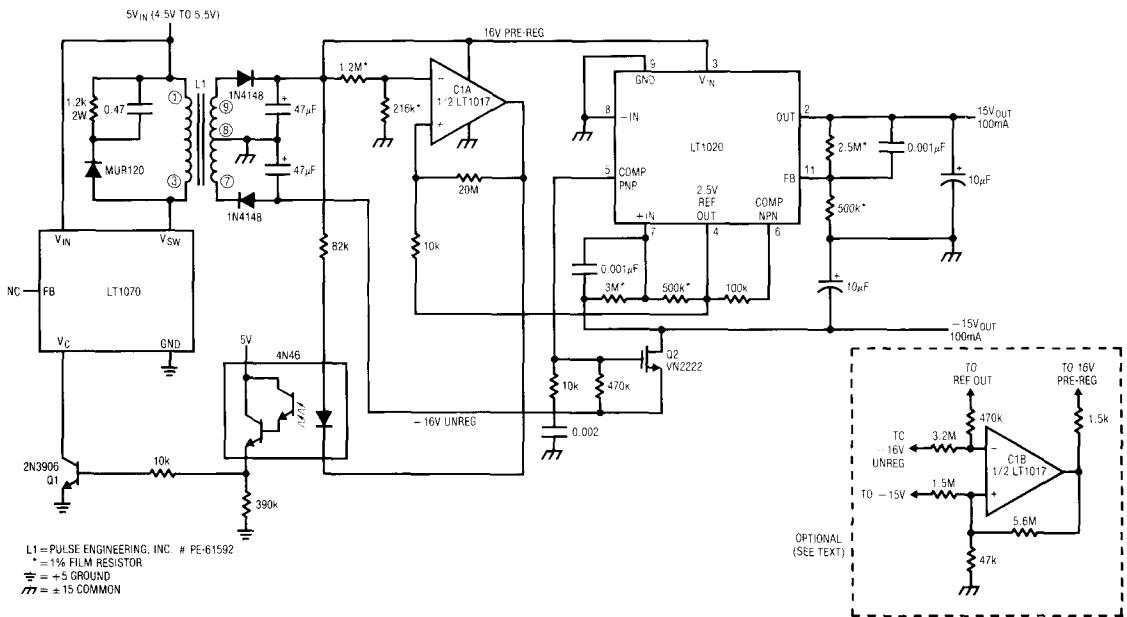


Figure 8. Low I_Q , Isolated 5V to $\pm 15V$ Converter

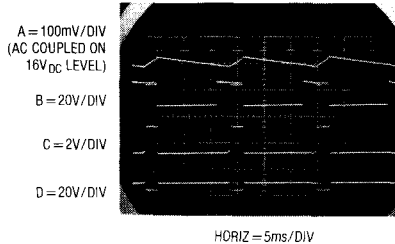


Figure 9. Waveforms for the Low I_Q 5V to $\pm 15V$ Converter

LT1070's control pin (V_C) pulls high (trace C). This causes full duty cycle 40kHz switching at the V_{SW} pin (trace D). The resultant energy into L1 forces the 16V output to ramp quickly positive, turning off C1A's output. The 20M value combined with the 4N46's slow response (note the delay between C1A going high and the V_C pin rise) gives about 40mV of hysteresis. The LT1070's on-off duty cycle is load dependent, saving significant power when the converter is lightly loaded. This characteristic is largely responsible for the 10mA quiescent current. The optoisolator preserves the converters input-output isolation. The LT1020, a low quiescent current regulator with low drop-out, further regulates the 16V line, giving the 15V

output. The linear regulation eliminates the 40mV ripple and improves transient response. The -16V output tends to follow the regulated -16V line, but regulation is poor. The LT1020's auxiliary on-board comparator is compensated to function as an op amp by the RC damper at pin 5. This amplifier linearly regulates the -16V line. MOSFET Q2 provides low drop-out current boost, sourcing the -15V output. The -15V output is stabilized with the op amp by comparing it with the 2.5V reference via the 500K - 3M current summing resistors. 1000pF capacitors frequency compensate each regulating loop. This converter functions well, providing $\pm 15V$ outputs at 100mA with only 10mA quiescent current. Figure 10 plots efficiency vs. a conventional design over a range of loads. For high loads results are comparable, but the low quiescent circuit is superior at lower current.

A possible problem with this circuit is related to the poor regulation of the -16V line. If the positive output is lightly loaded L1's magnetic flux is low. Heavy negative output loading under this condition results in the -16V line falling below its output regulators drop-out value. Specifically, with no load on the 15V output only 20mA is available from the -15V output. The full 100mA is only available from the

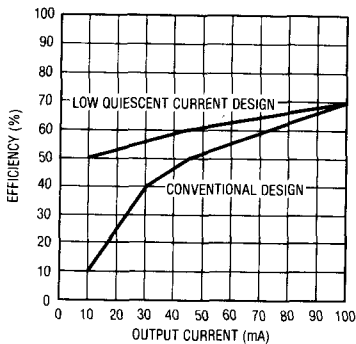


Figure 10. Efficiency vs Load for the Low I_Q Converter

-15V output when the 15V output is supplying more than 8mA. This restriction is often acceptable, but some situations may not tolerate it. The optional connection in Figure 8 (shown in dashed lines) corrects the difficulty. C1B detects the onset of -16V line decay. When this occurs its output pulls low, loading the 16V line to correct the problem. The biasing values given permit correction before the negative linear regulator drops out.

MICROPOWER QUIESCIENT CURRENT CONVERTERS

Many battery powered applications require very wide ranges of power supply output current. Normal conditions require currents in the ampere range, while standby or "sleep" modes draw only microamperes. A typical lap top computer may draw 1 to 2 amperes running while needing only a few hundred microamps for memory when turned off. In theory, any DC-DC converter designed for loop stability under no-load conditions will work. In practice, a converter's relatively large quiescent current may cause unacceptable battery drain during low output current intervals.

Figure 11 shows a typical flyback based converter. In this case the 6V battery is converted to a 12V output by the inductive flyback voltage produced each time the LT1070's V_{SW} pin is internally switched to ground (for commentary on inductor selection in flyback converters see Appendix D, "Inductor Selection for Flyback Converters"). An internal 40kHz clock produces a flyback event every 25 μ s. The energy in this event is controlled by the IC's internal error amplifier, which acts to force the feedback (FB) pin to a 1.23V reference. The error amplifiers high impedance

output (the V_C pin) uses an RC damper for stable loop compensation.

This circuit works well but pulls 9mA of quiescent current. If battery capacity is limited by size or weight this may be too high. How can this figure be reduced while retaining high current performance?

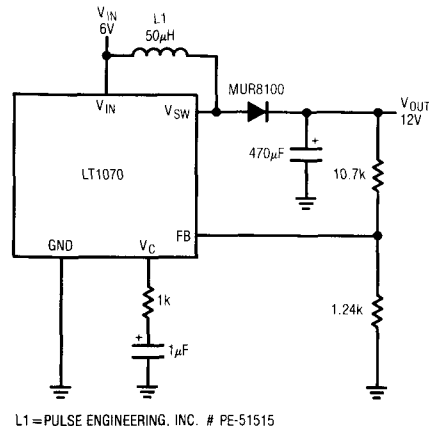


Figure 11. 6V to 12V, 2 Amp Converter with 9mA Quiescent Current

A solution is suggested by considering an auxiliary V_C pin function. If the V_C pin is pulled within 150mV of ground the IC shuts down, pulling only 50 microamperes. Figure 12's special loop exploits this feature, reducing quiescent current to only 150 microamperes. The technique shown is particularly significant, with broad implication in battery powered systems. It is easily applied to a wide variety of DC-DC converters, meeting an acknowledged need across a wide spectrum of applications.

Figure 12's signal flow is similar to Figure 11, but additional circuitry appears between the feedback divider and the V_C pin. The LT1070's internal feedback amplifier and reference are not used. Figure 13 shows operating waveforms under no load conditions. The 12V output (trace A) ramps down over a period of seconds. During this time comparator A1's output (trace B) is low, as are the 74C04 paralleled inverters. This pulls the V_C pin (trace C) low, putting the IC in its 50 μ A shutdown mode. The V_{SW} pin (trace D) is high, and no inductor current flows. When the 12V output drops about 20mV, A1 triggers and the inverters go high, pulling the V_C pin up and turning on the

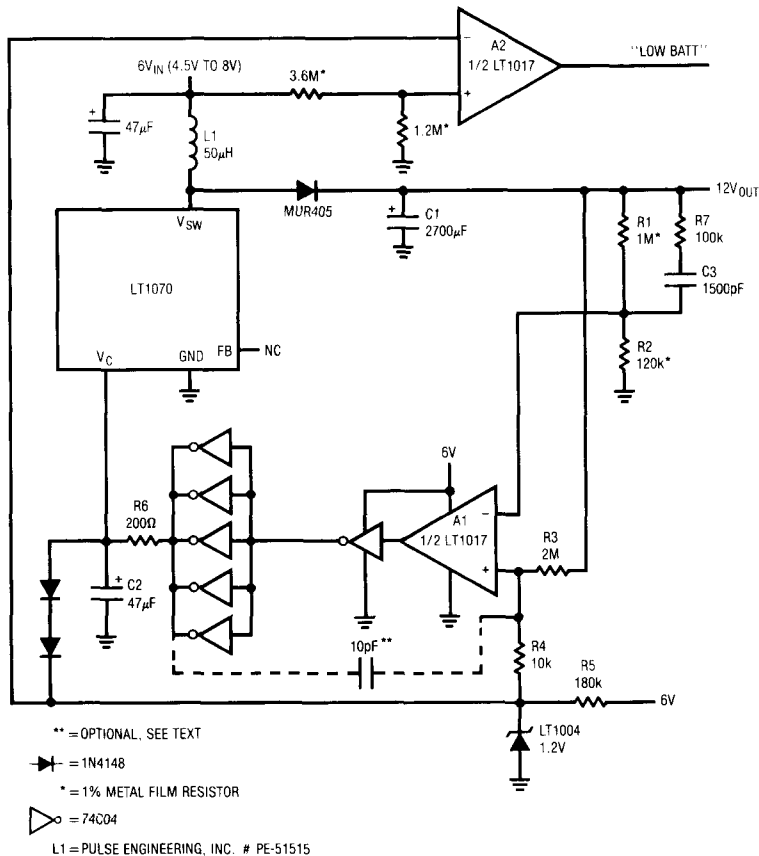


Figure 12. 6V to 12V, 2 Amp Converter with 150µA Quiescent Current

regulator. The V_{SW} pin pulses the inductor at the 40kHz clock rate, causing the output to abruptly rise. This action trips A1 low, forcing the V_C pin back into shutdown. This "bang-bang" control loop keeps the 12V output within the 20mV ramp hysteresis window set by R3-R4. Diode clamps prevent V_C pin overdrive. Note that the loop oscillation period of 4-5 seconds means the R6-C2 time constant at V_C is not a significant term. Because the LT1070 spends almost all of the time in shutdown, very little quiescent current (150µA) is drawn.

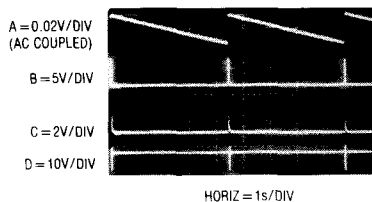


Figure 13. Low I_Q Converter Waveforms with No Load (Traces B and D Retouched for Clarity)

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Figure 14 shows the same waveforms with the load increased to 3mA. Loop oscillation frequency increases to keep up with the loads sink current demand. Now, the V_C pin waveform (trace C) begins to take on a filtered appearance. This is due to R6-C2's 10ms time constant. If the load continues to increase, loop oscillation frequency will also increase. The R6-C2 time constant, however, is fixed. Beyond some frequency, R6-C2 must average loop oscillations to DC. Figure 15 shows the same circuit points at 1 ampere loading. Note that the V_C pin is at DC, and repetition rate has increased to the LT1070's 40kHz clock frequency. Figure 16 plots what is occurring, with a pleasant surprise. As output current rises, loop oscillation frequency also rises until about 500Hz. At this point the R6-C2 time constant filters the V_C pin to DC and the LT1070 transitions into "normal" operation. With the V_C pin at DC it is convenient to think of A1 and the inverters as a linear error amplifier with a closed loop gain set by the R1-R2 feedback divider. In fact, A1 is still duty cycle modulating, but at a rate far above R6-C2's break frequency. The phase error contributed by C1 (which was selected for low loop frequency at low output currents) is dominated by the R6-C2 roll off and the R7-C3 lead into A1. The loop is stable and responds linearly for all loads beyond 80mA. In this high current region the LT1070 is desirably "fooled" into behaving like Figure 11's circuit.

A formal stability analysis for this circuit is quite complex, but some simplifications lend insight into loop operation. At $100\mu\text{A}$ loading ($120\text{k}\Omega$) C1 and the load form a decay time constant exceeding 300 seconds. This is orders of magnitude larger than R7-C3, R6-C2, or the LT1070's 40kHz commutation rate. As a result, C1 dominates the loop. Wideband A1 sees phase shifted feedback, and very low frequency oscillations similar to Figure 13's occur¹. Although C1's decay time constant is long, its charge time constant is short because the circuit has low sourcing impedance. This accounts for the ramp nature of the oscillations.

Increased loading reduces the C1-load decay time constant. Figure 16's plot reflects this. As loading increases, the loop oscillates at a higher frequency due to C1's decreased decay time. When the load impedance becomes low enough C1's decay time constant ceases to dominate the loop. This point is almost entirely determined by R6

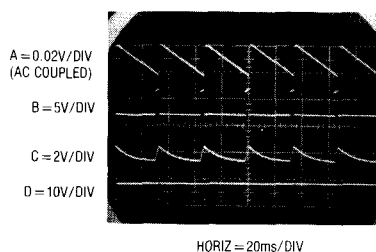


Figure 14. Low I_Q Converter Waveforms at Light Loading

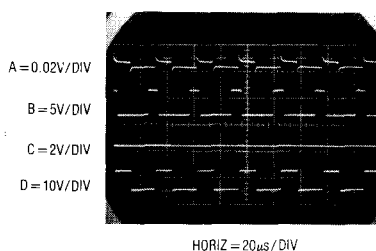


Figure 15. Low I_Q Converter Waveforms at 1 Amp Loading

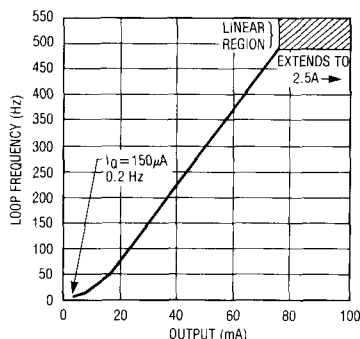


Figure 16. Figure 12's Loop Frequency vs Output Current. Note Linear Loop Operation Above 80mA.

and C2. Once R6 and C2 "take over" as the dominant time constant the loop begins to behave like a linear system. In this region (e.g. above about 75mA, per Figure 16) the LT1070 runs continuously at its 40kHz rate. Now, the R7-C3 time constant becomes significant, performing as a simple feedback lead² to smooth output response. There is a fundamental trade-off in the selection of the R7-C3 lead network values. When the converter is running in its linear

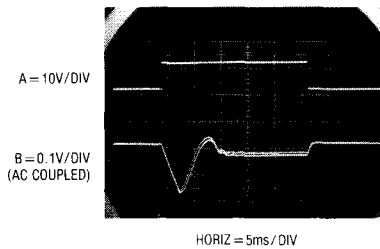


Figure 17. Load Transient Response for Figure 12's Low IQ Regulator

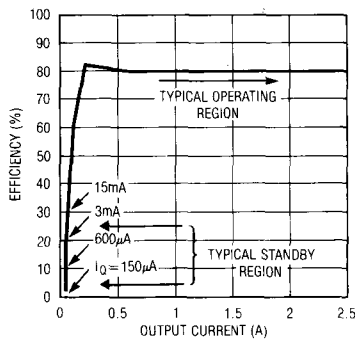


Figure 18. Efficiency vs Output Current for Figure 12. Standby Efficiency is Poor, But Power Loss Approaches Battery Self-Discharge.

region they must dominate the DC hysteresis deliberately generated by R3-R4. As such, they have been chosen for the best compromise between output ripple at high load and loop transient response.

Despite the complex dynamics transient response is quite good. Figure 17 shows performance for a step from no load to 1 ampere. When trace A goes high a 1 ampere load appears across the output (trace B). Initially, the output sags almost 150mV due to slow loop response time (the R6-C2 pair delay V_C pin response). When the LT1070 comes on (signaled by the 40kHz "fuzz" at the bottom extreme of trace B) response is reasonably quick and surprisingly well behaved considering circuit dynamics. The

multi-time constant decay³ ("rattling" is perhaps more appropriate) is visible as trace B approaches steady state between the 4th and 5th vertical divisions.

A2 functions as a simple low battery detector, pulling low when V_{IN} drops below 4.8V.

Figure 18 plots efficiency vs. output current. High power efficiency is similar to standard converters. Low power efficiency is somewhat better, although poor in the lowest ranges. This is not particularly bothersome, as *power* loss is very small.

This loop provides a controlled, conditional instability instead of the more usually desirable (and often elusive) unconditional stability. This deliberately introduced characteristic lowers converter quiescent current by a factor of 60 without sacrificing high power performance. Although demonstrated in a boost converter, it is readily exportable to other configurations. Figure 19A's step down (buck mode) configuration uses the same basic loop with almost no component changes. P-channel MOSFET Q1 is driven from the LT1072 (a low power version of the LT1070) to convert 12V to a 5V output. Q2 and Q3 provide current limiting, while Q4 supplies turn off drive to Q1. The lower output voltage mandates slightly different hysteresis biasing than Figure 12, accounting for the 1M Ω value at the comparators positive input. In other respects the loop and its performance are identical. Figure 19B uses the loop in a transformer based multi-output converter. Note that the floating secondaries allow a -12V output to be obtained with a positive voltage regulator.

Low Quiescent Current Micropower 1.5V to 5V Converter

Figure 20 extends our study of low quiescent current converters into the low voltage, micropower domain. In some circumstances, due to space or reliability considerations, it is preferable to operate circuitry from a single 1.5V cell. This eliminates almost all IC's as design candidates. Although it is possible to design circuitry which runs directly

¹ Some layouts may require substantial trace area to A1's inputs. In such cases the optional 10pF capacitor shown ensures clean transitions at A1's output.

² "Zero Compensation" for all you technosnobs out there.

³ Once again, "multi-pole settling" for those who adore jargon.

Application Note 29

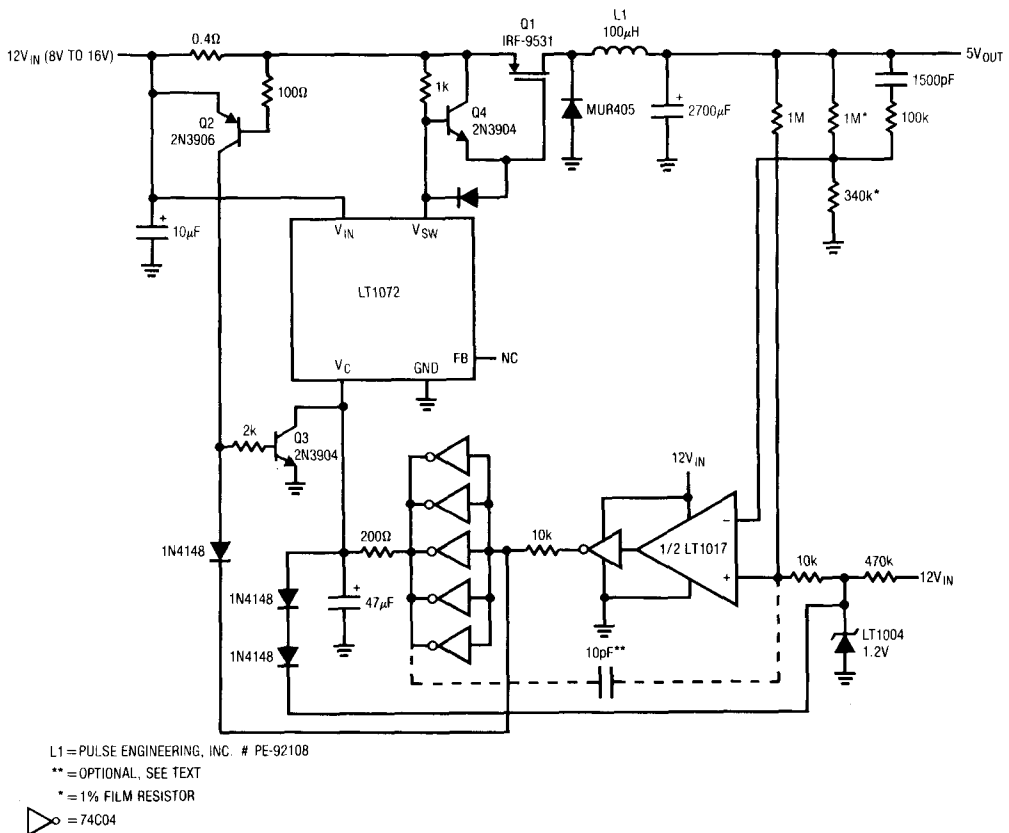


Figure 19A. The Low Quiescent Current Loop Applied to a Buck Converter

from a single cell (see LTC Application Note AN-15, "Circuitry For Single Cell Operation") a DC-DC converter permits using higher voltage IC's. Figure 20's design converts a single 1.5V cell to a 5V output with only 125 μ A quiescent current. Oscillator C1A's output is a 2kHz square wave (trace D, Figure 21). The configuration is conventional, except that the biasing accommodates the narrow common mode range dictated by the 1.5V supply. To maintain low power, C1A's integrating capacitor is small, with only 50mV of swing. The parallel connected sides of C2 drive L1. When the 5V output (trace A) coasts down far enough

C1B goes low (trace B), pulling both C2 positive inputs close to ground. C1A's clock now appears at the paralleled C2 outputs (trace C), forcing energy into L1. The paralleled outputs minimize saturation losses. L1's fly-back pulses, rectified and stored in the 47 μ F capacitor, form the circuit's DC output. C1B on-off modulates C2 at whatever duty cycle is required to maintain the circuit's 5V output. The LT1004 is the reference, with the resistor divider at C1B's positive input setting the output voltage. Schottky clamping of C2's outputs prevents negative going overdrives due to parasitic L1 behavior.

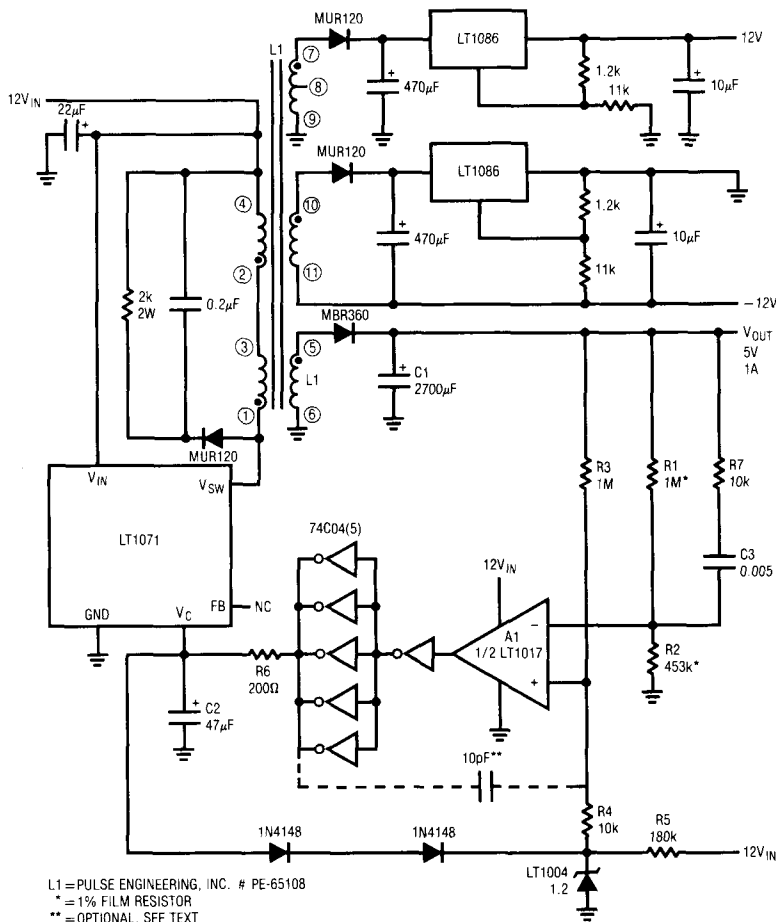


Figure 19B. Multi-Output, Transformer Coupled Low Quiescent Current Converter

The 1.2V LT1004 reference biasing is bootstrapped to the 5V output, permitting circuit operation down to 1.1V. A 10M bleed to supply ensures start-up. The 1M resistors divide down the 1.2V reference, keeping C1B inside common mode limits. C1B's positive feedback RC pair sets about 100mV hysteresis and the 22pF unit suppresses high frequency oscillation.

The micropower comparators and very low duty cycles at light load minimize quiescent current. The 125µA figure noted is quite close to the LT1017's steady state currents. As load increases the duty cycle rises to meet the

demand, requiring more battery power. Decrease in battery voltage produces similar behavior. Figure 22 plots available output current vs. battery voltage. Predictably, the highest power is available with a fresh cell (e.g. 1.5V-1.6V), although regulation is maintained down to 1.15V for 250µA loading. The plot shows that the test circuit continued to regulate below this point, but this cannot be relied on in practice (LT1017 V_{MIN} = 1.15V). The low supply voltage makes saturation and other losses in this circuit difficult to control. As such, efficiency is about 50%.

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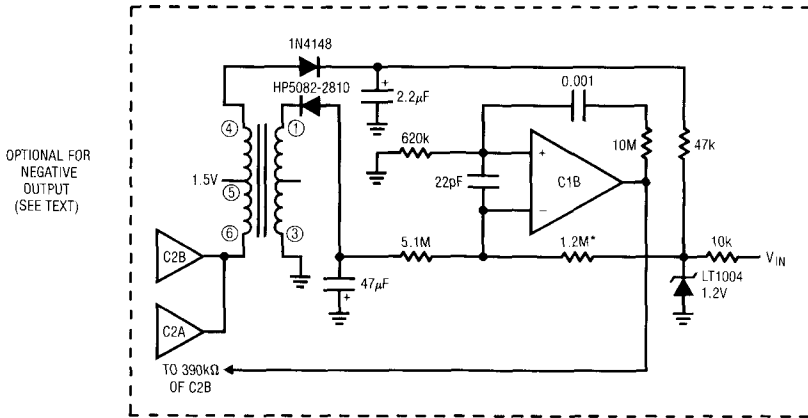
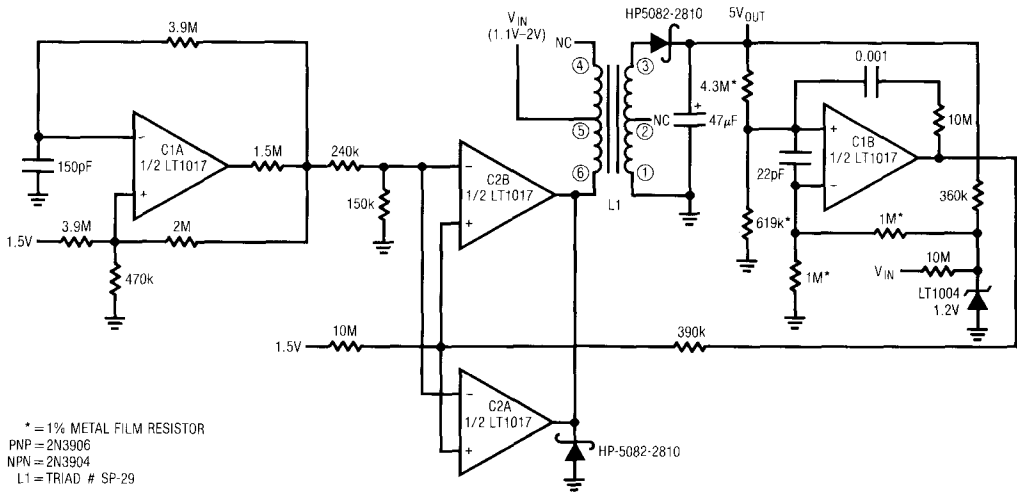


Figure 20. 800 μ A Output 1.5V to 5V Converter

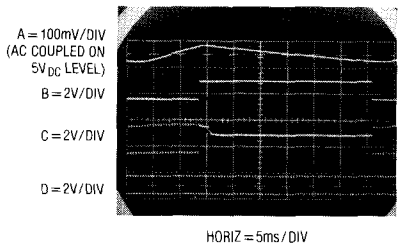


Figure 21. Waveforms for Low Power 1.5V to 5V Converter

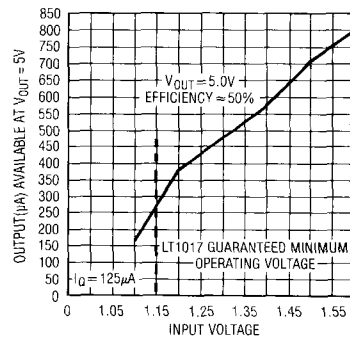


Figure 22. Output Current Capability vs Input Voltage for Figure 20

The optional connection in Figure 20 (shown in dashed lines) takes advantage of the transformers floating secondary to furnish a $-5V$ output. Drive circuitry is identical, but C1B is rearranged as a current summing comparator. The LT1004's bootstrapped positive bias is supplied by L1's primary flyback spikes.

200mA Output 1.5V to 5V Converter

Although useful, the preceding circuit is limited to low power operation. Some 1.5V powered systems (survival 2-way radios, remote, transducer fed data acquisition systems, etc.) require much more power. Figure 23's design supplies a 5V output with 200mA capacity. Some sacrifice in quiescent current is made in this circuit. This is predicated on the assumption that it operates continuously at

high power. If lowest quiescent current is necessary the technique detailed back in Figure 12 is applicable.

The circuit is essentially a flyback regulator, similar to Figure 11. The LT1070's low saturation losses and ease of use permit high power operation and design simplicity. Unfortunately, this device has a 3V minimum supply requirement. Bootstrapping its supply pin from the 5V output is possible, but requires some form of start-up mechanism. Dual comparator C1 and the transistors form a start-up loop. When power is applied C1A oscillates (trace A, Figure 24) at 5kHz. Q1 biases, driving Q2's base hard. Q2's collector (trace B) pumps L1, causing voltage step-up flyback events. These events are rectified and stored in the 500 μ F capacitor, producing the circuit's DC output. C1B is set up so it (trace C) goes low when circuit

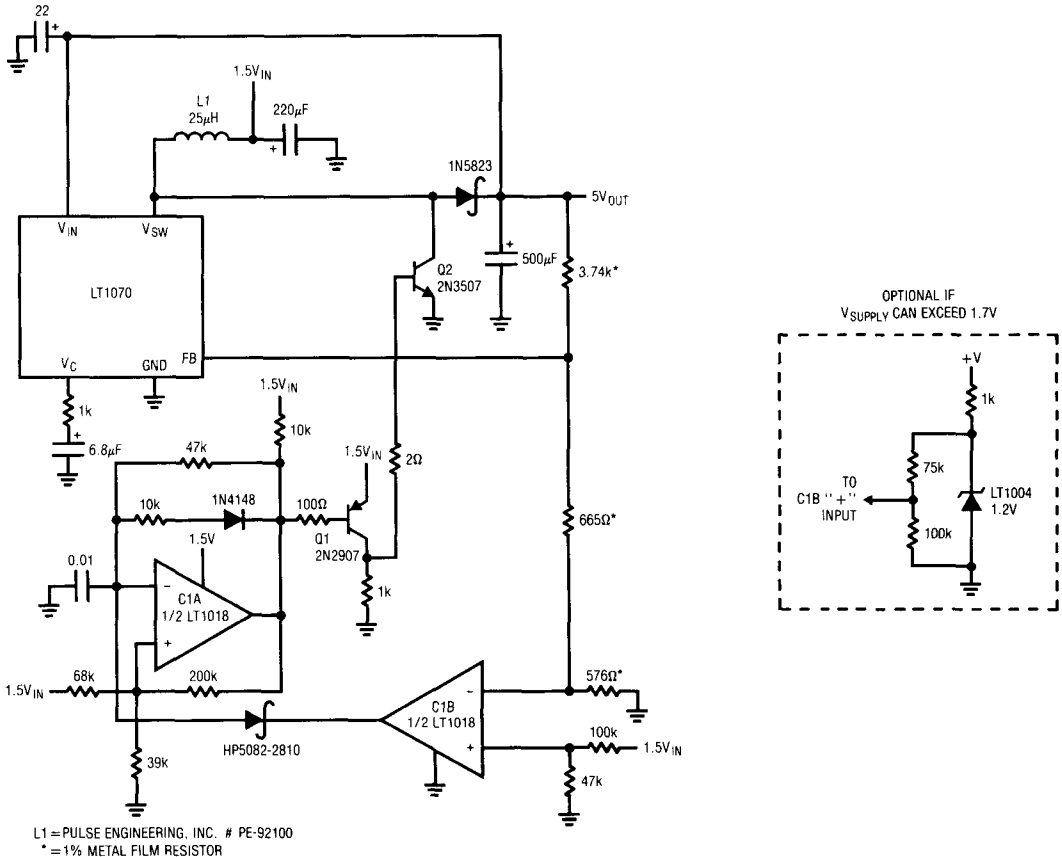


Figure 23. 200mA Output 1.5V to 5V Converter

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output crosses about 4.5V. When this occurs C1A's integration capacitor is pulled low, stopping it from oscillating. Under these conditions Q2 can no longer drive L1, but the LT1070 can. This behavior is observable at the LT1070's V_{SW} pin (the junction of L1, Q2's collector and the LT1070), trace D. When the start-up circuit goes off, the LT1070 V_{IN} pin has adequate supply voltage and it begins operation. This occurs at the 4th vertical division of the photograph. There is some overlap between start-up loop turn-off and LT1070 turn-on, but it has no detrimental effect. Once the circuit is running it functions similarly to Figure 11.

The start-up loop must be carefully designed to function over a wide range of loads and battery voltages. Start-up currents exceed 1 ampere, necessitating attention to Q2's saturation and drive characteristics. The worst case is a nearly depleted battery and heavy output loading. Figure 25 shows circuit output starting into a 100mA load at $V_{BATT} = 1.2V$. The sequence is clean, and the LT1070 takes over at the appropriate point. In Figure 26, loading is increased to 200mA. Start-up slope decreases, but starting still occurs. The abrupt slope increase (6th vertical

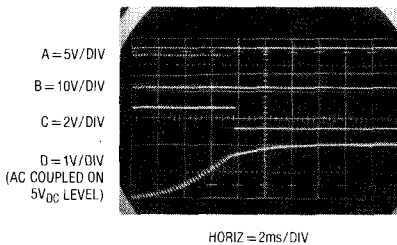


Figure 24. High Power 1.5V to 5V Converter Start-Up Sequence

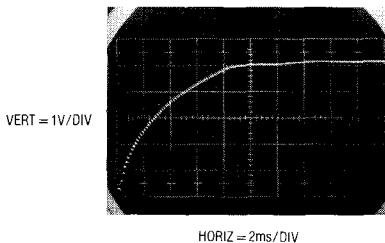


Figure 25. High Power 1.5V to 5V Converter Turn-On Into A 100mA Load at $V_{BATT} = 1.2V$

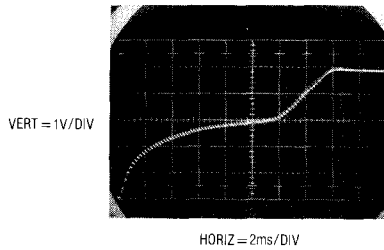


Figure 26. High Power 1.5V to 5V Converter Turn-On Into A 200mA Load at $V_{BATT} = 1.2V$

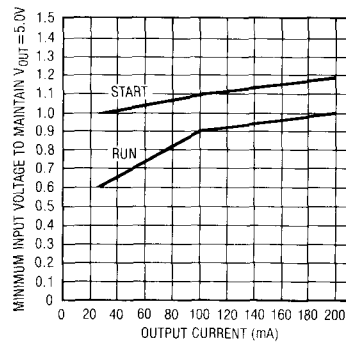


Figure 27. Input-Output Data for Figure 23

division) is due to overlapping operation of the start-up loop and the LT1070.

Figure 27 plots input-output characteristics for the circuit. Note that the circuit will start into all loads with $V_{BATT} = 1.2V$. Start-up is possible down to 1.0V at reduced loads. Once the circuit has started, the plot shows it will drive full 200mA loads down to $V_{BATT} = 1.0V$. Reduced drive is possible down to $V_{BATT} = 0.6V$ (a very dead battery)! Figures 28 and 29, dynamic XY crossplot versions of Figure 27, are taken at 20 and 200 milliamperes, respectively. Figure 30 graphs efficiency at two supply voltages over a range of output currents. Performance is attractive, although at lower currents circuit quiescent power degrades efficiency. Fixed junction saturation losses are responsible for lower overall efficiency at the lower supply voltage. Figure 31 shows quiescent current increasing as supply decays. Longer inductor current charge intervals are necessary to compensate the decreased supply voltage.

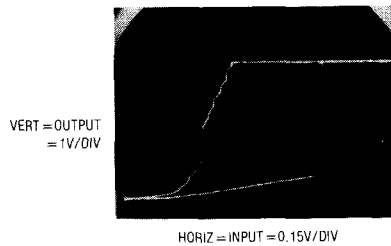


Figure 28. Input-Output XY Characteristics of the 1.5V to 5V Converter at 20mA Loading

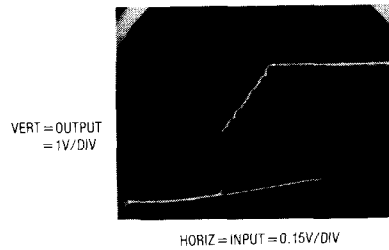


Figure 29. Input-Output XY Characteristics of the 1.5V to 5V Converter at 200mA Loading

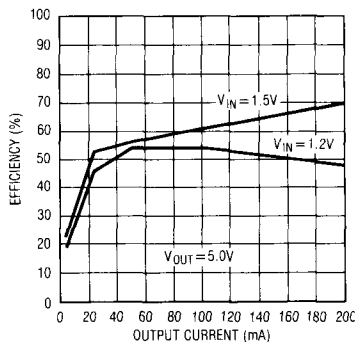


Figure 30. Efficiency vs Operating Point for Figure 23

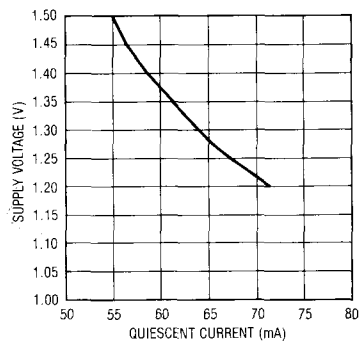


Figure 31. I_Q vs Supply Voltage for Figure 23

HIGH EFFICIENCY CONVERTERS

High Efficiency 12V to 5V Converter

Efficiency is sometimes a prime concern in DC-DC converter design (see Appendix E, "Optimizing Converters for Efficiency"). In particular, small portable computers frequently use a 12V primary supply which must be converted down to 5V. A 12V battery is attractive because it offers long life when all trade-offs and sources of loss are considered. Figure 32 achieves 90% efficiency. This circuit can be recognized as a positive buck converter. Transistor Q1 serves as the pass element. The catch diode is replaced with a synchronous rectifier, Q2, for improved efficiency. The input supply is nominally 12V but can vary from 9.5V to 14.5V. Power losses are minimized by utilizing low source-to-drain resistance, 0.028 Ω , NMOS transistors for the catch diode and pass element. The inductor, Pulse Engineering PE-92210K, is made from a low loss core material which squeezes a little more efficiency out of the

circuit. Also, keeping the current sense threshold voltage low minimizes the power lost in the current limit circuit.

Figure 33 shows the operating waveforms. Q5 drives the synchronous rectifier, Q2, when the V_{SW} pin (trace A) is turned "off". Q2 is turned off through D1 and D2 when the V_{SW} pin is "on". To turn on Q1, the gate (trace B) must be driven above the input voltage. This is accomplished by bootstrapping the capacitor, C1, off the drain of Q2 (trace C). C1 charges up through D1 when Q2 is turned on. When Q2 is turned off, Q3 is able to conduct, providing a path for C1 to turn Q1 on. During this time current flows through Q1 (trace D), through the inductor (trace E) and into the load. To turn Q1 off, the V_{SW} pin must be "off." Q5 is now able to turn on Q4 and the gate of Q1 is pulled low through D3 and the 50 Ω resistor. This resistor is used to reduce the voltage noise generated by fast switching characteristics of Q1. When Q2 is conducting (trace F), Q1

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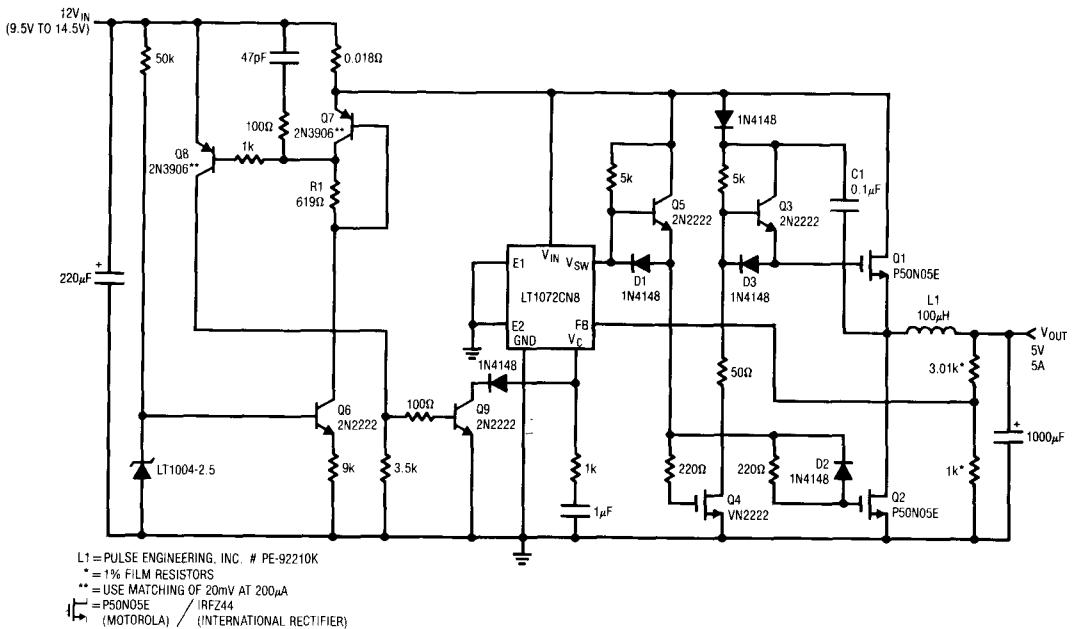


Figure 32. 90% Efficiency Positive Buck Converter with Synchronous Switch

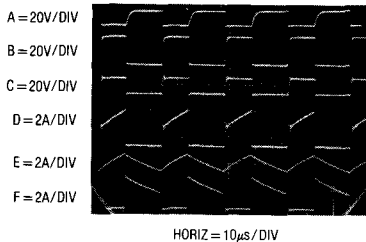


Figure 33. Waveforms for 90% Efficiency Buck Converter

must be off. The efficiency will be decreased if both transistors are conducting at the same time. The 220Ω resistors and D2 are used to minimize the overlap of the switch cycles. Figure 34 shows the efficiency vs. load plot for the circuit as shown. The other plots are for non-synchronously switched buck regulators (see indicated Figures).

Short circuit protection is provided by Q6 through Q9. A 200µA current source is generated from an LT1004, Q6 and the 9k resistor. This current flows through R1 and generates a threshold voltage of 124mV for the comparator, Q7

and Q8. When the voltage drop across the 0.018Ω sense resistor exceeds 124mV, Q8 is turned on. The LT1072's V_{SW} pin goes off when the V_C pin is pulled below 0.9V. This occurs when Q8 forces Q9 to saturate. An RC damper suppresses line transients that might prematurely turn on Q8.

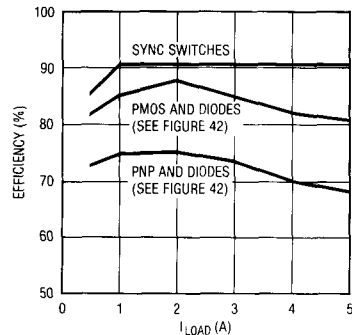
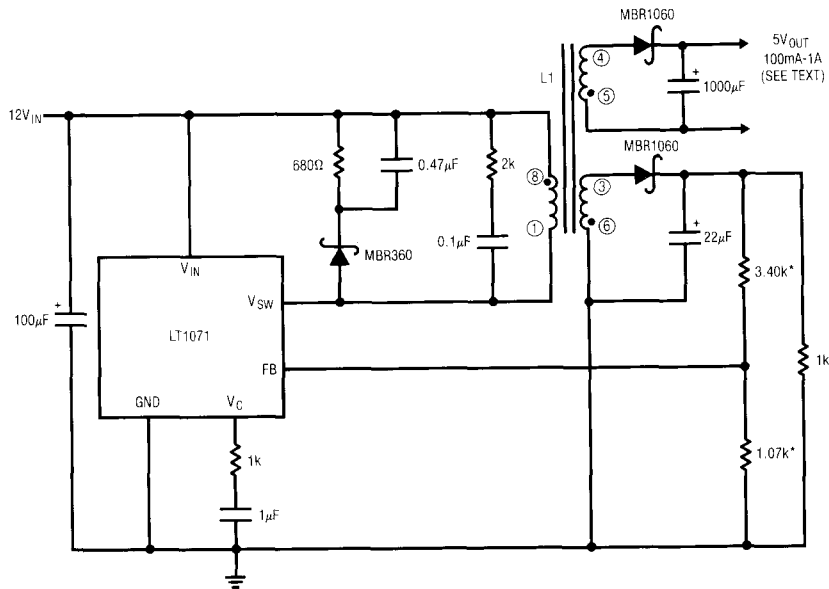


Figure 34. Efficiency vs Load for Figure 32. The Synchronous Switches Give Higher Efficiency than Simple FET or Bipolar Transistors and Diodes.



L1 = PULSE ENGINEERING, INC. # PE-65066
 * = 1% FILM RESISTORS
 MBR1060 = MOTOROLA

Figure 35. High Efficiency Flux Sensed Isolated Converter

High Efficiency, Flux Sensed Isolated Converter

Figure 35's 75% efficiency is not as good as the previous circuit, but it has a fully floating output. This circuit uses a bifilar wound flux sensing secondary to provide isolated voltage feedback. In operation the LT1070's V_{SW} pin (trace A, Figure 36) pulses L1's primary, producing identical waveforms at the floating power and flux sensing secondaries (traces B and C). Feedback occurs from the flux sense winding via the diode and capacitive filter. The 1k resistor provides a bleed current, while the 3.4k-1.07k divider sets output voltage. The diode partially compensates the diode in the power output winding, resulting in an overall temperature coefficient of about 100ppm/°C. The oversized diode aids efficiency, although significant improvement (e.g. 5%-10%) is possible if synchronous rectification is employed, as in Figure 32. The primary damper network is unremarkable, although the 2k-0.1μF network has been added to suppress excessive ringing at low output current. This ringing is not deleterious to circuit

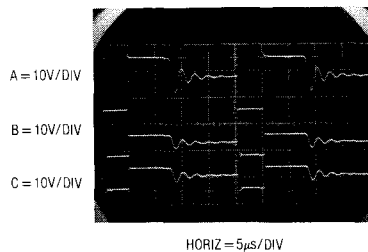


Figure 36. Waveforms for Flux Sensed Converter

operation, and the network is optional. Below about 10% loading non-ideal transformer behavior introduces significant regulation error. Regulation stays within $\pm 100\text{mV}$ from 10% to 100% of output rating, with excursion exceeding 900mV at no load. Figure 37's circuit trades away isolation for tight regulation with no output loading restrictions. Efficiency is the same.

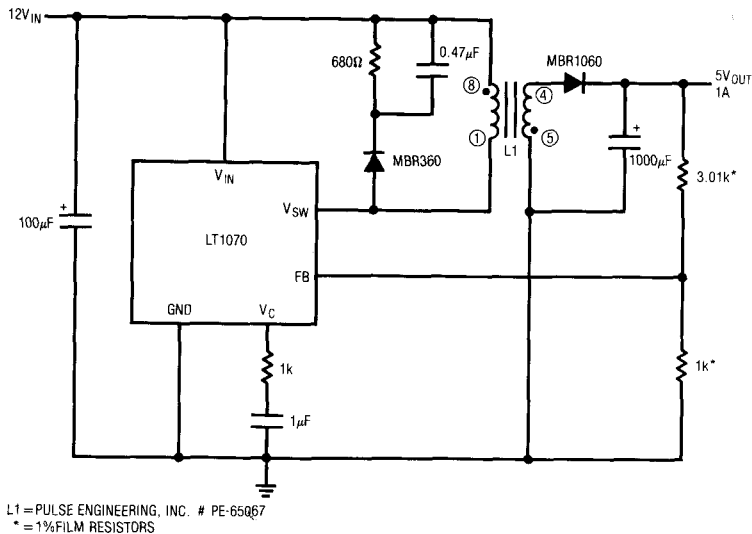


Figure 37. Non-Isolated Version of Figure 35

WIDE RANGE INPUT CONVERTERS

Wide Range Input – 48V to 5V Converter

Often converters must accommodate a wide range of inputs. Telephone lines can vary over considerable tolerances. Figure 38's circuit uses an LT1072 to supply a 5V output from a telecom input. The raw telecom supply is nominally –48V but can vary from –40V to –60V. This range of voltages is acceptable to the V_{SW} pin but protection is required for the V_{IN} pin ($V_{MAX} = 60V$). Q1 and the 30V zener diode serve this purpose, dropping V_{IN} 's voltage to acceptable levels under all line conditions.

Here, the "top" of the inductor is at ground and the LT1072's ground pin at –V. The feedback pin senses with respect to the ground pin, so a level shift is required from the 5V output. Q2 serves this purpose, introducing only –2mV/°C drift. This is normally not objectionable in a logic supply. It can be compensated with the optional appropriately scaled diode-resistor shown in Figure 38.

Frequency compensation uses an RC damper at the V_C pin. The 68V zener is a type designed to clamp and absorb excessive line transients which might otherwise damage the LT1072 (V_{SW} maximum voltage is 75V).

Figure 39 shows operating waveforms at the V_{SW} pin. Trace A is the voltage and trace B the current. Switching is crisp, with well controlled waveforms. A higher current version of this circuit appears in LTC Application Note AN-25, "Switching Regulators For Poets."

3.5V to 35V_{IN} – 5V_{OUT} Converter

Figure 40's approach has an even wider input range. In this case it produces either a –5V or 5V output (shown in dashed lines). This circuit is an extension of Figure 11's basic flyback topology. The coupled inductor allows the option for buck, boost, or buck-boost converters. This circuit can operate down to 3.5V for battery applications while accepting 35V inputs.

Figure 41 shows the operating waveforms for this circuit. During the V_{SW} (trace A) "on" time, current flows through the primary winding (trace B). No current is transferred to the secondary because the catch diode, D1, is reverse biased. The energy is stored in the magnetic field. When the switch is turned "off" D1 forward biases and the energy is transferred to the secondary winding. Trace C is

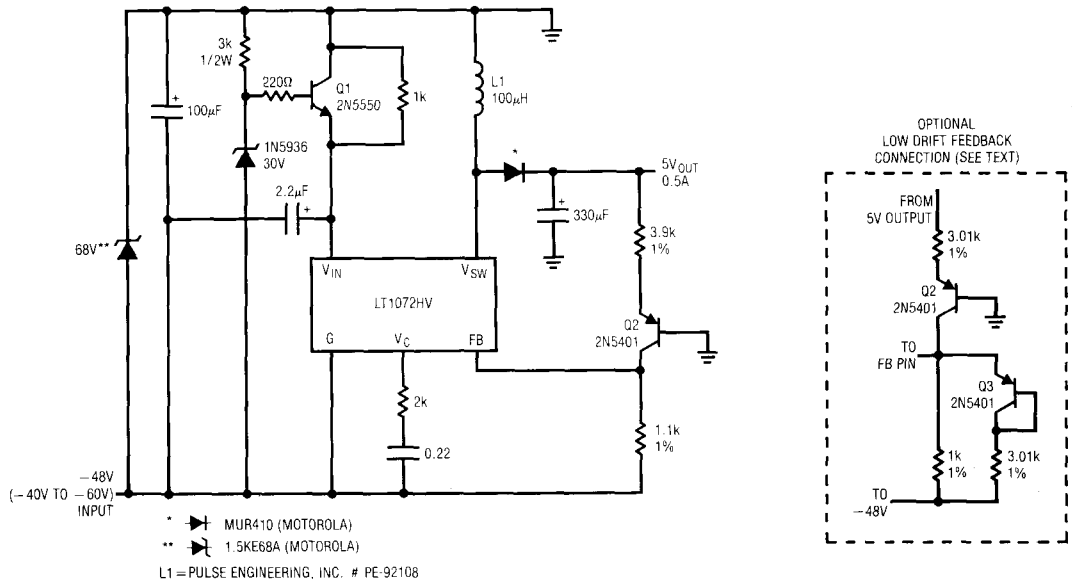


Figure 38. Wide Range Input Converter

the voltage seen on the secondary and trace D is the current flowing through it. This is not an ideal transformer so not all of the primary windings energy is coupled into the secondary. The energy left in the primary winding causes the overvoltage spikes seen on the V_{SW} pin (trace E). This phenomenon is modeled by a leakage inductance term which is placed in series with the primary winding. When the switch is turned "off" current continues to flow in the inductor causing the snubber diode to conduct (trace F). The snubber diode current falls to zero as the inductor loses its energy. The snubber network clamps the voltage spike. When the snubber diode current reaches zero, the V_{SW} pin voltage settles to a potential related to the turns ratio, output voltage and input voltage.¹

The feedback pin senses with respect to ground, so Q1 through Q3 provides the level shift from the -5V output. Q1 introduces a -2mV/°C drift to the circuit. This effect can be compensated by a circuit similar to the one shown in Figure 38. Line regulation is degraded due to Q3's output impedance. If this is a problem, an op amp must be used to perform the level shift (see AN-19, Figure 29).

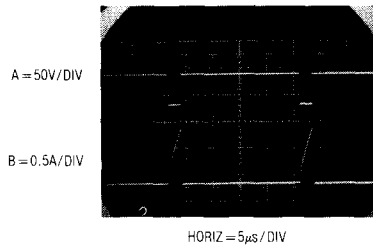


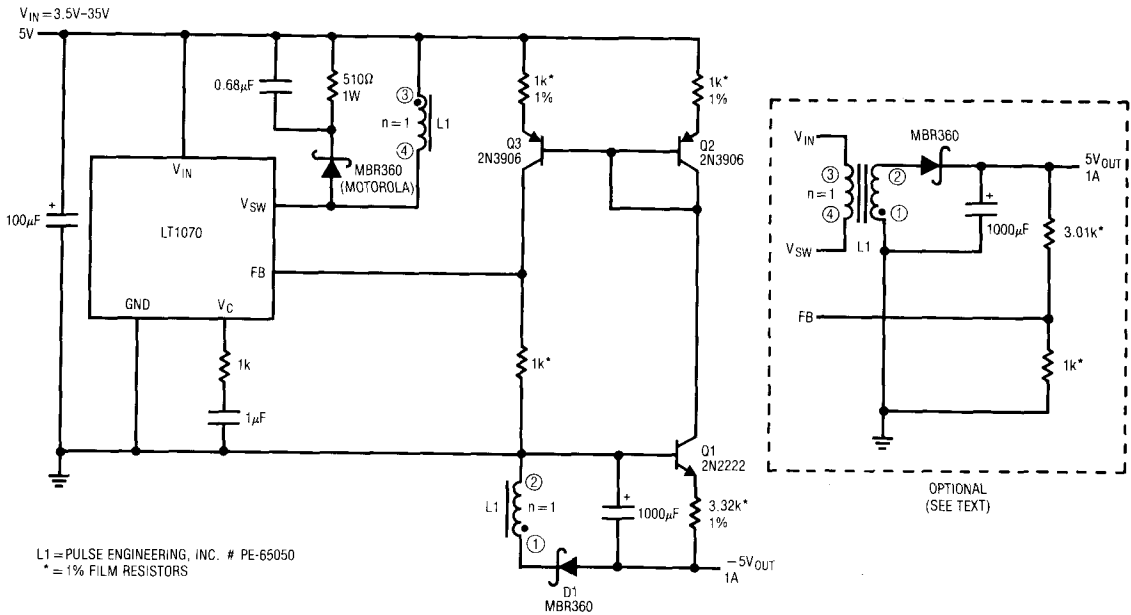
Figure 39. Waveforms for Wide Range Input Converter

Wide Range Input Positive Buck Converter

Figure 42 is another example of a positive buck converter. This is a simpler version compared to the synchronous switch buck, Figure 32. However, efficiency isn't as high (see Figure 34). If the PMOS transistor is replaced with a Darlington PNP transistor (shown in dashed lines) efficiency decreases further.

¹ Application Note AN-19, "LT1070 Design Manual," page 25.

Application Note 29



L1 = PULSE ENGINEERING, INC. # PE-65050
* = 1% FILM RESISTORS

Figure 40. Wide Range Input Positive to Negative Flyback Converter

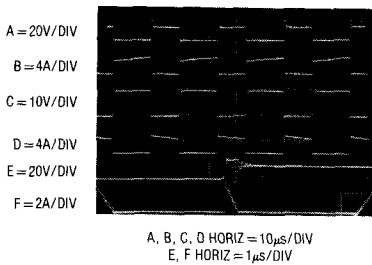


Figure 41. Waveforms for Wide Range Input Positive - 5V Output Flyback Converter

Figure 43A shows the operating waveforms for this circuit. The pass transistor's (Q1) drive scheme is similar to the one shown in Figure 32. During the V_{SW} (trace A) "on" time, the gate of the pass transistor is pulled down through D1. This forces Q1 to saturate. Trace B is the voltage seen on the drain of Q1 and trace C is the current passing through Q1. The supply current flows through the inductor (trace D) and into the load. During this time energy is being stored in the inductor. When voltage is applied to the inductor, current does not instantly rise. As

the magnetic field builds up, the current builds. This is seen in the inductor current waveform (trace D). When the V_{SW} pin is "off," Q2 is able to conduct and turns Q1 off. Current can no longer flow through Q1, instead D2 is conducting (trace E). During this period some of the energy stored in the inductor will be transferred to the load. Current will be generated from the inductor as long as there is any energy in it. This can be seen in Figure 43A. This is known as continuous mode operation. If the inductor is completely discharged, no current will be generated (see Figure 43B). When this happens neither switch, Q1 or D2, is conducting. The inductor looks like a short and the voltage on the cathode of D2 will settle to the output voltage. These "boingies" can be seen in trace B of Figure 43B. This is known as discontinuous mode operation. Higher input voltages can be handled with the gate-source zener clamped by D2. The 400 milliwatt zener's current must be rescaled by adjusting the 50Ω value. Maximum gate-source voltage is 20V. The circuit will function up to 35V V_{IN} . At inputs beyond 35V all semiconductor breakdown voltages must be considered.

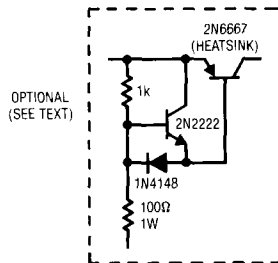
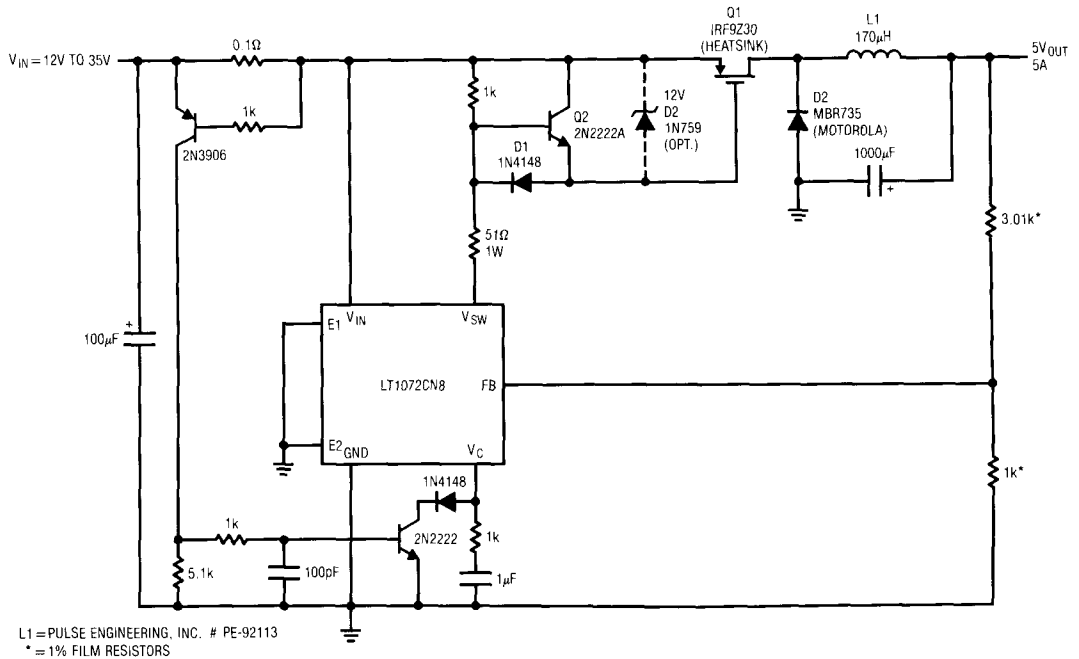


Figure 42. Positive Buck Converter

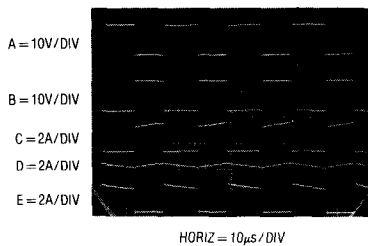


Figure 43A. Waveforms for Wide Range Input Positive Buck Converter (Continuous Mode)

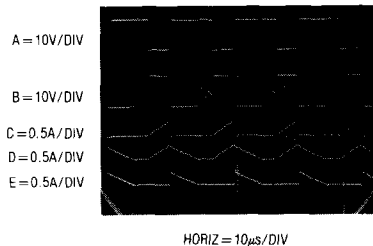


Figure 43B. Waveforms for Wide Range Input Positive Buck Converter (Discontinuous Mode)

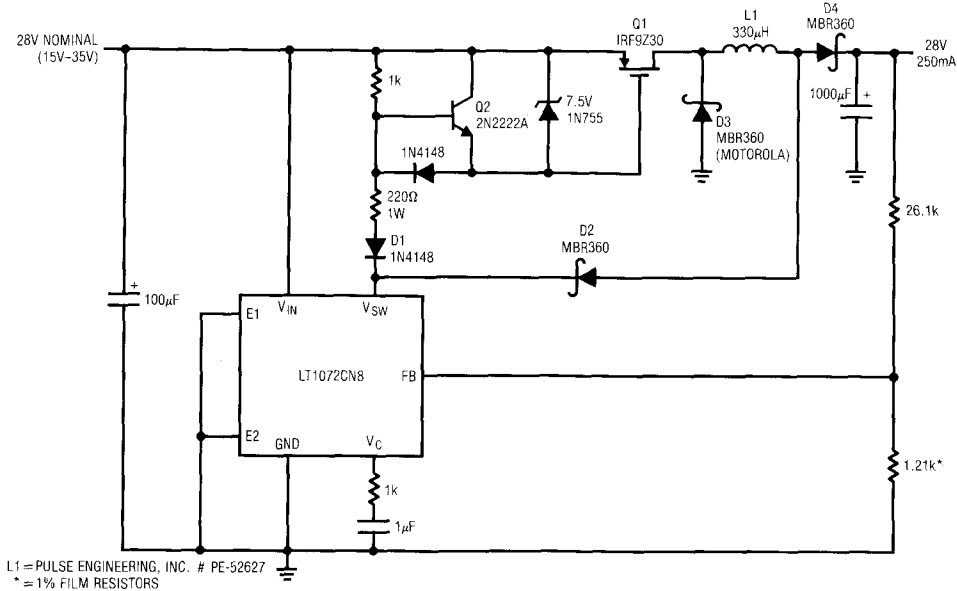


Figure 44. Positive Buck-Boost Converter

Buck Boost Converter

The buck boost topology is useful when the input voltage can either be higher or lower than the output. In this example, Figure 44, this is accomplished with a single inductor instead of a transformer, as in Figure 40 (optional). However, the input voltage range only extends down to 15V and can reach to 35V. If the maximum 1.25A switch current rating of the LT1072 is exceeded an LT1071 or LT1070 can be used instead. At high power levels package thermal characteristics should be considered.

The operation of the circuit is similar to the positive buck converter, Figure 42. The gate drive to the pass transistor is derived the same way except the gate-source voltage is clamped. Remember, the gate-source maximum voltage rating is specified at $\pm 20V$. Figure 45 shows the operating waveforms. When the V_{SW} pin is "on" (trace A), the pass transistor, Q1, is saturated. The gate voltage (trace B) is clamped by the zener diode. Trace C is the voltage on the drain of Q1 and trace D is the current through it. This is where the similarities between the two circuits end. Notice the inductor is pulled to within a diode drop, D2, above

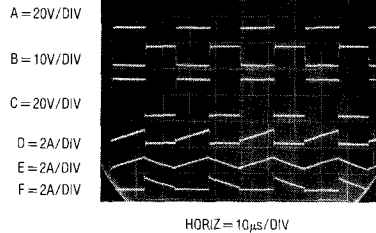


Figure 45. Waveforms for Positive Buck-Boost Converter

ground, instead of being tied to the output (see Figure 42). In this case, the inductor has the input voltage applied across it, except for a V_{be} and saturation losses. D4 is reverse biased and blocks the output capacitor from discharging into the V_{SW} pin. When the V_{SW} pin is "off" Q1 and D2 cease to conduct. Since the current in the inductor (trace E) continues to flow, D3 and D4 are forward biased and the energy in the inductor is transferred into the load. Trace F is the current through D3. Also, D2 keeps Q1 from staying on if the circuit is operating in buck mode. D1, on the other hand, blocks current from flowing into the gate drive circuit when operating in boost mode.

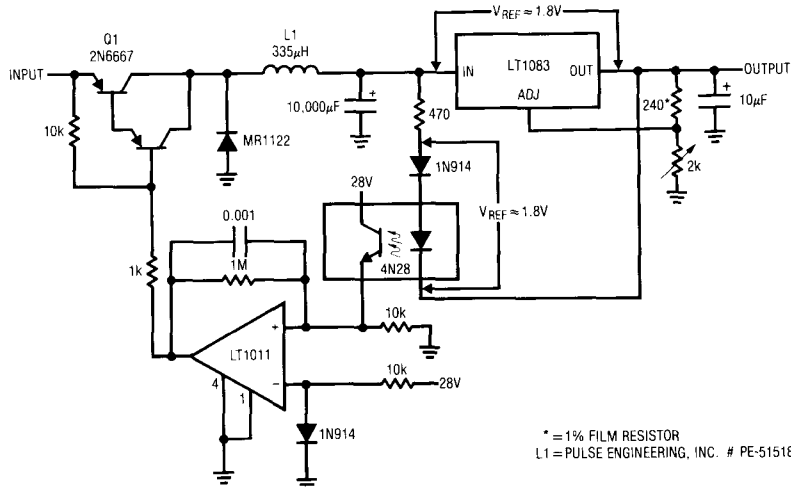


Figure 46. High Power Linear Regulator with Switching Pre-Regulator

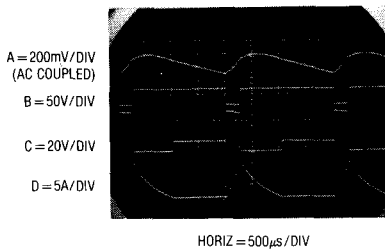


Figure 47. Switching Pre-Regulated Linear Regulators Waveforms

Wide Range Switching Pre-Regulated Linear Regulator

In a sense, linear regulators can be considered extraordinarily wide range DC-DC converters. They do not face the dynamic problems switching regulators encounter under varying ranges of input and output. Excess energy is simply dissipated as heat. This elegantly simplistic energy management mechanism pays dearly in terms of efficiency and temperature rise. Figure 46 shows a way a linear regulator can more efficiently control high power under widely varying input and output conditions.

The regulator is placed within a switched-mode loop that servo-controls the voltage *across* the regulator. In this arrangement the regulator functions normally while the switched-mode control loop maintains the voltage across

it at a minimal value, regardless of line, load or output setting changes. Although this approach is not quite as efficient as a classical switching regulator, it offers lower noise and the fast transient response of the linear regulator. The LT1083 functions in the conventional fashion, supplying a regulated output at 7.5A capacity. The remaining components form the switched-mode dissipation limiting control. This loop forces the potential across the LT1083 to equal the 1.8V value of V_{REF} . The opto-isolator furnishes a convenient way to single end the differentially sensed voltage across the LT1083. When the input of the regulator (trace A, Figure 47) decays far enough, the LT1011 output (trace B) switches low, turning on Q1 (Q1 collector is trace C). This allows current flow (trace D) from the circuit input into the 10,000µF capacitor, raising the regulator's input voltage.

When the regulator input rises far enough, the comparator goes high, Q1 cuts off and the capacitor ceases charging. The MR1122 damps the flyback spike of the current limiting inductor. The 0.001µF-1M combination sets loop hysteresis at about 100mVp-p. This free-running oscillation control mode substantially reduces dissipation in the regulator, while preserving its performance. Despite changes in the input voltage, different regulated outputs or load shifts, the loop always ensures minimum dissipation in the regulator.

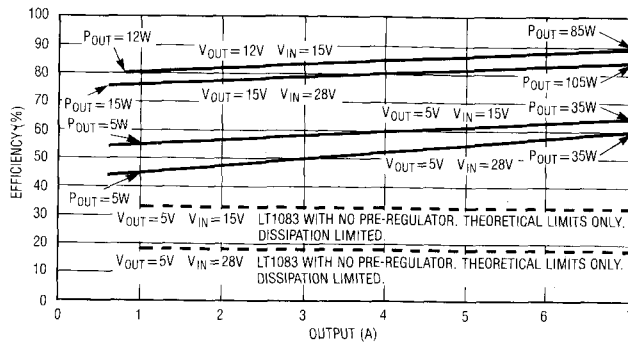


Figure 48. Efficiency vs Output Current for Figure 46 at Various Operating Points

Figure 48 plots efficiency at various operating points. Junction losses and the loop enforced 1.8V across the LT1083 are relatively small at high output voltages, resulting in good efficiency. Low output voltages do not fare as well, but compare very favorably to the theoretical data for the LT1083 with no pre-regulator. At the higher theoretical dissipation levels the LT1083 will shut down, precluding practical operation.

HIGH VOLTAGE CONVERTERS

High Voltage Converter — 1000V_{OUT}, Non-Isolated

Photomultiplier tubes, ion generators, gas based detectors, image intensifiers and other applications need high voltages. Converters frequently supply these potentials. Generally, the limitation on high voltage is transformer insulation breakdown. A transformer is almost always used because a simple inductor forces excessive voltages on the semiconductor switch. Figure 49's circuit, reminiscent of Figure 11's basic flyback configuration, is a 15V to 1000V_{OUT} converter. The LT1072 controls output by modulating the flyback energy into L1, forcing its feedback (FB) pin to 1.23V (the internal reference value). In this example loop compensation is heavily overdamped by the V_C pin capacitor. L1's damper network limits flyback spikes within the V_{SW} pin's 75V rating.

Fully Floating, 1000V_{OUT} Converter

Figure 50 is similar to Figure 49 but features a fully floating output. This provision allows the output to be referenced off system ground, often desirable for noise or

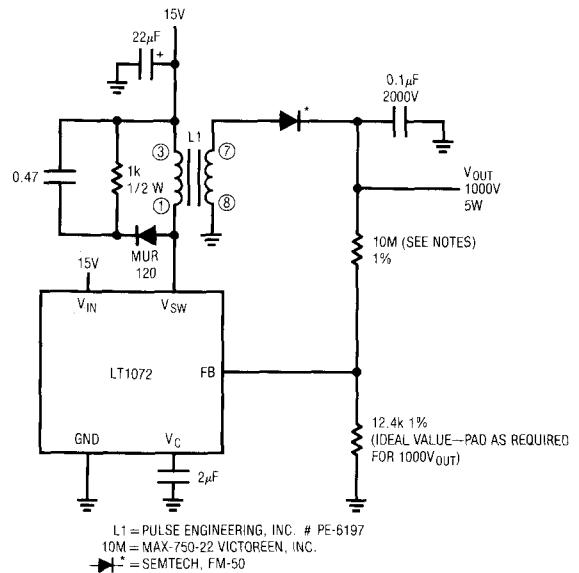


Figure 49. Non-Isolated 15V to 1000V Converter

biasing reasons. Basic loop action is as before, except that the LT1072's internal error amplifier and reference are replaced with galvanically isolated equivalents. Power for these components is bootstrapped from the output via source follower Q1 and its 2.2M ballast resistor. A1 and the LT1004, micropower components, minimize dissipation in Q1 and its ballast. Q1's gate bias, tapped from the output divider string, produces about 15V at its source. A1 compares the scaled divider output with the LT1004 reference. The error signal, A1's output, drives the optocoupler.

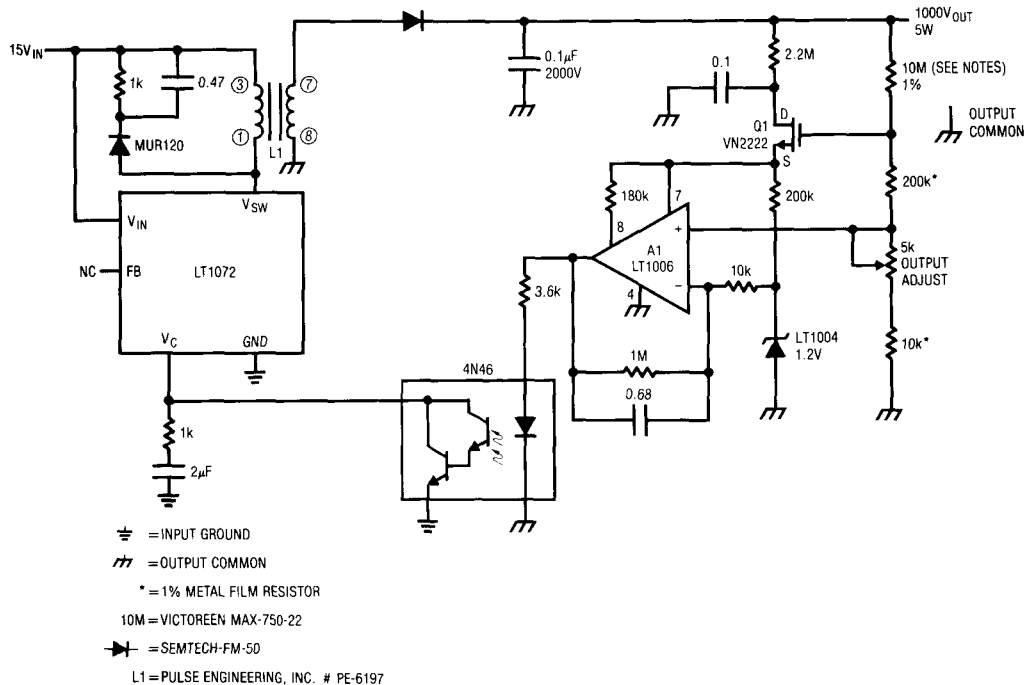


Figure 50. Isolated Output 15V to 1000V Converter

Photocurrent is kept low to save power. The optocoupler output pulls down on the V_C pin, closing a loop. Frequency compensation at the V_C pin and A1 stabilizes the loop.

The transformers isolated secondary and optical feedback produce a regulated, fully galvanically floating output. Common mode voltages of 2000V are acceptable.

20,000V_{CMV} Breakdown Converter

Figure 50's common mode breakdown limits are imposed by transformer and optocoupler restrictions. Isolation amplifiers, transducer measurement at high common mode voltages (e.g. winding temperature of a utility company transformer and ESD sensitive applications) require high breakdowns. Additionally, very precise floating measurements, such as signal conditioning for high impedance bridges, can require extremely low leakage to ground.

Achieving high common mode voltage capability with minimal leakage requires a different approach. Magnetics is usually considered the only approach for isolated transfer

of appreciable amounts of electrical energy. Transformer action is, however, achievable in the acoustic domain. Some ceramic materials will transfer electrical energy with galvanic isolation. Conventional magnetic transformers work on an electrical-magnetic-electrical basis using the magnetic domain for electrical isolation. The acoustic transformer uses an acoustic path to get isolation. The high voltage breakdown and low electrical conductance associated with ceramics surpasses isolation characteristics of magnetic approaches. Additionally, the acoustic transformer is simple. A pair of leads bonded to each end of the ceramic material forms the device. Insulation resistance exceeds $10^{12}\Omega$, with primary-secondary capacitances of 1-2pF. The material and its physical configuration determine its resonant frequency. The device may be considered as a high Q resonator, similar to a quartz crystal. As such, drive circuitry excites the device in the positive feedback path of a wideband gain element. Unlike a crystal, drive circuitry is arranged to pass substantial current through the ceramic, maximizing power into the transformer.

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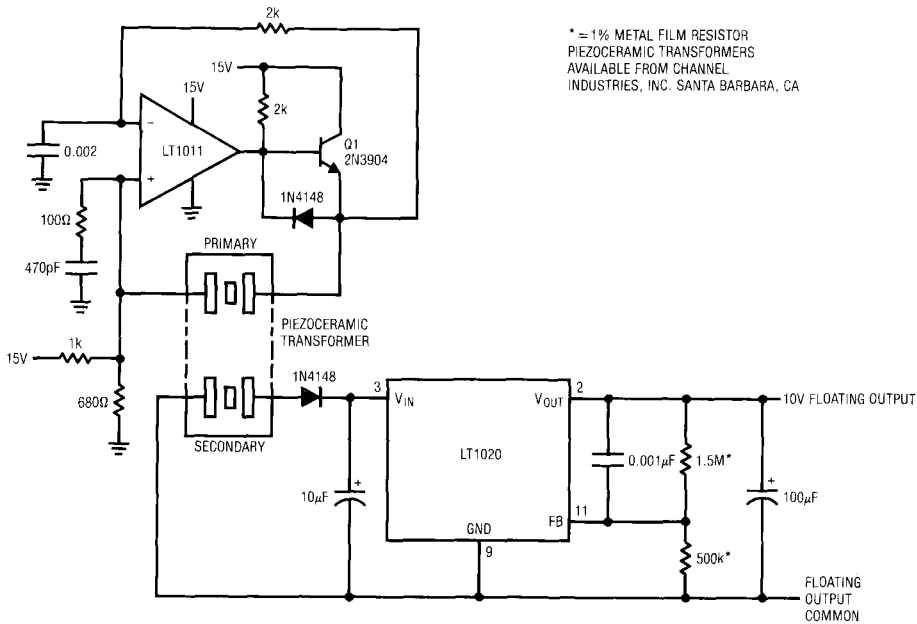


Figure 51. 15V to 10V Converter with 20,000V Isolation

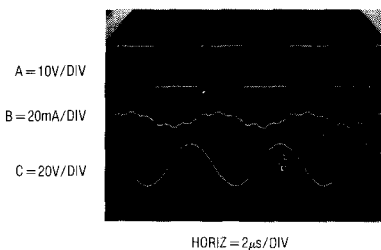


Figure 52. Waveforms for the 20,000V Isolation Converter

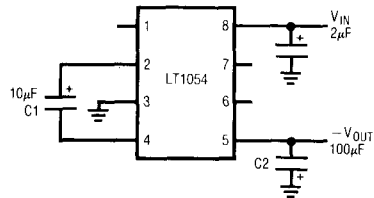


Figure 53. A Basic Switched Capacitor Converter

In Figure 51 the piezo-ceramic transformer is in the LT1011 comparators positive feedback loop. Q1 is an active pull-up for the LT1011, an open collector device. The 2k-0.002μF path biases the negative input. Positive feedback occurs at the transformers resonance, and oscillation commences (trace A, Figure 52 is Q1's emitter). Similar to quartz crystals, the transformer has significant harmonic and overtone modes. The 100Ω-470pF damper suppresses spurious oscillations and "mode hopping."

Drive current (trace B) approximates a sine wave, with peaking at the transitions. The transformer looks like a highly resonant filter to the resultant acoustic wave propagated in it. The secondary voltage (trace C) is sinusoidal. Additionally, the transformer has voltage gain. The diode and 10μF capacitor convert the secondary voltage to DC. The LT1020 low quiescent current regulator gives a stabilized 10V output. Output current for the circuit is a few milliamperes. Higher currents are possible with attention to transformer design.

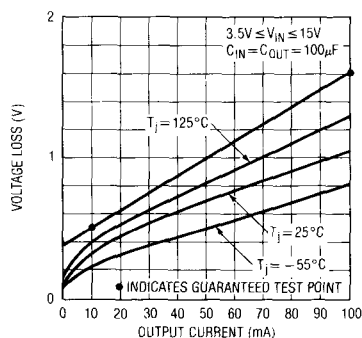


Figure 54. Losses for the Basic Switched Capacitor Converter

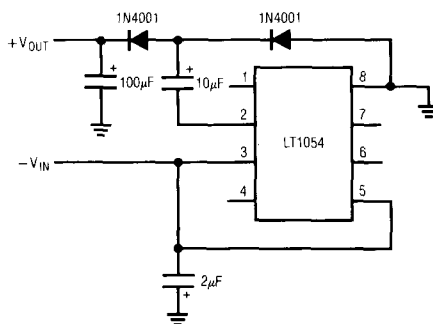


Figure 55. Switched Capacitor $-V_{IN}$ to $+V_{OUT}$ Converter

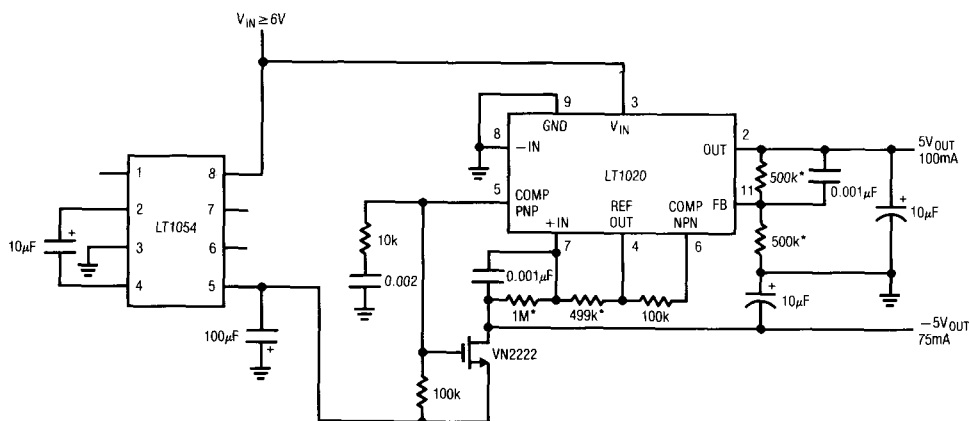


Figure 56. High Current Switched Capacitor 6V to $\pm 5\text{V}$ Converter

SWITCHED CAPACITOR BASED CONVERTERS

Inductors are used in converters because they can store energy. This stored magnetic energy, released and expressed in electrical terms, is the basis of converter operation. Inductors are not the only way to store energy with efficient release expressed in electrical terms. Capacitors store charge (already an electrical quantity) and as such, can be used as the basis for DC-DC conversion. Figure 53 shows how simple a switched capacitor based converter can be (the fundamentals of switched capacitor based conversion are presented in Appendix B, "Switched Capacitor Voltage Converters — How They Work"). The LT1054 provides clocked drive to charge C1. A second clock phase discharges C1 into C2. The internal switching

is arranged so C1 is "flipped" during the discharge interval, producing a negative output at C2. Continuous clocking allows C2 to charge to the same absolute value as C1. Junction and other losses preclude ideal results, but performance is quite good. This circuit will convert V_{IN} to $-V_{OUT}$ with losses shown in Figure 54. Adding an external resistive divider allows regulated output (see Appendix B).

With some additional steering diodes this configuration can effectively run "backwards" (Figure 55), converting a negative input to a positive output. Figure 56's variant gives low dropout linear regulation for 5V and -5V outputs from $6V_{IN}$. The LT1020 based dual output regulation

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scheme is adapted from Figure 8. Figure 57 uses diode steering to get voltage boost, providing $\approx 2V_{IN}$. Bootstrapping this configuration with Figure 54's basic circuit leads to Figure 58, which converts a 5V input to 12V and $-12V$ outputs. As might be expected output current capacity is traded for the voltage gain, although 25mA is still available. Figure 59, another boost converter, employs a dedicated version of Figure 58 (the LT1026) to get regulated $\pm 7V$ from a 6V input. The LT1026 generates unregulated $\pm 11V$ rails from the 6V input with the LT1020 and associated components (again, purloined from Figure 8) producing regulation. Current and boost capacity are reduced from Figure 58's levels, but the regulation and simplicity are noteworthy. Figure 60 combines the LT1054's clocked switched capacitor charging with classical diode voltage multiplication, producing positive and negative outputs. At no load $\pm 13V$ is available, falling to $\pm 10V$ with each side supplying 10mA.

High Power Switched Capacitor Converter

Figure 61 shows a high power switched capacitor converter with a 1A output capacity. Discrete devices permit high power operation.

The LTC1043 switched-capacitor building block provides non-overlapping complementary drive to the Q1-Q4 power MOSFETs. The MOSFETs are arranged so that C1 and C2 are alternately placed in series and then in parallel. During the series phase, the 12V supply current flows through both capacitors, charging them and furnishing load current. During the parallel phase, both capacitors deliver current to the load. Traces A and B, Figure 62, are the LTC1043-supplied drives to Q3 and Q4, respectively. Q1 and Q2 receive similar drive from pins 3 and 11. The diode-resistor networks provide additional non-overlapping drive characteristics, preventing simultaneous drive to the series-parallel phase switches. Normally, the output would be one-half of the supply voltage, but C1 and its associated components close a feedback loop, forcing the output to 5V. With the circuit in the series phase, the output (trace C) heads rapidly positive. When the output exceeds 5V, C1 trips, forcing the LTC1043's oscillator pin (trace D) high. This truncates the LTC1043's triangle wave oscillator cycle. The circuit is forced into the parallel phase and the output coasts down slowly until the next LTC1043 clock cycle begins. C1's output diode prevents the triangle down-slope from being affected and the 100pF capacitor provides sharp transitions. The loop regulates

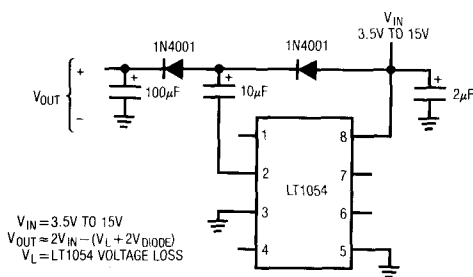


Figure 57. Voltage Boost Switched Capacitor Converter

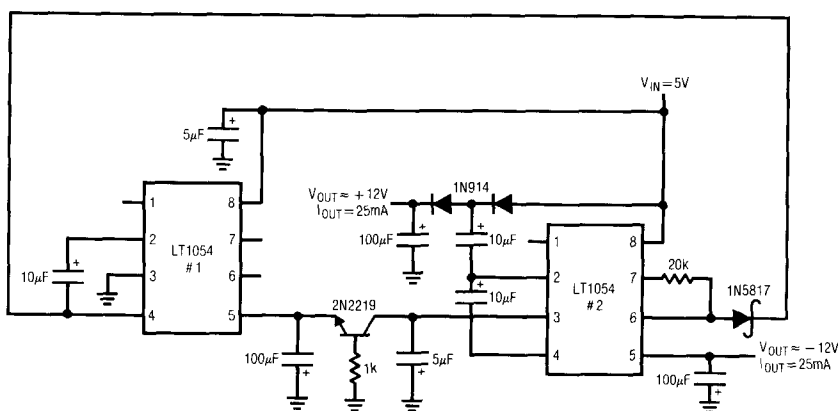


Figure 58. Switched Capacitor 5V to $\pm 12V$ Converter

the output to 5V by feedback controlling the turn-off point of the series phase. The circuit constitutes a large scale switched-capacitor voltage divider which is never allowed to complete a full cycle. The high transient currents are easily handled by the power MOSFETs and overall efficiency is 83%.

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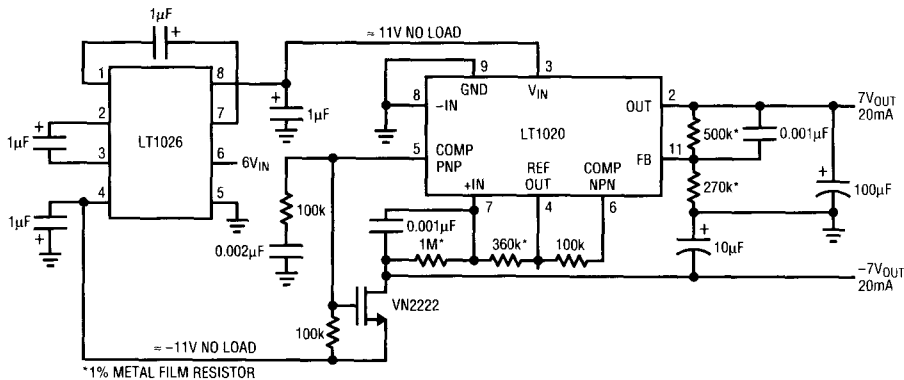


Figure 59. Switched Capacitor Based 6V to ±7V Converter

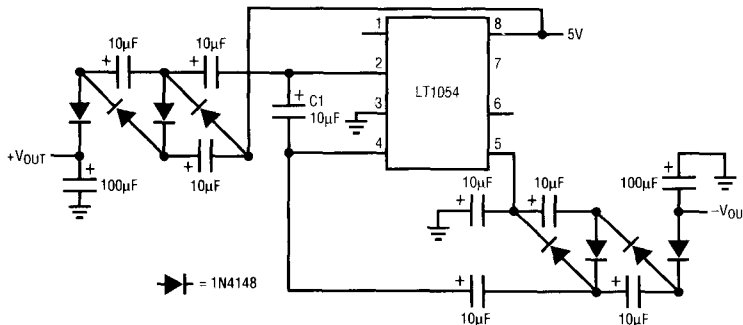


Figure 60. Switched Capacitor Charge Pump Based Voltage Multiplier

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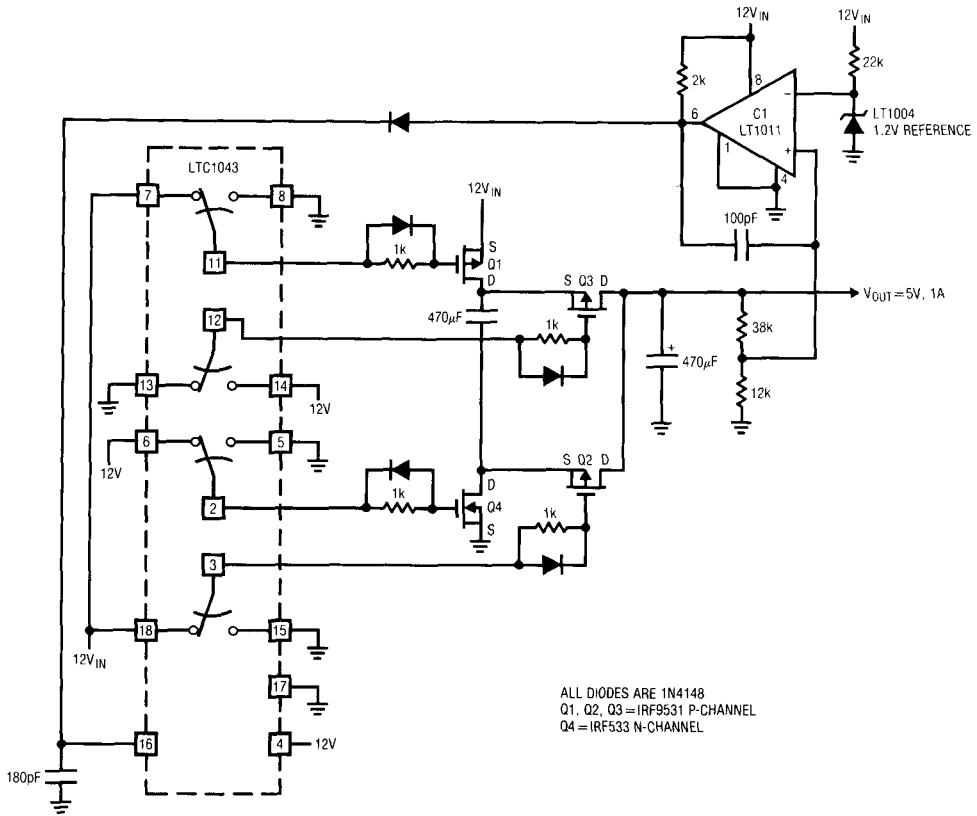


Figure 61. High Power Switched Capacitor Converter

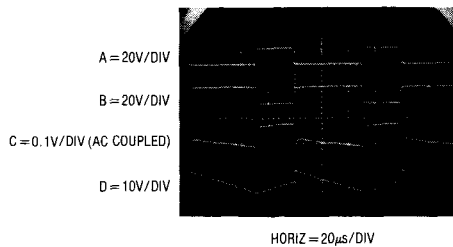


Figure 62. Waveforms for Figure 61

APPENDIX A

The 5V to $\pm 15V$ Converter — A Special Case

Five volt logic supplies have been standard since the introduction of DTL logic over twenty years ago. Preceding and during DTL's infancy the modular amplifier houses standardized on $\pm 15V$ rails. As such, popular early monolithic amplifiers also ran from $\pm 15V$ rails (additional historical perspective on amplifier power supplies appears in AN-11's appended section, "Linear Power Supplies—Past, Present, and Future"). The 5V supply offered process, speed and density advantages to digital IC's. The $\pm 15V$ rails provided a wide signal processing range to the analog components. These disparate needs defined power supply requirements for mixed analog-digital systems at 5V and $\pm 15V$. In systems with large analog component populations the $\pm 15V$ supply was and still is usually derived from the AC line. Such line derived $\pm 15V$ power becomes distinctly undesirable in predominantly digital systems. The inconvenience, difficulty and cost of distributing analog rails in heavily digital systems makes local generation attractive. 5V to $\pm 15V$ DC-DC converters were developed to fill this need and have been with us for about as long as 5V logic.

Figure A1 is a conceptual schematic of a typical converter. The 5V input is applied to a self-oscillating configuration composed of transistors, a transformer and a biasing network. The transistors conduct out of phase, switching (Figure A2, traces A and C are Q1's collector and base, while traces B and D are Q2's collector and base) each time the transformer saturates.¹ Transformer saturation causes a quickly rising, high current to flow (trace E). This current spike, picked up by the base drive winding, switches the transistors. Transformer current abruptly drops and then slowly rises until saturation again forces switching. This alternating operation sets transistor duty cycle at 50%. The transformer's secondary is rectified, filtered and regulated to produce the outputs.

This configuration has a number of desirable features. The complementary high frequency (typically 20kHz) square wave drive makes efficient use of the transformer and allows relatively small filter capacitors. The self-oscillating primary drive tends to collapse under overload, providing desirable short circuit characteristics. The transistors switch in saturated mode, aiding efficiency. This hard switching, combined with the transformer's deliberate saturation does, however, have a drawback. During the saturation interval a significant, high frequency current

Note 1: This type of converter was originally described by Royer, et al. See References.

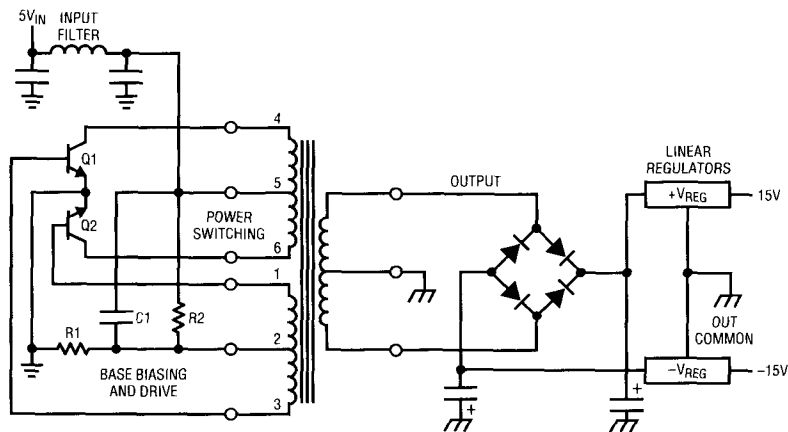


Figure A1. Conceptual Schematic of a Typical 5V to $\pm 15V$ Converter

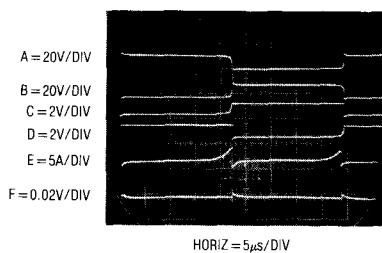


Figure A2. Typical 5V to ±15V Saturating Converters Waveforms

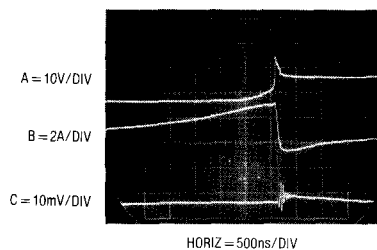


Figure A3. Switching Details of Saturating Converter

spike is generated (again, trace E). This spike causes noise to appear at the converter outputs (trace F is the AC coupled 15V output). Additionally, it pulls significant current from the 5V supply. The converter's input filter partially smooths the transient, but the 5V supply is usually so noisy the disturbance is acceptable. The spike at the output, typically 20mV high, is a more serious problem. Figure A3 is a time and amplitude expansion of Figure A2's traces B, E and F. It clearly shows the relationship between transformer current (trace B, Figure A3), transistor collector voltage (trace A, Figure A3) and the output spike (trace C, Figure A3). As transformer current rises the transistor starts coming out of saturation. When current rises high enough the circuit switches, causing the characteristic noise spike. This condition is exacerbated by the other transistors concurrent switching, causing both ends of the transformer to simultaneously conduct current to ground.

Selection of transistors, output filters and other techniques can reduce spike amplitude, but the converter's inherent operation ensures noisy outputs.

This noisy operation can cause difficulties in precision analog systems. IC power supply rejection at the high harmonic spike frequency is low, and analog system errors frequently result. A 12-bit SAR A-to-D converter is a good candidate for such spike-noise caused problems. Sampled data IC's such as switched capacitor filters and chopper amplifiers often show apparent errors which are due to spike induced problems. "Simple" DC circuits can exhibit baffling "instabilities" which in reality are spike caused problems masquerading as DC shifts.

The drive scheme is also responsible for high quiescent current consumption. The base biasing always supplies

full drive, ensuring transistor saturation under heavy loading but wasting power at lighter loads. Adaptive bias schemes will mitigate this problem, but increase complexity and almost never appear in converters of this type.

The noise problem is, however, the main drawback of this approach to 5V to ±15V conversion. Careful design, layout, filtering and shielding (for radiated noise) can reduce noise, but cannot eliminate it.

Some techniques can help these converters with the noise problem. Figure A4 uses a "bracket pulse" to warn the powered system when a noise pulse is about to occur. Ostensibly, noise sensitive operations are not carried out during the bracket pulse interval. The bracket pulse (trace A, Figure A5) drives a delayed pulse generator which triggers (trace B) the flip-flop. The flip-flop output biases the switching transistors (Q1 collector is trace C). The output noise spike (trace D) occurs within the bracket pulse interval. The clocked operation can also prevent transformer saturation, offering some additional noise reduction. This scheme works well, but presumes the powered system can tolerate periodic intervals where critical operations cannot take place.

In Figure A6 the electronic tables are turned. Here, the host system silences the converter when low noise is required. Traces B and C are base and collector drives for one transistor while traces D and E show drive to the other device. The collector peaking is characteristic of saturating converter operation. Output noise appears on trace F. Trace A's pulse gates off the converter's base bias, stopping switching. This occurs just past the 6th vertical division. With no switching, the output linear regulator sees the filter capacitor's pure DC and noise disappears.

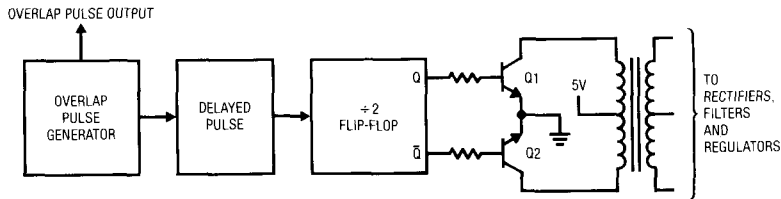


Figure A4. Overlap Generator Provides a “Bracket Pulse” Around Noise Spikes

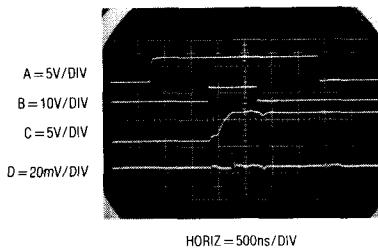


Figure A5. Waveforms for the Bracket Pulse Based Converter

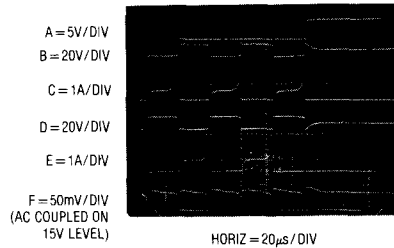


Figure A6. Detail of the Strobed Operation Converter

This arrangement also works nicely but assumes the control pulse can be conveniently generated by the system. It also requires larger filter capacitors to supply power during the low noise interval.

Other methods involve clock synchronization, timing skewing and other schemes which prevent noise spikes from coinciding with sensitive operations. While useful, none of these arrangements offer the flexibility of the inherently noise free converters shown in the text.

APPENDIX B

Switched Capacitor Voltage Converters — How They Work

To understand the theory of operation of switched capacitor converters, a review of a basic switched capacitor building block is helpful.

In Figure B1, when the switch is in the left position, capacitor C1 will charge to voltage V1. The total charge on C1 will be $Q1 = C1V1$. The switch then moves to the right, discharging C1 to voltage V2. After this discharge time, the charge on C1 is $Q2 = C1V2$. Note that charge has been transferred from the source, V1, to the output, V2. The amount of charge transferred is:

$$Q = Q1 - Q2 = C1(V1 - V2)$$

If the switch is cycled f times per second, the charge transfer per unit time (i.e., current) is:

$$I = fQ = fC1(V1 - V2)$$

To obtain an equivalent resistance for the switched-capacitor network we can rewrite this equation in terms of voltage and impedance equivalence:

$$I = \frac{V1 - V2}{(1/fC1)} = \frac{V1 - V2}{R_{EQUIV}}$$

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A new variable, R_{EQUIV} , is defined such that $R_{EQUIV} = 1/fC1$. Thus, the equivalent circuit for the switched capacitor network is as shown in Figure B2. The LT1054 and other switched capacitor converters have the same switching action as the basic switched capacitor building block. Even though this simplification doesn't include finite switch on-resistance and output voltage ripple, it provides an intuitive feel for how the device works.

These simplified circuits explain voltage loss as a function of frequency. As frequency is decreased, the output impedance will eventually be dominated by the $1/fC1$ term and voltage losses will rise.

Note that losses also rise as frequency increases. This is caused by internal switching losses which occur due to some finite charge being lost on each switching cycle. This charge loss per-unit-cycle, when multiplied by the switching frequency, becomes a current loss. At high frequency this loss becomes significant and voltage losses again rise.

The oscillators of practical converters are designed to run in the frequency band where voltage losses are at a mini-

mum. Figure B3 shows the block diagram of the LT1054 switched capacitor converter.

The LT1054 is a monolithic, bipolar, switched capacitor voltage converter and regulator. It provides higher output current than previously available converters with significantly lower voltage losses. An adaptive switch drive scheme optimizes efficiency over a wide range of output currents. Total voltage loss at 100mA output current is typically 1.1V. This holds true over the full supply voltage range of 3.5V to 15V. Quiescent current is typically 2.5mA.

The LT1054 also provides regulation. By adding an external resistive divider, a regulated output can be obtained. This output will be regulated against changes in input voltage and output current. The LT1054 can also be shut down by grounding the feedback pin. Supply current in shutdown is less than $100\mu A$.

The internal oscillator of the LT1054 runs at a nominal frequency of 25kHz. The oscillator pin can be used to adjust the switching frequency, or to externally synchronize the LT1054.

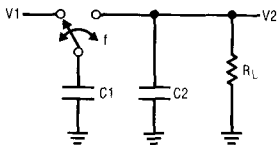


Figure B1. Switched Capacitor Building Block

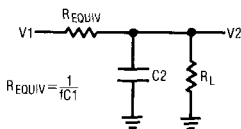


Figure B2. Switched Capacitor Equivalent Circuit

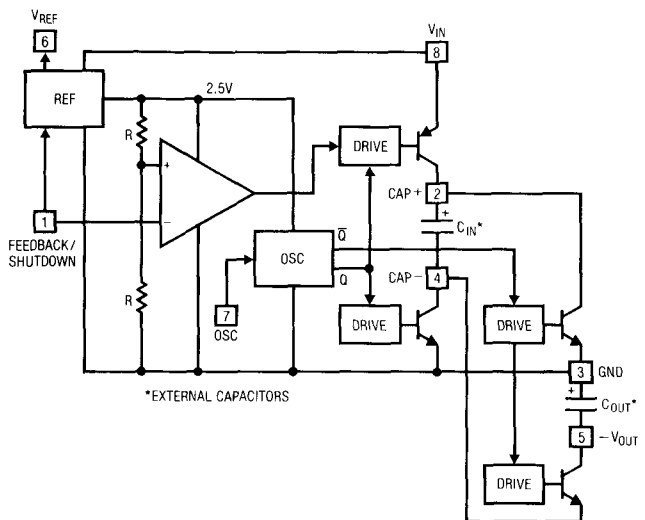


Figure B3. LT1054 Switched Capacitor Converter Block Diagram

APPENDIX C

Physiology of the LT1070

The LT1070 is a current-mode switcher. This means that switch duty cycle is directly controlled by switch current rather than by output voltage. Referring to Figure C1, the switch is turned on at the start of each oscillator cycle. It is turned off when switch current reaches a predetermined level. Control of output voltage is obtained by using the output of a voltage-sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike ordinary switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at mid-frequencies in the energy storage inductor. This greatly simplifies closed loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output

overload or short conditions. A low dropout internal regulator provides a 2.3V supply for all internal circuitry on the LT1070. This low dropout design allows input voltage to vary from 3V to 60V with virtually no change in device performance. A 40kHz oscillator is the basic clock for all internal timing. It turns on the output switch via the logic and driver circuitry. Special adaptive antisat circuitry detects onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

A 1.2V bandgap reference biases the positive input of the error amplifier. The negative input is brought out for output voltage sensing. This feedback pin has a second function; when pulled low with an external resistor, it programs

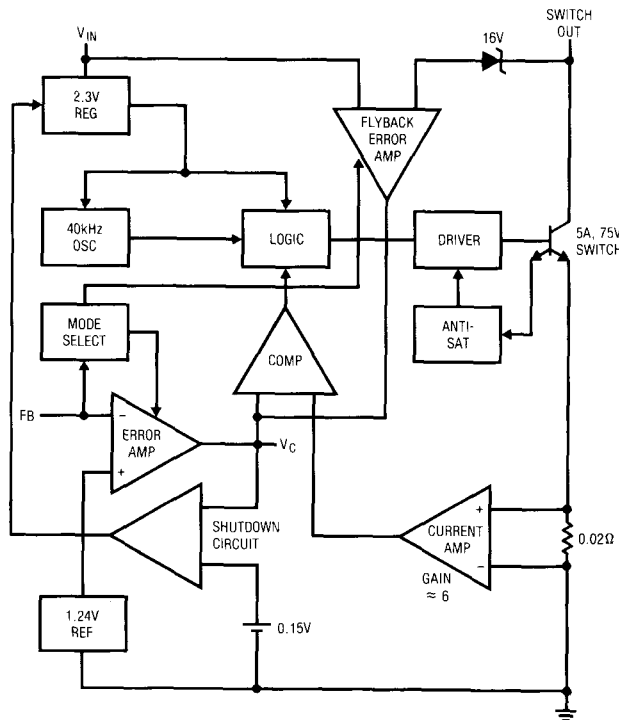


Figure C1. LT1070 Internal Details

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the LT1070 to disconnect the main error amplifier output and connects the output of the flyback amplifier to the comparator input. The LT1070 will then regulate the value of the flyback pulse with respect to the supply voltage. This flyback pulse is directly proportional to output voltage in the traditional transformer-coupled flyback topology regulator. By regulating the amplitude of the flyback pulse the output voltage can be regulated with no direct connection between input and output. The output is fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings. A special delay network inside the LT1070 ignores the leakage inductance spike at the leading edge of the flyback pulse to improve output regulation.

The error signal developed at the comparator input is brought out externally. This pin (V_C) has four different functions. It is used for frequency compensation, current limit adjustment, soft-starting, and total regulator shutdown. During normal regulator operation this pin sits at a voltage between 0.9V (low output current) and 2.0V (high output current). The error amplifiers are current output (gm) types, so this voltage can be externally clamped for adjusting current limit. Likewise, a capacitor-coupled external clamp will provide soft-start. Switch duty cycle goes to zero if the V_C pin is pulled to ground through a diode, placing the LT1070 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown with only 50 μ A supply current for shutdown circuitry biasing. For more details, see Linear Technology Application Note AN-19, pages 4-8.

APPENDIX D

Inductor Selection for Flyback Converters

A common problem area in DC-DC converter design is the inductor, and the most common difficulty is saturation. An inductor is saturated when it cannot hold any more magnetic flux. As an inductor arrives at saturation it begins to look more resistive and less inductive. Under these conditions current flow is limited only by the inductor's DC copper resistance and the source capacity. This is why saturation often results in destructive failures.

While saturation is a prime concern, cost, heating, size, availability and desired performance are also significant. Electromagnetic theory, although applicable to these issues, can be confusing, particularly to the non-specialist.

Practically speaking, an empirical approach is often a good way to address inductor selection. It permits real time analysis under actual circuit operating conditions using the ultimate simulator — a breadboard. If desired, inductor design theory can be used to augment or confirm experimental results.

Figure D1 shows a typical flyback based converter utilizing the LT1070 switching regulator. A simple approach may be employed to determine the appropriate inductor. A very useful tool is the #845 inductor kit¹ shown in Figure D2. This kit provides a broad range of inductors for evaluation in test circuits such as Figure D1.

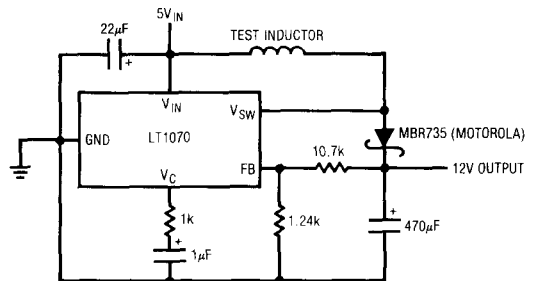


Figure D1. Basic LT1070 Flyback Converter Test Circuit

¹ Available from Pulse Engineering, Inc., P.O. Box 12235, San Diego, CA 92112, 619-268-2400

Figure D3 was taken with a $450\mu\text{H}$ value, high core capacity inductor installed. Circuit operating conditions such as input voltage and loading are set at levels appropriate to the intended application. Trace A is the LT1070's V_{SW} pin voltage while trace B shows its current. When V_{SW} pin voltage is low, inductor current flows. The high inductance means current rises relatively slowly, resulting in the shallow slope observed. Behavior is linear, indicating no saturation problems. In Figure D4, a lower value unit with equivalent core characteristics is tried. Current rise is steeper, but saturation is not encountered. Figure D5's selected inductance is still lower, although core characteristics are similar. Here, the current ramp is quite pronounced, but well controlled. Figure D6 brings some informative surprises. This high value unit, wound on a low capacity core, starts out well but heads rapidly into saturation, and is clearly unsuitable.

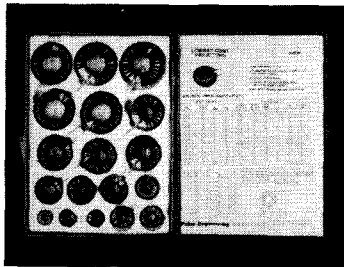


Figure D2. Model 845 Inductor Selection Kit from Pulse Engineering, Inc. (Includes 18 Fully Specified Devices)

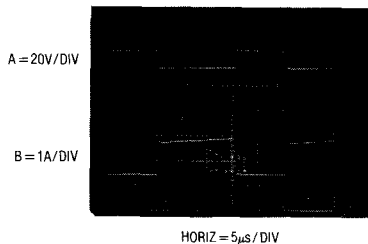


Figure D3. Waveforms for $450\mu\text{H}$, High Capacity Core Unit

The described procedure narrows the inductor choice within a range of devices. Several were seen to produce acceptable electrical results, and the "best" unit can be further selected on the basis of cost, size, heating and other parameters. A standard device in the kit may suffice, or a derived version can be supplied by the manufacturer.

Using the standard products in the kit minimizes specification uncertainties, accelerating the dialogue between user and inductor vendor.

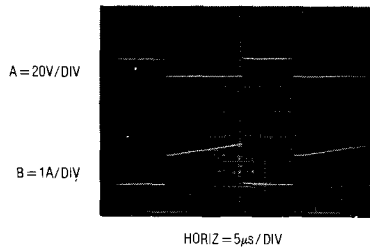


Figure D4. Waveforms for $170\mu\text{H}$, High Capacity Core Unit

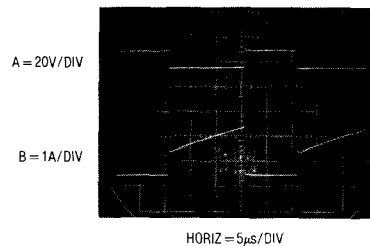


Figure D5. Waveforms for $55\mu\text{H}$, High Capacity Core Unit

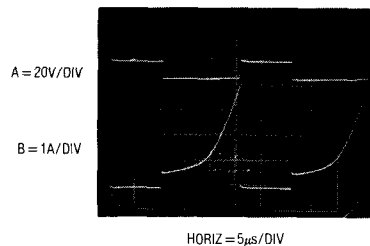


Figure D6. Waveforms for $500\mu\text{H}$, Low Capacity Core Inductor (Note Saturation Effects)

APPENDIX E

Optimizing Converters for Efficiency

Squeezing the utmost efficiency out of a converter is a complex, demanding design task. Efficiency exceeding 80–85% requires some combination of finesse, witchcraft and just plain luck. Interaction of electrical and magnetic terms produces subtle effects which influence efficiency. A detailed, generalized method for obtaining maximum converter efficiency is not readily described but some guidelines are possible.

Losses fall into several loose categories including junction, ohmic, drive, switching, and magnetic losses.

Semiconductor junctions produce losses. Diode drops increase with operating current and can be quite costly in low voltage output converters. A 700mV drop in a 5V output converter introduces more than 10% loss. Schottky devices will cut this nearly in half, but loss is still appreciable. Germanium (rarely used) is lower still, but switching losses negate the low DC drop at high speeds. In very low power converters Germanium's reverse leakage may be equally oppressive. Synchronously switched rectification is more complex, but can sometimes simulate a more efficient diode (see text Figure 32). When evaluating such a scheme remember to include both AC and DC drive losses in efficiency estimates. DC losses include base or gate current in addition to DC consumption in any driver stage. AC losses might include the effects of gate (or base) capacitance, transition region dissipation (the switch spends some time in its linear region) and power lost due to timing skew between drive and actual switch action.

Transistor saturation losses are also a significant term. Channel and collector-emitter saturation losses become increasingly significant as operating voltages decrease. The most obvious way to minimize these losses is to select low saturation components. In some cases this will work, but remember to include the drive losses (usually higher) for lower saturation devices in overall loss estimates. Actual losses caused by saturation effects and diode drops is sometimes difficult to ascertain. Changing duty cycles and time variant currents make determination tricky. One simple way to make relative loss judgements is to measure device temperature rise. Appropriate tools

here include thermal probes and (at low voltages) the perhaps more readily available human finger. At lower power (e.g., less dissipation, even though loss percentage may be as great) this technique is less effective. Sometimes deliberately adding a known loss to the component in question and noting efficiency change allows loss determination.

Ohmic losses in conductors are usually only significant at higher currents. "Hidden" ohmic losses include socket and connector contact resistance and equivalent series resistance (ESR) in capacitors. ESR generally drops with capacitor value and rises with operating frequency, and should be specified on the capacitor data sheet. Consider the copper resistance of inductive components. It is often necessary to evaluate trade-offs of an inductor's copper resistance vs magnetic characteristics.

Drive losses were mentioned, and are important in obtaining efficiency. MOSFET gate capacitance draws substantial AC drive current per cycle, implying higher average currents as frequency goes up. Bipolar devices have lower capacitance, but DC base current eats power. Large area devices may appear attractive for low saturation, but evaluate drive losses carefully. Usually, large area devices only make sense when operating at a significant percentage of rated current. Drive stages should be thought out with respect to efficiency. Class A type drives (e.g., resistive pull-up or pull-down) are simple and fast, but wasteful. Efficient operation usually requires active source-sink combinations with minimal cross conduction and biasing losses.

Switching losses occur when devices spend significant amounts of time in their linear region relative to operating frequency. At higher repetition rates transition times can become a substantial loss source. Device selection and drive techniques can minimize these losses.

Magnetics design also influences efficiency. Design of inductive components is well beyond the scope of this appended section, but issues include core material selection, wire type, winding techniques, size, operating frequency, current levels, temperature and other issues.

Some of these topics are discussed in LTC Application Note AN-19, but there is no substitute for access to a skilled magnetics specialist. Fortunately, the other categories mentioned usually dominate losses, allowing good

efficiencies to be obtained with standard magnetics. Custom magnetics are usually only employed after circuit losses have been reduced to lowest practical levels.

APPENDIX F

Instrumentation for Converter Design

Instrumentation for DC-DC converter design should be selected on the basis of *flexibility*. Wide bandwidths, high resolution and computational sophistication are valuable features, but are usually not required for converter work. Typically, converter design requires simultaneous observation of many circuit events at relatively slow speeds. Single ended and differential voltage and current signals are of interest, with some measurements requiring fully floating inputs. Most low level measurement involves AC signals and is accommodated with a high sensitivity plug-in. Other situations call for observation of small, slowly changing (e.g., 0.1Hz to 10Hz) events on top of DC levels. This range falls outside the AC coupled cut-off of most oscilloscopes, mandating differential DC nulling or "slide-back" plug-in capability. Other requirements include high impedance probes, filters and oscilloscopes with very versatile triggering and multi-trace capability. In our converter work we have found a number of particularly noteworthy instruments in several categories.

PROBES

For many measurements standard 1x and 10x scope probes are fine. In most cases the ground strap may be used, but low level measurements, particularly in the presence of wideband converter switching noise, should be taken with the shortest possible ground return. A variety of probe tip grounding accessories are available, and are usually supplied with good quality probes (see Figure F1). In some cases, directly connecting the breadboard to the 'scope may be necessary (Figure F2).

Wideband FET probes are not normally needed, but a moderate speed, high input impedance buffer probe is quite useful. Many converter circuits, especially micropower designs, require monitoring of high impedance nodes. The 10M Ω loading of standard 10x probes usually suffices, but sensitivity is traded away. 1x probes retain

sensitivity, but introduce heavier loading. Figure F3 shows an almost absurdly simple, but useful, circuit which greatly aids probe loading problems. The LT1022 high speed FET op amp drives an LT1010 buffer. The LT1010's output allows cable and probe driving and also biases the circuit's input shield. This bootstraps the input capacitance, reducing its effect. DC and AC errors of this circuit are low enough for almost all converter work, with enough bandwidth for most circuits. Built into a small enclosure with its own power supply, it can be used ahead of a 'scope or DVM with good results. Pertinent specifications appear in the diagram.

Figure F4 shows a simple probe filter which sets high and low bandwidth restrictions. This circuit, placed in series with the 'scope input, is useful for eliminating switching artifacts when observing circuit nodes.

An *isolated* probe allows fully floating measurements, even in the presence of high common mode voltages. It is often desirable to look across floating points in a circuit. The ability to directly observe an ungrounded transistor's saturation characteristics or monitor waveforms across a floating shunt makes this probe valuable. One probe, the Signal Acquisition Technologies, Inc. Model SL-10, has 10MHz bandwidth and 600V common mode capability.

Current probes are an indispensable tool in converter design. In many cases current waveforms contain more valuable information than voltage measurements. The clip-on types are quite convenient. Hall effect based versions respond down to DC, with bandwidths of 50MHz. Transformer types are faster, but roll off below several hundred cycles (Figure F5). Both types have saturation limitations which, when exceeded, cause odd results on the CRT, confusing the unwary. The Tektronix P6042 (and the more recent AM503) Hall type and P6022/134 transformer based type give excellent results. The Hewlett-Packard 428B

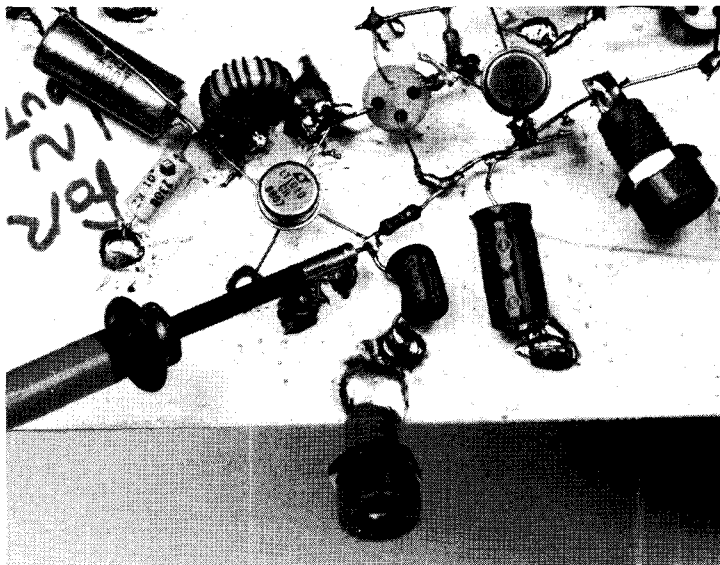


Figure F1. Proper Probing Technique for Low Level Measurements in the Presence of High Frequency Noise

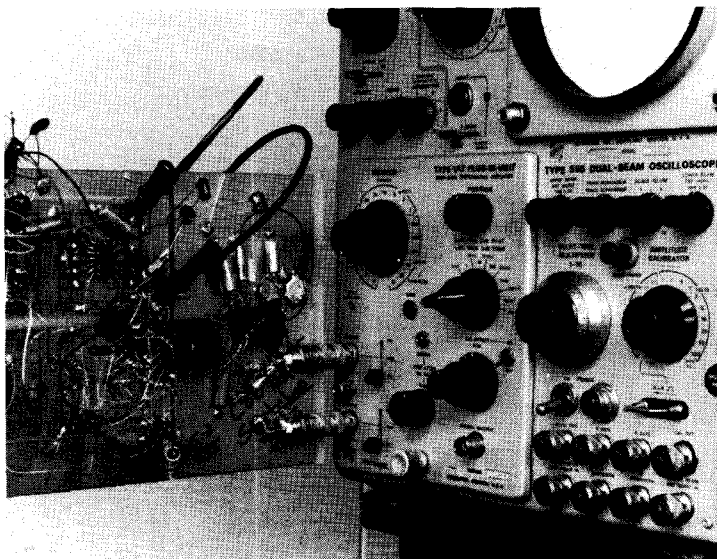


Figure F2. Direct Connections to the Oscilloscope Give Best Low Level Measurements. Note Ground Reference Connection to the Differential Plug-In's Negative Input.

clip-on current probe responds from DC to only 400Hz, but features 3% accuracy over a 100 μ A to 10A range. This instrument, useful for determining efficiency and quiescent current, eliminates shunt caused measurement errors.

OSCILLOSCOPES AND PLUG-INS

The oscilloscope plug-in combination is an important choice. Converter work almost demands multi-trace capability. Two channels are barely adequate, with four far preferable. The Tektronix 2445/6 offers four channels, but two have limited vertical capability. The Tektronix 547 (and

the more modern 7603), equipped with a type 1A4 (2 dual trace 7A18's required for the 7603) plug-in, has four full capability input channels with flexible triggering and superb CRT trace clarity. This instrument, or its equivalent, will handle a wide variety of converter circuits with minimal restrictions. The Tektronix 556 offers an extraordinary array of features valuable in converter work. This dual beam instrument is essentially two fully independent oscilloscopes sharing a single CRT. Independent vertical, horizontal and triggering permit detailed display of almost any converters operation. Equipped with two type 1A4

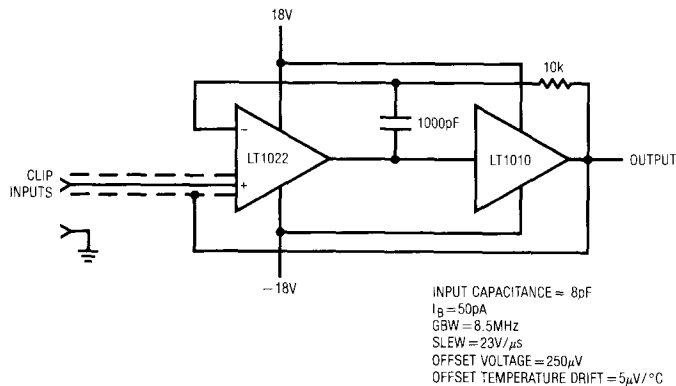


Figure F3. A Simple High Impedance Probe

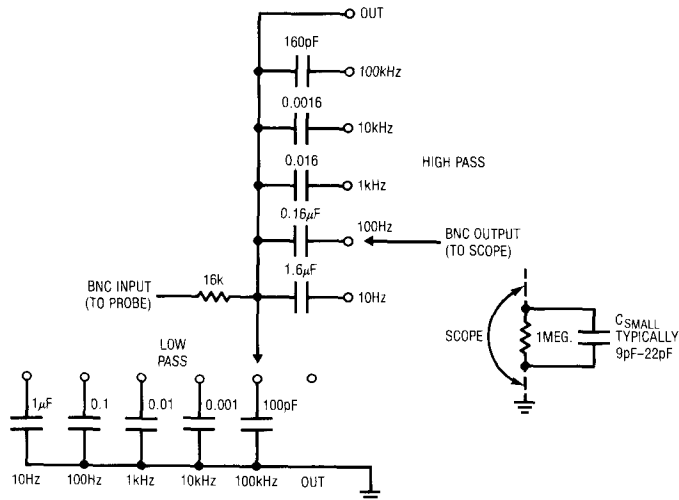


Figure F4. Oscilloscope Filter

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plug-in's, the 556 will display eight real time inputs. The independent triggering and time bases allow stable display of asynchronous events. Cross beam triggering is also available, and the CRT has exceptional trace clarity.

Two oscilloscope plug-in types merit special mention. At low level, a high sensitivity differential plug-in is indispensable. The Tektronix 1A7 and 7A22 feature $10\mu\text{V}$

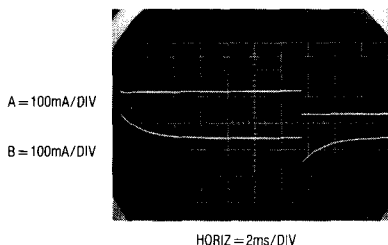


Figure F5. Hall (Trace A) and Transformer (Trace B) Based Current Probes Responding to Low Frequency

APPENDIX G

The Magnetics Issue

Magnetics is probably the most formidable issue in converter design. Design and construction of suitable magnetics is a difficult task, particularly for the non-specialist. It is our experience that the majority of converter design problems are associated with magnetics requirements. This consideration is accentuated by the fact that most converters are employed by non-specialists. As a purveyor of

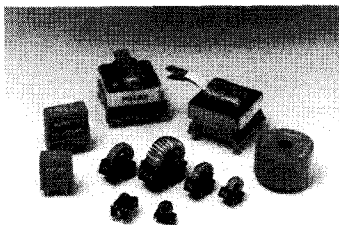


Figure G1. Magnetics for LTC Applications Circuits are Designed and Supplied as Standard Product by Pulse Engineering, Inc.

sensitivity, although bandwidth is limited to 1MHz. The units also have selectable high and low pass filters and good high frequency common mode rejection. Tektronix types W, 1A5 and 7A13 are differential comparators. They have calibrated DC nulling ("slideback") sources, allowing observation of small, slowly moving events on top of common mode DC.

VOLTMETERS

Almost any DVM will suffice for converter work. It should have current measurement ranges and provision for battery operation. The battery operation allows floating measurements and eliminates possible ground loop errors. Additionally, a *non-electronic* (VOM) voltmeter (e.g., Simpson 260, Triplett 630) is a worthwhile addition to the converter design bench. Electronic voltmeters are occasionally disturbed by converter noise, producing erratic readings. A VOM contains no active circuitry, making it less susceptible to such effects.

switching power IC's we incur responsibility towards addressing the magnetics issue (our publicly spirited attitude is, admittedly, capitalistically influenced). As such, it is LTC's policy to use off-the-shelf magnetics in our circuits. In some cases, available magnetics serve a particular design. In other situations the magnetics have been specially designed, assigned a part number and made available as standard product. In these endeavors our magnetics supplier and partner is;

Pulse Engineering, Inc.
P.O. Box 12235
7250 Convoy Court
San Diego, California 92112
619-268-2400

In many circumstances a standard product is suitable for production. Other cases may require modifications or changes which Pulse Engineering can provide. Hopefully, this approach serves the needs of all concerned.

Switching Regulator Circuit Collection

Brian Huffman

Switching regulators are of universal interest. Linear Technology has made a major effort to address this topic. A catalog of circuits has been compiled so that a design engineer can swiftly determine which converter type is best. This catalog serves as a visual index to be browsed through for a specific or general interest.

The catalog is organized so that converter topologies can be easily found. There are 12 basic circuit categories: Battery, Boost, Buck, Buck-Boost, Flyback, Forward, High Voltage, Multi-Output, Off-Line, Pre-Regulator, Switched Capacitor, and Telecom. Additional circuit information can be located in the references listed in the index. The reference works as follows, i.e., AN8, Page 2 = Application Note 8, Page 2; LTC1044 DS = LTC1044 data sheet; DN17 = Design Note 17.

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SUGGESTED READING

Pulse Engineering Catalog — Switching Magnetics

Pulse Engineering, Inc.

P.O. Box 12235

San Diego, CA 92112

Phone: 619-268-2400

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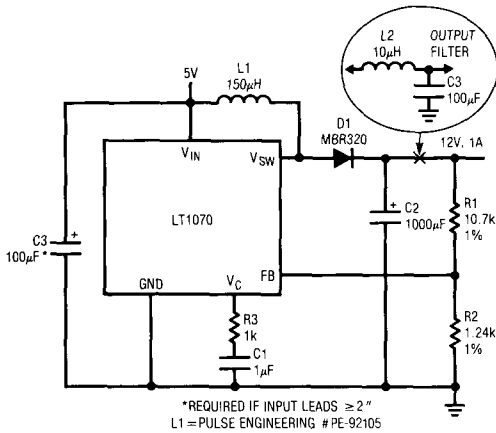


Figure 1. Boost Converter (5V to 12V)

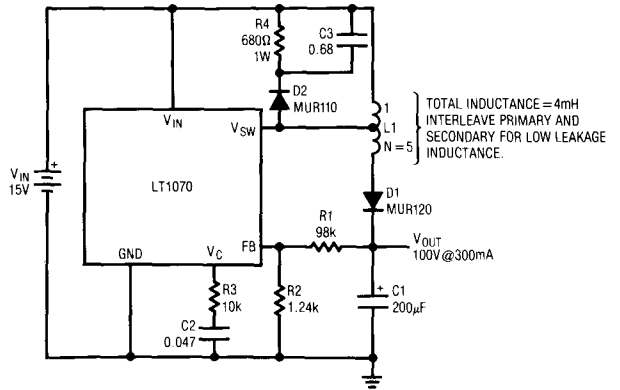


Figure 2. Voltage Boosted Boost Converter (15V to 100V)

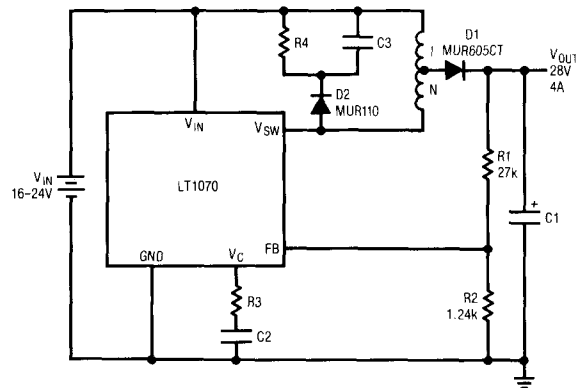


Figure 3. Current Boosted Boost Converter (16V-24V to 28V)

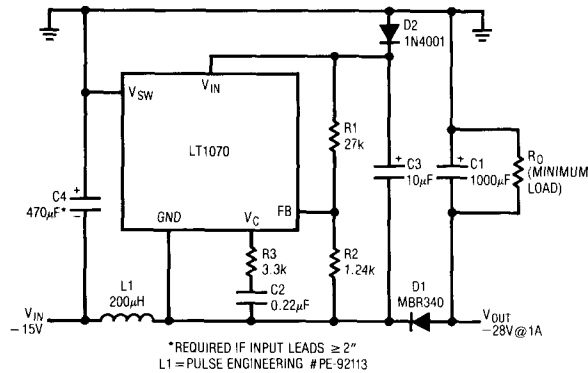


Figure 4. Negative Boost Regulator (-15V to -28V)

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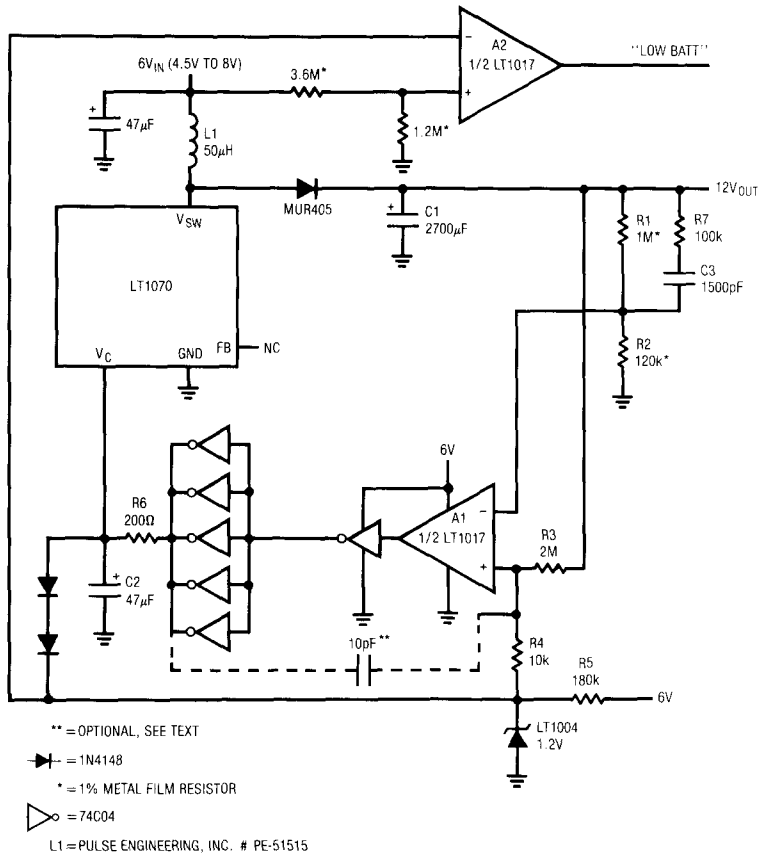


Figure 5. 2 Amp Converter with 150µA Quiescent Current (4.5V-8V to 12V)

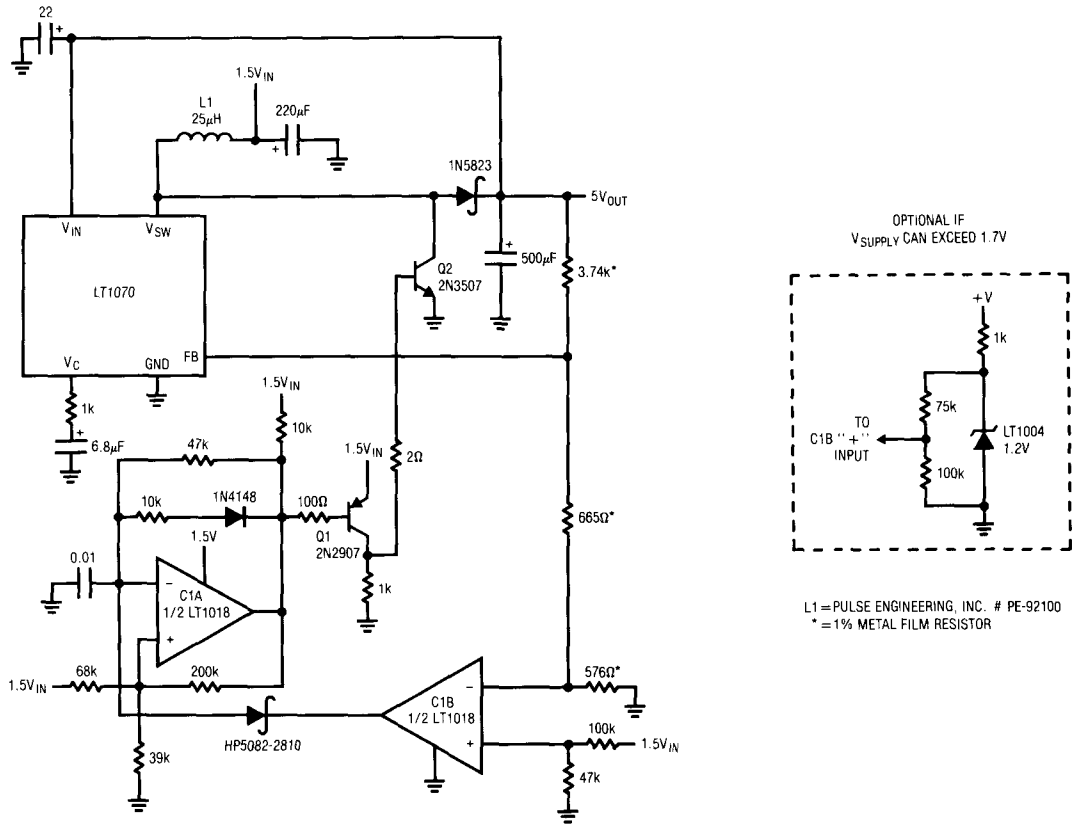


Figure 6. 200mA Output Converter (1.5V to 5V)

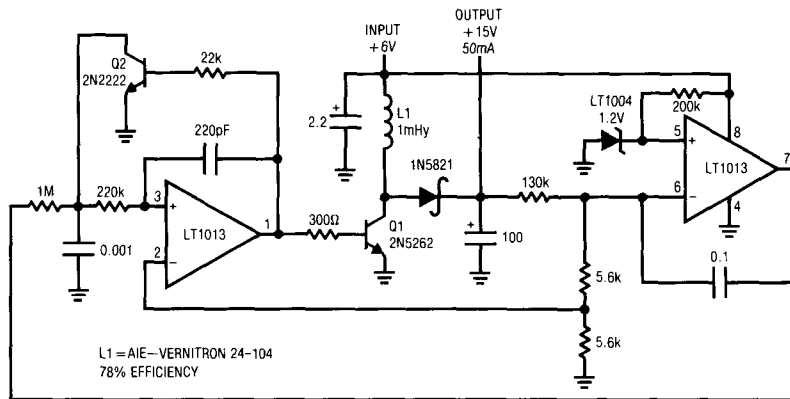


Figure 7. Up Converter (6V to 15V)

Application Note 30

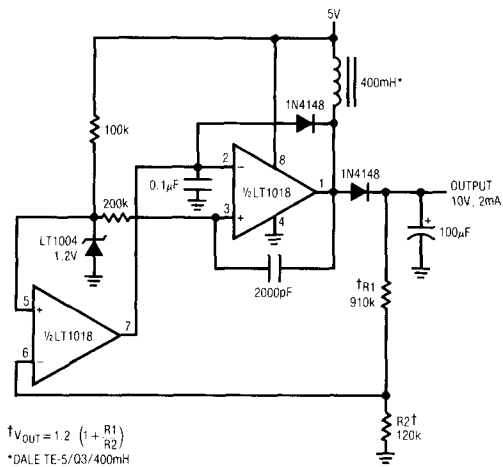


Figure 8. Regulated Up Converter (5V to 10V)

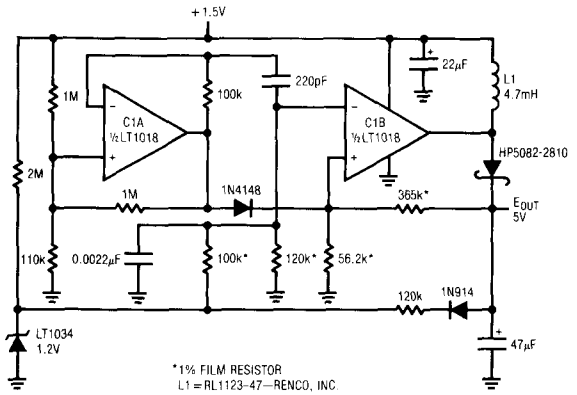


Figure 9. Boost Converter (1.5V to 5V)

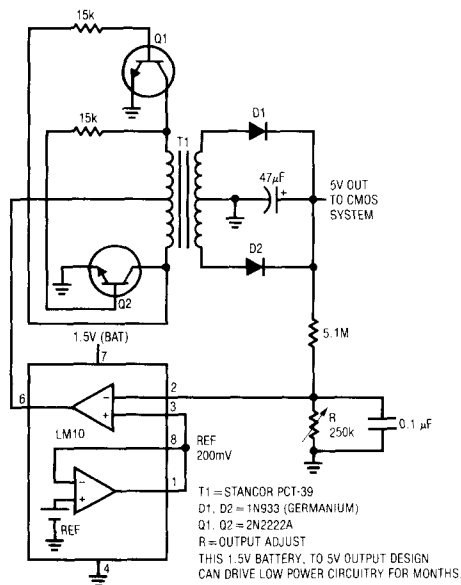


Figure 10. Up Converter (1.5V to 5V)

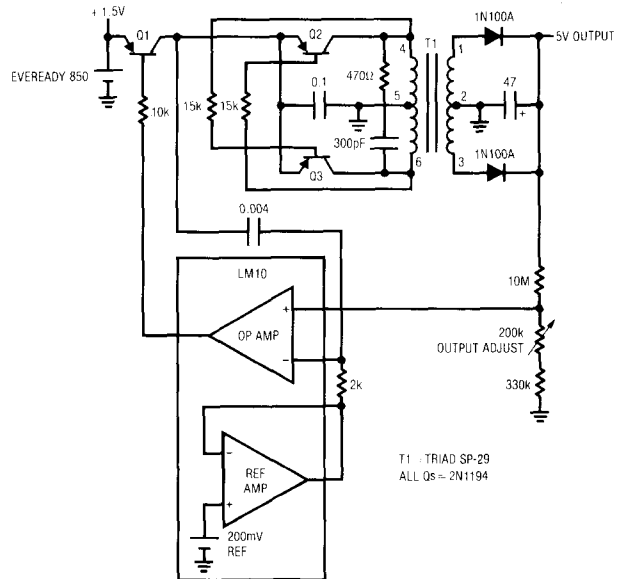


Figure 11. Single Cell Up Converter (1.5V to 5V)

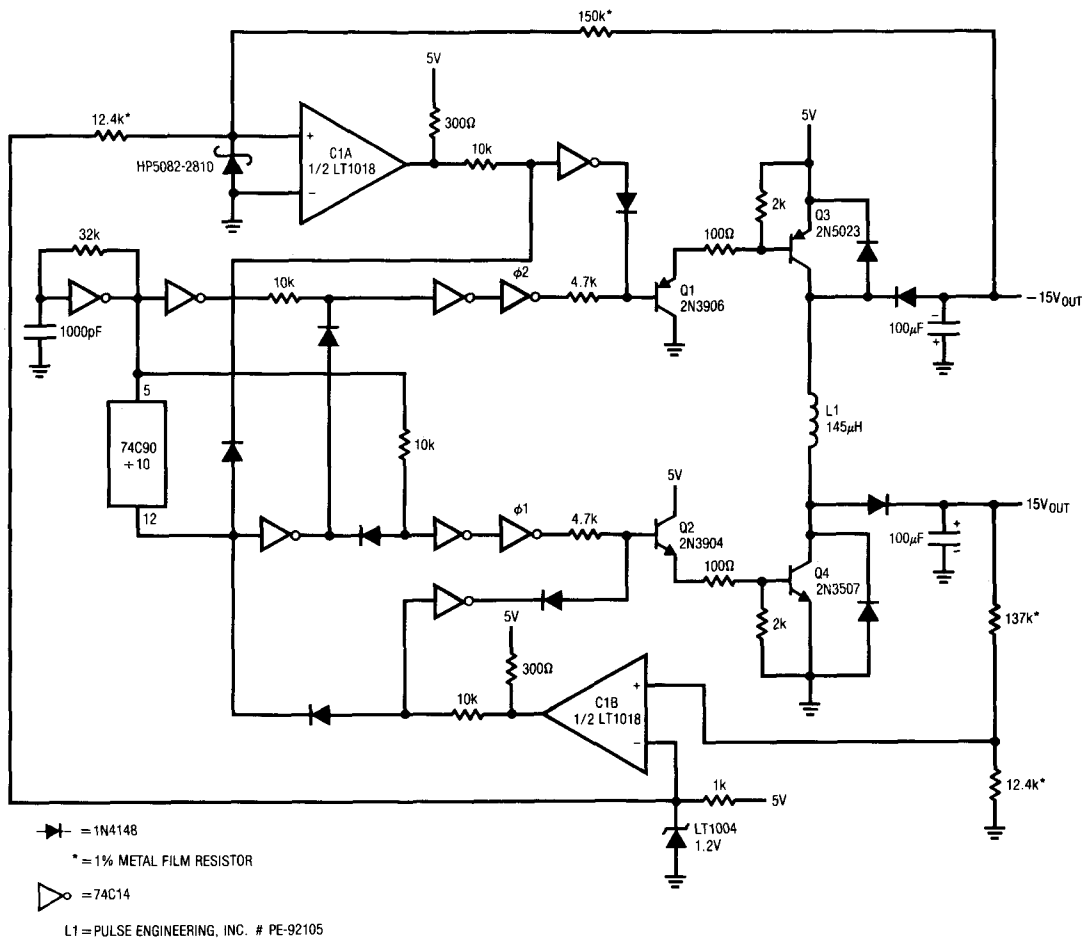


Figure 13. Single Inductor Regulated Converter (5V to ±15V)

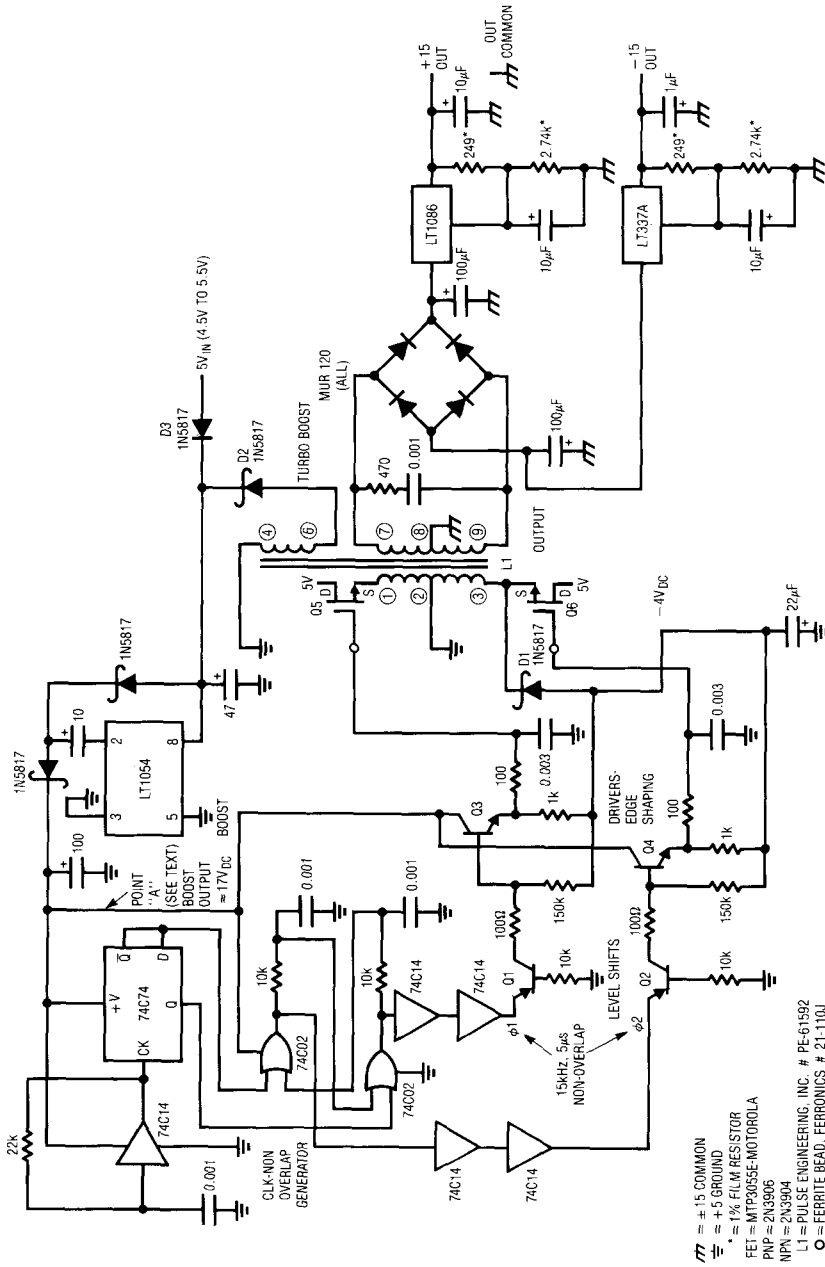


Figure 14. Low Noise Converter (5V to ±15V)

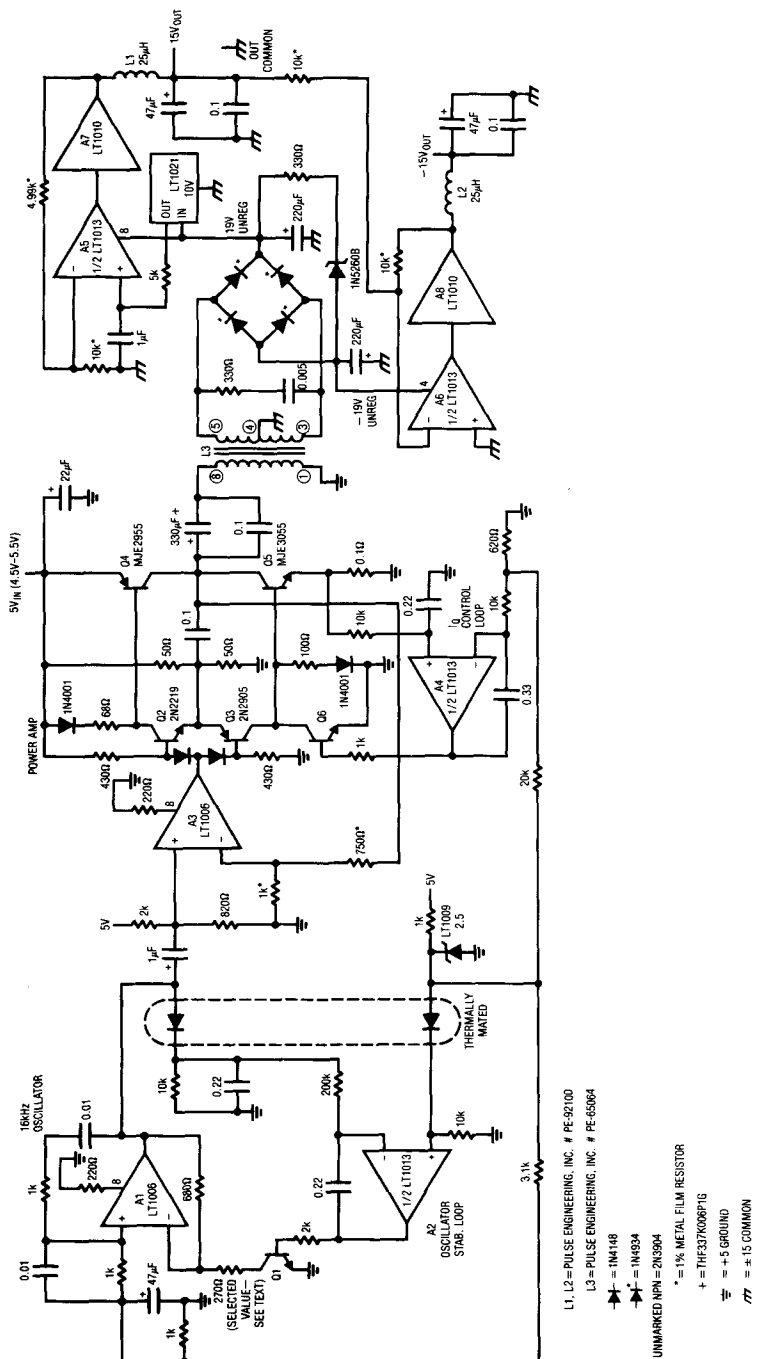


Figure 15. Ultra Low Noise Sine Wave Drive Converter (5V to ± 15V)

L1, L2 = PULSE ENGINEERING, INC. # PE-92100
 L3 = PULSE ENGINEERING, INC. # PE-6064
 —▶— = 1N4148
 —▶— = 1N4934
 UNMARKED NPN = 2N3904
 * = 1% METAL FILM RESISTOR
 + = THE37K06P7IG
 ⊕ = +5 GROUND
 // = ±15 COMMON

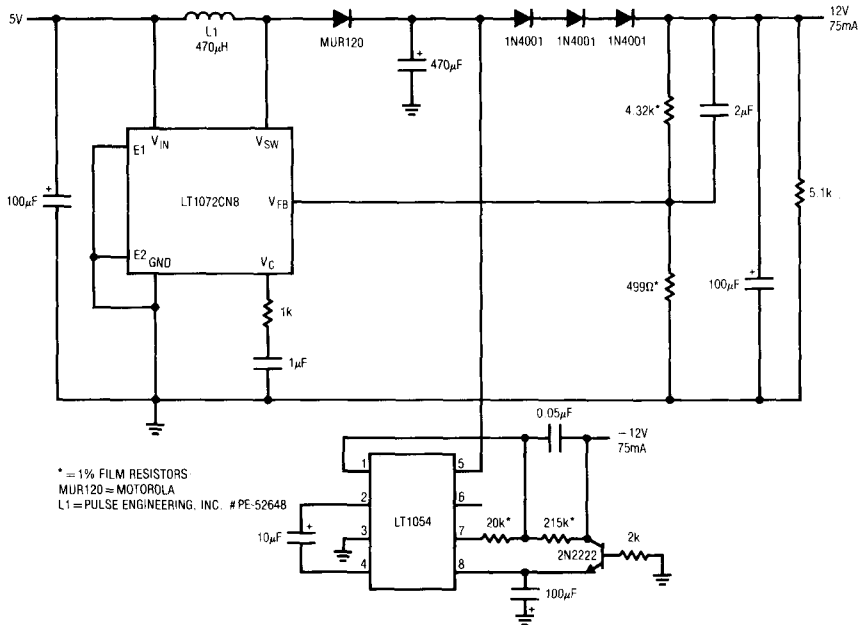


Figure 16. Single Inductor, Dual Output Converter (5V to ±15V)

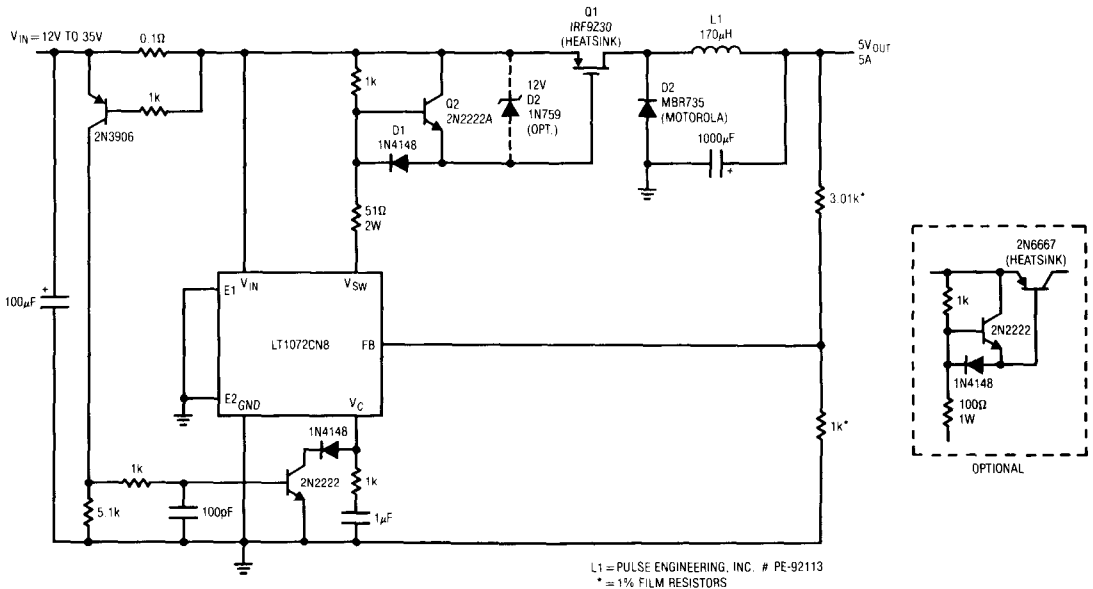
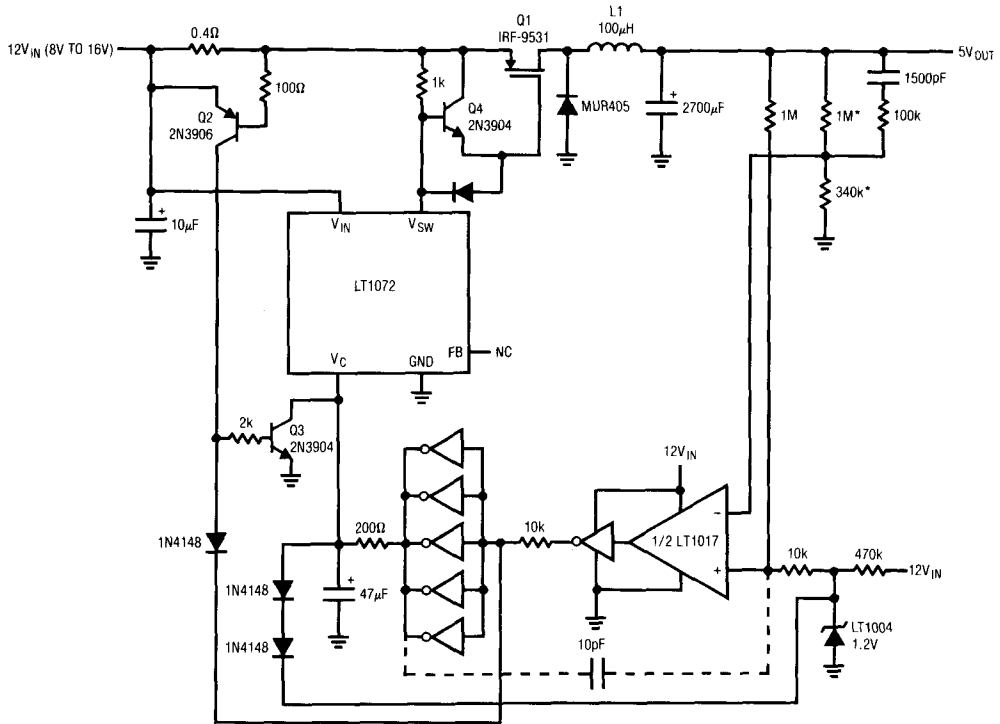


Figure 17. Positive Buck Converter (15V-35V to 5V)

Application Note 30



L1 = PULSE ENGINEERING, INC. # PE-92108

* = 1% FILM RESISTOR


 = 74C04

Figure 18. The Low Quiescent Current Loop Applied to a Buck Converter (8V-16V to 5V)

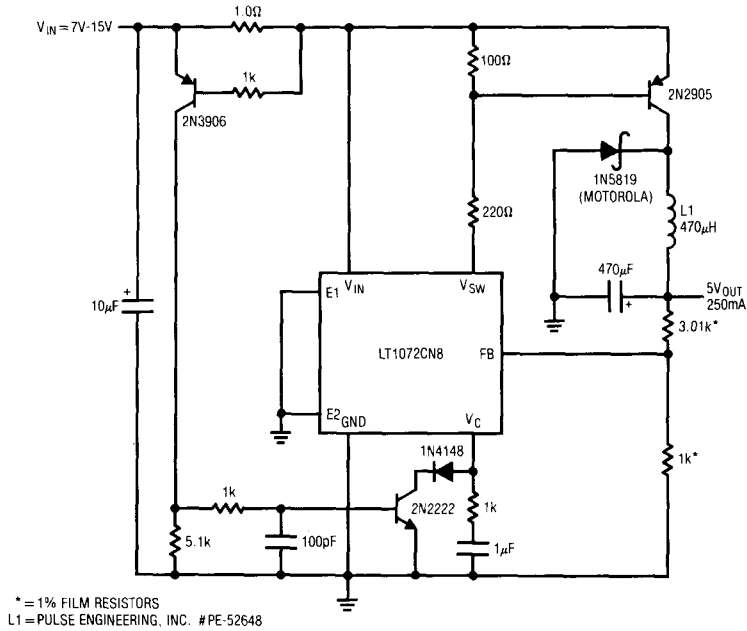


Figure 19. Positive Buck Converter (7V-15V to 5V)

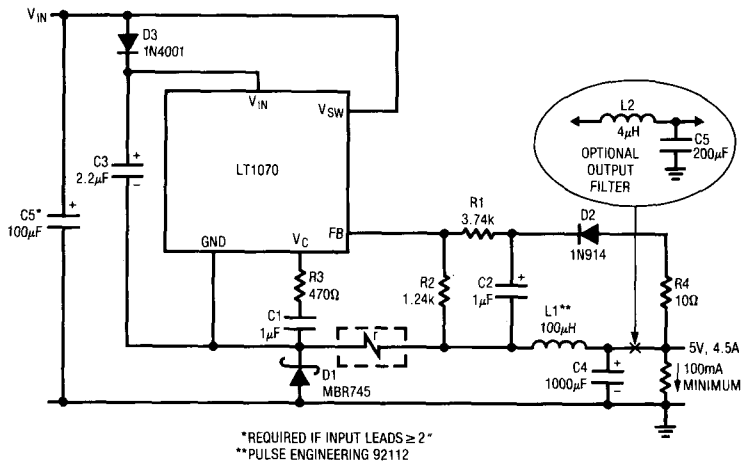


Figure 20. Positive Buck Converter

Application Note 30

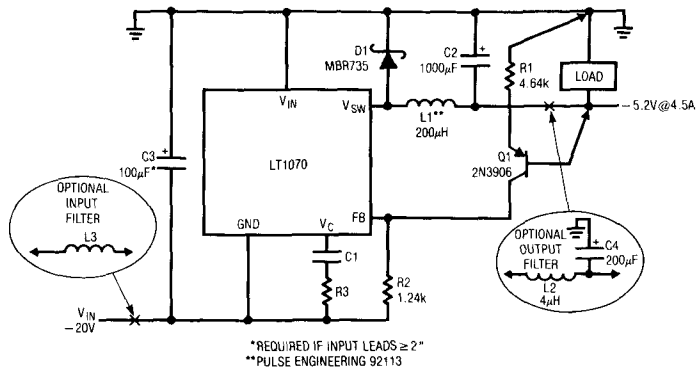


Figure 21. Negative Buck Converter (-20V to -5.2V)

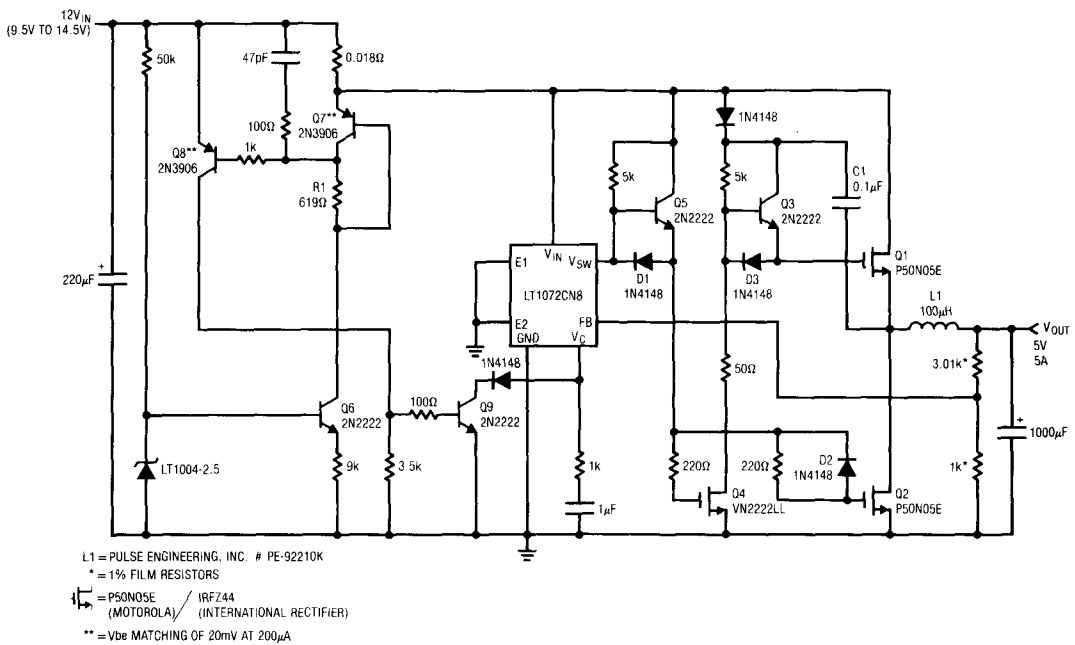


Figure 22. 90% Efficiency Positive Buck Converter with Synchronous Switch (9.5V-14V to 5V)

Application Note 30

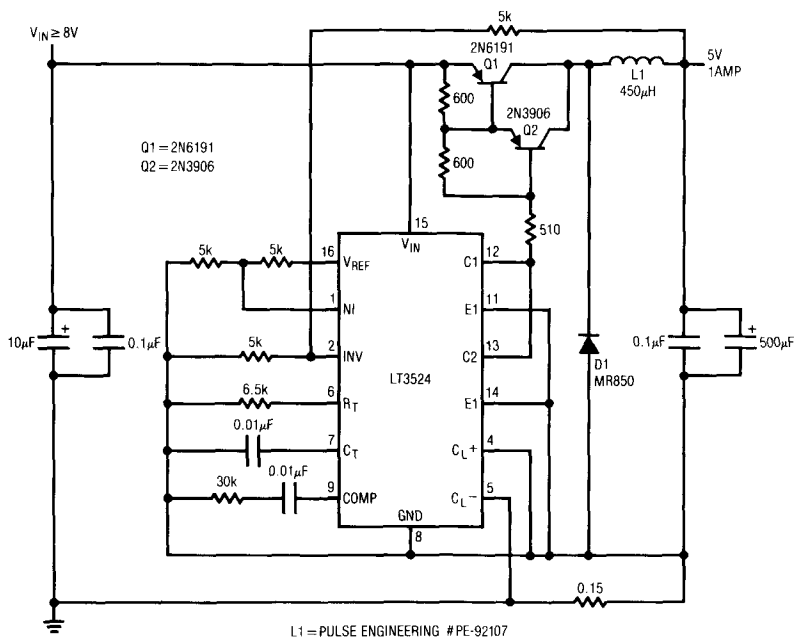


Figure 25. 5V, 1 Amp Regulator (8V-30V to 5V)

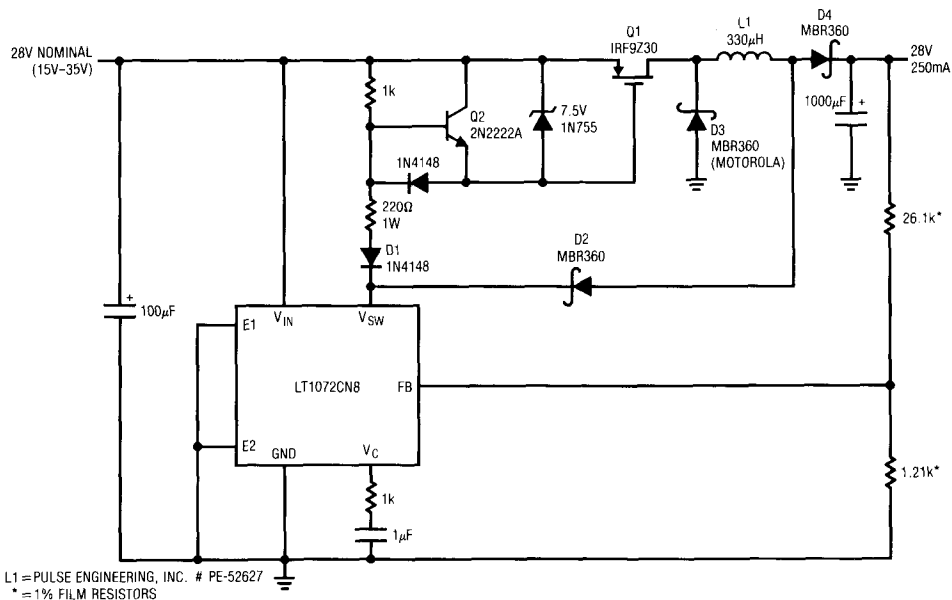


Figure 26. Positive Buck-Boost Converter (15V-35V to 28V)

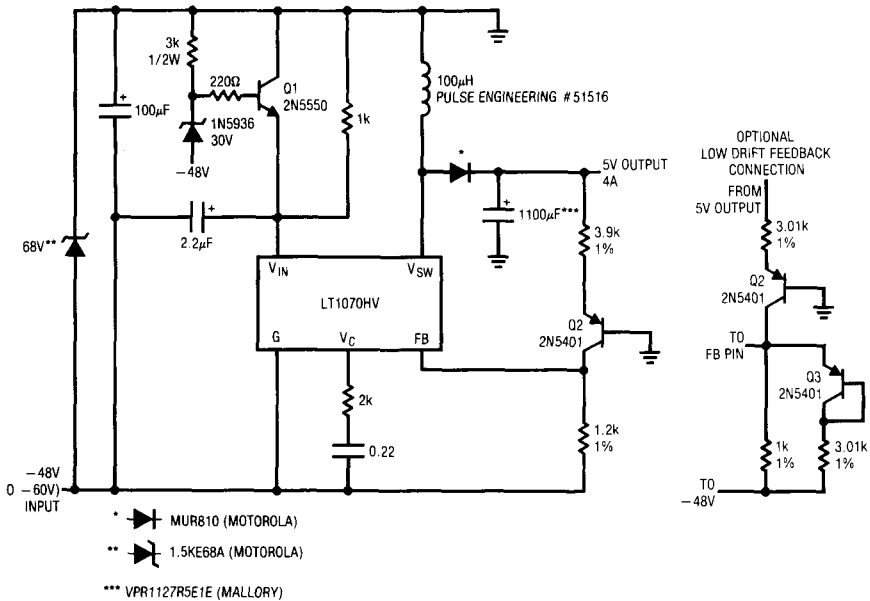


Figure 27. Non-Isolated Regulator (-48V to 5V)

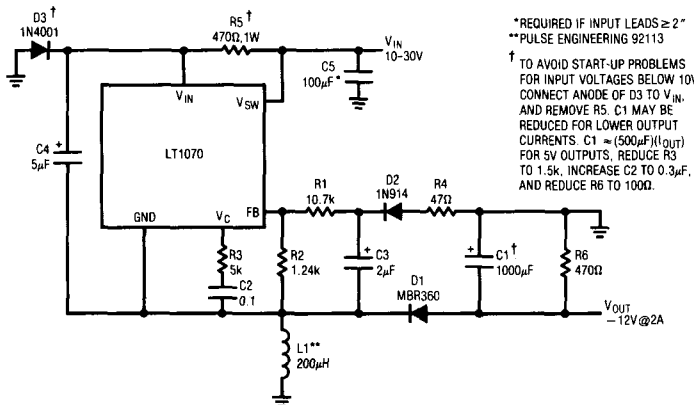


Figure 28. Positive to Negative Buck-Boost Converter (10V-30V to -12V)

Application Note 30

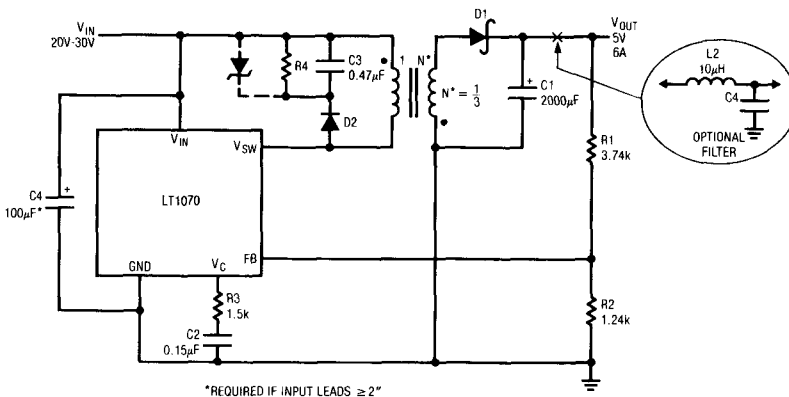


Figure 29. Flyback Converter (20V-30V to 5V)

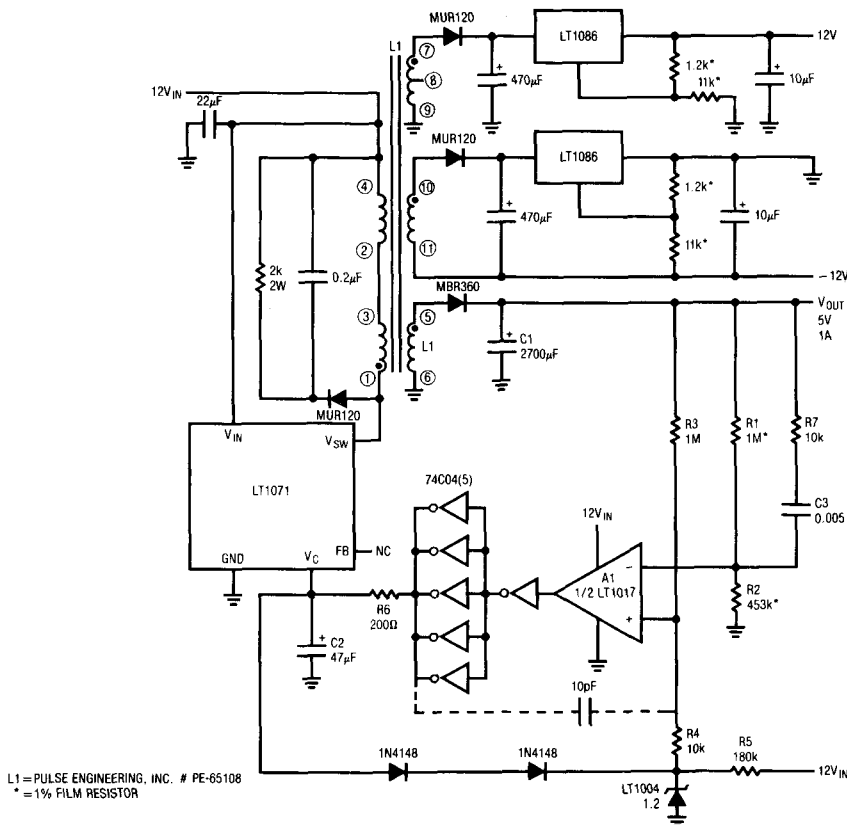


Figure 30. Transformer Coupled Low Quiescent Current Converter (12V to 5V, ±12V)

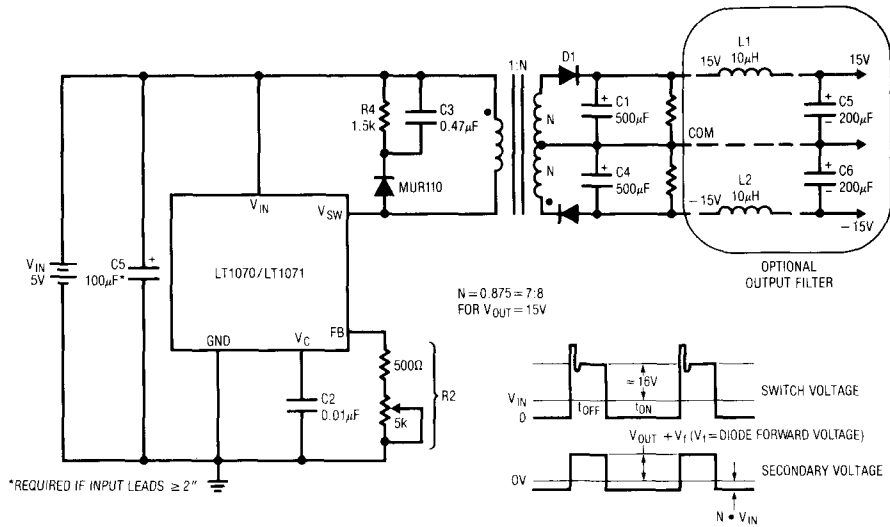


Figure 31. Totally Isolated Converter (5V to ±15V)

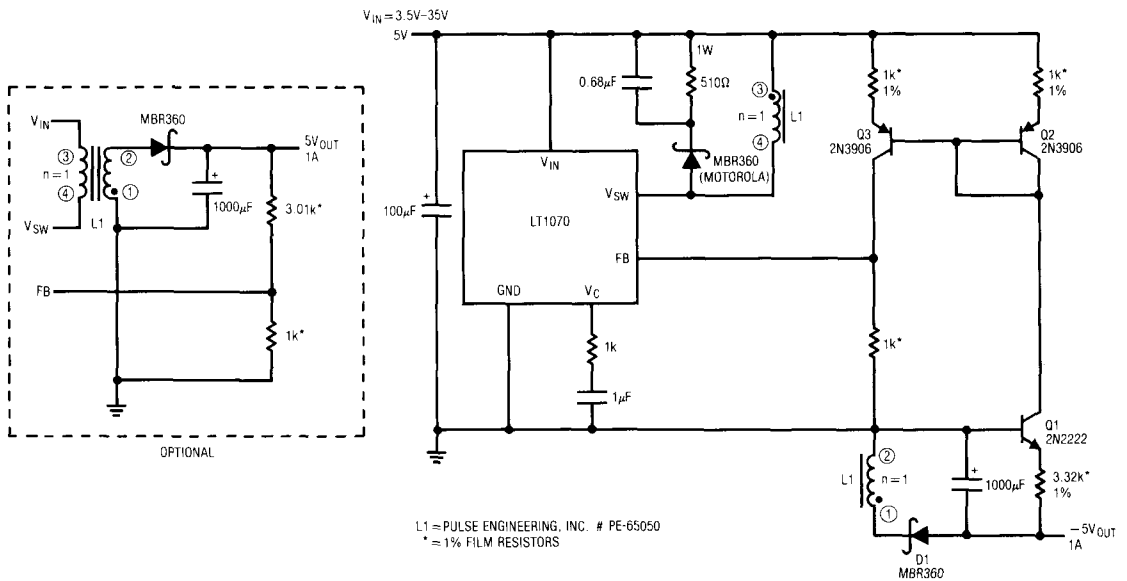


Figure 32. Input Positive Output Negative Flyback Converter (3.5V-35V to -5V)

Application Note 30

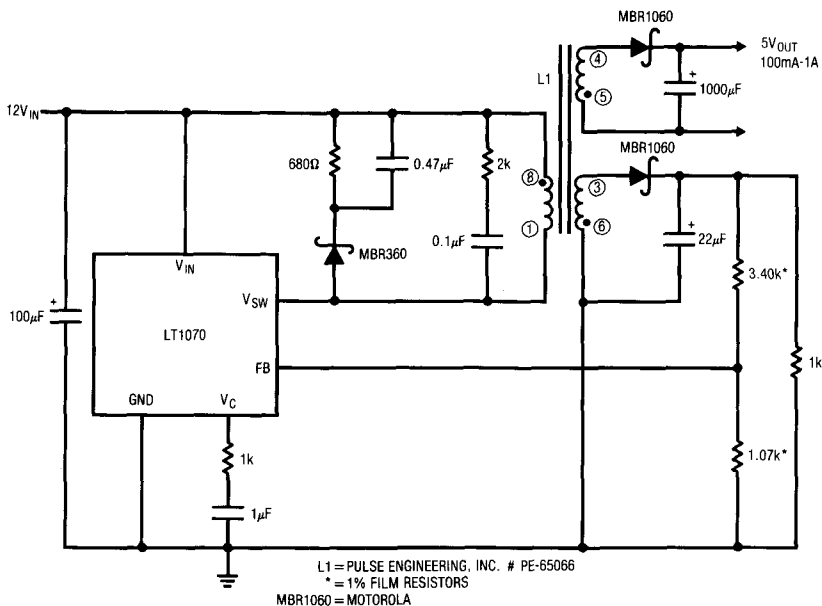


Figure 33. High Efficiency Flux Sensed Isolated Converter (12V to 5V)

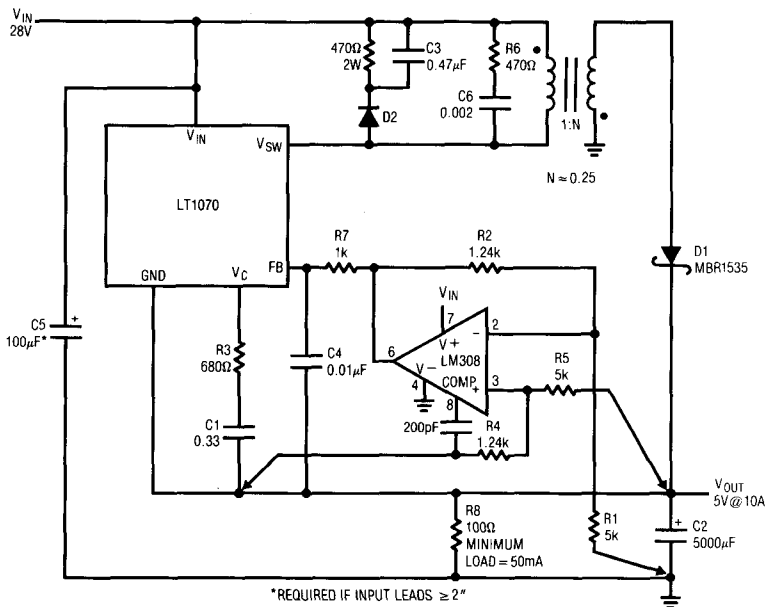


Figure 34. Positive Current Boosted Buck Converter (28V to 5V)

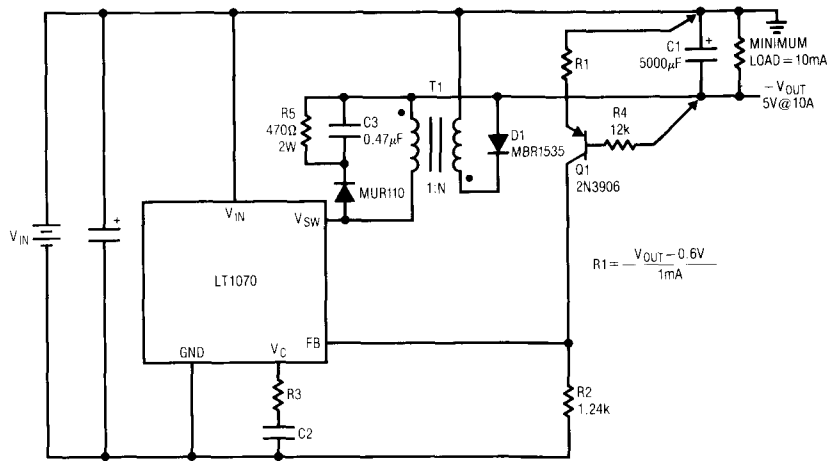


Figure 35. Negative Current Boosted Buck Converter

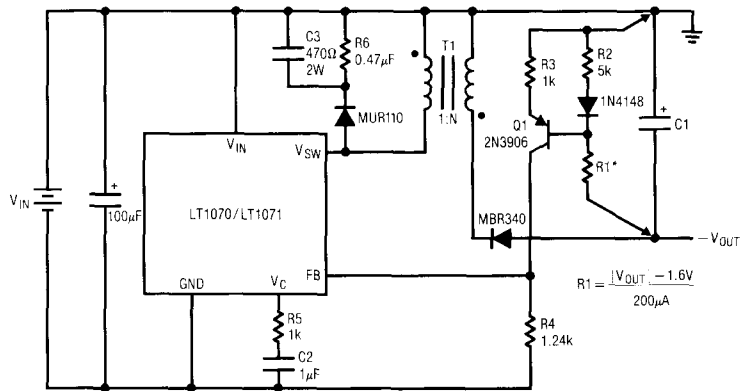


Figure 36. Negative Input-Negative Output Flyback Converter

Application Note 30

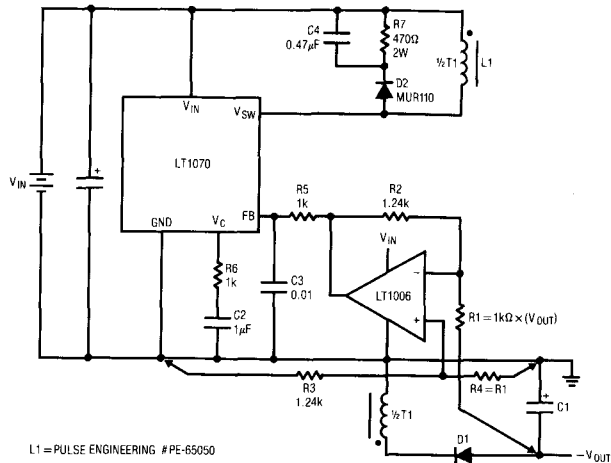


Figure 37. Positive Input-Negative Output Flyback Converter

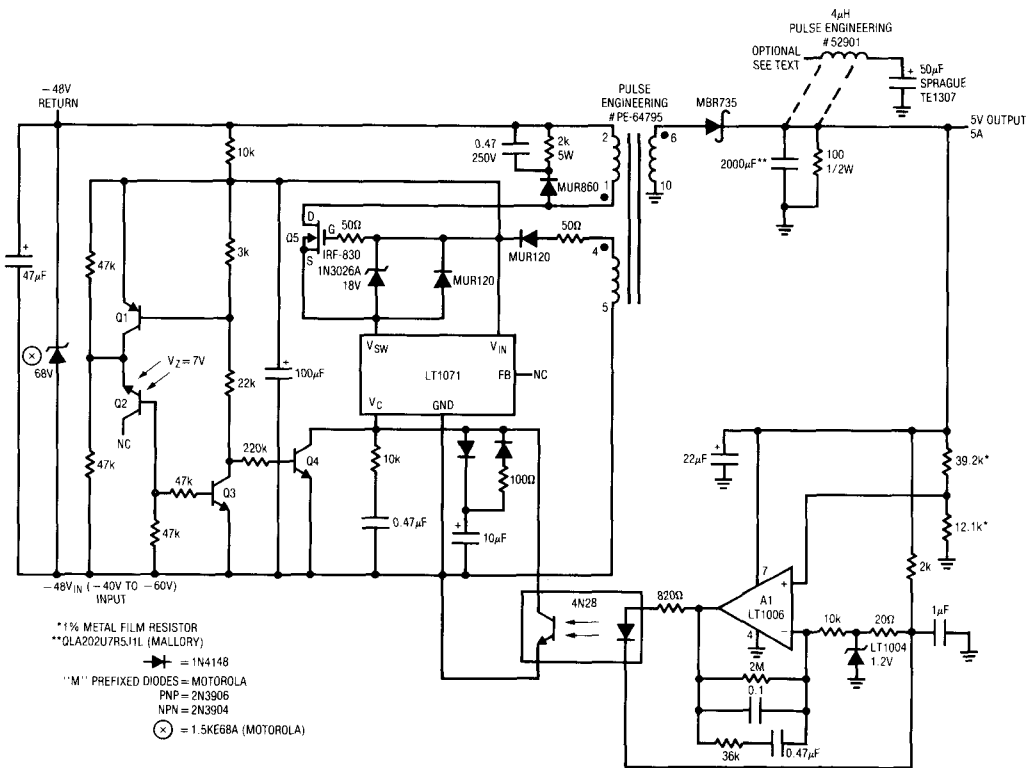


Figure 38. Fully Isolated Regulator (-48V to 5V)

Application Note 30

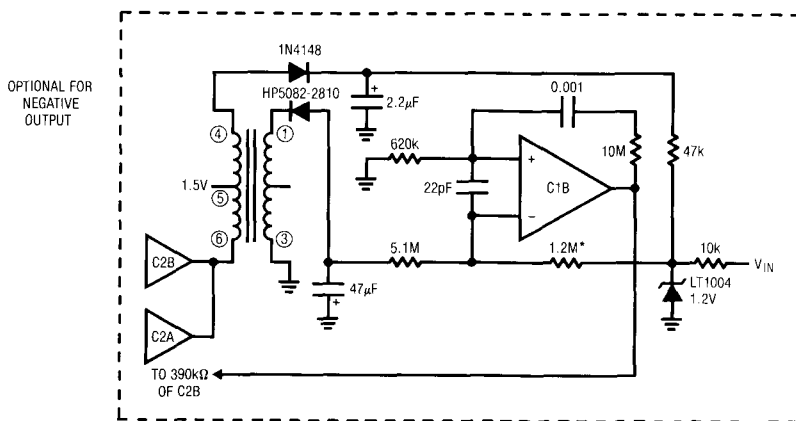
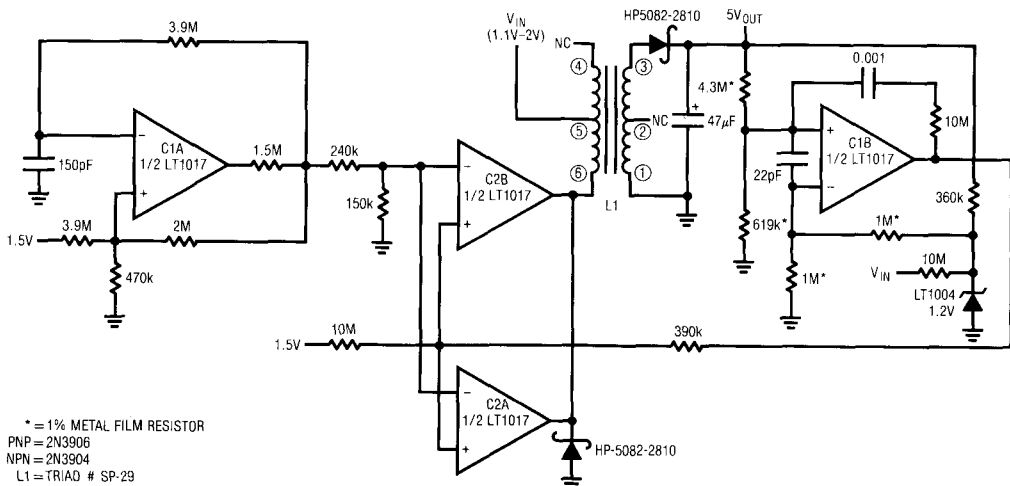


Figure 40. 800µA Output Converter (1.5V to 5V)

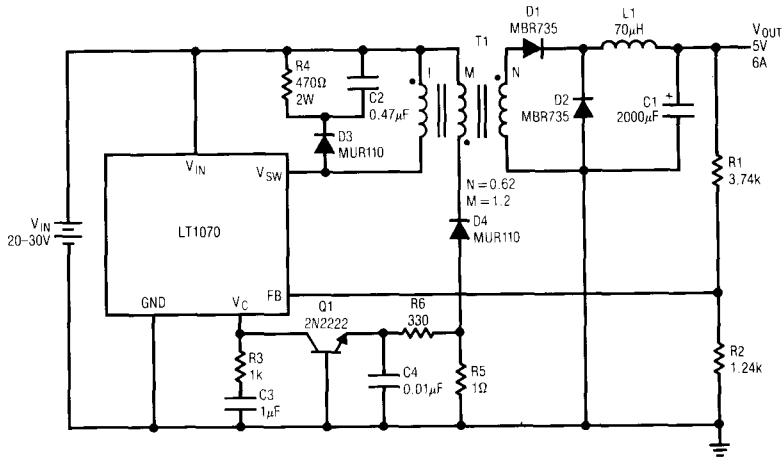
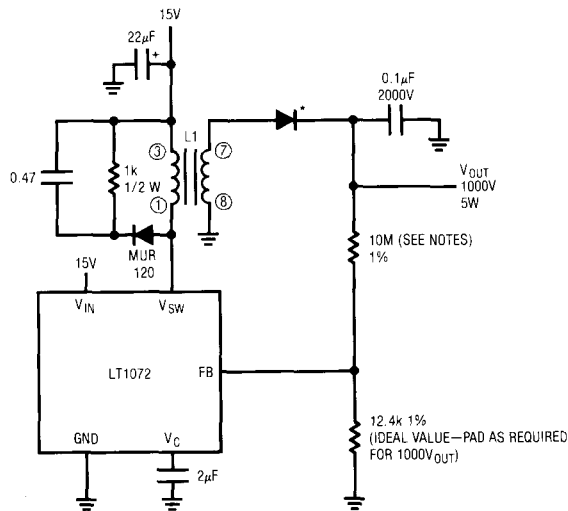


Figure 41. Forward Converter (20V-30V to 5V)



L1 = PULSE ENGINEERING, INC. # PE-6197
 10M = MAX-750-22 VICTOREN, INC.
 ⤴ = SEMTECH, FM-50

Figure 42. Non-Isolated Converter (15V to 1000V)

Application Note 30

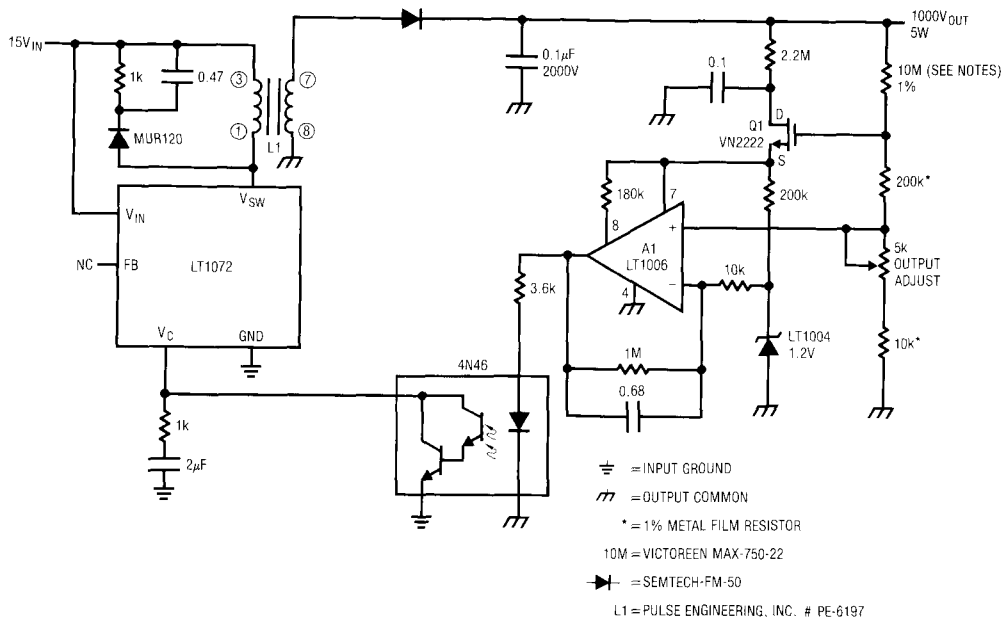


Figure 43. Isolated Output Converter (15V to 1000V)

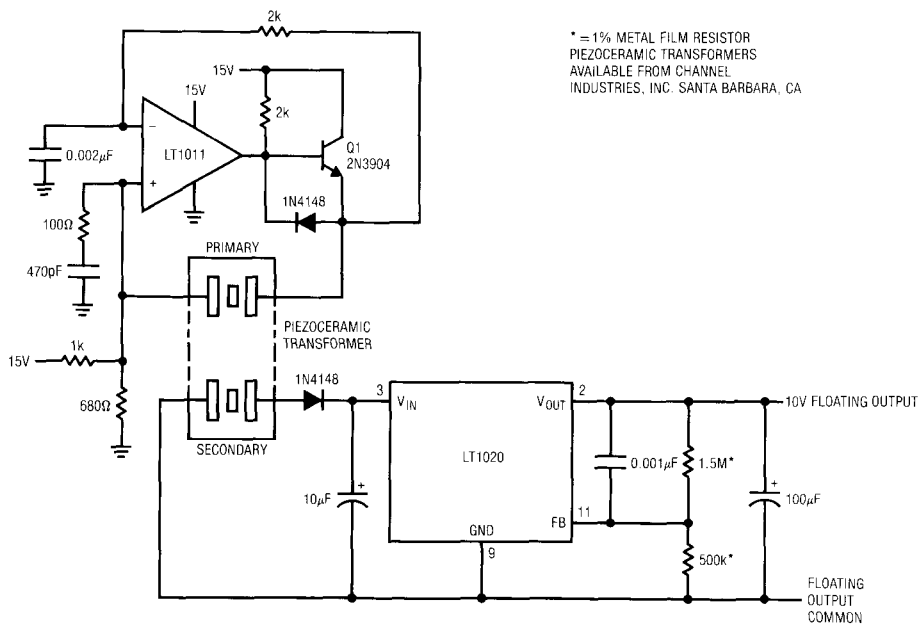
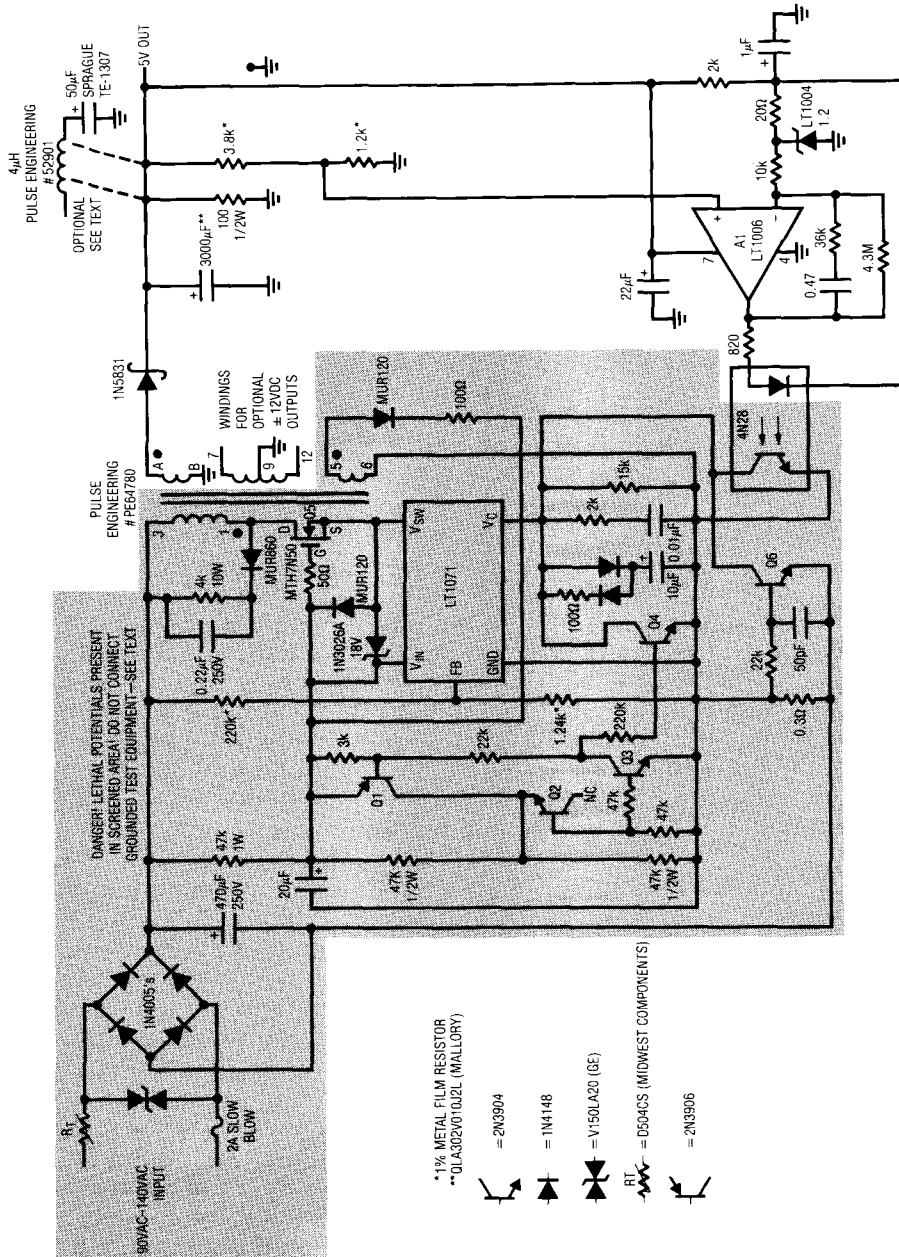


Figure 44. Converter with 20,000V Isolation (15V to 10V)



DANGER: LETHAL POTENTIALS PRESENT IN SCREENED AREA DO NOT CONNECT GROUNDLED TEST EQUIPMENT—SEE TEXT

PULSE ENGINEERING #52901
50μF SPRAGUE TE-1307
OPTIONAL SEE TEXT

PULSE ENGINEERING #PE64780

- *1% METAL FILM RESISTOR
- **0LA302V0102L (MALLORY)
- = 2N3904
- = 1N4148
- = V150LA20 (GE)
- RT = D5040CS (MIDWEST COMPONENTS)
- = 2N3906

Figure 45. 100W Off-Line Switching Regulator. DANGER: Lethal Potentials Present.

Application Note 30

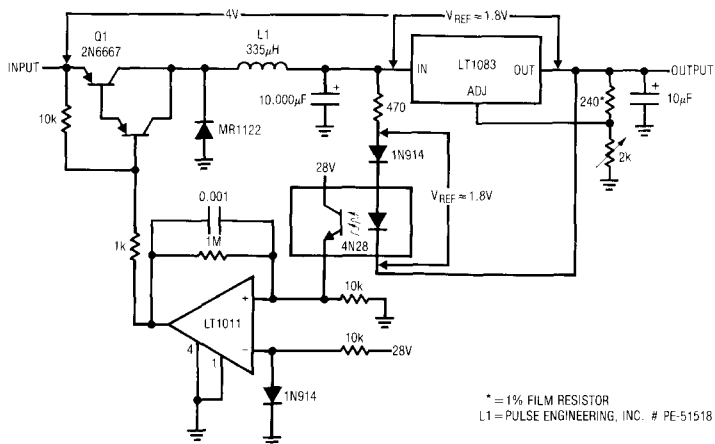


Figure 46. High Power Linear Regulator with Switching Pre-Regulator

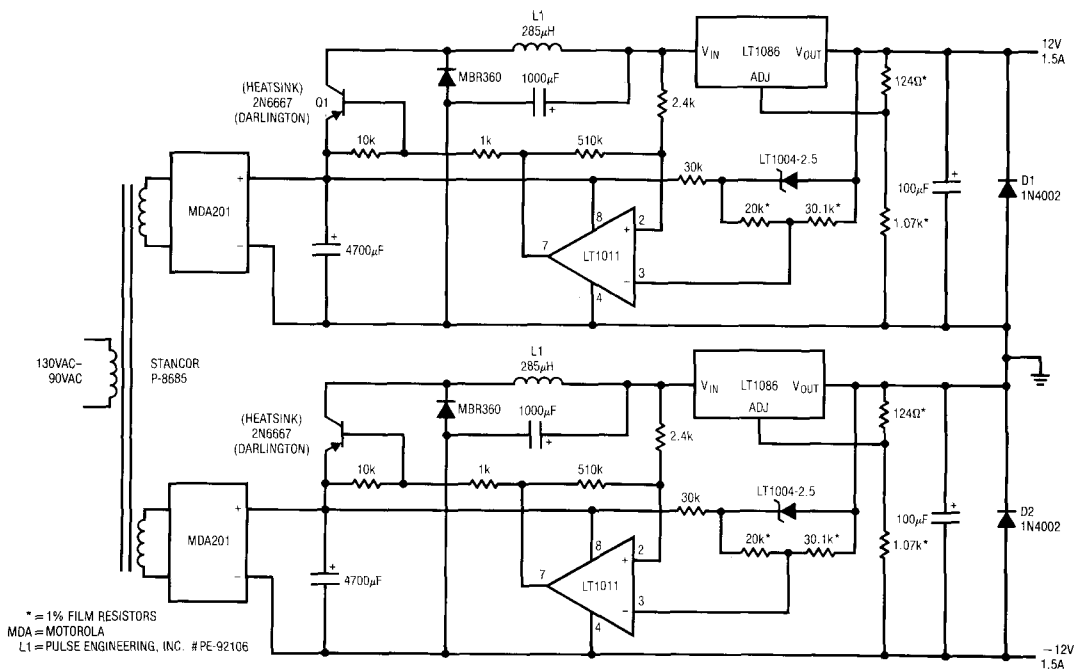


Figure 47. Dual Pre-Regulated Supply (90-130VAC to $\pm 12V$)

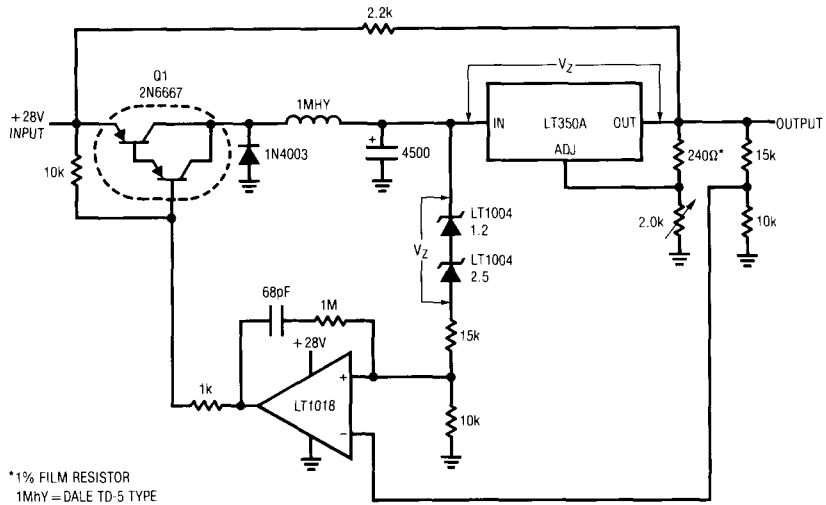


Figure 48. Linear Regulator with Switching Pre-Regulator

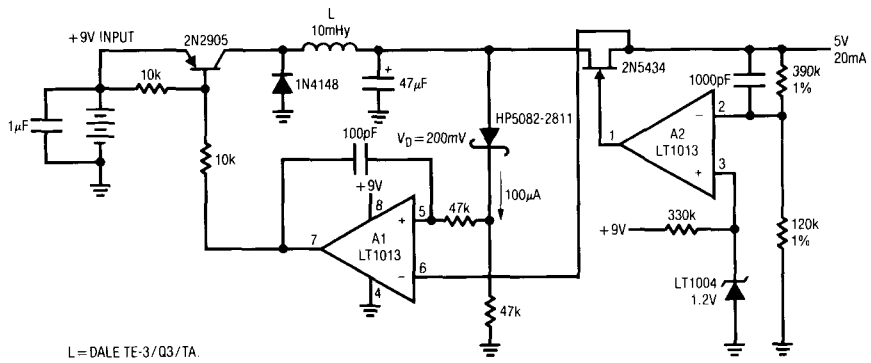
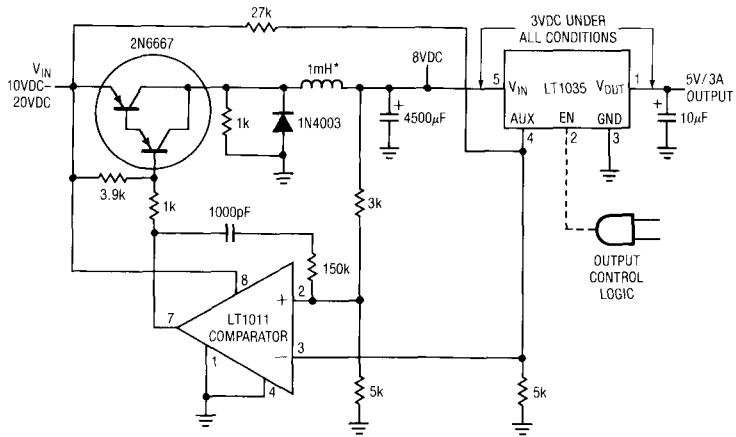


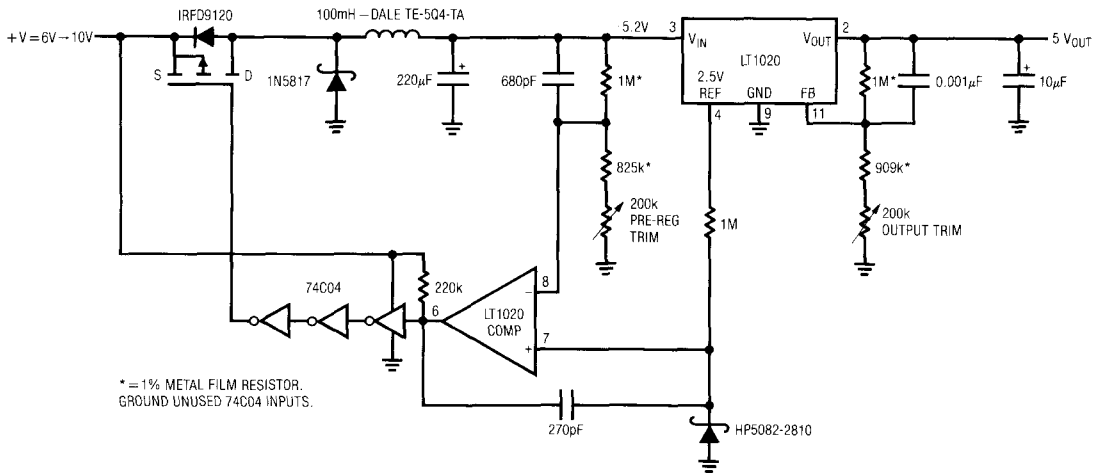
Figure 49. Switching Pre-Regulated Linear Regulator (9V to 5V)

Application Note 30



*DALE TD-5
THIS CIRCUIT IS DESIGNED TO REDUCE POWER DISSIPATION
IN THE LT1035 OVER A 90VAC-140VAC INPUT RANGE.

Figure 50. Low Dissipation Regulator (10V-20V to 5V)



* = 1% METAL FILM RESISTOR.
GROUND UNUSED 74C04 INPUTS.

Figure 51. Micropower Post-Regulated Switching Regulator (6V-10V to 5V)

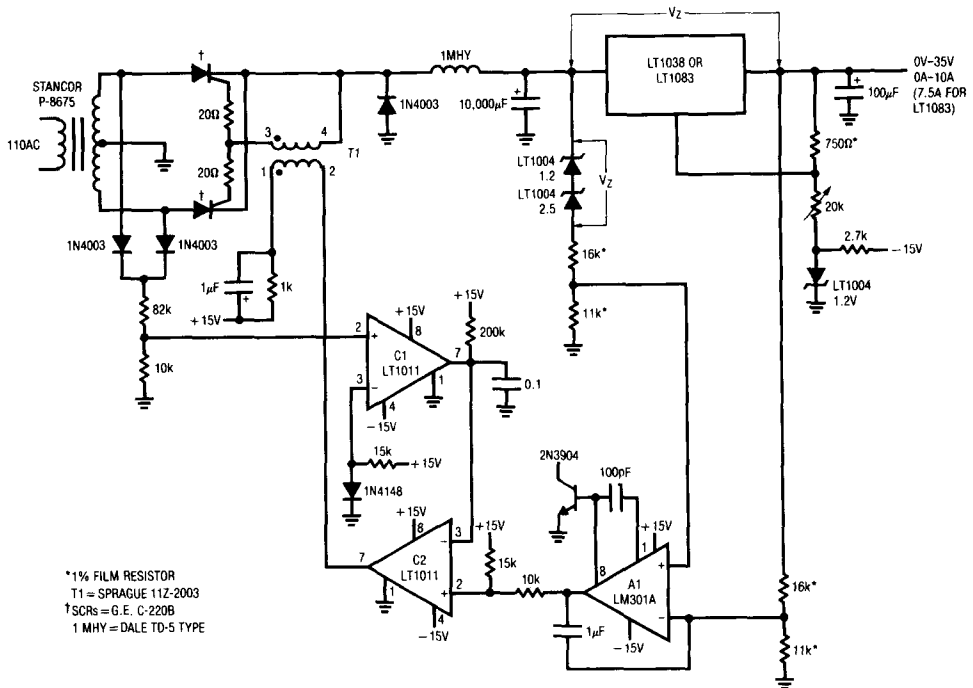


Figure 52. High Current Low Dissipation Pre-Regulated Linear Regulator

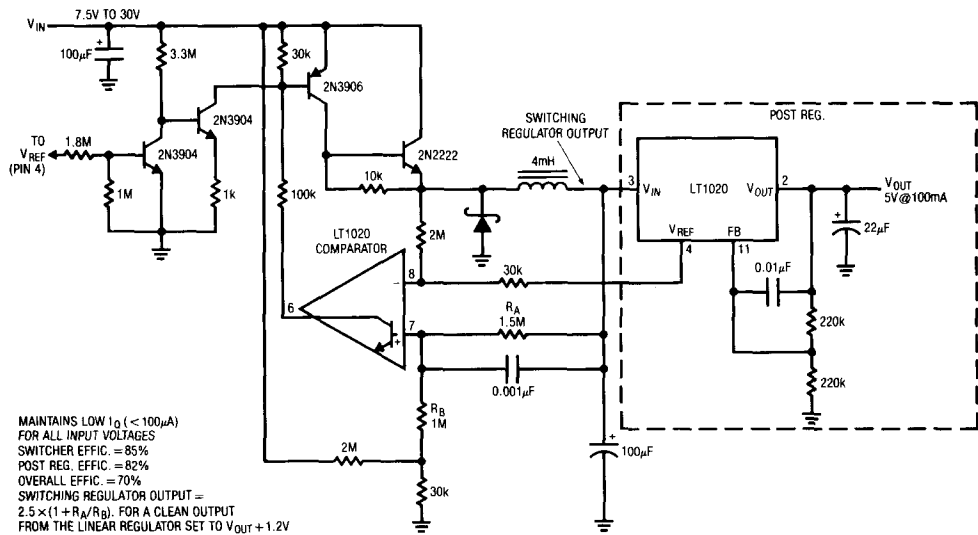


Figure 53. Switching Pre-Regulator for Wide Input Voltage Range (7.5V-30V to 5V)

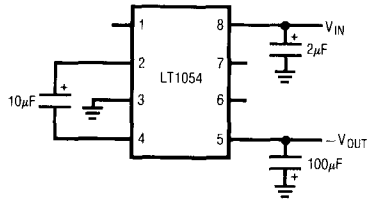
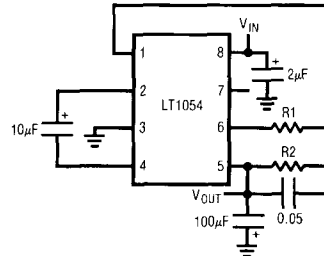
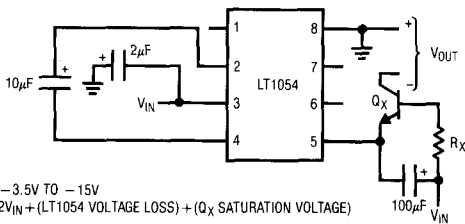


Figure 54. Basic Voltage Inverter



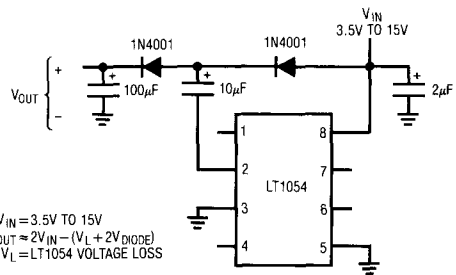
$$R2 = R1 \left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40\text{mV}} + 1 \right) = 20\text{k} \left(\frac{|V_{OUT}|}{1.21\text{V}} + 1 \right)$$

Figure 55. Basic Voltage Inverter/Regulator



$V_{IN} = -3.5\text{V TO } -15\text{V}$
 $V_{OUT} = 2V_{IN} + (\text{LT1054 VOLTAGE LOSS}) + (Q_X \text{ SATURATION VOLTAGE})$

Figure 56. Negative Voltage Doubler



$V_{IN} = 3.5\text{V TO } 15\text{V}$
 $V_{OUT} \approx 2V_{IN} - (V_L + 2V_{DIODE})$
 $V_L = \text{LT1054 VOLTAGE LOSS}$

Figure 57. Positive Doubler

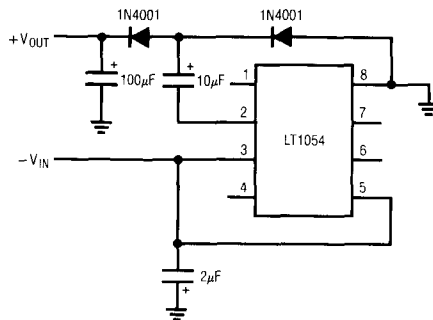


Figure 58. Switched Capacitor - V_{IN} to + V_{OUT} Converter

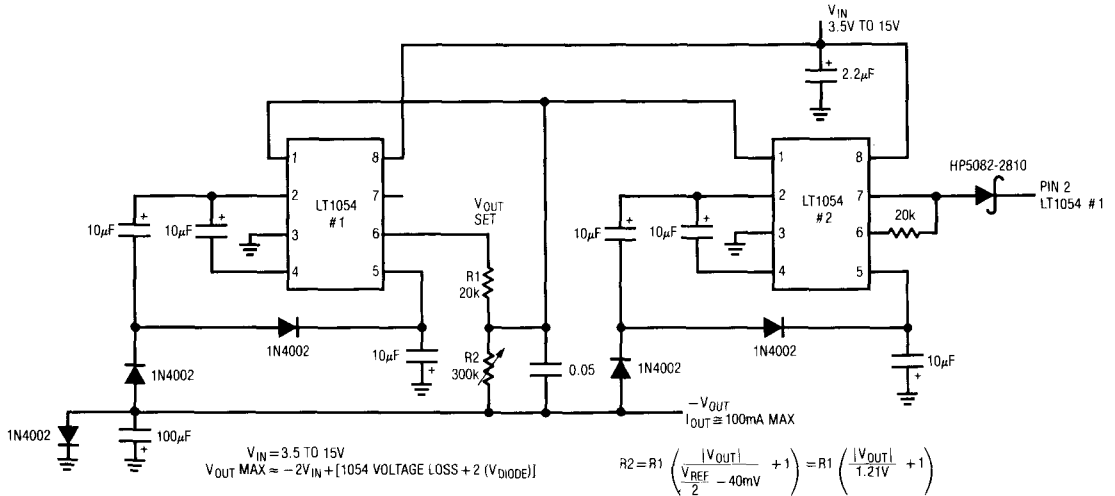


Figure 59. 100mA Regulating Negative Doubler

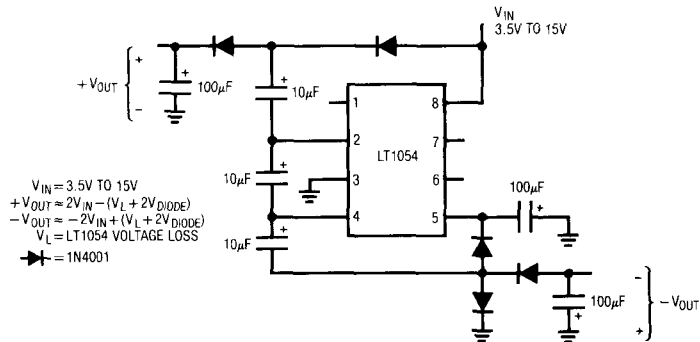


Figure 60. Dual Output Voltage Doubler

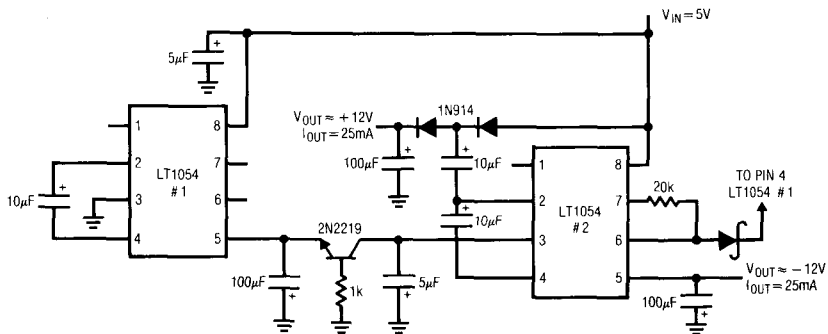


Figure 61. Switched Capacitor Converter (5V to ±12V)

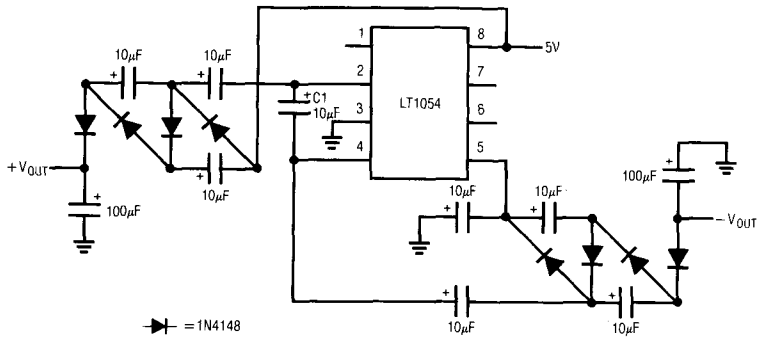


Figure 62. Switched Capacitor Charge Pump Based Voltage Multiplier (5V to ±12V)

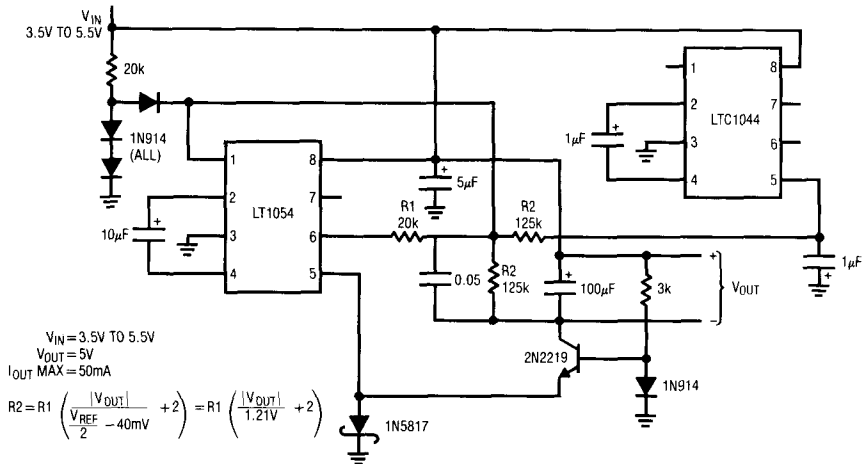


Figure 63. Regulator (3.5V to 5V)

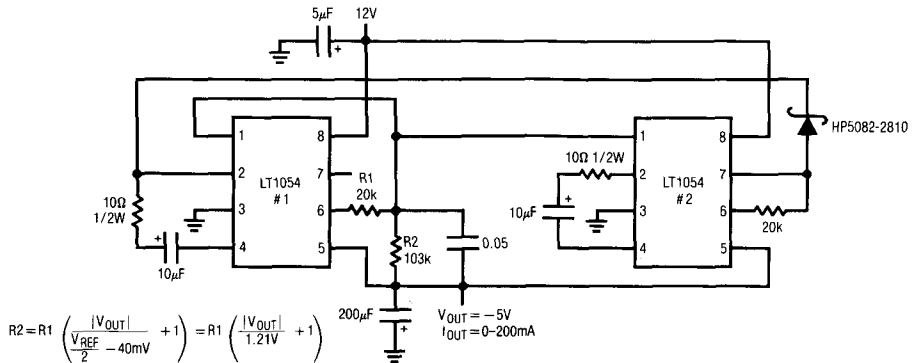


Figure 64. Regulating 200mA Converter (12V to -5V)

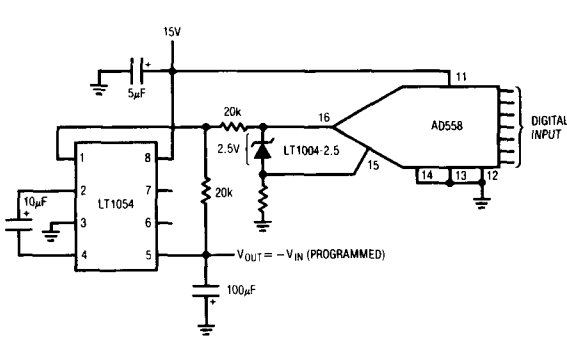


Figure 65. Digitally Programmable Negative Supply

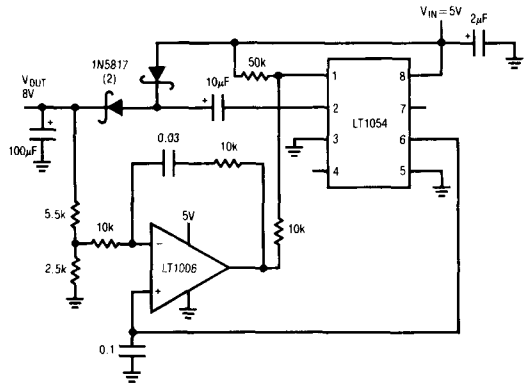


Figure 66. Positive Doubler with Regulation (5V to 8V)

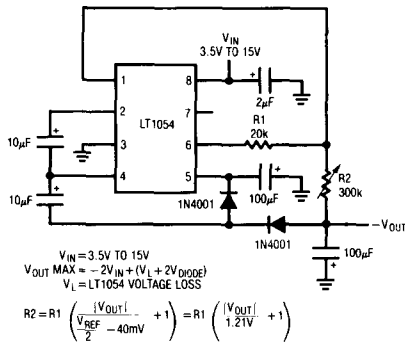


Figure 67. Negative Doubler with Regulator

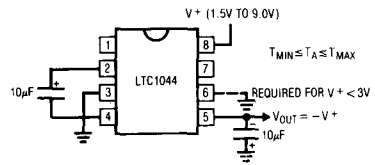


Figure 68. Negative Voltage Converter

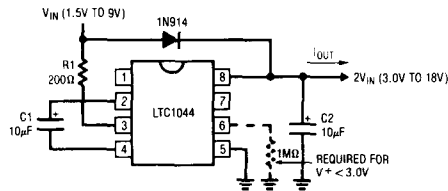


Figure 69. Voltage Doubler

Application Note 30

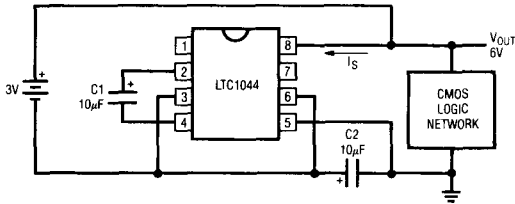


Figure 70. Voltage Doubler

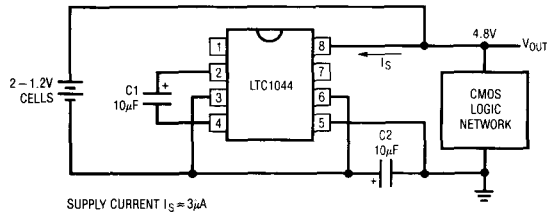


Figure 71. Generating CMOS Logic Supply from 2 Mercury Batteries (2.4V to 4.8V)

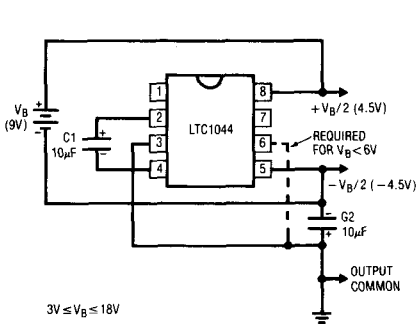


Figure 72. Battery Splitter (9V to ±4.5V)

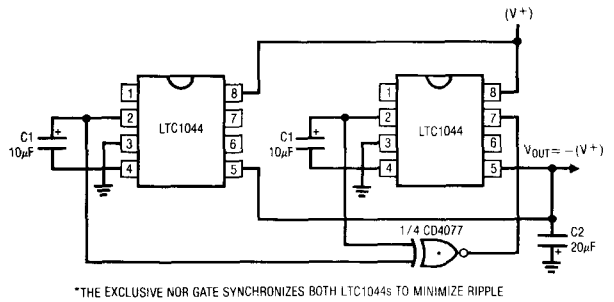


Figure 73. Paralleling for Lower Output Resistance

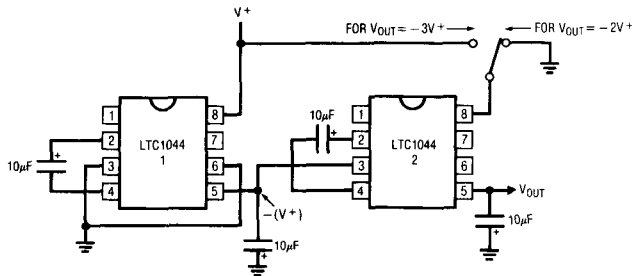


Figure 74. Stacking for Higher Voltage

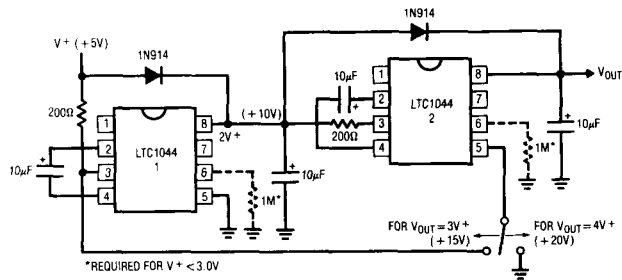


Figure 75. Voltage Tripler/Quadrupler

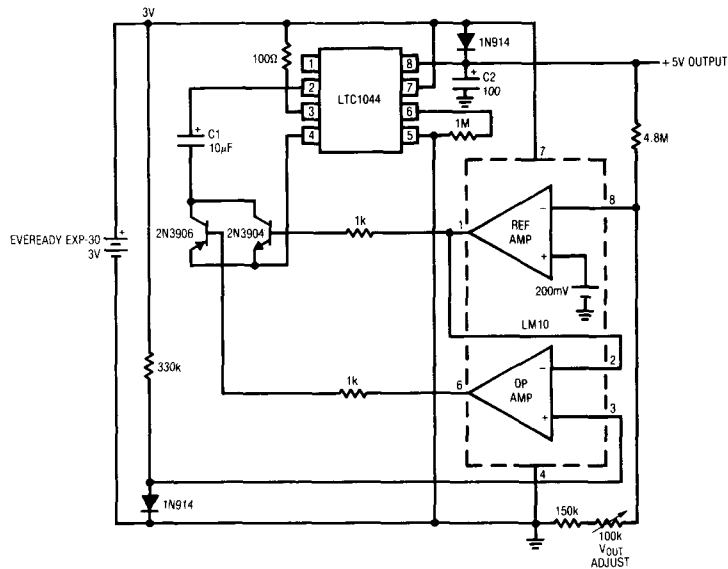


Figure 76. Regulated Voltage Up Converter (3V to 5V)

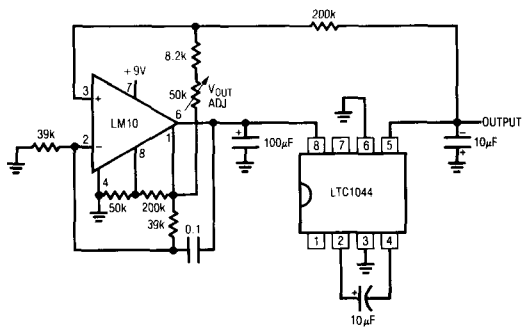


Figure 77. Regulated Negative Voltage Converter

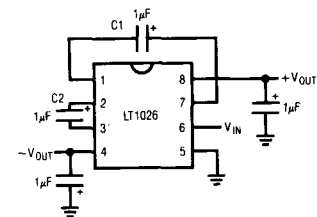


Figure 78. Dual Output Switched Capacitor Voltage Generator

Application Note 30

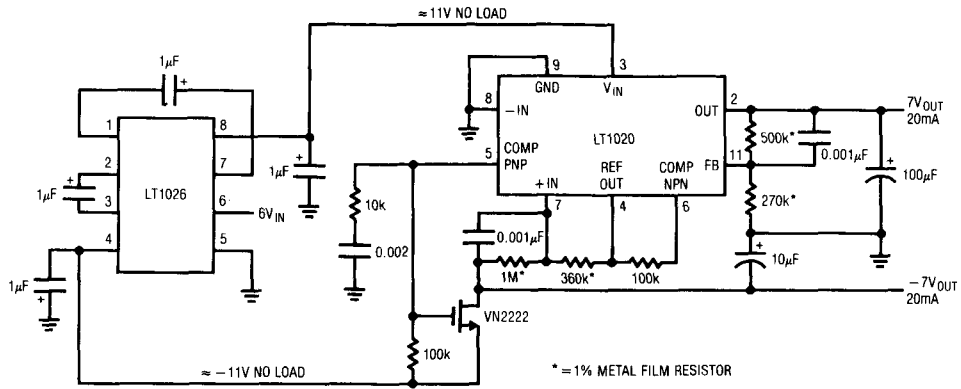


Figure 79. Switched Capacitor Based Converter (6V to ±7V)

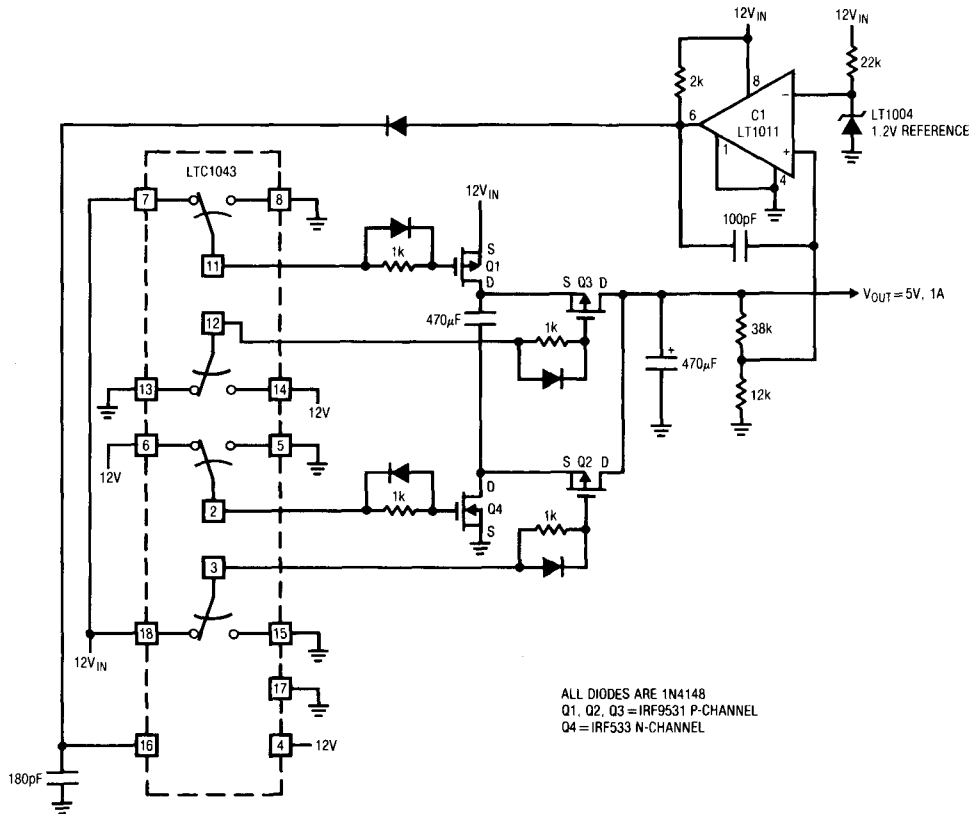


Figure 80. High Power Switched Capacitor Converter (12V to 5V)

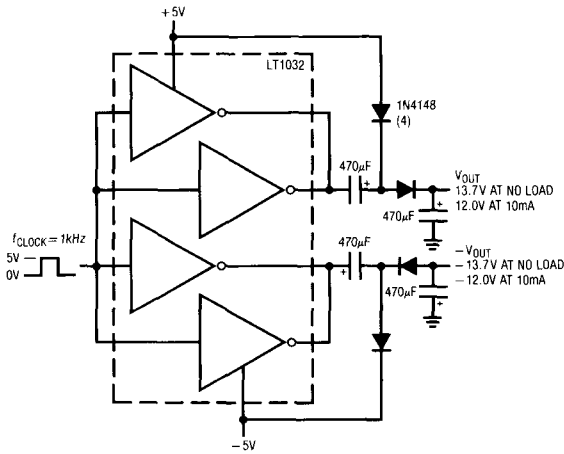


Figure 81. Voltage Multiplier ($\pm 5V$ to $\pm 15V$)

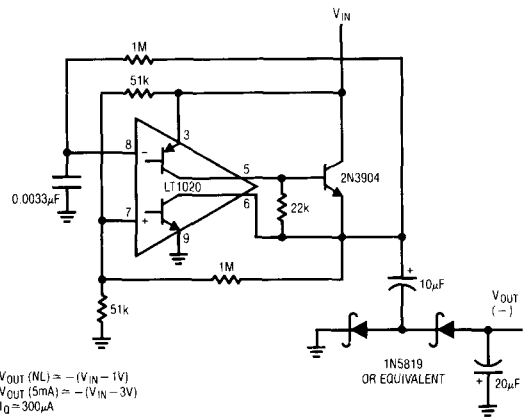


Figure 82. Charge-Pump Negative Voltage Generator

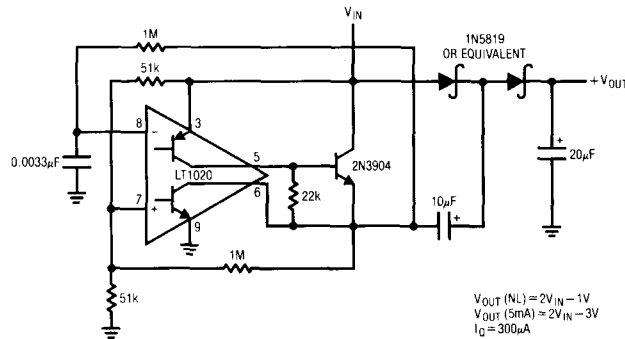


Figure 83. Charge-Pump Voltage Doubler

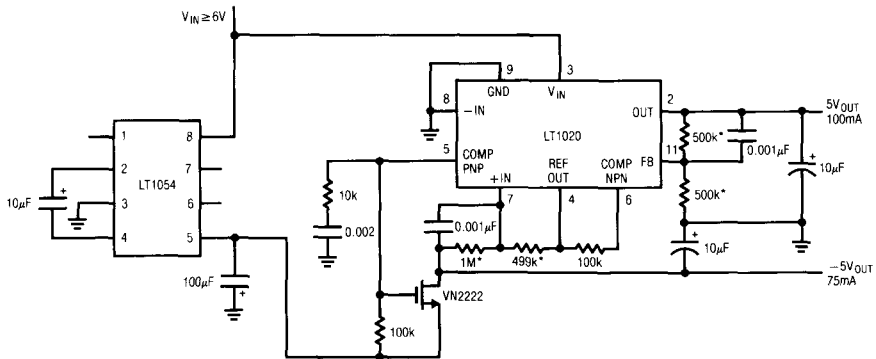


Figure 84. High Current Switched Capacitor Converter (6V to $\pm 5V$)

Application Note 30

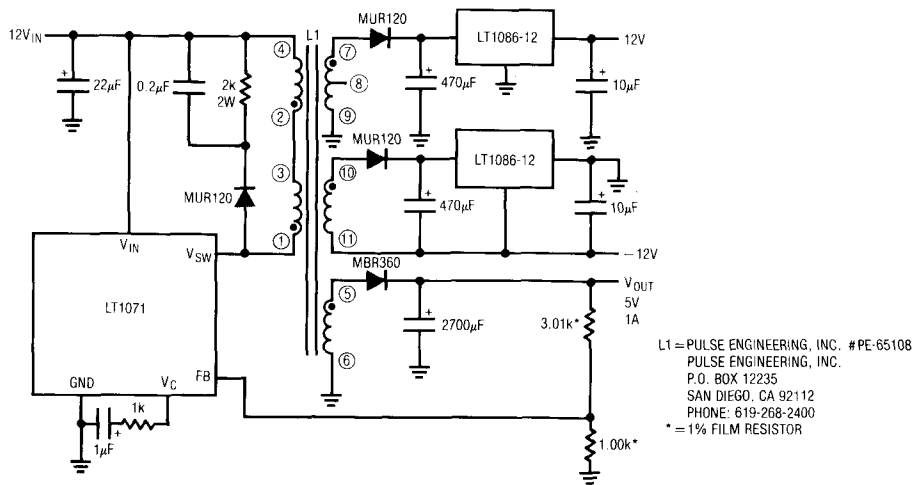


Figure 85. Multi-Output Flyback Converter (12V to 5V, ±12V)

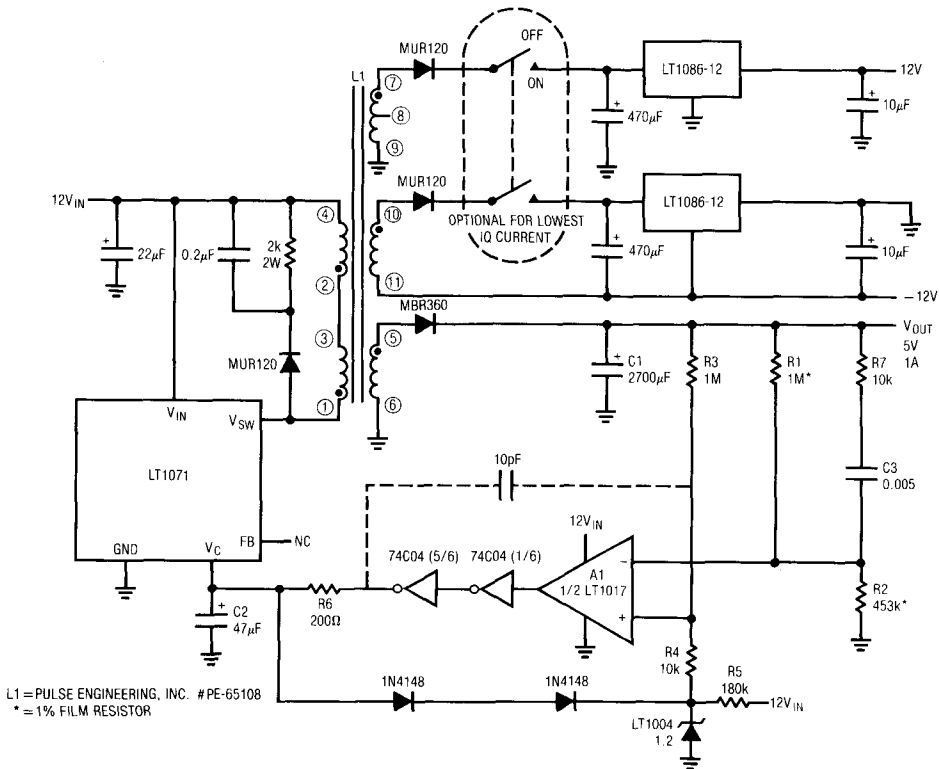
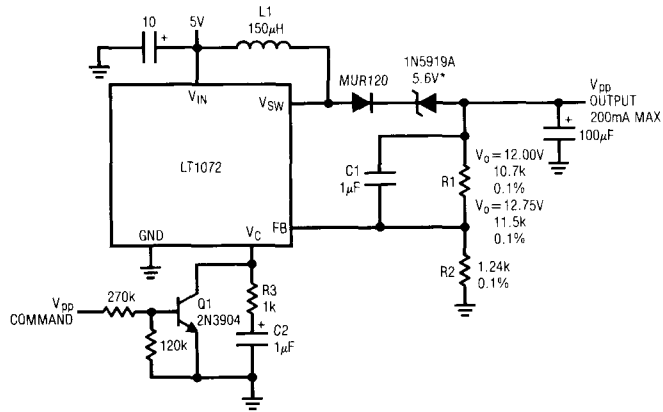
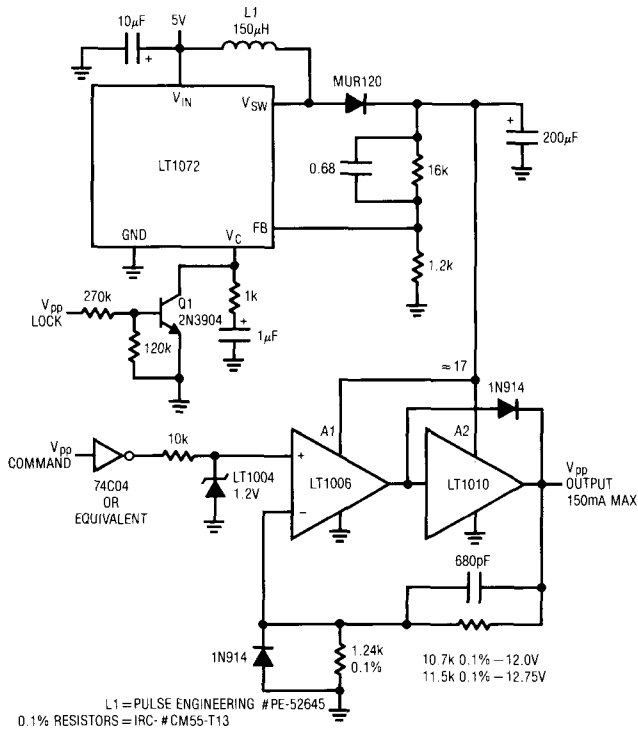


Figure 86. Multi-Output, Transformer Coupled Low Quiescent Current Converter (12V to 5V, ±12V)



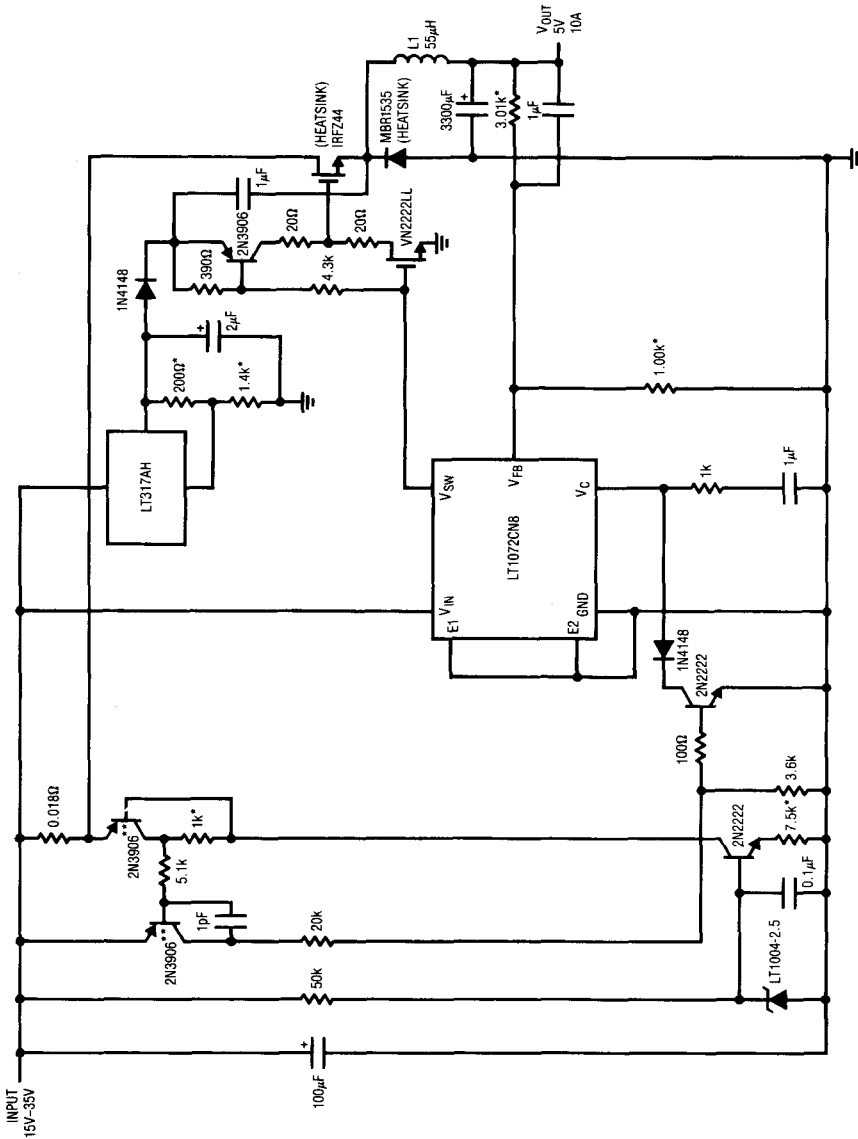
0.1% RESISTORS = IRC- #CM55-T13
 L1 = PULSE ENGINEERING #PE-52645
 * = ZENER DIODE OPTIONAL — SEE TEXT

Figure 87. Basic Flash EPROM Vpp Pulse Generator (5V to 12.75V or 12.00V)



L1 = PULSE ENGINEERING #PE-52645
 0.1% RESISTORS = IRC- #CM55-T13

Figure 88. High Repetition Rate Vpp Pulse Generator (5V to 12.75V or 12.00V)



* = 1% FILM RESISTORS
 IREF244 = INTERNATIONAL RECTIFIER
 L1 = PULSE ENGINEERING, INC. # PE-92117
 ** = V_{BE} MATCHING OF 20mV AT 240μA

Figure 89. High Current Positive Buck with Bootstrapped NMOS Gate Drive (15V-35V to 5V)

Linear Circuits for Digital Systems

Some Affordable Analogs for Digital Devotees

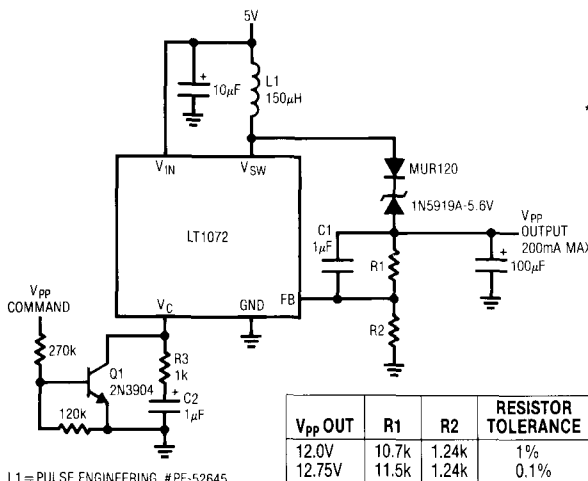
Jim Williams

The pristine, regimented symmetry of digital circuit boards is occasionally interrupted by an irregular huddle of linear components. These aberrants are tolerated because they perform a variety of ancillary tasks necessary to keep the digital system running. While I certainly wouldn't wish lifetime employment on a digital circuit board to anyone*, the reality is that the need exists. Power control, clock circuits and memory management are areas where linear circuits are needed in digital systems. Recently introduced flash memories offer a good example of linear circuits supporting a predominantly digital function. Flash memory adds electrical chip-erase and reprogramming to conventional EPROM capability. A full chip erasure takes 1 second with 100 μ s byte-program times and 4 seconds for full chip programming. These features make flash memories an attractive non-volatile memory option. Additional information on these devices appears in Appendix A, "A Primer on Flash Memory," guest written by Saul Zales of Intel Corporation.

These devices require carefully controlled, high voltage programming power. A typical unit, the Intel 28F010 1 megabit flash memory, specifies V_{PP} ($V_{PROGRAM\ POWER}$) pulses of $12V \pm 0.6V$ or $12.75V \pm 0.2V$, depending on part type. V_{PP} excursions beyond 14V (for 20ns or longer) will destroy the ETOX[†] process based device. Reliably generating such pulses in a 5V powered digital system involves several analog issues. High voltage must be derived and controlled within the tight tolerances noted (see Appendix B for an expanded discussion of this topic). Additionally, it is desirable to control the high voltage pulses from a 5V logic command.

Basic Flash Memory Programming Voltage Supply

Figure 1's circuit meets almost all flash memory V_{PP} requirements. When the V_{PP} command goes low (Trace A, Figure 2) the LT1072** switching regulator drives L1, producing high voltage. DC feedback occurs via R1 and R2,



*I suppose it's not all that bad. Some of my best friends are digital circuits. If I had a daughter, I'd even consider letting her go out with one.

[†]ETOX is a trademark of Intel Corporation.

**See Appendix C and References for detailed information on the LT1072.

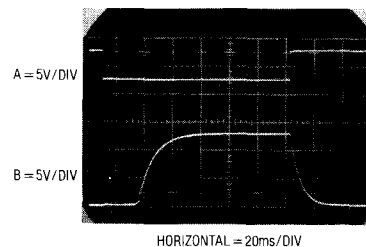


Figure 1. Basic Flash Memory V_{PP} Programming Voltage Supply

Figure 2. Waveforms for Basic Flash Programming Supply

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with AC roll-off controlled by C1 and R3-C2. The result is a smoothly rising V_{pp} (Trace B) which settles to the required value. The specified R1 values allow either 12.0V or 12.75V outputs. The 5.6V zener permits the output to return to 0V when the V_{pp} command goes high. It may be deleted in cases where a 4.5V minimum output is acceptable or desirable (see Intel 28F010 datasheet). Precision resistors combine with the LT1072's tight internal reference to eliminate circuit trimming requirements. Alternately, 1% resistors and a trimmer may be used. Additionally, this circuit will not spuriously overshoot during power-up or down, preventing memory destruction. Figure 3's table details circuit changes permitting higher power outputs. The synchronous switch option can be used to eliminate the zener and its attendant power dissipation.

High Repetition Rate V_{pp} Programming Supplies

Figure 1's repetition rate is limited because the regulator must fully rise and settle for each V_{pp} command. Figure 4's circuit serves special cases which require higher repetition rate. Here, the switching regulator runs continuously, with the V_{pp} generated by the A1-A2 loop. If desired, the V_{pp} lock line can be driven, shutting down the regulator to preclude any possibility of inadvertent V_{pp} outputs. When V_{pp} lock goes low (Trace A, Figure 5) the LT1072 loop

comes on (Trace B), stabilizing at about 17V. 2 pole compensation ensures a clean rise time. Pulling the V_{pp} command line low causes the 74C04 (Trace C) to bias the LT1004 reference. The LT1004 clamps at 1.23V with A1 and A2 giving a scaled output (Trace D). The 680pF capacitor controls loop slewing, eliminating overshoots. Figure 6 details the V_{pp} output. Trace A is the 74C04 output, with Trace B showing clean V_{pp} characteristics.

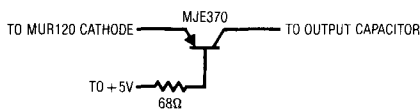
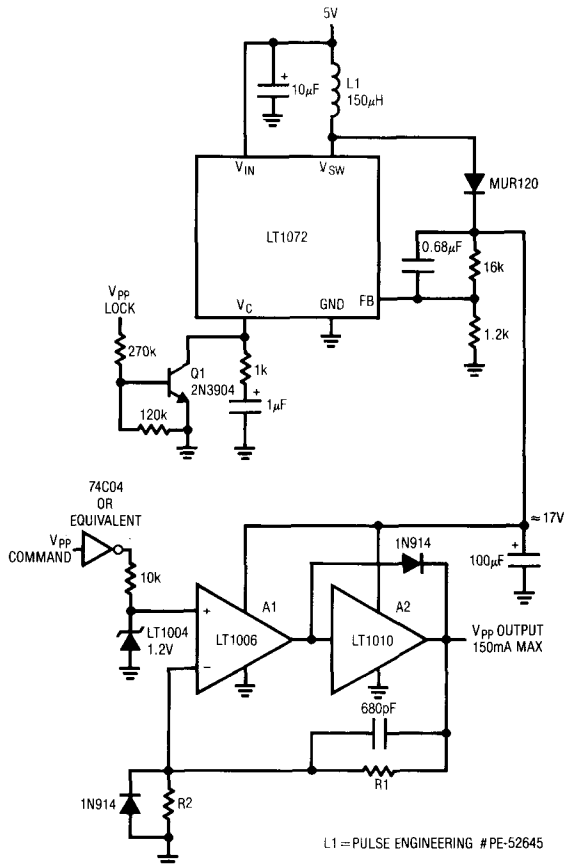


Figure 3. Synchronous Switch Option

Power Options for Basic V_{pp} Pulse Generator

OUTPUT CURRENT	C_{OUT}	REGULATOR	INDUCTOR	ZENER
400mA	200 μ F	LT1071	PE-52645	1N5339A or Synchronous Switch Option
800mA	400 μ F	LT1070	PE-51516	1N5339A or Synchronous Switch Option

Note: Assume each 28F010 device requires 30mA of V_{pp} current.



V_{pp} OUT	R1	R2	RESISTOR TOLERANCE
12.0V	10.7k	1.24k	1%
12.75V	11.5k	1.24k	0.1%

Figure 4. High Repetition Rate V_{pp} Programming Supply

As in Figure 1, spurious V_{pp} outputs are suppressed during power-up or down. The LT1010 provides 150mA drive (5 28F010's) and short circuit protection. The diode path around the LT1010 prevents destructive overshoot when the circuit is recovering from output shorts. The diode at A1's input clips excessive negative voltages due to the 680pF unit's differentiated response. Figure 7's circuit is similar to Figure 4's, except that the LT1010 has been replaced with a discrete power output stage, Q2-Q3. Q3 furnishes up to 800mA (26 28F010 memories), with Q2 used for current limiting. The feedback values have been increased, preventing Q2's collector current from causing excessive heating in the grounded resistor. This could occur during prolonged short circuit conditions. The feedback capacitor is re-established accordingly. The circuit's AC dynamics, including a glitchless short circuit recovery, are identical to Figure 4.

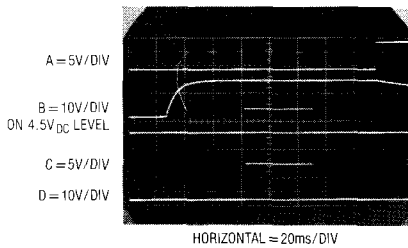


Figure 5. Operating Details of High Repetition Rate Flash Memory Programming Supply

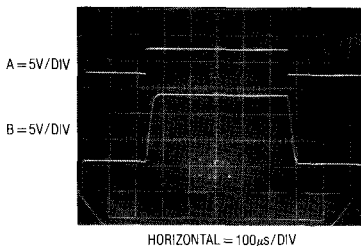
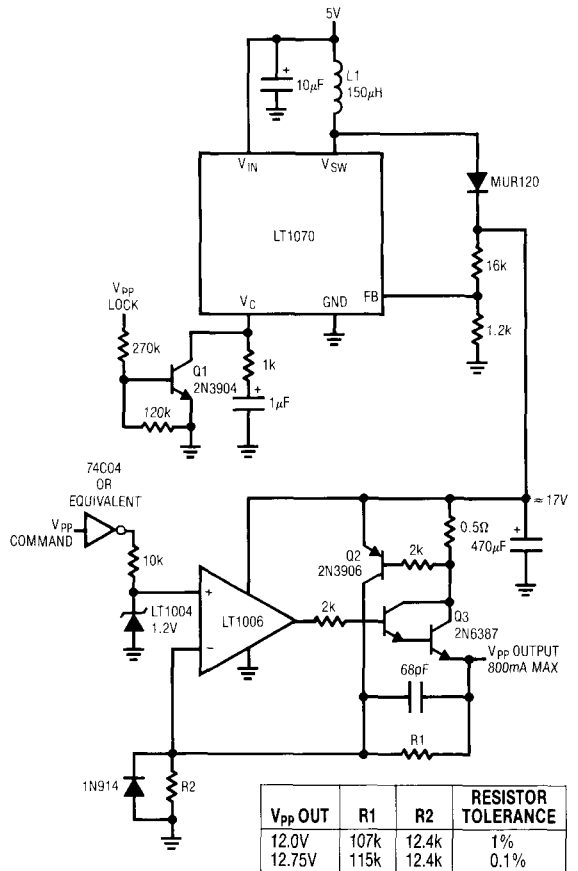


Figure 6. Expanded Scale Display of Figure 4's V_{pp} Output. Controlled Rise Time Eliminates Overshoots

In some systems high voltage is already available. In such cases the LT1070/72 circuitry may be deleted from Figures 4 and 7.

A good question might be: "Why not set the switching regulator output voltage at the desired V_{pp} level and use a simple low resistance FET or bipolar switch?". In theory, this approach will work. In practice, transmission line effects in printed circuit trace runs may cause memory destroying overshoots. Appendix B, "Preventing Memory Destruction," details this phenomenon.



L1 = PULSE ENGINEERING # PE-51516

Figure 7. High Power, High Repetition Rate V_{pp} Pulse Generator

V_{pp} Handshake Circuit

Both V_{pp} circuits shown require a small waiting period for the regulator to settle before proceeding with a V_{pp} operation. In almost all circumstances this is acceptable, but some situations may require verification that V_{pp} is within tolerance before pulsing begins. Figure 8's circuit, used in conjunction with either V_{pp} circuit, gives a handshake output when V_{pp} has settled. This simple circuit works by comparing the V_{pp} output against the known LT1004 reference voltage. The resistor values given allow for possible variations in V_{pp} voltage due to component tolerance stack-up. When this circuit is in use, the output of the V_{pp} generator circuit should be set within 0.4% of nominal value. This can be done by trimming, or using 0.05% resistors in place of the 0.1% units specified.

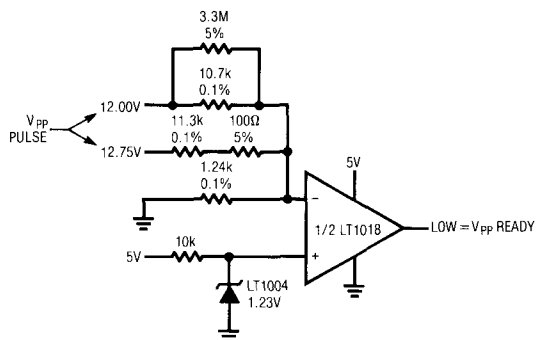


Figure 8. V_{pp} Handshake Circuit

EEPROM V_{pp} Pulse Generator

EEPROMs do not offer the advantages of flash memories, but are sometimes used. Their V_{pp} pulse requirements have commonalities with flash types. The 2816 specifies 21V ± 1V V_{pp} amplitude with a maximum allowable voltage of 22.5. A special EEPROM stipulation is that the V_{pp} pulse must have a 600μs rise time. Figure 9's circuit meets these requirements. The LT1072 generates the high voltage while A1 and A2 form the actual V_{pp} pulse. With the

Erase/Write lock line low (Trace A, Figure 10), the LT1072 is in standby; no high voltage is produced and there is no circuit activity. Under these conditions the V_{pp} output line is pulled towards +5V via the 1N914 diode (see 2816 data-sheet for details). When the Erase/Write lock line (Trace A, Figure 10) goes high, the regulator output (Trace C) builds smoothly and regulates at 25V. The 2 pole LT1072 compensation allows the regulator output to rise relatively quickly. When the V_{pp} command line (Trace B) is pulsed high, the LT1004 reference clamps at 1.23V and the RC network delivers a 600μs edge to A1's input. A1 combines with power buffer A2 and the feedback resistors to produce a 21V pulse at the V_{pp} output (Trace D). Trace E is a time and amplitude expanded version of this pulse. The 600μs RC rise time condition is met, with the 21V amplitude assured by the LT1004 reference and closed loop operation. When the V_{pp} command goes low, the V_{pp} output returns cleanly to 4.5 V. The diode path speeds recovery of the 0.005μF capacitor at A1's input. A2 provides a 150mA (ten 2816 EEPROMs) output with short circuit protection. As in Figure 4, a diode path around the LT1010 prevents overshoot when the circuit is recovering from output shorts. When the Erase/Write lock line returns low, the regulator output decays towards zero. As with the other V_{pp} circuits, this design does not produce undesired outputs during power-up or down.

5V Powered 4-20mA Current Loop Generator

Figure 11's circuit also employs voltage step-up, but for a different purpose. Transmission of industry standard 4-20mA current loop signals to valves and other actuators is a common requirement. Resistive line losses and actuator impedances require current transmitters to be able to force a compliance voltage of at least 20V. Because of this, 5V powered systems usually cannot meet current loop transmitter requirements, but Figure 11 shows a way to do this. This 5V powered circuit utilizes a servo controlled DC-DC converter to generate the compliance voltage necessary for loop current requirements. It will drive 4-20mA into loads as high as 2200Ω (44V compliance) and is inherently short circuit protected. Its digital inputs permit easy interface to digital systems.

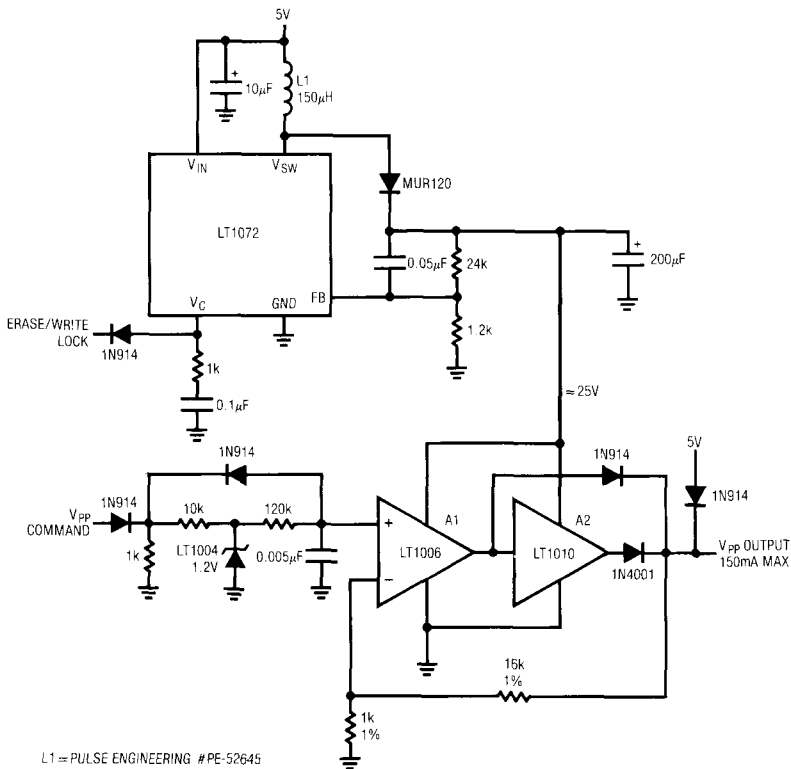


Figure 9. EEPROM V_{pp} Pulse Generator

The AD558 8 bit D→A converter receives the circuit's digital inputs, producing a 2.56V full-scale output. A1's positive input voltage is determined by the D→A output and the 4mA trim network output. A1's output biases the LT1072's V_C pin. This forces the switching regulator to run at the output voltage necessary to balance A1's inputs. The feedback path for this action is through the load, across the 75Ω resistor and back to A1's negative input. The 240Ω-0.05µF combination stabilizes the loop. The 7.5V zener permits regulator output down to 0V. The resistors connected to the LT1072's feedback (FB) pin prevent circuit output from running away in the event the load opens up. Normally, A1 controls the loop, forcing the LT1072 to produce the voltage required to maintain the D→A directed current through the load. If the load opens, A1 receives no feedback, but the FB pin becomes active at 1.2V, forc-

ing the loop to close locally around the LT1072. In this fashion the circuit automatically crosses over from a current to a voltage regulator, preventing excessive output voltages from occurring.

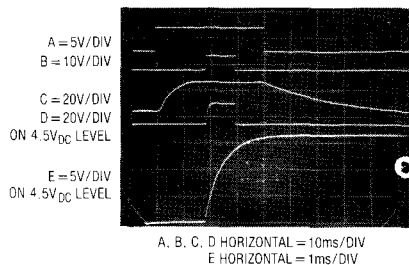


Figure 10. EEPROM Pulse Generator Waveforms

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Figure 12 details LT1072 operation under normal conditions. Trace A is V_{SWITCH} pin voltage, while Trace B indicates its current. Trace C, the MUR120 diode current, clearly shows the switched packets of energy delivered to the $22\mu\text{F}$ output capacitor. The resultant output ripple voltage (Trace D) measures only 25mV at the load.

Figure 13 catches circuit output at the instant a load open has occurred. Normal current mode operation ceases just past the third vertical division. The “+” output line heads positive until the LT1072 FB pin rises to 1.2V. At this point (just past the 6th vertical division), the LT1072’s internal feedback amplifier activates, causing local loop closure and regulating the output at about 57V. The non-linear slew characteristic is due to A1’s feedback capacitor re-

strained response. Once A1’s output rails, slew increases to a limit imposed by L1, the $22\mu\text{F}$ output capacitor and the LT1072’s 40kHz switching rate.

To trim this circuit, connect any load below $2\text{k}\Omega$ and set all DAC bits low. Adjust the 4mA trim for 0.300V across the 75Ω resistor. Next, put all DAC bits high and set the 20mA trim for 1.500V across the 75Ω resistor. Repeat this procedure until both points are fixed.

AC Line Dropout Detector

Digital systems driven from the AC line often require power dropout detection. Fast AC line dropout detection allows a memory store command to be issued before DC

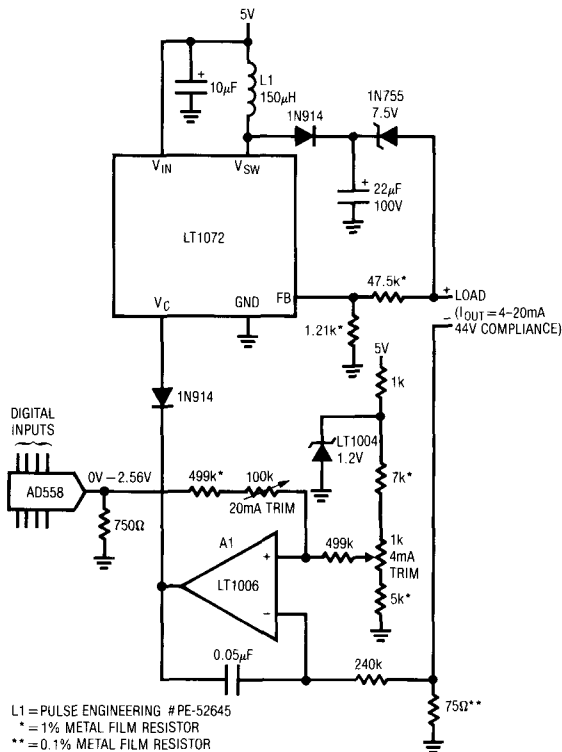


Figure 11. 5V Powered, Digitally Controlled 4–20mA Current Loop Generator

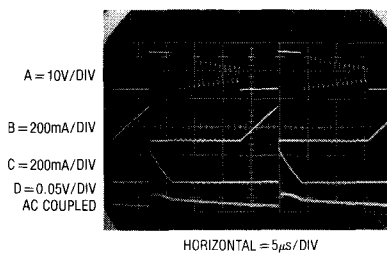


Figure 12. Figure 11’s Waveforms

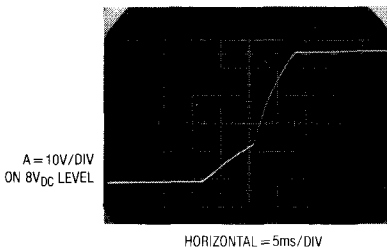


Figure 13. Open Load Characteristics for Figure 11’s Current Source. LT1072 Crosses over into Constant Voltage Mode at 57V

power falls. Figure 14's circuit detects AC dropout by connecting an optoisolator across the power transformer's rectified secondary. Normally, the AC line (Trace A, Figure 15) turns on the LED every 8ms (1/2 cycle of the line), causing the output transistor to reset the 0.01 μ F capacitor (Trace B). When the line drops out, the capacitor charges via the 33k resistor. The resultant ramp voltage is compared by C1A to a +5V supply derived reference. In this case, the 2k-3k resistors bias C1A to go low (Trace C) within one cycle of AC line dropout. Typically, the DC regulator will supply 50ms-100ms of hold-up before it begins to sag.

This hold-up period, which should be verified in any individual application, permits adequate time to execute a memory store operation. C1B serves as a final warning that power failure is imminent. It goes low when the 5V regulator input drops below the threshold set by the selected resistor shown on the schematic. This value should be chosen so that C1B trips when the regulator input approaches its specified dropout voltage.

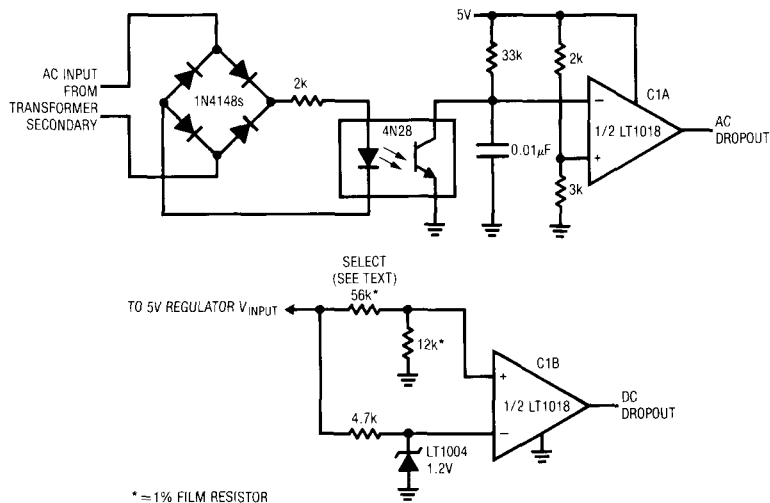


Figure 14. AC-DC Dropout Detector

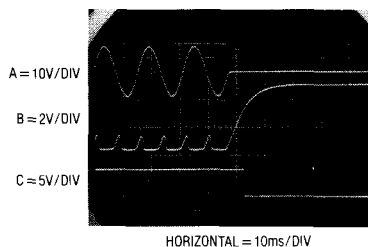


Figure 15. AC Line Dropout Detector Operates within a Half Cycle

Application Note 31

Memory Save Circuit

Figure 16 is another circuit for saving memory contents when power goes down. This DC sensing circuit is useful where AC line dropout detection is not feasible. It functions by utilizing the different dropout voltages of two regulators. In operation, the LT1086 supplies 5V power to the main system, while the LT1020 drives the memory section. When input power, which could be from a battery or filter capacitor, falls (Trace A, Figure 17) the LT1086 drops out first (Trace B). This is detected by the LT1020's on-board auxiliary comparator, which goes low (Trace C). This alerts the memory section to store data. The LT1020 regulator output (Trace D) maintains memory power for additional time due to its extremely low dropout characteristics. It finally begins to fall about 50ms after the memory store command. The optional connections shown allow extended hold up times.

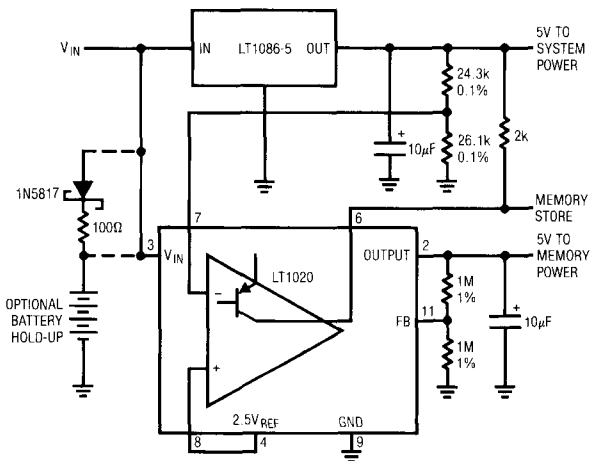


Figure 16. Memory-Save-On-Power Down

Overvoltage Protection Circuit

Figure 18's circuit represents the other extreme in power supply protection. It prevents system damage due to overvoltage produced by regulator failure. If the regulator fails in a way which effectively connects the raw DC supply to the 5V rail, overvoltage will occur. This failure mode is possible if the pass transistor shorts or the feedback loop opens up. C1A compares the 5V supply (Trace A, Figure 19) to the LT1004 reference via a resistive divider. If the supply rises beyond 5.5V (rise starts just past the first vertical division), C1A's output goes high (Trace B), turning on the SCR via Q1. SCR current (Trace C) peaks at almost 6A as it "crowbars" the supply, blowing the downstream fuse. C1B simultaneously pulls the supply feedback node low, ensuring minimum pass transistor on-resistance if the overvoltage is due to feedback or error amplifier malfunction. About 5μs elapses from the time the supply peaks (5.5V) until it begins to shut down. In this case the maximum overvoltage is 5.7V. The 4.3k-1.2k resistor string ratio can be altered for different trip values, and the optional filter used to suppress transients. Note that the LT1018's 1.2V minimum supply voltage combines with the diode in the SCR's gate to eliminate false tripping on power-up.

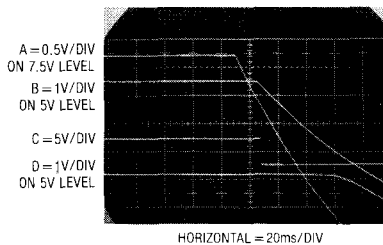


Figure 17. Differential Dropout Between Regulators Provides a Memory Store Pulse and Power Hold-Up

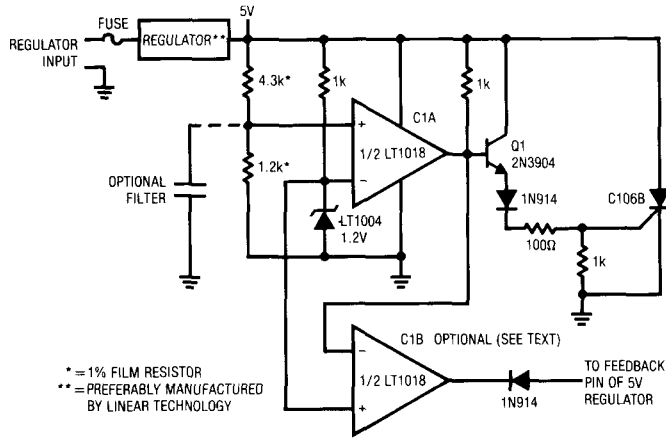


Figure 18. "Crowbar" Overvoltage Protection Circuit

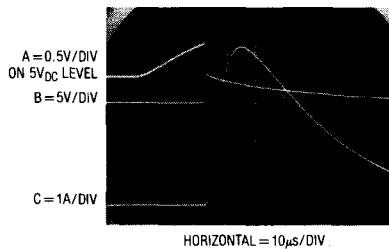


Figure 19. "Crowbar" Stops Overvoltage in 5μs

Power-On-Reset Generator

Another power related requirement involves generating a system reset pulse after supply turn-on. When supply power is applied to Figure 20, the 5V rail comes up (Trace A, Figure 21). The LT1004 clamps at 1.2V and C1A's positive input (Trace B) ramps at a time constant determined by the 0.5% resistors and the 0.1μF capacitor. When C1A's positive input ramps beyond the LT1004 potential, its output goes high, delivering a differentiated pulse to C1B's negative input (Trace C). C1B's output (Trace D) goes low for a period determined by the 0.01μF-680k differentiator. This pulse is used for system reset. The 1N914 gives quick reset for the 0.1μF delay capacitor and the Schottky diode clip's differentiator

caused negative voltages at C1B's input. The turn-on threshold, in this case 4.8V, is set by the ratio of the 0.5% resistors. The output pulse delay time is controlled by the 0.1μF unit, which may be varied. Similarly, the RC combination at C1B sets output pulse width, and may be varied. The LT1018's 1.2V minimum supply voltage prevents spurious output during supply power-up.

"Watchdog" Timer Circuit

Figure 22's circuit is not for power supply management, but serves to prevent lock-up in processor based systems. This can occur if the system misses an instruction due to transient hardware or software events. Such a processor hang-up will usually cause predictable cessation of pulse events somewhere in the system. This circuit issues a reset command in response to such a cessation. In normal operation, a pulse train (Trace A, Figure 23) appears at the circuit input, causing C1A's output (Trace B) to pulse low. The diode path discharges the 0.01μF capacitor (Trace C) each time C1A's output goes low. Interruption of the input pulse train (after the 7th vertical division) allows the capacitor to charge beyond C1B's threshold, triggering it low. This pulse can be used to reset the system. C1B's negative input RC values may be adjusted to accommodate various input pulse train repetition rates.

Application Note 31

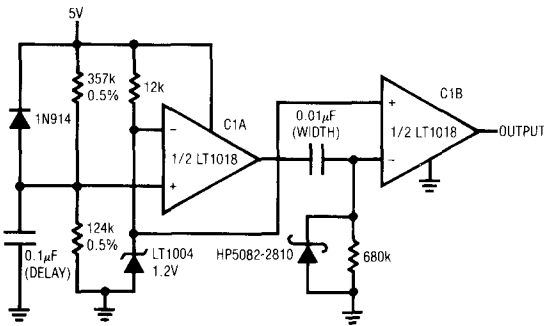


Figure 20. Power-On-Reset Pulse Generator

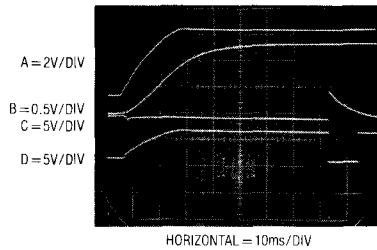


Figure 21. Power-On-Reset Pulse is Generated after Supply Stabilizes

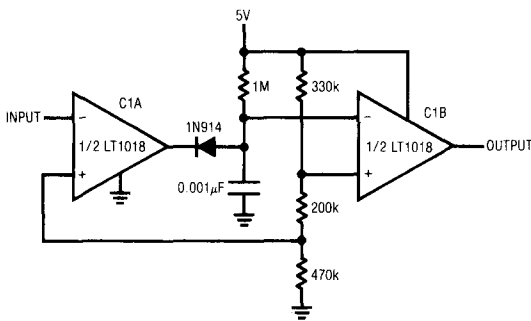


Figure 22. "Watchdog" Timer Circuit

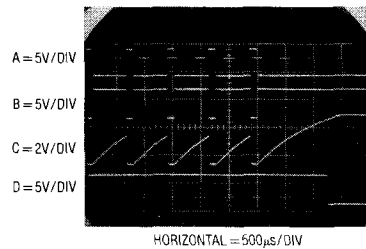


Figure 23. "Watchdog" Drops Low (Trace D) when Pulse Train Ceases

Clock Circuits

Almost all digital systems require a clock source. Generating accurate and reliable clock pulses usually involves quartz based circuits. Figure 24's two circuits cover a 1MHz-25MHz range. In Figure 24A, the LT1016 comparator is set up with DC negative feedback. The 2k resistors set the common-mode level at the device's positive input. Without the crystal, the circuit may be considered as a very wideband (50GHz GBW) amplifier biased at 2.5V. With the crystal inserted, positive feedback occurs and oscillation commences. Figure 24A is useful with AT-cut funda-

mental mode crystals up to 10MHz. Figure 24B is similar, but supports oscillation frequencies to 25MHz. Above 10MHz, AT-cut crystals operate in overtone mode. Because of this, oscillation can occur at multiples of the desired frequency. The damper network rolls off gain at high frequency, ensuring proper operation.

Figure 25's circuit is also similar, but optimized for lower frequency crystals. C1A is the oscillator, with C1B and Q1 used as a sink-source buffer if desired. These circuits also operate with lower cost and lower performance ceramic resonators substituted for the crystal.

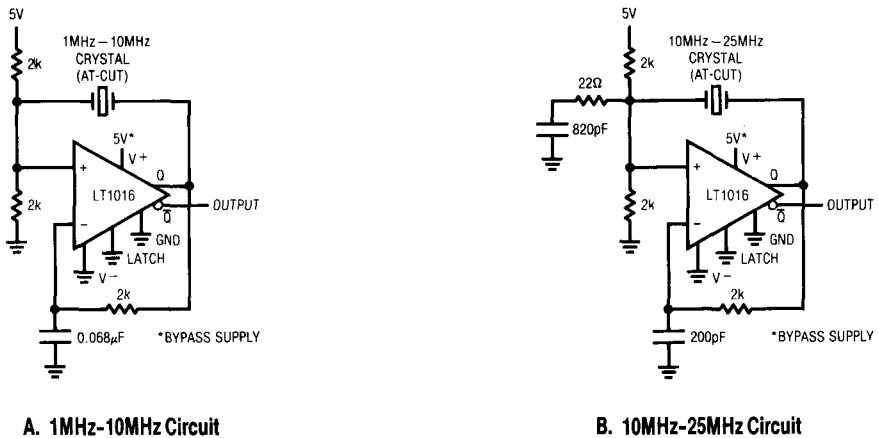


Figure 24. Crystal Oscillator Clock Circuits

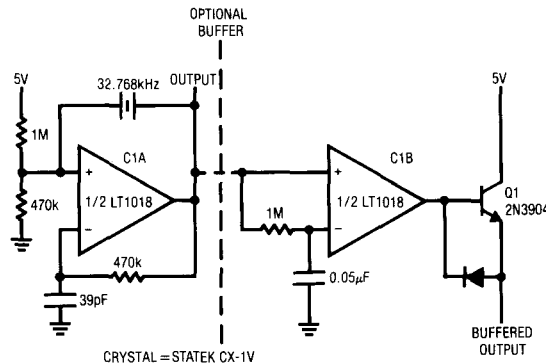


Figure 25. Low Frequency Crystal Oscillator Clock

High Noise Immunity Line Synchronous Clock

Although crystal based circuits are universally applied, they cannot serve all clock requirements. As an example, many systems require a reliable 60Hz line synchronous clock. Zero crossing detectors or simple voltage level detectors are often employed, but have poor noise rejection characteristics. The key to achieving a good line clock under adverse conditions is to design a circuit which takes advantage of the narrow bandwidth of the 60Hz fundamental. Approaches utilizing wide gain-bandwidth, even if hys-

teresis is applied, invite trouble with noise. Figure 26 shows a line synchronous clock which will not lose lock under noisy line conditions. The basic RC multivibrator is tuned to free run near 60Hz, but the AC-line-derived synchronizing input forces the oscillator to lock to the line. The circuit derives its noise rejection from the integrator characteristics of the RC network. As Figure 27 shows, noise and fast spiking on the 60Hz input (Trace A, Figure 27) has little effect on the capacitor's charging characteristics (Trace B) and the circuit's output (Trace C) is stable.

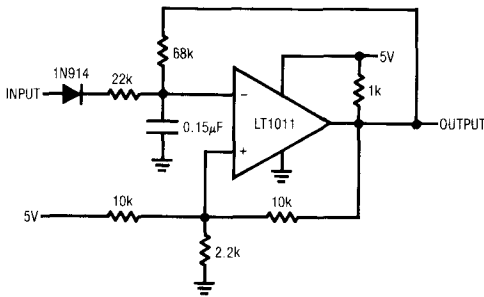


Figure 26. High Noise Immunity Line Synchronization Circuit

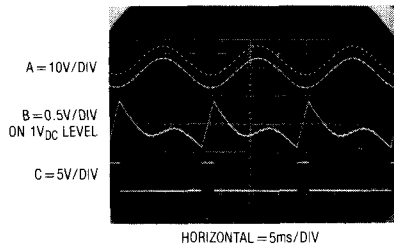


Figure 27. Line Synchronization is Maintained Despite Noisy Input

Note: This application note was derived from a manuscript originally prepared for publication in EDN magazine.

APPENDIX A A Primer on Flash Memory

Saul Zales
Intel Corporation

High integration, supported by dense memory, is the key to compact, reliable firmware-based equipment. These products often need post-sales update service for the latest software revisions. While providing high density, EPROMs are costly to update. Equipment must be dismantled, either to UV-erase and then reprogram the EPROMs or to replace them with new ones. This takes at least 15 minutes of a technician's time. Double that if you wait for UV erasure. In contrast, flash memories allow reprogramming "in-system" — in seconds. They are not discarded as EPROMs often are. The simplicity and speed of

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the update process yields even bigger savings. Thus, flash memory technology dramatically reduces firmware update costs in EPROM applications.

Non-volatile memory history illustrates flash memory technology's utility. EPROM gave users more control over their code than with ROM by moving the memory coding operation from component purchasing to factory assembly. Similarly, flash technology extends this flexibility. In the factory, it allows multiple test code programming during a single board-testing step. Testing enhances product quality while reducing rework and warranty repair costs.

Beyond the factory, flash technology provides the highest level of code management functionality. Though E²PROM has more functions, its characteristics best suit parameter, as opposed to code, storage. Parameters need to be rewritten individually in real time, that is, while the system is on-line, in normal operation. Parameters also require less memory than code. E²PROM trades off density for the byte-alterable functionality needed for parameter storage.

In contrast, flash memories ideally match embedded code needs. Even if only one line of code needs modification, an entirely new microcomputer program results. Software updates are done as a complete copy for simple code verification. This ensures error-free updating. Flash memory technology mirrors this process with its full-chip erase characteristics in a few seconds of off-line system time.

This framework for delineating non-volatile memory roles is summarized in Figure A1. ROM, EPROM, and flash memory handle large amounts of code, which is installed or modified (excepting ROM) off-line, along an 'increasing flexibility' scale. E²PROM handles smaller amounts of on-line-modified parameters.

The most powerful reprogramming method is In-System Write (ISW). ISW eliminates external programming equipment altogether. It facilitates updates through an existing data communication channel, such as a modem. ISW utilizes the embedded, local CPU for the flash memory device

reprogramming 'intelligence,' taking advantage of the off-line nature of updates. The only new requirement for ISW is providing a local programming power supply (V_{pp}), either 12.0V or 12.75V, depending on device specifications. Intel's command register architecture drives reprogramming control: 1) without extra device pins, 2) from a fixed V_{pp} supply, and 3) using standard system read and write timings (though some operations require millisecond-range durations, they are initiated and terminated with standard memory interface timings). See Figure A2 for system block diagram.

Reliability

Intel's ETOX flash memory devices endure up to 10,000 reprogramming cycles, just like E²PROM, yet with EPROM-like quality. The cycling advantage over E²PROM is derived partly from lower-voltage operation. This reduces the electric field intensity across the tunnel oxide by about 2 megavolts per centimeter. Each MV/cm electric field reduction increases the device reliability lifetime by at least one thousand (and as much as ten million) times.

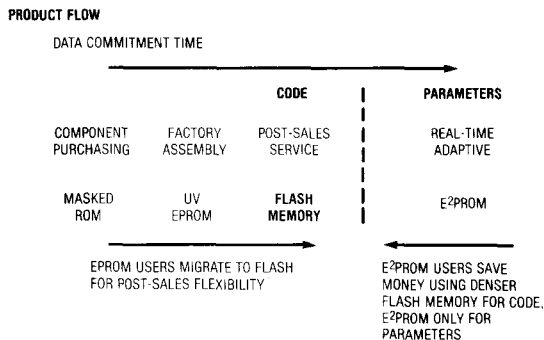


Figure A1. Non-Volatile Memory Flexibility Spectrum

In-System Write Minimizes Update Cost

- Local CPU Provides Programming Intelligence
- Flash Memory Stores Application Code and Configuration Files
- Update from Floppy Disk or Remote Serial Link

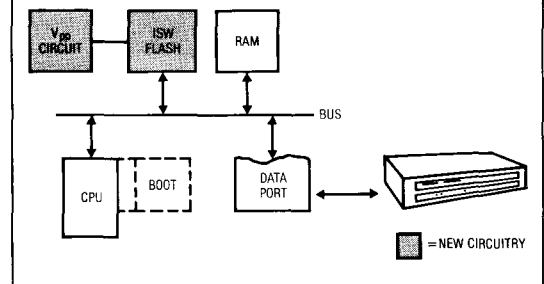


Figure A2. In-System Write

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The common-source approach for erasure is another key contributor. Unlike other E²PROM and flash technologies, ETOX technology uses separate junctions for program and erase which yields: 1) much lower oxide stress, and 2) the ability to optimize the manufacturing process for both program and erase performance and durability. Finally, cycling and overall reliability of ETOX technology-based products is enhanced by the tunnel oxide process employed.

Intel specifies flash memory endurance to be less than 0.01% failures over 100 cycles and 0.1% for 10,000 cycles. In contrast, E²PROMs typically specify 5% failure rates for 10,000 cycles. Lifetime reliability testing of the data retention shows that ETOX technology meets or exceeds EPROM reliability.

APPENDIX B Preventing Memory Destruction

The 12V or 12.75V V_{pp} supplies used with flash memories seem uncomfortably close to the devices 14V breakdown limit. In actuality, the precautions required are similar to overvoltage considerations for 5V rails. Excursions beyond 14V for durations longer than 20ns exceed the chip's absolute maximum rating. As such, the design of V_{pp} generating circuitry requires care to avoid seemingly mysterious memory failures. Although this section uses the 28F010 flash memory as an example, the considerations are generally applicable to other type devices (e.g., 2816).

In theory, a simple low loss transistor switching a low impedance power supply will work. In practice, this is a hazardous approach. Figure B1 shows an ideal V_{pp} pulse produced by simple transistor switching from a power

supply. Settling to the desired V_{pp} level occurs quickly, with no overshoots or aberrations. Figure B2 shows *the same output* measured at the memory pins after a printed circuit trace run. The PC trace looks like an unterminated transmission line with ill-defined characteristics. Reflections occur, causing ringing which exceeds 20V. This is well beyond specified destructive levels, and almost guarantees chip failures. Similar overshooting on the falling edge can cause equally destructive negative voltages to appear at the memory pins.

These effects demonstrate the necessity for rise time control. The controlled edge times of the text's closed loop circuits eliminate this problem. Some other features of these circuits make them attractive. Short circuit protection is obviously desirable to protect the V_{pp} generator.

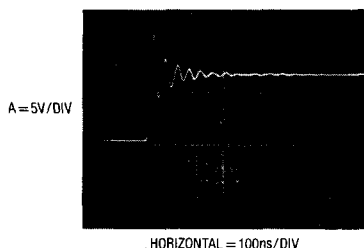
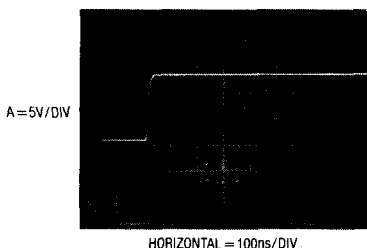


Figure B1. An "Ideal" Flash Memory V_{pp} Output Figure B2. Rings at Destructive Voltages After a PC Trace Run

More subtly, it also protects the memory. In an unprotected V_{PP} generator, the pass switch may fail in a shorted condition. This will cause the memory to see destructive overvoltage and fail. The short circuit protection must be designed so that it does not cause overshoots when operating or recovering from overload. For example, removing A2's shunt diode path in text Figure 4 causes dangerous overshoots on short circuit recovery. Figure B3 shows V_{PP} output recovery with the diode removed. In

Figure B4, the diode is installed and recovery is benign. Similar considerations apply on power-up and down. The V_{PP} generator must not produce spurious outputs during power application or removal. In the text circuits, this is facilitated by employing circuit techniques and ICs which operate down to low voltages. This makes V_{PP} outputs predictable and controllable during transient supply conditions.

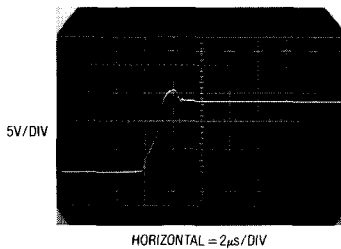


Figure B3.

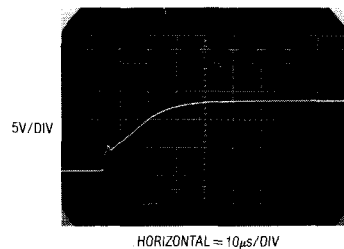


Figure B4.

Short Circuit Recovery for Poorly (Figure B3) and Properly (Figure B4) Designed Connections. Figure B3's Overshoot on Recovery Can Cause Memory Chip Failures

APPENDIX C

Physiology of the LT1070/LT1071/LT1072

The LT1070 series is a family of current-mode switchers with switch duty cycle directly controlled by switch current rather than by output voltage. Referring to Figure C1, the switch is turned on at the start of each oscillator cycle. It is turned off when switch current reaches a predetermined level. Control of output voltage is obtained by using the output of a voltage-sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike ordinary switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at mid-frequencies in the energy storage inductor. This greatly simplifies closed loop frequency compensation under widely varying input voltage or

output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short circuit conditions. A low dropout internal regulator provides a 2.3V supply for all internal circuitry on the LT1070. This low dropout design allows input voltage to vary from 3V to 60V with virtually no change in device performance. A 40kHz oscillator is the basic clock for all internal timing. It turns on the output switch via the logic and driver circuitry. Special adaptive antisaturation circuitry detects onset of saturation in the power switch and adjusts drive current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

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A 1.2V bandgap reference biases the positive input of the error amplifier. The negative input is brought out for output voltage sensing. This feedback pin has a second function; when pulled low with an external resistor, it programs the LT1070 to disconnect the main error amplifier output and connects the output of the flyback amplifier to the comparator input. The LT1070 will then regulate the value of the flyback pulse with respect to the supply voltage. This flyback pulse is directly proportional to output voltage in the traditional transformer-coupled flyback topology regulator. By regulating the amplitude of the flyback pulse, the output voltage can be regulated with no direct connection between input and output. The output is fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings. A special delay network inside the LT1070 ignores the leakage inductance spike at the leading edge of the flyback pulse to improve output regulation.

The error signal developed at the comparator input is brought out externally. This pin (V_C) has four different functions. It is used for frequency compensation, current limit adjustment, soft-starting, and total regulator shutdown. During normal regulator operation this pin sits at a voltage between 0.9V (low output current) and 2.0V (high output current). The error amplifiers are current output (gm) types, so this voltage can be externally clamped for adjusting current limit. Likewise, a capacitor-coupled external clamp will provide soft-start. Switch duty cycle goes to zero if the V_C pin is pulled to ground through a diode, placing the LT1070 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown with only 50 μ A supply current for shutdown circuitry biasing. For more details, see Linear Technology Application Note AN-19, pages 4-8.

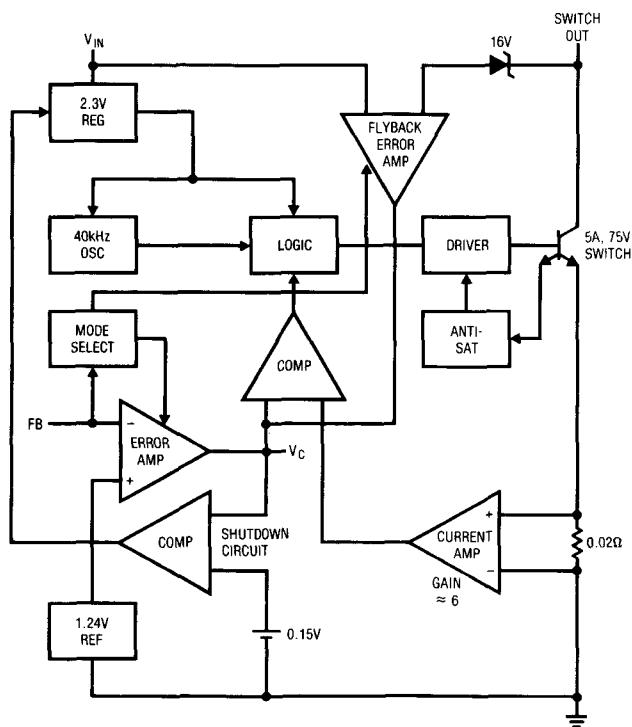


Figure C1. LT1070 Internal Details

High Efficiency Linear Regulators

Jim Williams

Introduction

Linear voltage regulators continue to enjoy widespread use despite the increasing popularity of switching approaches. Linear regulators are easily implemented, and have much better noise and drift characteristics than switchers. Additionally, they do not radiate RF, function with standard magnetics, are easily frequency compensated, and have fast response. Their largest disadvantage is inefficiency. Excess energy is dissipated as heat. This elegantly simplistic regulation mechanism pays dearly in terms of lost power. Because of this, linear regulators are associated with excessive dissipation, inefficiency, high operating temperatures and large heat-sinks. While linears cannot compete with switchers in these areas they can achieve significantly better results than generally supposed. New components and some design techniques permit retention of linear regulator's advantages while improving efficiency.

One way towards improved efficiency is to minimize the input-to-output voltage across the regulator. The smaller this term is, the lower the power loss. The minimum input-output voltage required to support regulation is referred to as the "dropout voltage." Various design techniques and technologies offer different performance capabilities. Appendix A, "Achieving Low Dropout," compares some approaches. Conventional three terminal linear regulators have a 3V dropout, while newer devices feature 1.5V dropout (see Appendix B, "A Low Dropout Regulator Family") at 7.5A, decreasing to 0.05V at 100 μ A.

Regulation from Stable Inputs

Lower dropout voltage results in significant power savings where input voltage is relatively constant. This is normally the case where a linear regulator post-regulates a switching supply output. Figure 1 shows such an arrangement.

The main output ("A") is stabilized by feedback to the switching regulator. Usually, this output supplies most of the power taken from the circuit. Because of this, the amount of energy in the transformer is relatively unaffected by power demands at the "B" and "C" outputs. This results in relatively constant "B" and "C" regulator input voltages. Judicious design allows the regulators to run at or near their dropout voltage, regardless of loading or switcher input voltage. Low dropout regulators thus save considerable power and dissipation.

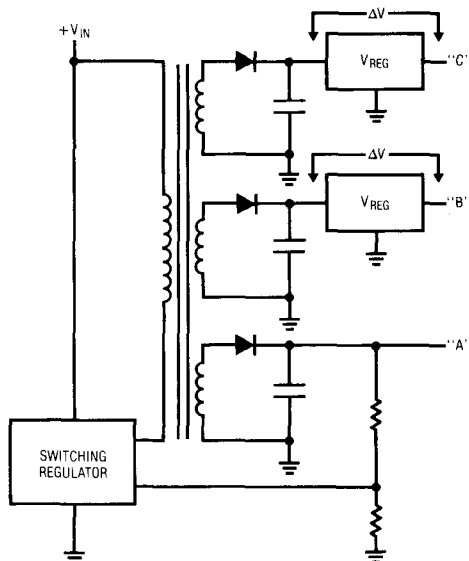


Figure 1. Typical Switching Supply Arrangement Showing Linear Post-Regulators

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Regulation from Unstable Input — AC Line Derived Case

Unfortunately, not all applications furnish a stable input voltage. One of the most common and important situations is also one of the most difficult. Figure 2 diagrams a classic situation where the linear regulator is driven from the AC line via a step-down transformer. A 90VAC (brown-out) to 140VAC (high line) line swing causes the regulator to see a proportionate input voltage change. Figure 3 details efficiency under these conditions for standard (LM317) and low dropout (LT1086) type devices. The LT1086's lower dropout improves efficiency. This is particularly evident at 5V output, where dropout is a significant percentage of the output voltage. The 15V output

comparison still favors the low dropout regulator, although efficiency benefit is somewhat reduced. Figure 4 derives resultant regulator power dissipation from Figure 3's data. These plots show that the LT1086 requires less heatsink area to maintain the same die temperature as the LM317.

Both curves show the deleterious effects of poorly controlled input voltages. The low dropout device clearly cuts losses, but input voltage variation degrades obtainable efficiency.

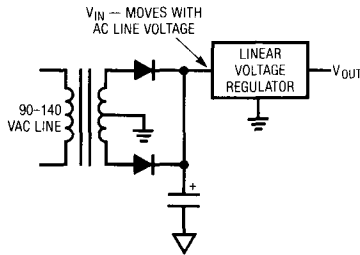


Figure 2. Typical AC Line Driven Linear Regulator

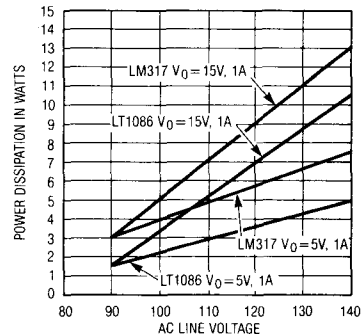


Figure 4. Power Dissipation for Different Regulators vs AC Line Voltage. Rectifier Diode Losses are not included.

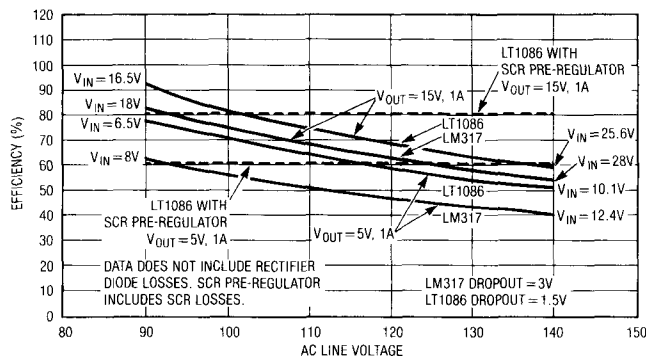


Figure 3. Efficiency vs AC Line Voltage for LT1086 and LM317 Regulators

SCR Pre-Regulator

Figure 5 shows a way to eliminate regulator input variations, even with wide AC line swings. This circuit, combined with a low dropout regulator, provides high efficiency while retaining all the linear regulators desirable characteristics. This design servo controls the firing point of the SCR's to stabilize the LT1086 input voltage. A1 compares a portion of the LT1086's input voltage to the LT1004 reference. The amplified difference voltage is applied to C1B's negative input. C1B compares this to a line synchronous ramp (trace B, Figure 6) derived by C1A from the transformer's rectified secondary (trace A is the "sync." point in the figure). C1B's pulse output (trace C) fires the

appropriate SCR and a path from the main transformer to L1 (trace D) occurs. The resultant current flow (trace E), limited by L1, charges the 4700 μ F capacitor. When the transformer output drops low enough the SCR commutates and charging ceases. On the next half-cycle the process repeats, except that the alternate SCR does the work (traces F and G are the individual SCR currents). The loop phase modulates the SCR's firing point to maintain a constant LT1086 input voltage. A1's 1 μ F capacitor compensates the loop and its output 10 Ω -diode network ensures start-up. The three terminal regulator's current limit protects the circuit from overloads.

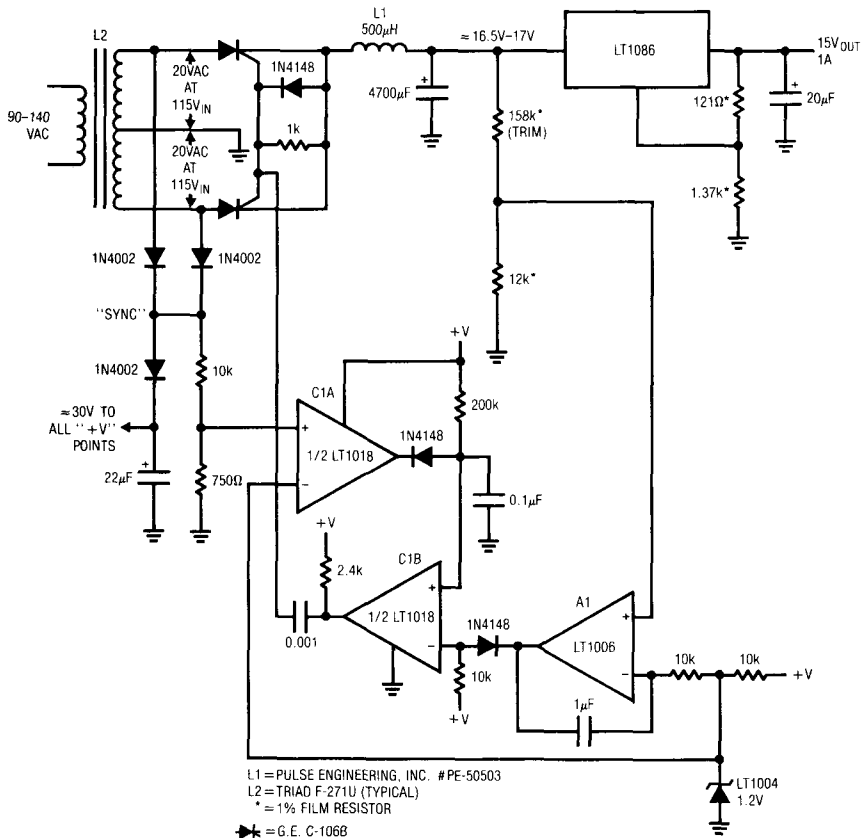


Figure 5. SCR Pre-Regulator

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This circuit has a dramatic impact on LT1086 efficiency vs AC line swing*. Referring back to Figure 3, the data shows good efficiency with no change for 90VAC-140VAC input variations. This circuit's slow switching preserves the linear regulators low noise. Figure 7 shows slight 120Hz residue with no wideband components.

*The transformer used in a pre-regulator can significantly influence overall efficiency. One way to evaluate power consumption is to measure the actual power taken from the 115VAC line. See Appendix C, "Measuring Power Consumption."

DC Input Pre-Regulator

Figure 8A's circuit is useful where the input is DC, such as an unregulated (or regulated) supply or a battery. This circuit is designed for low losses at high currents. The LT1083 functions in conventional fashion, supplying a regulated output at 7.5A capacity. The remaining components form a switched-mode dissipation regulator. This regulator maintains the LT1083 input just above the dropout voltage under all conditions. When the LT1083 input (trace A, Figure 9) decays far enough, C1A goes high,

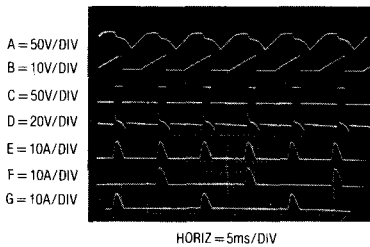


Figure 6. Waveforms for the SCR Pre-Regulator

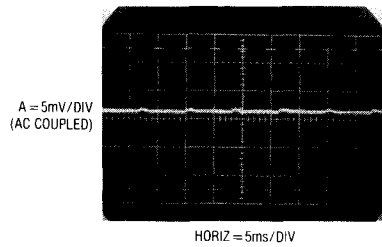


Figure 7. Output Noise for the SCR Pre-Regulated Circuit

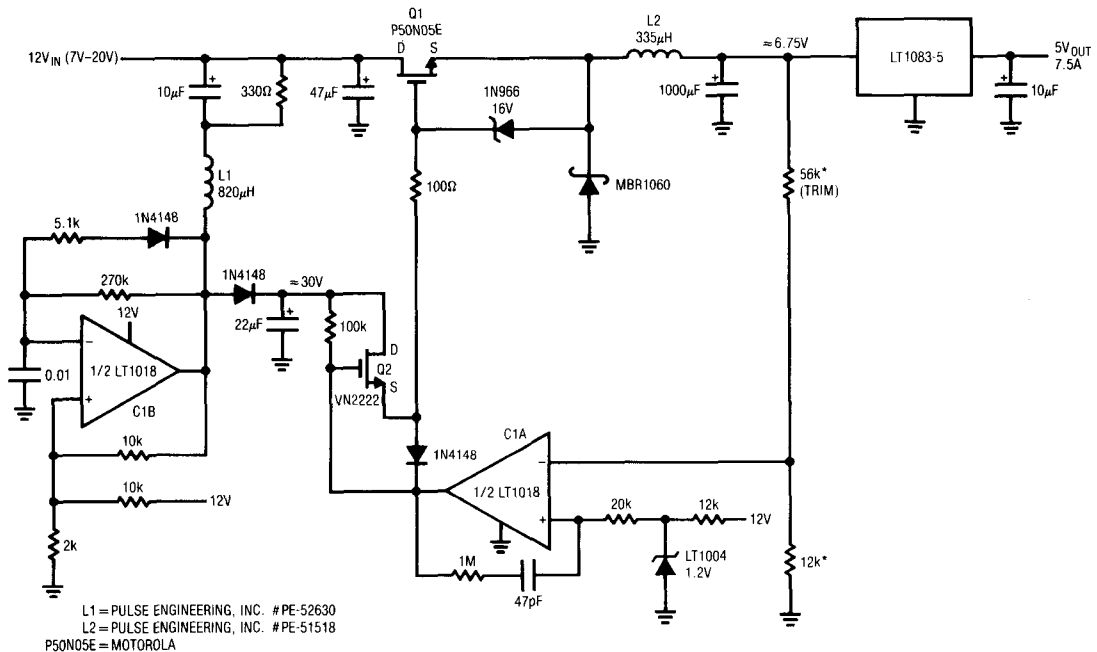


Figure 8A. Pre-Regulated Low Dropout Regulator

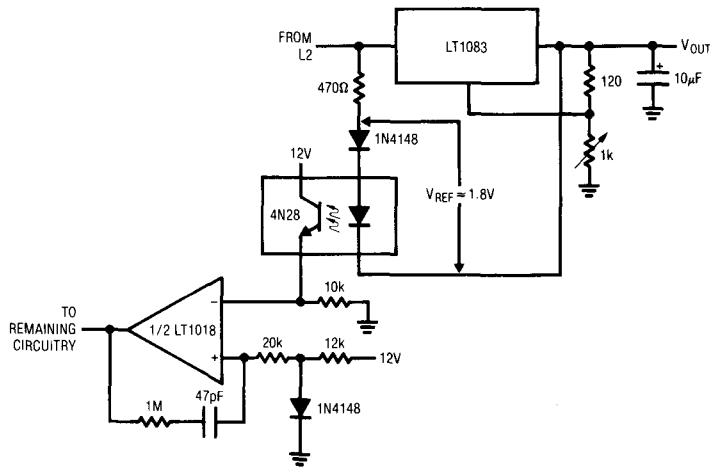


Figure 8B. Differential Sensing for the Pre-Regulator Allows Variable Outputs

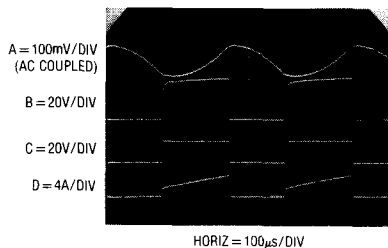


Figure 9. Pre-Regulator Waveforms

allowing Q1's gate (trace B) to rise. This turns on Q1, and its source (trace C) drives current (trace D) into L2 and the 1000 μ F capacitor, raising regulator input voltage. When the regulator input rises far enough C1A returns low, Q1 cuts off and capacitor charging ceases. The MBR1060 damps L2's flyback spike and the 1M–47pF combination sets loop hysteresis at about 100mV.

Q1, an N-channel MOSFET, has only 0.028 Ω of saturation loss but requires 10V of gate-source turn-on bias. C1B, set up as a simple flyback voltage booster, provides about 30V DC boost to Q2. Q2, serving as a high voltage pull-up for C1A, provides voltage overdrive to Q1's gate. This ensures Q1 saturation, despite its source follower connection. The zener diode clamps excessive gate-source overdrives.

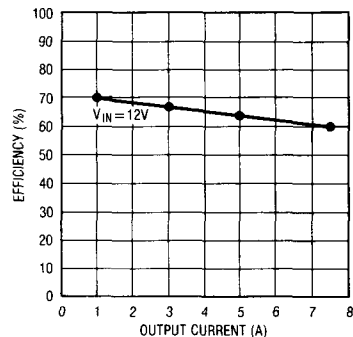


Figure 10. Efficiency vs Output Current for Figure 8A

These measures are required because alternatives are unattractive. Low loss P-channel devices are not currently available, and bipolar approaches require large drive currents or have poor saturation. As before, the linear regulator's current limit protects against overloads. Figure 10 plots efficiency for the pre-regulated LT1083 over a range of currents. Results are favorable, and the linear regulator's noise and response advantages are retained.

Figure 8B shows an alternate feedback connection which maintains a fixed small voltage across the LT1083 in applications where variable output is desired. This scheme maintains efficiency as the LT1083's output voltage is varied.

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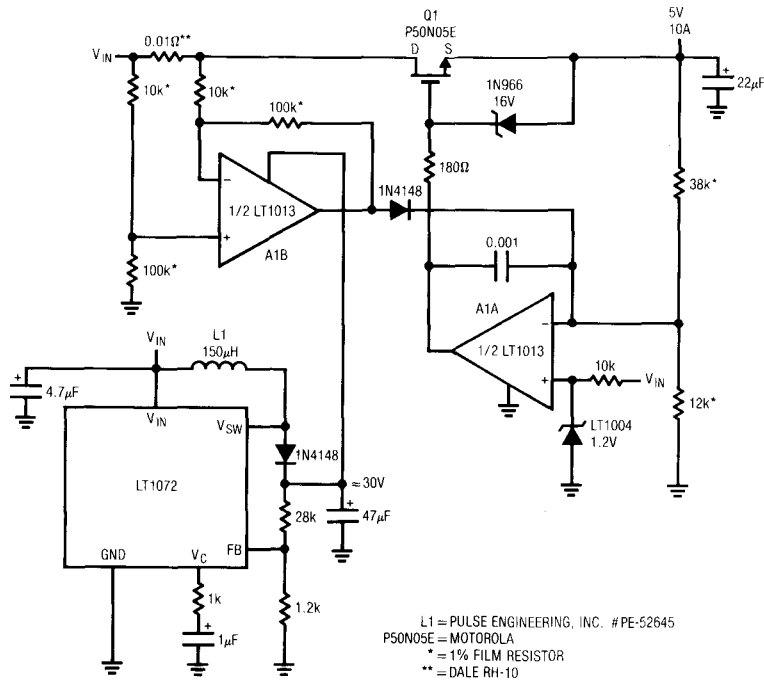


Figure 11. 10A Regulator with 400mV Dropout

10A Regulator with 400mV Dropout

In some circumstances an extremely low dropout regulator may be required. Figure 11 is substantially more complex than a three terminal regulator, but offers 400mV dropout at 10A output. This design borrows Figure 8A's overdriven source follower technique to obtain extremely low saturation resistance. The gate boost voltage is generated by the LT1072 switching regulator, set up as a flyback converter.* This configuration's 30V output powers A1, a dual op amp. A1A compares the regulators output to the LT1004 reference and servo controls Q1's gate to close the loop. The gate voltage overdrive allows Q1 to attain its 0.028Ω saturation, permitting the extremely low dropout noted. The zener diode clamps excessive gate-source voltage and the 0.001μF capacitor stabilizes the loop. A1B, sensing current across the 0.01Ω shunt, pro-

vides current limiting by forcing A1A to swing negatively. The low resistance shunt limits loss to only 100mW at 10A output. Figure 12 plots current limit performance for the regulator. Roll-off is smooth, with no oscillation or undesirable characteristics.

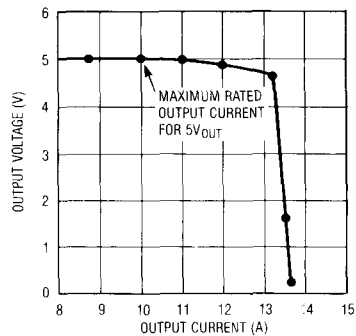


Figure 12. Current Limit Characteristics for the Discrete Regulator

*If boost voltage is already present in the system, significant circuit simplification is possible. See LTC Design Note 32, "A Simple Ultra-Low Dropout Regulator."

Application Note 32

Ultra High Efficiency Linear Regulator

Figure 13 combines the preceding discrete circuits to achieve highly efficient linear regulation at high power. This circuit combines Figure 8A's pre-regulator with Figure 11's discrete low dropout design. Modifications include deletion of the linear regulators boost supply and slight adjustment of the gate-source zener diode values. Similarly, a single 1.2V reference serves both pre-regulator and linear output regulator. The upward adjustment in the zener clamp values ensures adequate boost voltage under low voltage input conditions. The pre-regulator's feedback resistors set the linear regulators input voltage just above its 400mV dropout.

This circuit is complex, but performance is impressive. Figure 14 shows efficiency of 86% at 1A output, decreasing to 76% at full load. The losses are approximately evenly distributed between the MOSFETs and the MBR1060 catch diode. Replacing the catch diode with a synchronously switched FET (see LTC AN-29, Figure 32) and trimming the linear regulator input to the lowest possible value could improve efficiency by 3%–5%.

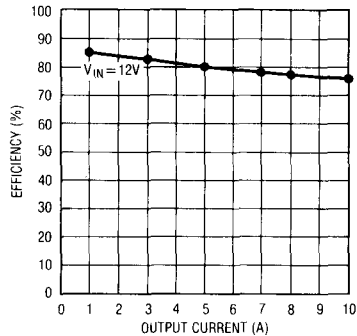


Figure 14. Efficiency vs Output Current for Figure 13

Micropower Pre-Regulated Linear Regulator

Power linear regulators are not the only types which can benefit from the above techniques. Figure 15's pre-regulated micropower linear regulator provides excellent efficiency and low noise. The pre-regulator is similar to Figure 8A. A drop at the pre-regulator's output (pin 3 of the LT1020 regulator, trace A, Figure 16) causes the LT1020's

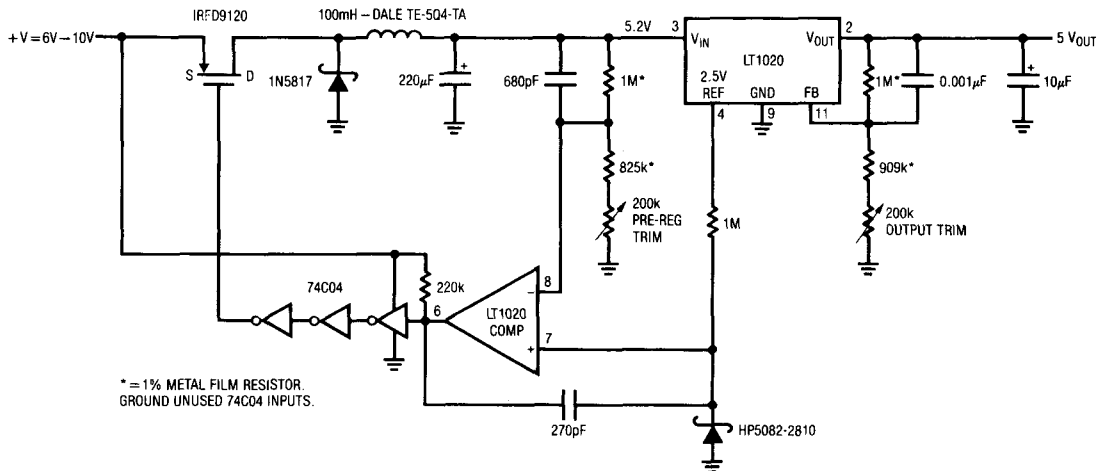


Figure 15. Micropower Pre-Regulated Linear Regulator

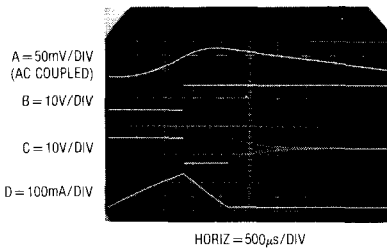


Figure 16. Figure 15's Waveforms

comparator to go high. The 74C04 inverter chain switches, biasing the P-channel MOSFET switch's grid (trace B). The MOSFET comes on (trace C), delivering current to the inductor (trace D). When the voltage at the inductor-220 μ F junction goes high enough (trace A), the comparator switches high, turning off MOSFET current flow. This loop regulates the LT1020's input pin at a value set by the resistor divider in the comparator's negative input and the LT1020's 2.5V reference. The 680pF capacitor stabilizes the loop and the 1N5817 is the catch diode. The 270pF capacitor aids comparator switching and the 2810 diode prevents negative overdrives.

The low dropout LT1020 linear regulator smoothes the switched output. Output voltage is set with the feedback pin associated divider. A potential problem with this circuit is start-up. The pre-regulator supplies the LT1020's input but relies on the LT1020's internal comparator to function. Because of this, the circuit needs a start-up mechanism. The 74C04 inverters serve this function. When power is applied, the LT1020 sees no input, but the inverters do. The 200k path lifts the first inverter high, causing the chain to switch, biasing the MOSFET and starting the circuit. The inverter's rail-to-rail swing also provides good MOSFET grid drive.

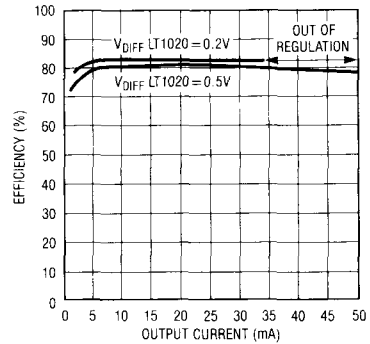


Figure 17. Efficiency vs Output Current for Figure 15

The circuit's low 40 μ A quiescent current is due to the low LT1020 drain and the MOS elements. Figure 17 plots efficiency vs output current for two LT1020 input-output differential voltages. Efficiency exceeding 80% is possible, with outputs to 50mA available.

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4. Williams, J., "Micropower Circuits for Signal Conditioning," Linear Technology Corp. AN-23
5. Williams, J. and Huffman, B., "Some Thoughts on DC-DC Converters," Linear Technology Corp. AN-29
6. Analog Devices, Inc., "Multiplier Application Guide"

Note: This application note was derived from a manuscript originally prepared for publication in EDN magazine.

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APPENDIX A

Achieving Low Dropout

Linear regulators almost always use Figure A1A's basic regulating loop. Dropout limitations are set by the pass elements on-impedance limits. The ideal pass element has zero impedance capability between input and output and consumes no drive energy.

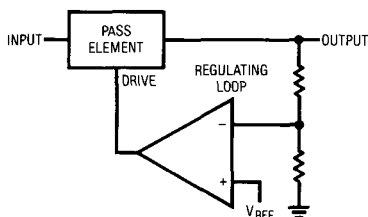


Figure A1A. Basic Regulating Loop

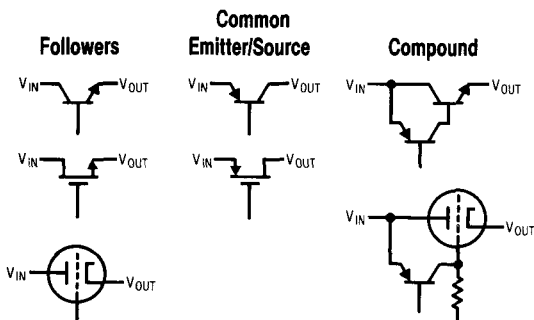


Figure A1B. Linear Regulator with Some Pass Element Candidates

A number of design and technology options offer various trade-offs and advantages. Figure A1B lists some pass element candidates. Followers offer current gain, ease of loop compensation (voltage gain is below unity) and the drive current ends up going to the load. Unfortunately, saturating a follower requires voltage overdriving the input (e.g. base, gate). Since drive is usually derived directly from V_{IN} this is difficult. Practical circuits must either generate the overdrive or obtain it elsewhere. This is not easily done in IC power regulators, but is realizable in discrete circuits (e.g. Figure 11). Without voltage overdrive the saturation loss is set by V_{be} in the bipolar case and channel on-resistance for MOS. MOS channel on-resistance varies considerably under these conditions,

although bipolar losses are more predictable. Note that voltage losses in driver stages (Darlington, etc.) add directly to the dropout voltage. The follower output used in conventional three terminal IC regulators combines with drive stage losses to set dropout at 3V.

Common emitter/source is another pass element option. This configuration removes the V_{be} loss in the bipolar case. The PNP version is easily fully saturated, even in IC form. The trade-off is that the base current never arrives at the load, wasting substantial power. At higher currents, base drive losses can negate a common emitter's saturation advantage. This is particularly the case in IC designs, where high beta, high current PNP transistors are not practical. As in the follower example, Darlington connections exacerbate the problem. At moderate currents PNP common emitters are practical for IC construction. The LT1020/LT1120 uses this approach.

Common source connected P-channel MOSFETs are also candidates. They do not suffer the drive losses of bipolars, but typically require 10V of gate-channel bias to fully saturate. In low voltage applications this usually requires generation of negative potentials. Additionally, P-channel devices have poorer saturation than equivalent size N-channel devices.

The voltage gain of common emitter and source configurations is a loop stability concern, but is manageable.

Compound connections using a PNP driven NPN are a reasonable compromise, particularly for high power (beyond 250mA) IC construction. The trade-off between the PNP V_{ce} saturation term and reduced drive losses over a straight PNP is favorable. Also, the major current flow is through a power NPN, easily realized in monolithic form. This connection has voltage gain, necessitating attention to loop frequency compensation. The LT1083-6 regulators use this pass scheme with an output capacitor providing compensation.

Readers are invited to submit results obtained with our emeritus thermionic friends, shown out of respectful courtesy.

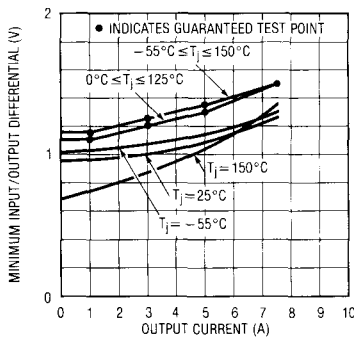
APPENDIX B

A Low Dropout Regulator Family

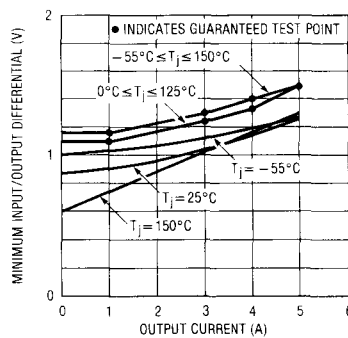
The LT1083-6 series regulators detailed in Figure B1 feature maximum dropout below 1.5V. Output currents range from 1.5A to 7.5A. The curves show dropout is significantly lower at junction temperatures above 25°C. The NPN pass transistor based devices require only 10mA load current for operation, eliminating the large base drive loss characteristic of PNP approaches (see Appendix A for discussion).

In contrast, the LT1020/LT1120 series is optimized for lower power applications. Dropout voltage is about 0.05V at 100 μ A, rising to only 400mV at 100mA output. Quiescent current is 40 μ A.

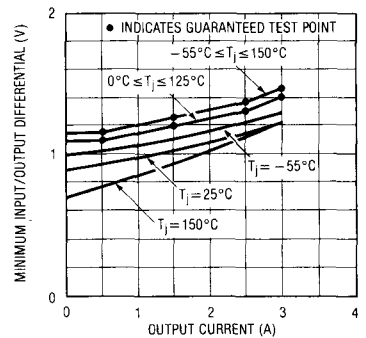
LT1083 Dropout Voltage vs Output Current



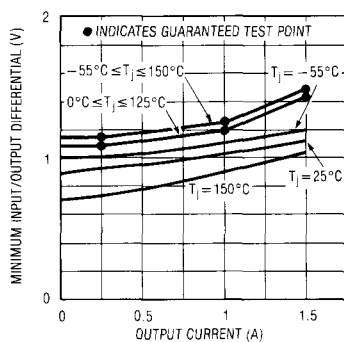
LT1084 Dropout Voltage vs Output Current



LT1085 Dropout Voltage vs Output Current



LT1086 Dropout Voltage vs Output Current



LT1020/LT1120 Dropout Voltage and Supply Current

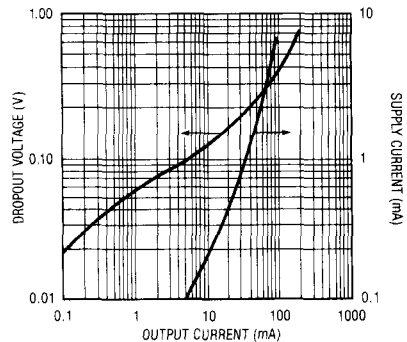


Figure B1. Characteristics of Low Dropout IC Regulators

Converting Light to Digits: LTC1099 Half Flash 8-Bit A/D Converter Digitizes Photodiode Array

Richard Markell

INTRODUCTION

Automated pricing at the supermarket check out counter has been around for years. A quick swipe across the bar code reader produces funny beeping noises, and as quickly as you can say "laser," the product is priced. Bar code readers are expensive since the A/D's required conversion time is usually too fast for inexpensive dual slope converters. This application note describes a Linear Technology "Half Flash" A/D converter, the LTC1099, being connected to a 256 element line scan photodiode array. This technology adapts itself to hand held (i.e. low power) bar code readers, as well as high resolution automated machine inspection applications. Many FAX machines and page scanners use photodiode arrays and A/D converters to transmit and/or store digitized data. For the esoteric at heart, the photodiode array may be digitized and used in astronomical applications such as star tracking.

The LTC1099 includes an internal sample-and-hold (S/H). This allows the A/D to sample the individual elements (pixels) of the photodiode array at rates which maintain 8-bit accuracy to 156kHz. This is fast enough to allow good throughput on machine vision or bar code scanner applications. Some video systems only require 6-bits of accuracy; in these cases the sample rate can be 215kHz (typical). Additional benefits may be derived from digital signal processing, allowing machine vision systems to do digital filtering, baseline correction, and correlated double sampling.

Figure 1 shows a block diagram of the system. The circuit, timing and some of the optical constraints are detailed in the following paragraphs.

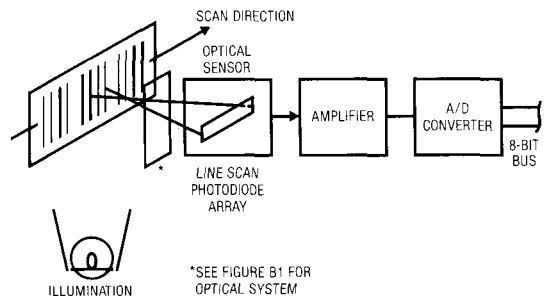


Figure 1. Optical-Digital Converter Block Diagram

ELECTRONIC SYSTEM DESIGN

Adding D/A to A/D System Makes Troubleshooting Easy

Finding bugs in an A/D system is never easy. When a photodiode array is added, system integration problems usually are very difficult to locate. In this application note, an inexpensive 12-bit D/A converter configured to accept only 8-bits was included as a troubleshooting aide. This D/A can be omitted in any final system design incorporating the LTC1099 and a photodiode array.

The schematic diagram for the system is shown in Figure 2. The LTC1099 (U3) is configured in WR-RD Mode using the stand alone configuration. This allows the 8-bit digital output to be continuously input to a D/A. The amplified D/A output at U6, (8), is the reconstructed digital signal. That is, this output represents the analog signal

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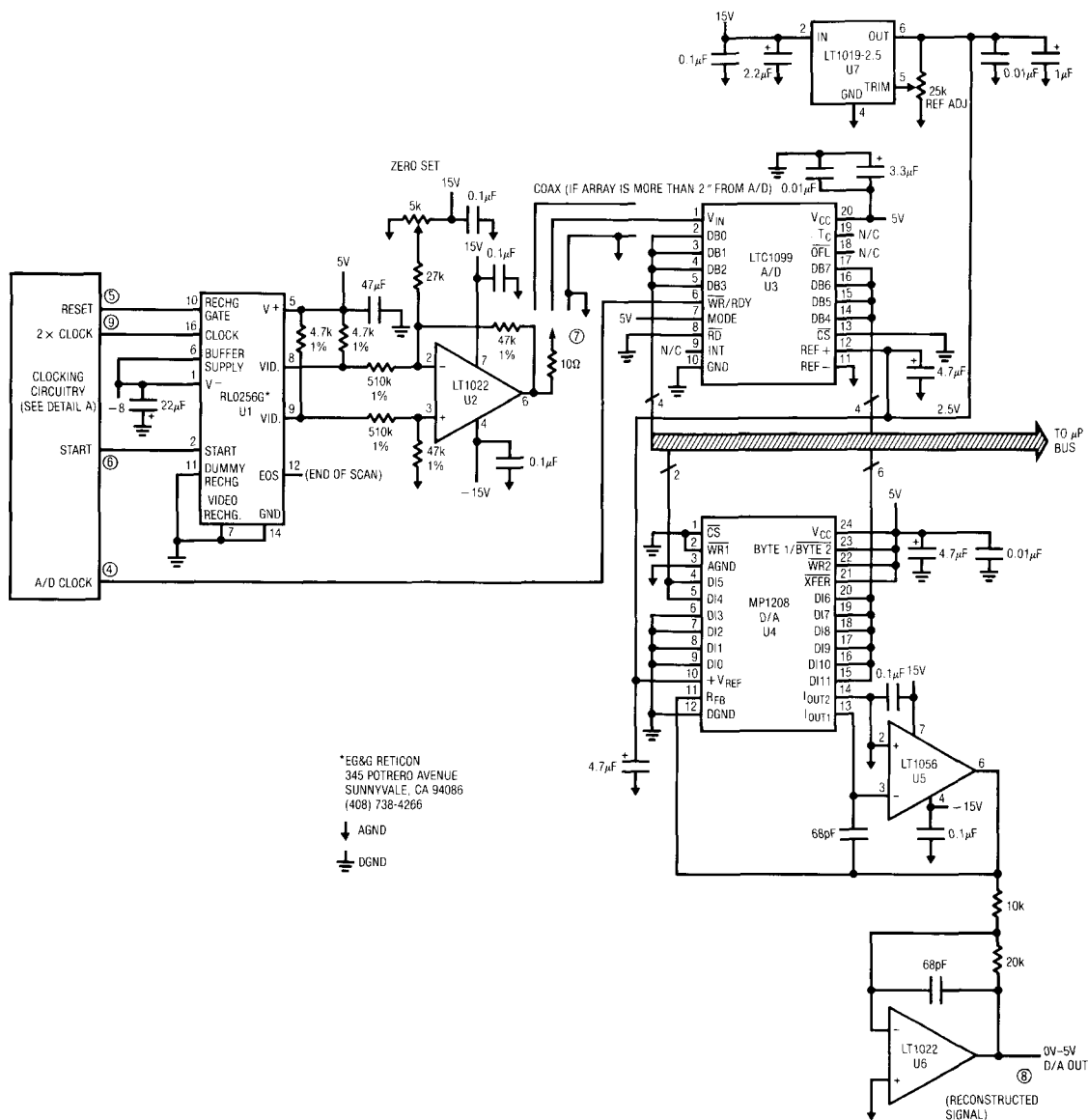


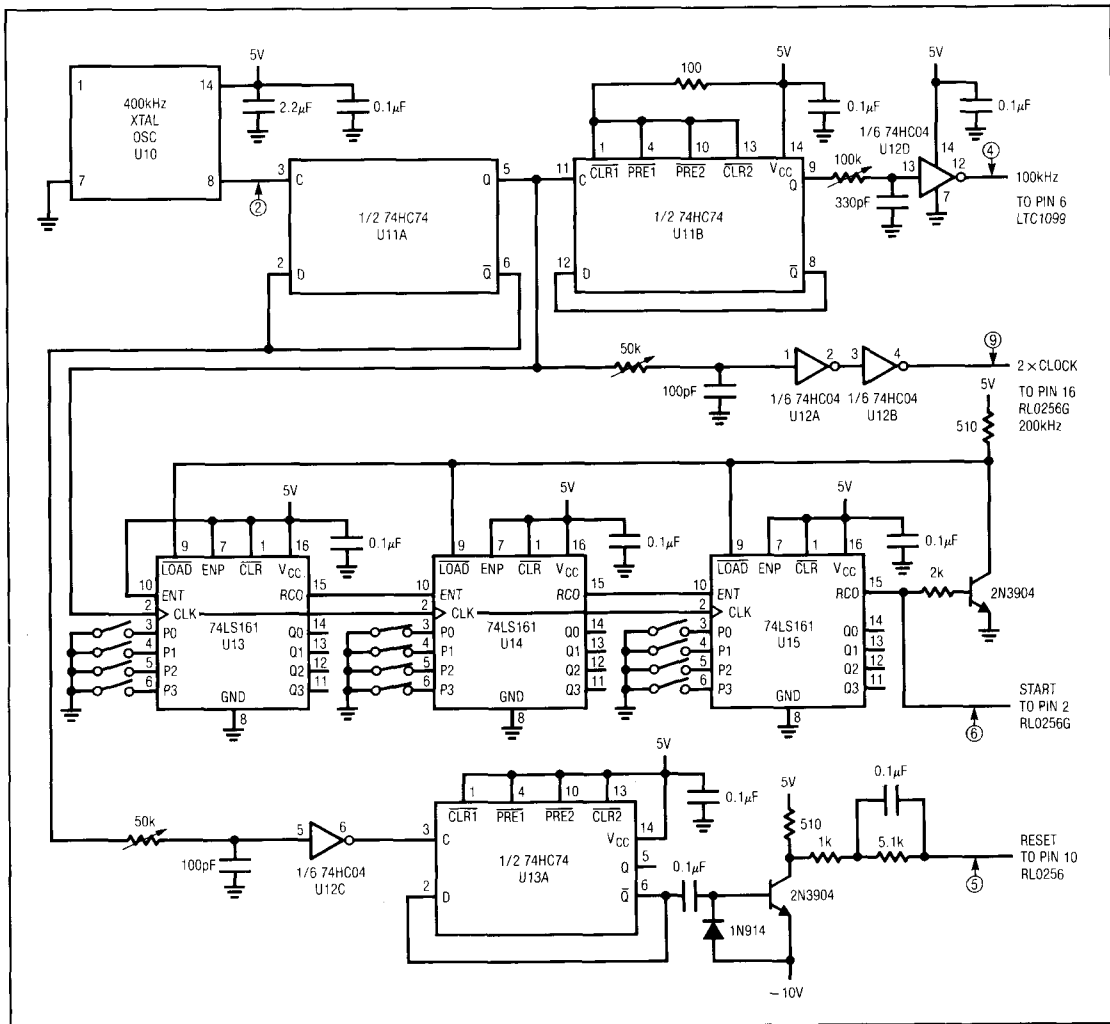
Figure 2. Schematic Diagram

that has been digitized and then converted back to analog by the D/A. This output allows the designer to directly compare the system output to the analog output of the photodiode array that is to be digitized.

As shown in Figure 2, the LTC1099 (U3) drives the 8-bit microprocessor bus and the D/A (U4). The current output of the D/A is converted to an output voltage by U5, an LT1056

JFET input operational amplifier. U6, an LT1022, amplifies and bandlimits the signal. Its output is 0 to 5V.

The system reference for the converters (both the A/D and the D/A) is an LT1019-2.5. This third generation bandgap voltage reference provides the 2.5V reference for the LTC1099 (which actually may be used with references as low as 1V) and the D/A.

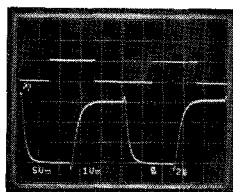


Detail A of Schematic Diagram (Figure 2)

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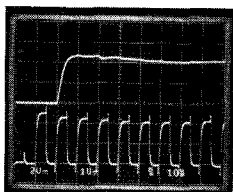
Figures 3 and 4 detail the A/D converter's operation. Figure 3 shows the \overline{WR}/RDY pulse from the clocking circuitry (top trace) and the analog output of the photodiode array at point (7). See Appendix A for discussion of clocking circuitry. The voltage output of the photodiode array is 256 "pulses" each of which represents the "exposure" of the individual photodiode. If a grating could be fabricated consisting of 128 black lines separated by 128 transparent spaces, and this grating could then be placed over the photodiode array with the proper magnification, the output pulses would represent alternating full scale and zero analog levels. Figures 3 and 4 show the analog and reconstructed digital outputs from a few pixels of the "evenly illuminated" array. Figure 3 details the timing required of the LTC1099. The falling edge of the \overline{WR}/RDY pulse initiates the conversion cycle of the LTC1099. As seen in the timing diagram, Figure 5, the analog input must be a stable 130ns before the falling edge of \overline{WR}/RDY occurs. Approximately 110ns after the falling edge, the internal sample-and-hold goes to hold mode and the analog input is ignored until the next conversion cycle. Figure 3 shows how this timing cycle is used to sample the output of the photodiode array.

The circuit as shown in Figure 2 allows easy interfacing to a microprocessor. The microprocessor system may contain, for example, a ROM with bar codes stored as they



TOP- \overline{WR}/RDY SIGNAL TO LTC1099 (5V/CM) (4)
 BOTTOM-ANALOG OUTPUT FROM PHOTODIODE ARRAY (1V/CM) (7)

Figure 3. A/D Clocking



TOP-OUTPUT FROM D/A ILLUSTRATING PROPER DIGITIZATION (6)
 BOTTOM-INPUT TO LTC1099 A/D FROM PHOTODIODE ARRAY THRU LT1022 BUFFER (7)

NOTE 1: CLOCK DELAY IN DAC RESPONSE.

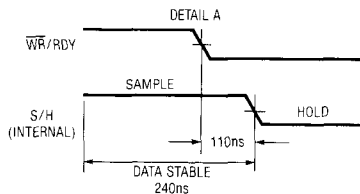
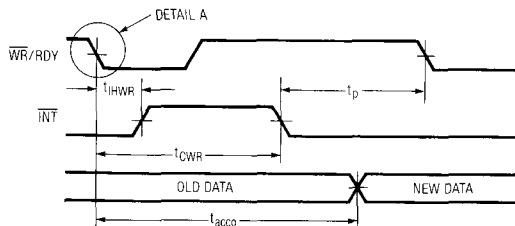
Figure 4. Photodiode Array Output

would appear when scanned optically and digitized. When an item is scanned, the microprocessor can compare (called a digital correlation) the scanned code to the stored codes and decide which product is being scanned.

Optical

The line scan array used in this application was an EG&G Reticon RL0256G photodiode array.* The array contains 256 photodiodes (also called pixels for "picture elements") on $25\mu\text{m}$ centers. See Figure 6 for more details. The device contains a row of silicon photodiodes, each with an associated storage capacitor on which to integrate photocurrent, and a multiplex switch for periodic readout. Readout is accomplished by an integrated shift register scanning circuit. A TTL clock is required for outputting the row of photodiodes to the output pin. A row of dummy photodiodes (photodiodes that have an opaque covering) is simultaneously read out with the active photodiodes to allow cancellation of multiplex switching transients. This array allows resolution to $25\mu\text{m}$ with standard optical techniques.

*The author would like to thank Mike Satterlund, Tom Silvey and Kevin Heher at EG&G Reticon for technical assistance with the Reticon part.



t_{IHWR} = DELAY FROM \overline{WR} TO \overline{INT} = 240ns TYP
 t_p = DELAY BETWEEN CONVERSIONS = 700ns TYP
 t_{CWR} = CONVERSION TIME = 2.5 μs TYP
 t_{acc} = DELAY TIME \overline{WR} TO NEW DATA VALID = t_{CWR} + 40ns TYP

Figure 5. Timing Diagram

Medium speed photodiode arrays have become inexpensive in recent years and, when connected to a "Half Flash" A/D converter like the LTC1099, provide an elegant, inexpensive solution to supermarket pricing, inventory control and other bar coding applications.

In the schematic of Figure 2 the photodiode array is shown as U1. It is clocked by a single phase TTL clock and associated driving signals which will be described later. The output of the array is a train of 256 charge pulses for each of the video and dummy video lines. The pulses on the dummy line contain switching transients only while those on the video line contain switching transients plus the video signal. The LT1022 FET input operational amplifier shown as U2 is used as a differential current amplifier. The output (as shown, for instance, in Figure 3) is a pulse whose peak amplitude has been scaled to a reasonable voltage (here it is 2.5V) to drive the A/D converter. Note that if the photodiode array amplifier (U2) is located any distance (greater than 3") from the A/D converter, a coaxial cable should be used to interconnect the two.

Figure 4 (bottom trace) shows a series of pulses output from operational amplifier U2. It is necessary to sample each pulse on the "flat top" to provide an accurate analog

signal to the A/D converter. The top trace of Figure 4 is the reconstructed analog signal through the A/D—D/A chain, the test output. Note that it nicely follows the tops of the analog photodiode pulses (it is delayed one clock pulse).

The ease with which the A/D may be interfaced to a microprocessor and its speed makes the use of "baseline correction" easy. Baseline correction is an often used technique with photodiode arrays where the baseline or "dark" value of each photodiode is stored in memory. At power on, the dark value of each photodiode, or 256 individual 8-bit values are stored in memory. This allows the user greater dynamic range than by simply using an average of all the photodiodes "dark" values. The A/D converter's 156kHz maximum sampling rate allows the microprocessor to do baseline correction rapidly with little system "overhead."

Optical to Digital System Response

The photodiode array is clocked from the clocking circuitry as shown in the boxed section of Figure 2. U4, the D/A and operational amplifiers U5 and U6 provide a digitally reconstructed analog output which should closely resemble the analog pulse amplitudes at point ⑦.

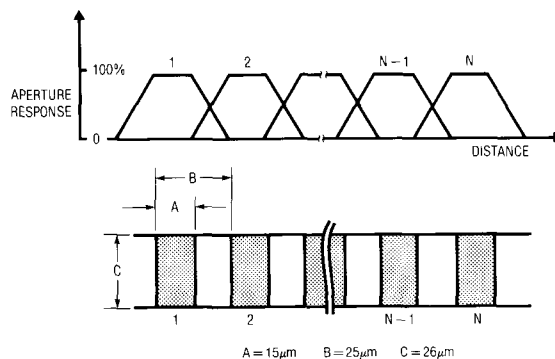


Figure 6. Sensor Geometry

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Figure 7 shows the systems response to placing an optical grating directly on the glass window which covers the photodiode array. The bottom trace is the analog output from operational amplifier U2—point (7). The top trace is the output of the D/A taken at point (8). The linewidths that appear as “notches” in the traces are (from left to right): 400, 350, 300, 250 and 200 μm (millionth of a meter). Similarly, Figure 8 shows the response to linewidths of 200, 150, 100, 90 and 80 μm (from left to right in the photo). As before, the top trace is the output of the D/A taken at point (8), while the bottom trace is the analog output from operational amplifier U2 — point (7). It should be noted that this crude system only illustrates the power of the optical to digital concept. For an optimized system uniform illumination is required and a good optical system is needed to properly image the item to be inspected onto the line scan photodiode array. Some thoughts on an optical system are described in Appendix B.

The designer must be aware of the integration time of the photodiode array. Integration time is analogous to the shutter speed of a film camera. The longer the shutter is open, the more light is collected onto the film media, and hence the darker the film will be. Figure 9 shows two scans of the photodiode array. The integration time of the photodiode array or the “exposure time” is equivalent to the time between start pulses. Figure 9 shows the integration time to be about 6.4ms. This is not a fixed parameter, but varied by the settings of the DIP switches connected to U13, U14 and U15. It is recommended that integration times not exceed approximately 40ms (at room temperature) to prevent integrated dark current (the leakage current that flows in photodiode that is not illuminated) from making a significant contribution to the output charge. Cooling of the photodiode sensor may be used (as is always the case in astronomical applications) to lower the dark current and therefore allow an increase in integration time.

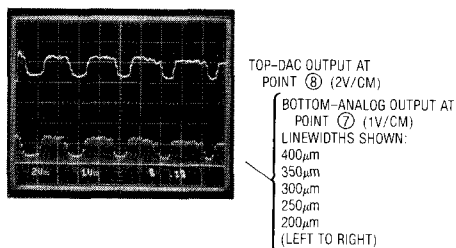


Figure 7. Optical Resolution

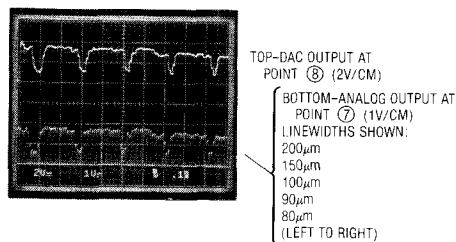


Figure 8. Resolution Photo

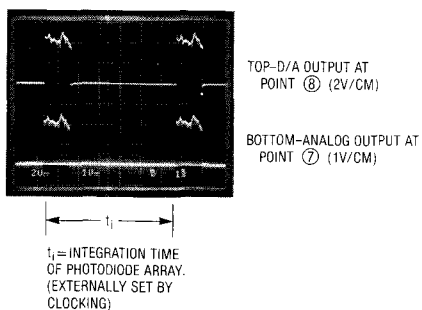


Figure 9. Photodiode Array Integration Time

APPENDIX A

Clocking Circuitry

The boxed section of Figure 2 details the clocking circuitry required to drive the photodiode array. There is nothing very unusual about the simple TTL circuitry required to drive the array. The clock signals are obtained from U10, a crystal oscillator. Counters U13 through U15 and the DIP switches set the number of clock periods between start pulses to any value up to 4096. This is the integration time, as described previously. The variable low pass filters (pots and capacitors) before the three sections of U12 allow delaying of the clocking signals to ensure that all the signals occur in the proper sequence. Figure A1 shows the reset pulse for the photodiodes (top) ⑤, the A/D WR/RDY pulse (starts A/D conversion) ④ and the clock signal from the crystal oscillator ②.

Figure A2 details: the 2x clock to the photodiode array at ⑨, the A/D clock at ④ and the analog photodiode output at ⑦. Figure A3 shows the photodiode reset pulse signal at ⑤ along with the 2x clock at ⑨ and the A/D clock signal at ④.

Figure A4 shows the start pulse and the analog CCD output.

Note that for those intending on prototyping this circuitry, the EG&G Reticon data sheet on the RL0256G array is an absolute necessity to set up proper timing signals.

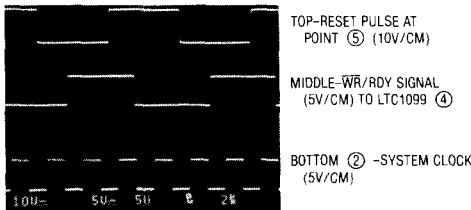


Figure A1. Timing Waveforms

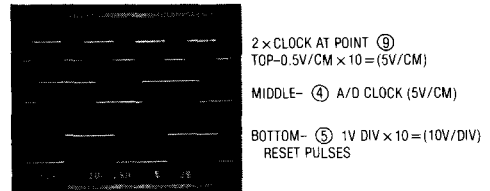


Figure A3. Timing Signals

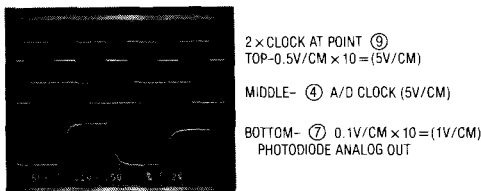


Figure A2. A/D "Convert" Signal Clock and Diode Array Output

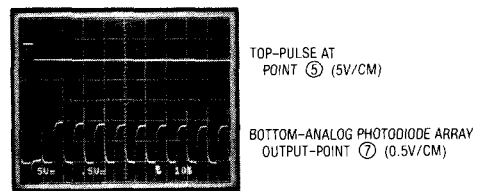


Figure A4. Start Pulse and Diode Array Output

APPENDIX B

Optical System Design

Optical system design is a complex subject in which one may obtain a Ph.D. In lieu of this option, Figure B1 shows in rough form the top view of an imaginary tin can inspection system. Lens A and lens B are two cylindrical lenses rotated 90 degrees from each other. Lens A as shown in the example system takes the columnated illumination and produces a line into the paper. When an object interrupts the illumination, the line imaged onto the photodiode array to be dark. In this way height can be measured.

Similarly, using lens B, a line of illumination may be formed parallel to the paper. When an object interrupts

this illumination, a dark line is imaged onto a second photodiode array. In this way width may be measured.

Note carefully here, that we have not covered the issues of image magnification/demagnification. Obviously, an object 6 inches in height and 1 inch in width needs to be demagnified to fit the constraints of the photodiode aperture. These issues are beyond the scope of this Application Note.**

**See for example:

Jenkins and White, "Fundamentals of Optics," McGraw Hill Book Co., NY, NY 1976

Hecht and Zajac, "Optics," Addison-Wesley Publishing Co., Reading, MASS Dec. 1976

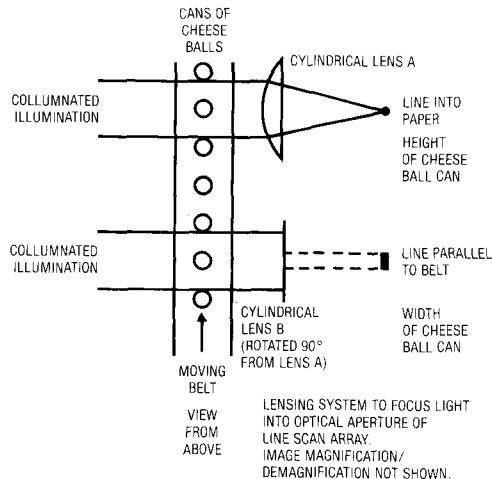


Figure B1. Optical System Design

LTC1099 Enables PC Based Data Acquisition Board to Operate DC-20kHz A "C" Cruise through Data Acquisition

Richard Markell

Introduction

A complete design for a data acquisition card for the IBM PC is detailed in this application note. Additionally, C language code is provided to allow sampling of data at speeds of more than 20kHz. The speed limitation is strictly based on the execution speed of the "C" data acquisition loop. A "Turbo" XT can acquire data at speeds greater than 20kHz as can machines with 80286 and 80386 processors. The computer that was used as a test bed in this application was an XT running at 4.77MHz and therefore all system timing and acquisition time measurements are based on the 4.77MHz clock speed.

The board may be used, as designed, for data acquisition and/or it may be used as a test vehicle for incorporating an A/D converter into a system. The optical to digital converter described in AN33 could be integrated into the PC plug-in board to build a simple, yet highly accurate, machine vision system. The fast sampling available with the LTC1099 allows voice quality audio to be acquired and stored in PC memory. This could be useful in a PC based voice analysis system.

This note is broken into two parts. First, the hardware will be described. The hardware description is broken into four sections. Figure 1 details the address decoding section. Figure 2 details the A/D converter section. Figure 3 details the timer circuitry. The D/A section is detailed in Figure 4.

The second part of the application note describes the software written in "C" to control the board hardware. These functions and main programs were written and tested using Turbo C available from Borland International. These programs include: 1) The function named "newatod.c."

This function is the main function for using the PC plug-in board for data collection. 2) The function named "ntimer.c." This function controls the 8253 hardware timer on the plug-in board. 3) The function called "dacout.c." This is a debug program for testing the address decoding circuitry on the plug-in board. 4) The function "atodcon.c." is another debug program allowing the user to test the A/D function of the plug-in board.

Hardware

This application note does not pretend to cover all aspects of interfacing to the IBM PC. The intent is to allow the analog circuit designer to get a data collection system up and running with as little pain as possible. Schematic diagrams and explanations are provided in as much depth as possible, but the designer is encouraged to see the additional sources at the end of this application note for a more complete treatment of interfacing to the PC.

Figure 1 details the Address Decoding Section of the plug-in board. Signals from the IBM PC bus are buffered via 74LS244 unidirectional (U2, U3) or 74LS245 bidirectional (U1) buffers to the expansion board. The direction line of the 74LS245 is controlled from the $\overline{\text{BIOR}}$ line (Buffered IO Read) of the IBM Bus. Therefore, when the PC wants to read data from the plug-in board, the 74LS245 lets data flow in only that direction. Figure 5 shows the correct timing of an LTC1099 read operation as viewed on a logic state analyzer. Data in the write mode can only flow in the opposite direction. Since an A/D converter can only provide data to the PC for the PC to read, an LTC1099 write does not mean that the PC writes to it. An LTC1099 write

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strobe switches the LTC1099 internal S/H (sample and hold) to hold mode and then starts the A/D conversion. Figure 6 shows the correct timing of the LTC1099 write operation. The Gate input to the 74LS245 is controlled by U10A such that the '245 is active only when a valid PC plug-in board address ($\overline{ENI/O}$) and a \overline{BIOR} or \overline{BIOW} line is asserted. For non-vulcans this means that the data bus to the PC plug-in board can only be accessed when the computer is trying to read or write to the addresses on the board.

U6 (74LS154) and U8 (74LS688) provide address decoding for the on-board devices that must be read from or written

to. U8 is an 8-bit digital comparator that allows only hex addresses 0300 to 031F to be accessible on the board. U6 further decodes the addressing so that we may address each address from 300 to 30F. We could, at a later time, add another 74LS154 should we need to decode addresses 310 to 31F hex.

Figure 2 details the Analog to Digital Converter Section of the board. The LTC1099 8-bit A/D is a half flash CMOS converter with a built-in sample and hold. It can sample at rates to 156kHz. In this application, the data acquisition speed is limited by the software. In the circuit of Figure 2, an analog signal is input to the A/D through an anti-alias-

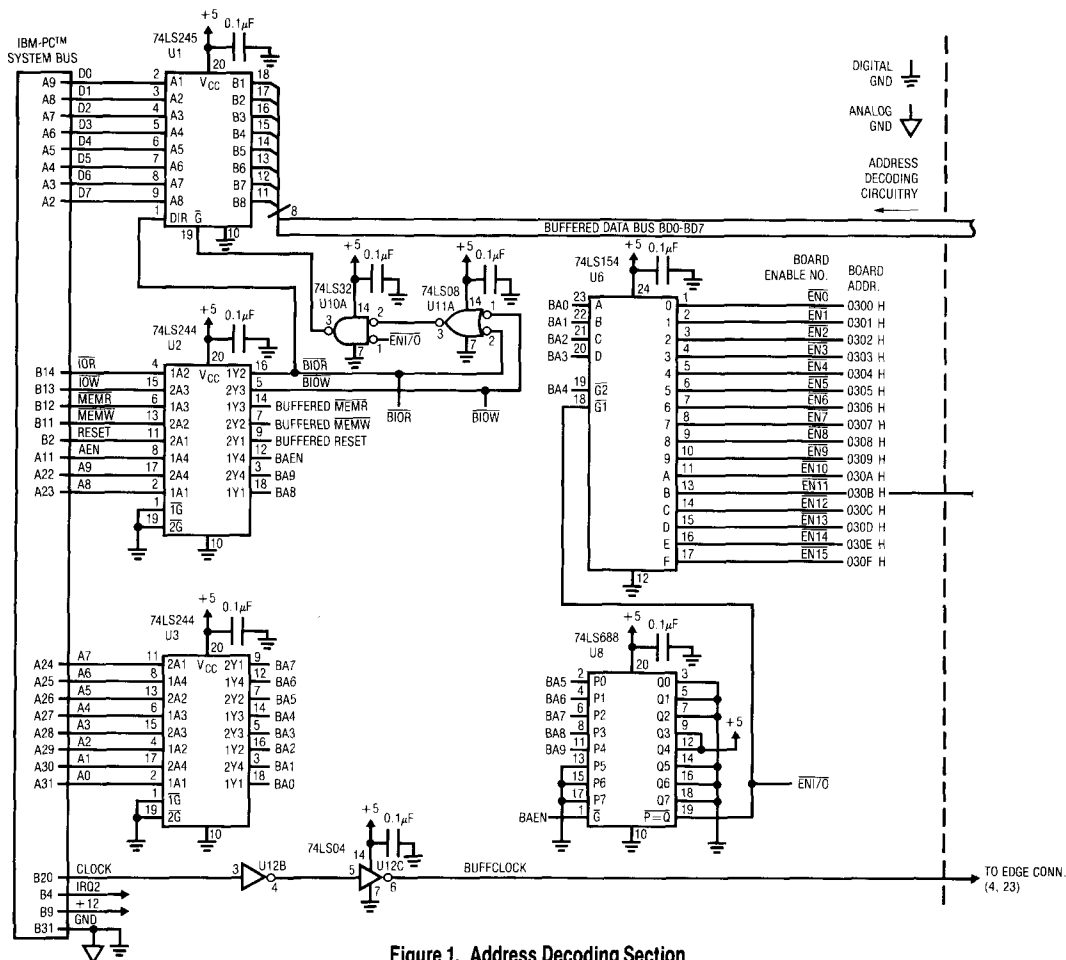


Figure 1. Address Decoding Section

ing low pass filter. U23 (an LT1019-5) is a third generation bandgap reference which supplies the 5V reference to the A/D. The A/D's chip select is asserted when $\overline{EN8}$ and the $TIMERCLK'$ signals are low. U20, a 74LS126, is used to choose which signal starts a conversion. The user can, via the software, choose if the conversion is started by the $TIMERCLK'$ signal or via the $\overline{EN10}$ signal. In a similar manner, the INT select line is used to select whether the $TIMERCLK'$ signal or the INT (Interrupt) signal is used to assert the IRQ2 (Interrupt #2) line of the IBM bus. Carefully note that Figure 2 has both analog and digital ground con-

nections. It is *critically* important to separate these grounds on the board and only bring them together at a single point at the board edge. If this layout is not followed the digital devices will cause switching noise which will appear at the analog device's inputs and cause inaccurate data to be taken.

Figure 3 shows the 8253 timer and associated circuitry. The 8253 is a programmable interval timer with three independent 16-bit counters. The device has six different modes of operation. The mode used to control the A/D in

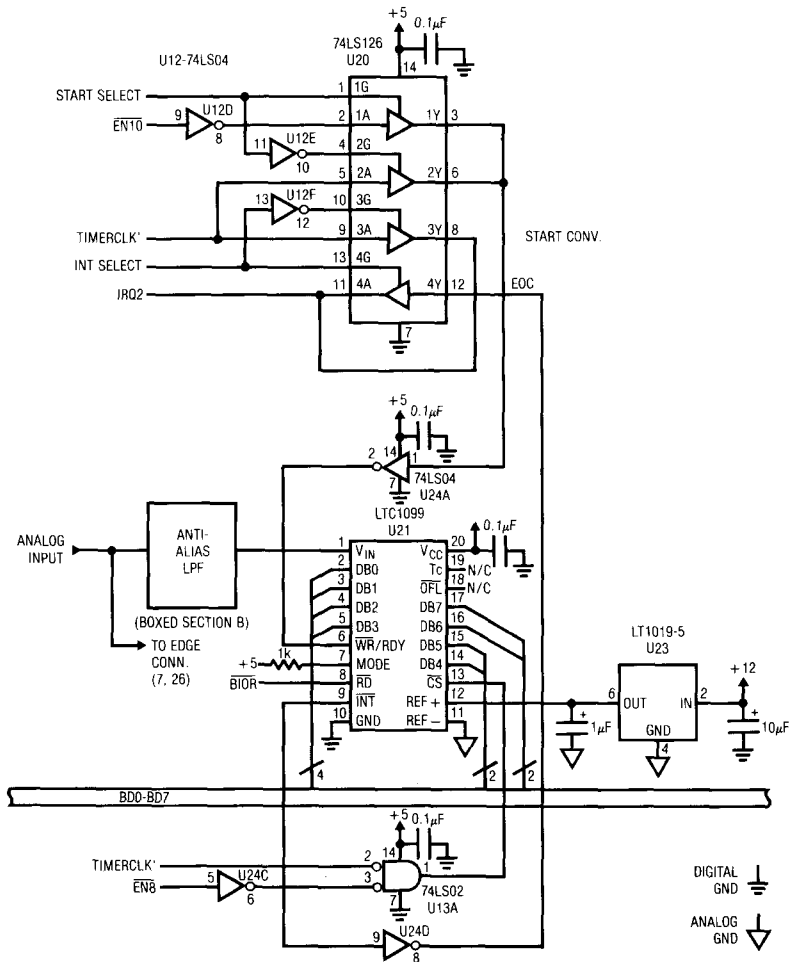


Figure 2. A/D Section

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this application note is Mode 2 which produces a string of pulses. These pulses are accurately spaced as they are generated from the 4.77MHz (PC XT) clock signal in the computer. These pulses are used to start the LTC1099 conversion cycles. As seen in Figure 3, U17, a 74LS393 serves to divide the buffered clock signal by 4. This signal, at 1.1925MHz, is then input to the 8253. In this application, the three counters of the 8253 are fed one into the next. This has the effect of providing an output whose period

may be divided by up to $2^{48} - 1$. Table 1 details the addressing of the counters, the gate ports and the control registers of the 8253. The CS must be controllable from the first four addresses shown in Table 1, thus the configuration of U11B, C and D. Figure 7 shows in the top trace, the buffered clock at U12C pin 6 (Figure 1) and, in the bottom trace the 8253 (U15) output at pin 17. The timer was programmed for (50, 'u') or 50 microseconds. Note that this period is correct, as seen in the photo. U18 (a 74LS74) and

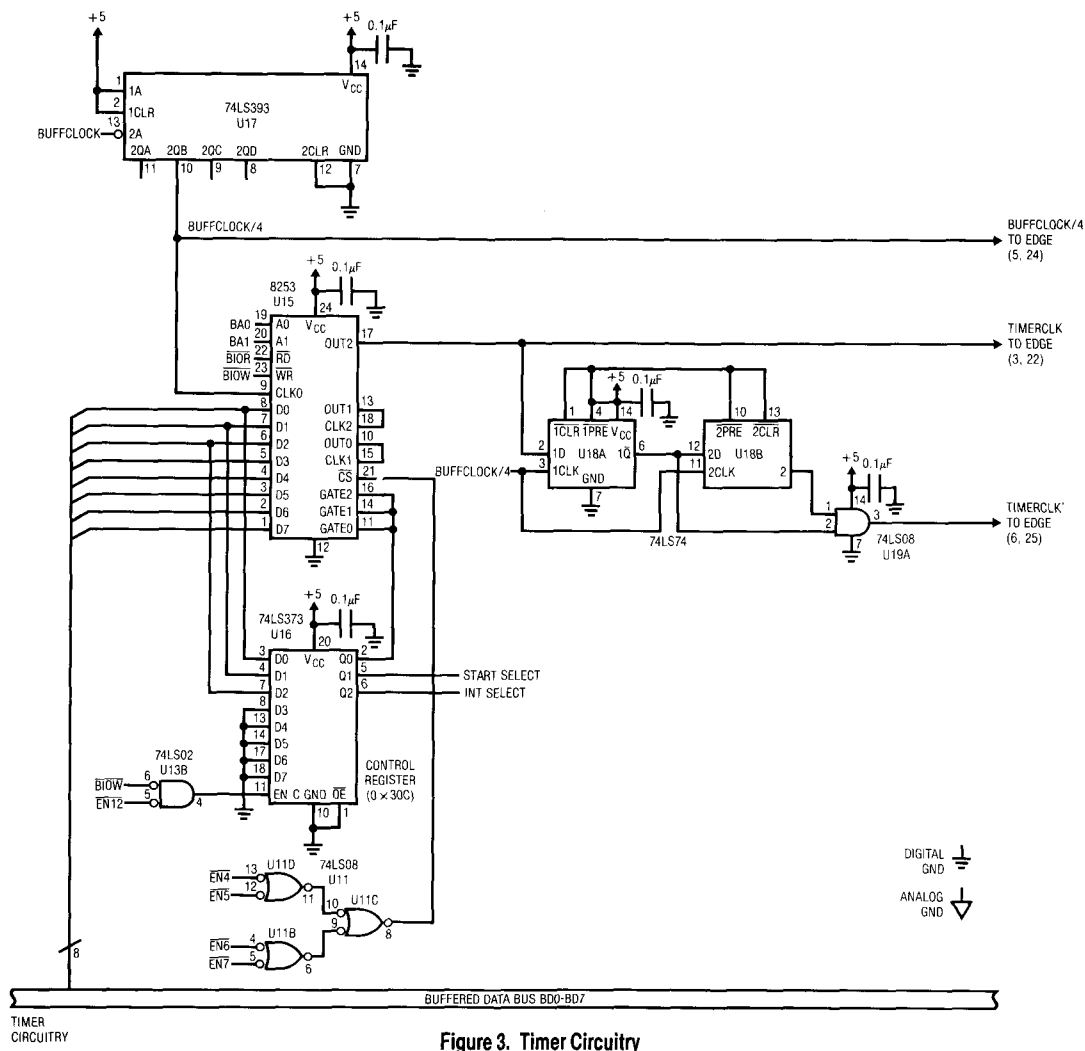


Figure 3. Timer Circuitry

U19A (a 74LS08 gate) are used to process the signal from the timer to produce pulses of pulse width equal to BCLK/4. Figure 8 shows this process. The top trace is the narrowed pulse at pin 3 (U19A) 74LS08. The bottom trace from pin 17 of the 8253 is the unshaped pulse. The next photo, Figure 9, shows more dramatically why the process of pulse narrowing is required. The bottom trace set to 10 microseconds is almost square. Should a digital process start on the falling edge of the clock and continue until the clock rises, this would be almost 5 microseconds for the square wave. This is far too much time for most processors. In the top trace a narrow pulse is only a few hundred nanoseconds wide. This width is what the microprocessor in the PC wants to see. Thus the pulse width processing is necessary for proper circuit operation.

Figure 4 shows the D/A section of the board. It is simply the D/A converter attached to the buffered data bus and the \overline{CE} and \overline{CS} pins connected to BIOW and EN11 respectively. The D/A port is connected to output connector pins to allow analog output from the PC plug-in board.

Table 1. 8253 Timer Port Addresses

PORT ADDRESS	
304 H	8253 Counter 0
305 H	8253 Counter 1
306 H	8253 Counter 2
307 H	Control Register-8253
30C H	Gate Port of 8253 (Bit 0 only)

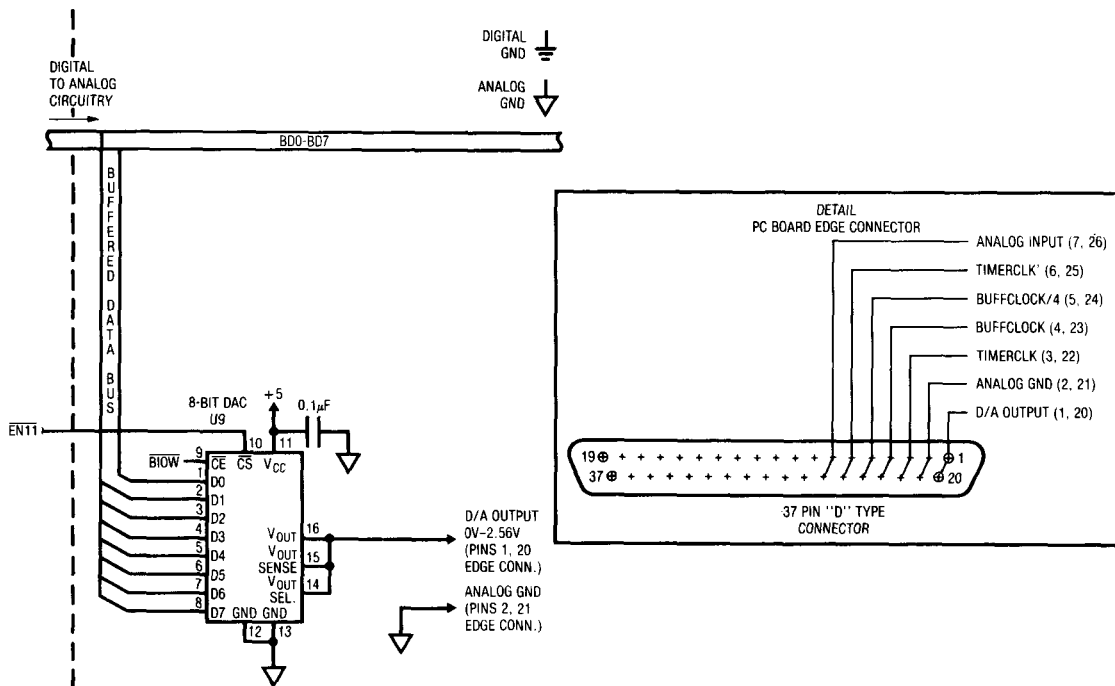


Figure 4. D/A Section

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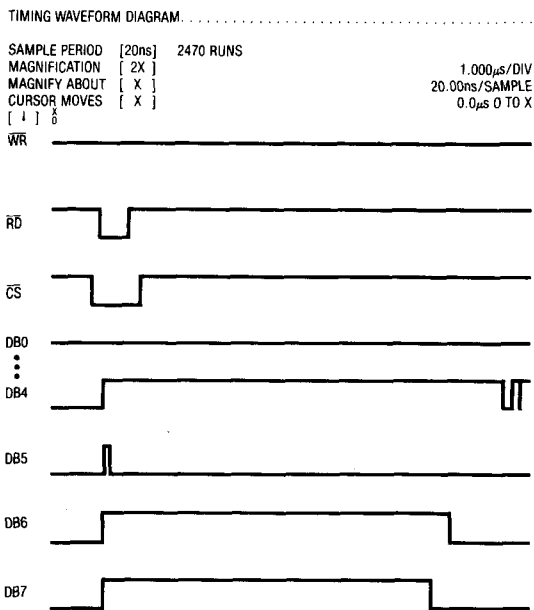


Figure 5. Logic State Analyzer Output Showing Proper LTC1099 Read Timing. LTC1099 is Operating in WR-RD Mode.

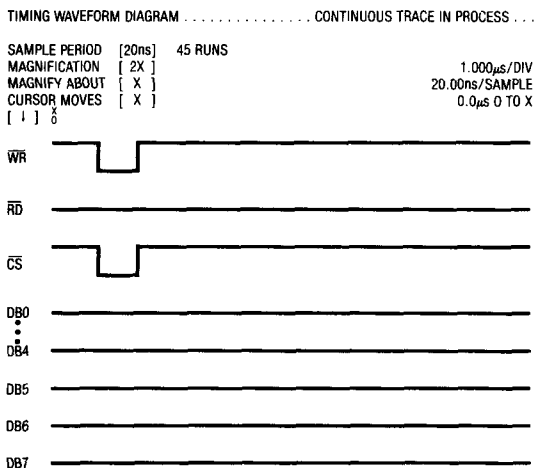


Figure 6. Logic State Analyzer Output Showing Proper LTC1099 Write Timing. LTC1099 is Operating in WR-RD Mode.

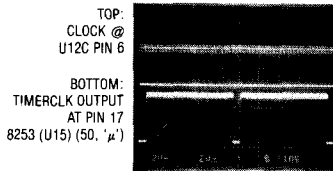


Figure 7. Buffered XT System Clock and 8253 Timer Output

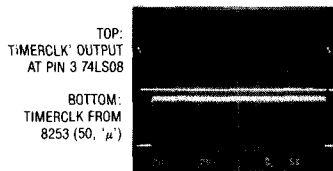


Figure 8. Timer Output (Bottom) and Processed Timer Output (Top) with Decreased Pulse Width (50 μ s Pulse Period)

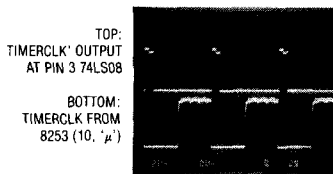


Figure 9. Timer Output (Bottom) and Narrowed Timer Output (Top) (10 μ s Pulse Period)

Software

Software for the PC plug-in board was written in Borland's Turbo C. Turbo C provides a good base for interfacing software to real world hardware as it has input and output instructions (some languages do not). Turbo C will also allow machine code to be called in the middle of a program. This feature is very useful if speed is of the essence. Most of the C code shown here should be portable to other compilers, i.e. Microsoft. Note that some of the individual instructions will differ slightly in syntax (i.e. Turbo C: Outport; Microsoft: Outp. See either the Microsoft C Bible or another reference for more information).

The individual programs used for data collection and testing of the plug-in board will be described briefly. For more information see the comments interspersed throughout the code and the C references at the end of this article.

Figure 10 details the code called "dacout.c." The code, when compiled to produce executable code, will continuously output to the D/A converter on the PC plug-in board. This is useful when first testing the board and/or one's knowledge of the C language. The code will produce a ramp which can be viewed on an oscilloscope using the

output connector on the PC plug-in board. A photograph of this output is shown in Figure 11.

Figure 12 details the code called "ntimer.c." This is the code used to set up the 8253 timer integrated circuit on the PC plug-in board. The code scans the time unit selected: microseconds, milliseconds, or seconds. Then the division ratio is selected based on the user input. While the code may appear formidable, it really is simple to understand if the potential user calculates the values loaded into the clock[x] registers. Try it!

```

/* This is a test program to test the address decoding circuitry on */
/* the pc plug in board. The program outputs continuously to a DAC */
/* producing a ramp which can be viewed on an oscilloscope. The program */
/* is called dacout.c and it must be compiled to an executable file to */
/* run. */
/* Richard Markell/Linear Technology Corp./408 432-1900 */
/* Copyright Linear Technology Corp. 1989. License to use this */
/* code is granted when used in conjunction with LTC devices. */
/* Rev. 1.00/May 8, 1989 */
/* dacout.c */

#include<dos.h>
#include<signal.h>
#include<stdio.h>

#define DACO 0x30B /*This is the DAC port corresponding */
/*to address line E11. */

main()
{
    int i;
    while(1)
    {
        /*Repeat until Control-break hit */
        for(i=0; i <= 255;i++) /*Increment i and send */
            dacout(i); /*Increment i and send */
        signal(SIGINT, SIG_DFL); /*Set to DACO. */
        /*Look for Control-Break */
    }
}

/* DACO output */
dacout(val)
int val;
{
    outportb(DACO, val); /*Send number to DACO */
}

```

Figure 10. "dacout.c" Program Listing

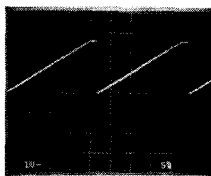


Figure 11. D/A Test Output at Pin 16 U9

```

/* Function to set up Intel 8253 timer to provide timing pulses to */
/* A to D converter. Mode 2 of the counter/timer is used to produce */
/* a string of pulses. In this application the three counters inside */
/* the 8253 are daisy chained together. Counter 0's output is input */
/* to the clock of Counter 1 and Counter 1's output is input to the */
/* clock of Counter 2. The output is taken from Counter 2's output. */
/* See Intel data sheet for more details. */
/* Richard Markell/Linear Technology Corp./408 432-1900 */
/* Copyright Linear Technology Corp. 1989. License to use this */
/* code is granted when used in conjunction with LTC devices. */
/* Rev. 1.00/May 8, 1989 */
/* ntimer.c */

#include<ctdio.h>
#include<dos.h>

#define CNT0 0x304 /*First counter register */
#define CNT1 0x305 /*Second counter register */
#define CNT2 0x306 /*Third counter register */
#define TCNTL 0x307 /*Timer control word register */
#define CNTRL 0x30C /*Plug in board control register */

/*main() */
{
    /* Enable 8253 output */
    outportb(CNTRL, 5);
    timer(50, 'u');
}

timer(rate, unit)
int rate;
char unit;
{
    char clock[6];
    unsigned int tocks;
    switch(unit)
    {
        case 'u': /*Microseconds */
            tocks = (float) rate / 3.3543; /*(1/4.77MHz)=209.5ns */
            clock[5] = tocks / 256; /*209.5ns x 4 x 4 = 3.3543us */
            clock[4] = tocks % 256; /* Example: 20 & 256 = 20 */
            clock[3] = 0;
            clock[2] = 2;
            clock[1] = 0;
            clock[0] = 2;
            break;
        case 'm': /*Milliseconds */
            clock[5] = (rate*2) / 256;
            clock[4] = (rate*2) % 256;
            clock[3] = 0;
            clock[2] = 149;
            clock[1] = 0;
            clock[0] = 4;
            break;
        case 's': /*Seconds */
            clock[5] = (rate*2) / 256;
            clock[4] = (rate*2) % 256;
            clock[3] = 23;
            clock[2] = 75;
            clock[1] = 0;
            clock[0] = 100;
            break;
    }
    outportb(TCNTL, 0x34); /* Counter 0, load LSB then MSB, mode 2 */
    outportb(TCNTL, 0x74); /* Counter 1, load LSB then MSB, mode 2 */
    outportb(TCNTL, 0xB4); /* Counter 2, load LSB then MSB, mode 2 */
    outportb(CNT0, clock[0]);
    outportb(CNT0, clock[1]);
    outportb(CNT1, clock[2]);
    outportb(CNT1, clock[3]);
    outportb(CNT2, clock[4]);
    outportb(CNT2, clock[5]);
}

```

Figure 12. "ntimer.c" Program Listing

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Figure 13 is the test program, called "atodcon.c," for testing the analog to digital to analog path through the board. The user inputs data (usually a sine wave) to the A/D via the board edge connector and views the data on an oscilloscope to verify correct operation of the digitization process. Figure 14 shows an oscilloscope photo of a 40Hz sine wave which was input to the A/D and then reconverted to analog via the D/A portion of the board. The speed with which data can be output using this program is not a valid indication of the data acquisition speed of the program called "newatod.c." This is because of the extra time needed to output data with the D/A.

```

/* This is the main function for testing the A to D, D to A functions
 * on the pc plug in board. The code below is called atodcon.c. The
 * user calls the compiled program, pcpplug.exe, from the command line
 * while in DOS. The compiled program contains atodcon.obj and ntimer.
 * obj linked with the various header files. The program allows the
 * designer to test the hardware by inputting a 0 to 5v signal into
 * the A to D converter and observing the output of the D to A converter
 * on an oscilloscope to confirm proper operation of the A to D and
 * D to A functions.
 *
 * Richard Markell/Linear Technology Corp./408 432-1900
 * Copyright Linear Technology Corp. 1989. License to use this
 * code is granted when used in conjunction with LTC devices.
 * Rev. 1.00/May 8, 1989
 */
atodcon.c

#include<dos.h>
#include<signal.h>
#include<stdio.h>
#define STAT 0x309 /* Protoboard status register */
#define CNTRL 0x30C /* Control register */
#define ADC 0x308 /* A to D address and data */
#define DAC 0x30B /* D to A address */
#define SIZE_DATA 2048 /* Number of samples */

main()
{
    char data;

    outportb (CNTRL,5); /* Start conversion; enable 8253 */
    timer (10, 'u'); /*Set timer rate

    while (1) /*Continue until Control-Break hit
    {
        outportb (ADC,1); /* Start A to D */
        data=inputrb(ADC); /*Input */
        outportb(DAC, data); /*Output */
        signal (SIGINT, SIG_DFL); /*Looks for Ctrl-Brk */
    }
}

```

Figure 13. "atodcon.c" Program Listing

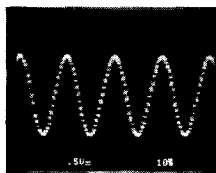


Figure 14. D/A Output for 40Hz Sine Input to A/D (70, μ s) Timer Setting

```

/*This is the main function for using the PC Plug in board for data
 *collection. This function is named newatod.c. The user calls the
 *compiled program, here titled: nppcplug.exe, on the command line while
 */
/*in DOS. The compiled program contains newatod.obj and ntimer.obj linked
 *with the various header files. The user must enter on the DOS command
 */
/*line: C:\nppcplug dest.xxx. The destination file may reside on any
 */
/*disk in the system, ie dest.xxx may be a:\data5.
 */
/*The program collects SIZE_DATA 8 bit bytes of data. This data is
 */
/*then displayed on screen and written to the destination file.
 */
/*
 */
/* Richard Markell/Linear Technology Corp./408 432-1900
 */
/* Copyright Linear Technology Corp. 1989. License to use this code
 */
/* is granted when used in conjunction with LTC devices.
 */
/* Rev. 1.01/June 5, 1989
 */
/* newatod.c
 */

#include<dos.h>
#include<stdio.h>
#include<stdlib.h>

#define STAT 0x309 /* Protoboard status register */
#define CNTRL 0x30C /* Control register */
#define ADC 0x308 /* A to D address and data */
#define DAC 0x30B /* D to A address */
#define SIZE_DATA 2048 /* Number of samples */

main(argc, argv)
int argc; /*Command line argument count */
char *argv[]; /*Command line arguments */

{
    unsigned char *buffer; /*Data Buffer */
    int outhandle; /*Destination file handle */
    int bytes_written=0, bytes=0, data_points=0;

    unsigned char data, *ptr;

    if (argc!=2) /* Check args */
        (printf("Format: C:\TC\nppcplug dest.xxx "); exit(0));

    if ((outhandle=fopen(argv[1], "wb" )) == NULL )
        (printf ("Can't open file %s.", argv[1]); exit(0));

    /*This statement is specific to IBM-PC or clones ( ie non-
    /* portable */

    outportb (CNTRL,5); /* Start conversion; enable 8253 */
    timer (8, 'u'); /*Set timer rate

    if ( (buffer = /*Set up data buffer
    (unsigned char *)malloc(SIZE_DATA) ) == NULL)
    {
        printf("Memory allocation failed.\n");
        exit(0);
    }

    ptr=buffer;

    /* Note carefully: the time between samples set by the timer
    /* must be greater than the 'while' loop time of execution
    /* or there may be errors in the acquired data.

    while (bytes < SIZE_DATA) /*Continue until buff full*/
    {
        outportb (ADC,1); /* Start A to D */
        data=inputrb(ADC); /*Input byte */
        *(ptr++)=data; /*Put data in buffer */
        bytes++; /*Do again */

    }

    printf("\n\n---Contents of file---\n");
    ptr=buffer; /*Point to start of buffer*/
    bytes=0;
    while (bytes < SIZE_DATA)
    {
        printf("%4d",*(ptr++)); /*Print buffer to screen */
        bytes++;
        if( bytes % 20 == 0 )
            printf("\n");
    }

    ptr=buffer;
    bytes=0;
    while (bytes < SIZE_DATA)
    {
        if (bytes_written = fprintf ( outhandle, "%4d",
        *(ptr++))!=20) /*Write data to disk file */
            perror ("Write failed");
        else
            bytes++;
        data_points = bytes;
    }
    printf("\n\nData Written to File OK. \n");
    printf("\nBytes written = %d ", data_points);

    fclose(outhandle); /*IBM or clone specific
    /* statement
    */
}

```

Figure 15. "newatod.c" Program Listing

Figure 15 details the main function for data collection. This function is called "newatod.c." The program collects SIZE_DATA 8-bit bytes of data and writes them to a disk file. The program runs very fast because data is stored to memory until all the data points are collected. Then the data is written to disk. In use the user must type C:\TC\npcplug dest.xxx on the DOS command line. "C" recognizes the "\" as a special character, so typing it twice lets the compiler recognize the "\" in the usual DOS manner. If the user is already in the Turbo C directory, TC, then only the command "npcplug dest.xxx" need be typed. (Where npcplug is the compiled program containing the various header files linked with newatod.obj and

ntimer.obj.) Note that the data acquisition speed could perhaps be improved somewhat by substituting machine code for the "C" code in the "while" loop starting with the statement:

```
while (bytes < SIZE_DATA).
```

The code as written allows data to be collected at maximum sampling rates of approximately 20kHz (with a 4.77MHz XT).

Note also that although all the code has been extensively tested (by an analog hacker), no claims are made as to its optimization. All reader comments are solicited as to writing better, faster, or more analog sounding code.

BOX SECTION A

Analog to Digital Converter Selection

The job of the A/D converter on the PC plug-in board is to digitize voice, transducers and other types of analog system inputs.

The LTC1099 was chosen as the on-board A/D for the PC plug-in board. It is a CMOS part with 8-bits of resolution requiring only 75mW of power. Its total unadjusted error is ± 1 LSB for the LTC1099 and $\pm 1/2$ LSB for the "A" part. All timing inputs of the LTC1099 are edge sensitive for easy microprocessor interface.

A major benefit of the LTC1099 is that it contains an integral sample and hold function that allows signals of 156kHz at levels up to 5Vp-p to be directly digitized. This is at least an order of magnitude better than most converters of this type.

The LTC1099 is ideal for Digital Signal Processing applications such as digital filtering, pattern recognition and FFT signal analysis. In DSP applications, the dynamic characteristics of the converter (be it A/D or D/A) are critical. Dynamic characteristics are usually measured by inputting a spectrally

pure sine wave to the A/D and collecting the digitized output data. This data is then analyzed for such things as SNR, Harmonic Distortion and Effective Number of Bits (ENOBs). It is beyond the scope of this application note to discuss every aspect of dynamic signal testing of A/D and D/A converters.

Figures 16 and 17 show FFT plots of the LTC1099 converter. Figure 16 shows the plot for an input signal, $f_{IN} = 85.61790$ kHz, with a dynamically tested SNR of 49.0dB. The next figure, Figure 17, shows the plot for an input signal $f_{IN} = 103.898440$ kHz. Its SNR is calculated to be also 49.0dB. These numbers are remarkable for the fact that the relationship between SNR and resolution is related by the following equation:

$$\text{SNR} = (6.02N + 1.76\text{dB}) \text{ where } N \text{ is the resolution of the A/D in bits.}$$

Thus, the tests conclude that the LTC1099 is very close to the theoretical in its dynamic signal to noise ratio. A plot of SNR versus frequency is shown in Figure 18.

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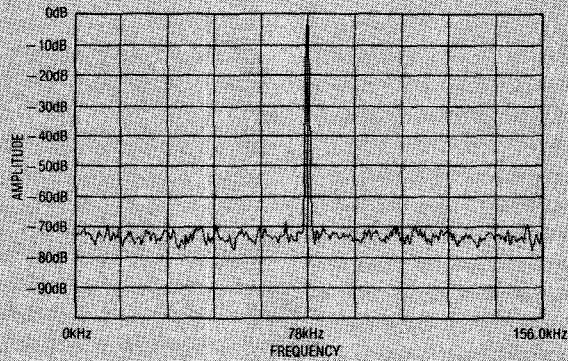


Figure 16. LTC1099 FFT Plot for $f_{IN} = 78.144251\text{kHz}$ (0V to 5V), $f_{SAMPLE} = 312.000000\text{kHz}$, $S/N = 49.0\text{dB}$, $T_A = 25^\circ\text{C}$

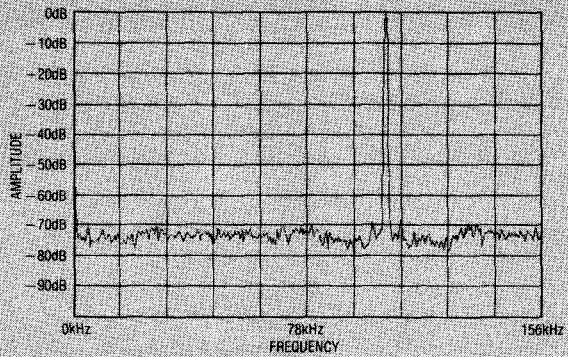


Figure 17. LTC1099 FFT Plot for $f_{IN} = 103.898440\text{kHz}$ (0V to 5V), $f_{SAMPLE} = 312.000000\text{kHz}$, $S/N = 49.0\text{dB}$, $T_A = 25^\circ\text{C}$

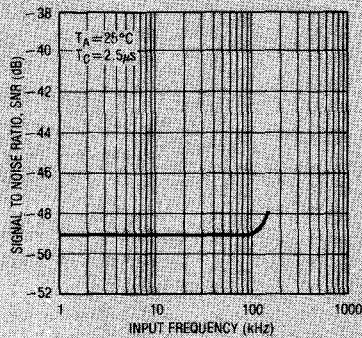


Figure 18. Signal to Noise Ratio (SNR) vs Input Frequency

BOX SECTION B

Anti-Aliasing Lowpass Filter

In all sampled data systems, the phenomenon of aliasing can rear its ugly head. This can, and usually will, happen when the analog input frequency exceeds half the sample frequency. Thus, when we say that we can collect data at 20kHz (and therefore sample at 40kHz), we must have an anti-aliasing filter at the input to the A/D to limit the input frequency

range to this limit. Obviously, in the selection of the anti-aliasing filter we must give careful consideration to the input signal's frequency components and the fact that we cannot build a filter with an infinitely steep cutoff slope. Figures 19, 20, 21 and 22 detail some choices for anti-aliasing filters.

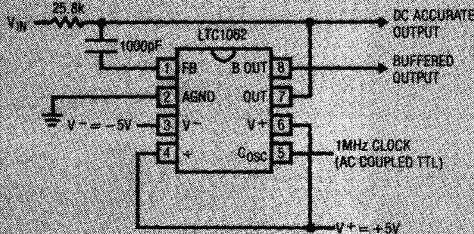


Figure 19. LTC1062 in 10kHz Anti-Aliasing Application

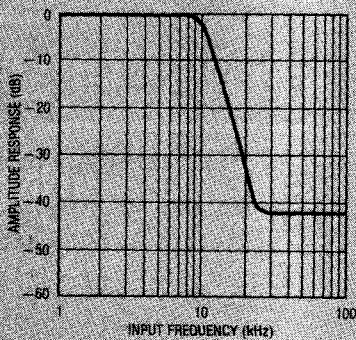
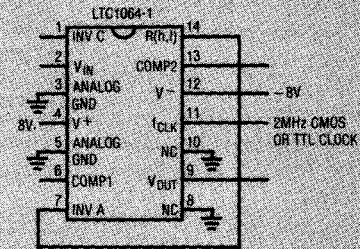
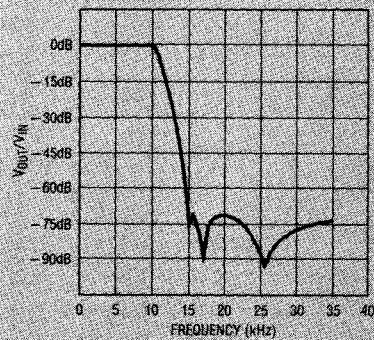


Figure 20. Amplitude Response of Circuit Shown in Figure 19



NOTE: THE POWER SUPPLIES SHOULD BE BYPASSED BY A 0.1μF CAPACITOR CLOSE TO THE PACKAGE.

Figure 21. LTC1064-1 in 20kHz Anti-Aliasing Application



8TH ORDER CLOCK SWEEPABLE LOWPASS ELLIPTIC ANTIALIASING FILTER

Figure 22. Frequency Response of Circuit Shown in Figure 21

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REFERENCES

1. "Turbo C," Borland International, 1800 Green Hills Road, PO Box 660001, Scotts Valley, CA 95066-0001
2. "Interfacing Sensors to the IBM PC," Tompkins, Willis J. and Webster, John, Prentice Hall, Englewood Cliffs, NJ 07632, 1988
3. "The Waite Group's Microsoft C Bible," Barkakati, Nabajyoti, Howard W. Sams and Company, Indianapolis, IN, 1988
4. "Interfacing to the IBM Personal Computer," Eggebrecht, Lewis C., Howard W. Sams and Company, Indianapolis, IN, 1983
5. PC Plug-In Prototype Board Manufacturer: JDR Microdevices, 2233 Branham Lane, San Jose, CA 95124 800-538-5000 (This is where you get the prototype board to plug into your computer.)

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Step Down Switching Regulators

Jim Williams

A substantial percentage of regulator requirements involve stepping down the primary voltage. Although linear regulators can do this, they cannot achieve the efficiency of switching based approaches¹. The theory supporting step down ("buck") switching regulation is well established, and has been exploited for some time. Convenient, easily applied IC's allowing implementation of practical circuits are, however, relatively new. These devices permit broad application of step down regulation with minimal complexity and low cost. Additionally, more complex functions incorporating step down regulation become realizable.

Basic Step Down Circuit

Figure 1 is a conceptual voltage step down or "buck" circuit. When the switch closes the input voltage appears at the inductor. Current flowing through the inductor-capaci-

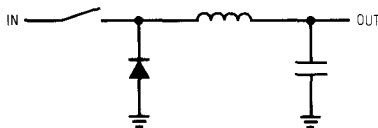


Figure 1. Conceptual Voltage Step Down ("Buck") Circuit

tor combination builds over time. When the switch opens current flow ceases and the magnetic field around the inductor collapses. Faraday teaches that the voltage induced by the collapsing magnetic field is opposite to the originally applied voltage. As such, the inductor's left side heads negative and is clamped by the diode. The capacitor's accumulated charge has no discharge path, and a DC potential appears at the output. This DC potential is lower than the input because the inductor limits current during the switches on-time. Ideally, there are no dissipative elements in this voltage step down conversion. Although the output voltage is lower than the input, there is no energy

lost in this voltage-to-current-to-magnetic field-to-current-to-charge-to-voltage conversion. In practice, the circuit elements have losses, but step down efficiency is still higher than with inherently dissipative (e.g. voltage divider) approaches. Figure 2 feedback controls the basic circuit to regulate output voltage. In this case switch on-time (e.g. inductor charge time) is varied to maintain the output against changes in input or loading.

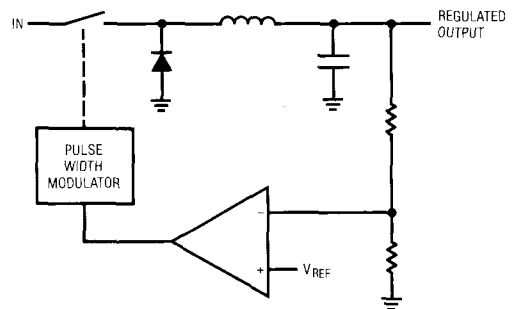


Figure 2. Conceptual Feedback Controlled Step Down Regulator

Practical Step Down Switching Regulator

Figure 3, a practical circuit using the LT1074² IC regulator, shows similarities to the conceptual regulator. Some new elements have also appeared. Components at the LT1074's "VCOMP" pin control the IC's frequency compensation, stabilizing the feedback loop. The feedback resistors are selected to force the "feedback" pin to the device's internal 2.5V reference value. Figure 4 shows operating waveforms for the regulator at $V_{IN} = 28V$ with a 5V, 1A load.

Note 1: While linear regulators cannot compete with switchers, they can achieve significantly better efficiencies than generally supposed. See LTC Application Note 32, "High Efficiency Linear Regulators," for details.

Note 2: See Appendix A for details on this device.

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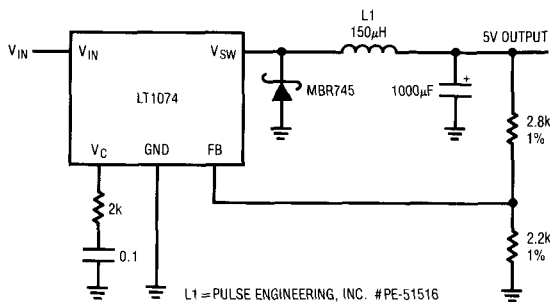


Figure 3. A Practical Step Down Regulator Using the LT1074

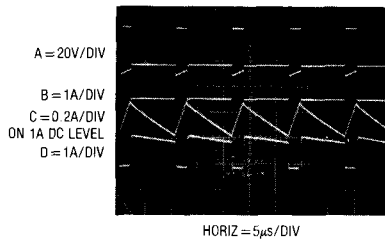


Figure 4. Waveforms for the Step Down Regulator at $V_{IN} = 28V$ and $V_{OUT} = 5V$ at 1A

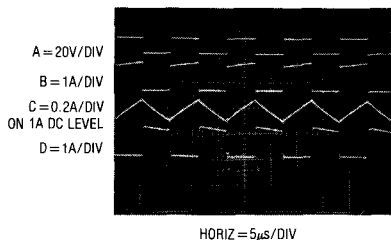


Figure 5. Waveforms for the Step Down Regulator at $V_{IN} = 12V$ and $V_{OUT} = 5V$ at 1A

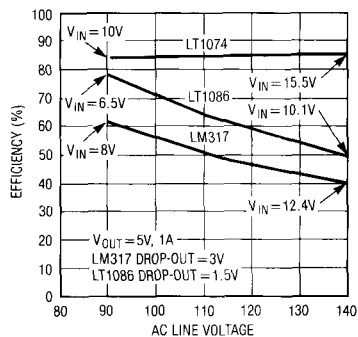


Figure 6. Efficiency vs AC Line Voltage for the LT1074, LT1086 and LM317 Linear Regulators Are Shown for Comparison.

Trace A is the V_{SW} pin voltage and trace B is its current. Inductor current³ appears in trace C and diode current is trace D. Examination of the current waveforms allows determination of the V_{SW} and diode path contributions to inductor current. Note that the inductor current's waveform occurs on top of a 1A DC level. Figure 5 shows significant duty cycle changes when V_{IN} is reduced to 12V. The lower input voltage requires longer inductor charge times to maintain the output. The LT1074 controls inductor charge characteristics (see Appendix A for operating details), with resulting waveform shape and time proportioning changes.

Figure 6 compares this circuit's efficiency with linear regulators in a common and important situation. Efficient regulation under varying AC line conditions is a frequent requirement. The figure assumes the AC line has been transformed down to acceptable input voltages. The input voltages shown correspond to the AC line voltages given on the horizontal axis. Efficiency for the LM317 and LT1086 linear regulators suffers over the wide input range.

Note 3: Methods for selecting appropriate inductors are discussed in Appendix B.

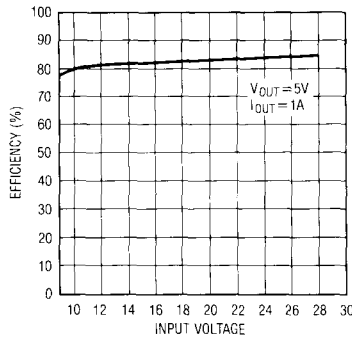


Figure 7. Efficiency Plot for Figure 3. Higher Input Voltages Minimize Effects of Saturation Losses, Resulting in Increased Efficiency.

The LT1086 is notably better because its lower dropout voltage cuts dissipation over the range. Switching pre-regulation⁴ can reduce these losses, but cannot equal the LT1074's performance. The plot shows minimum efficiency of 83%, with some improvement over the full AC line excursion. Figure 7 details performance. Efficiency approaches 90% as input voltage rises. This is due to minimization of the effects of fixed diode and LT1074 junction losses as input increases. At low inputs these losses are a higher percentage of available supply, degrading efficiency. Higher inputs make the fixed losses a smaller percentage, improving efficiency. Appendix D presents detail on optimizing circuitry for efficiency.

Dual Output Step Down Regulator

Figure 8, a logical extension of the basic step down converter, provides positive and negative outputs. The circuit is essentially identical to Figure 3's basic converter with the addition of a coupled winding to L1. This floating winding's output is rectified, filtered and regulated to a -5V output. The floating bias to the LT1086 positive voltage regulator permits negative outputs by assigning the regulator's output terminal to ground. Negative output power is set by flux pick-up from L1's driven winding. With a 2A load at the +15 output the -5V output can supply over 500mA. Because L1's secondary winding is floating its output may be referred to any point within the breakdown capability of the device. Hence, the secondary output could be 5V or, if stacked on the +15 output, 20V.

Negative Output Regulators

Negative outputs can also be obtained with a simple two terminal inductor. Figure 9 demonstrates this by essentially grounding the inductor and steering the catch diodes negative current to the output. A1 facilitates loop closure by providing a scaled inversion of the negative output to the LT1074's feedback pin. The 1% resistors set the scale factor (e.g. output voltage) and the RC network around A1 gives frequency compensation. Waveforms for this circuit are reminiscent of Figure 5, with the exception

Note 4: See Reference 1.

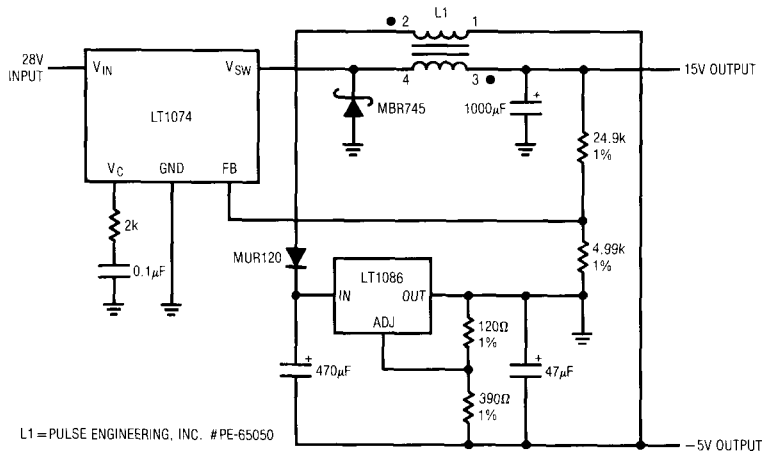


Figure 8. Coupled Inductor Provides Positive and Negative Outputs

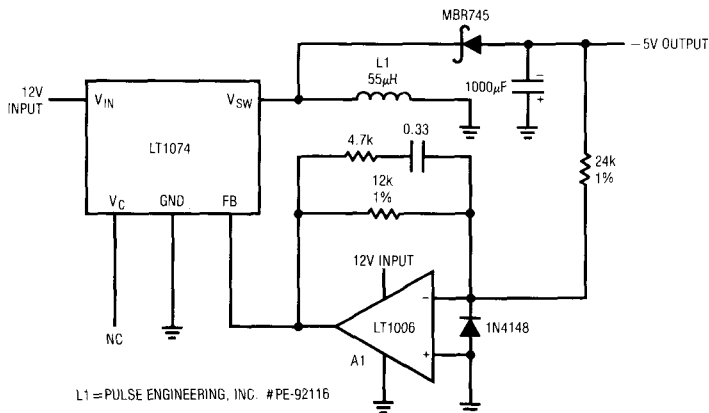


Figure 9. A Negative Output Step Down Regulator

that diode current (trace D) is negative. Traces A, B and C are V_{SW} voltage, inductor current and V_{SW} current respectively.

Figure 11, commonly referred to as "Nelson's Circuit," provides the same function as the previous circuit, but eliminates the level-shifting op amp. This design accomplishes the level shift by connecting the LT1074's "ground" pin to the negative output. Feedback is sensed from circuit ground, and the regulator forces its feedback pin 2.5V above its "ground" pin. Circuit ground is common to input and output, making system use easy. Operating waveforms are essentially identical to Figure 10. Advantages of the previous circuit compared to this one are that the LT1074 package can directly contact a grounded heat sink and that control signals may be directly interfaced to the ground referred pins.

The inductor values in both negative output designs are notably lower than in the positive case. This is necessitated

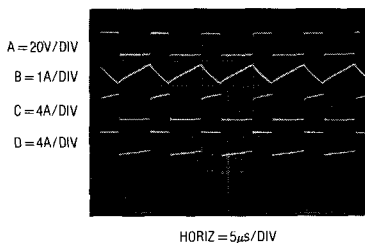


Figure 10. Figure 9's Waveforms

by the reduced loop phase margin of these circuits. Higher inductance values, while preferable for limiting peak current, will cause loop instability or outright oscillation.

Current-Boosted Step Down Regulator

Figure 12 shows a way to obtain significantly higher output currents by utilizing efficient energy storage in the LT1074 output inductor. This technique increases the duty cycle over the standard step down regulator allowing more energy to be stored in the inductor. The increased output current is achieved at the expense of higher output voltage ripple.

The operating waveforms for this circuit are shown in Figure 13. The circuit operating characteristics are similar to that of the step down regulator (Figure 3). During the V_{SW} (trace A) "on" time the input voltage is applied to one end of the coupled inductor. Current through the V_{SW} pin (trace B) ramps up almost instantaneously (since inductor current (trace F) is present) and then slows as energy is stored in the core. The current proceeds into the inductor (trace D) and finally is delivered to the load. When the V_{SW} pin goes off, current is no longer available to charge the inductor. The magnetic field collapses, causing the V_{SW} pin voltage to go negative. At this point similarity with the basic regulator vanishes. In this modified version the output current (trace F) receives a boost as the magnetic field collapses. This results when the energy stored in the core is transferred to the output. This current step circulates

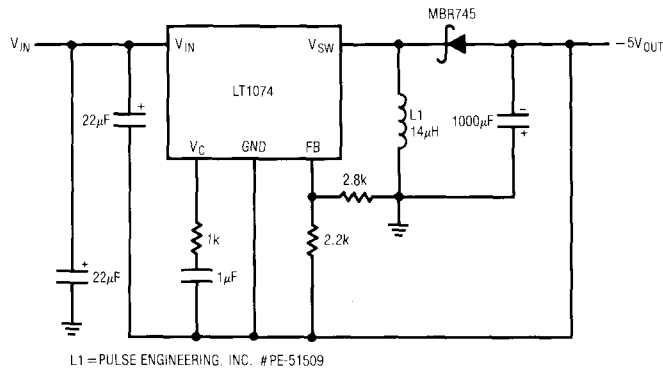


Figure 11. Nelson's Circuit . . . A (Better) Negative Output Step Down Regulator

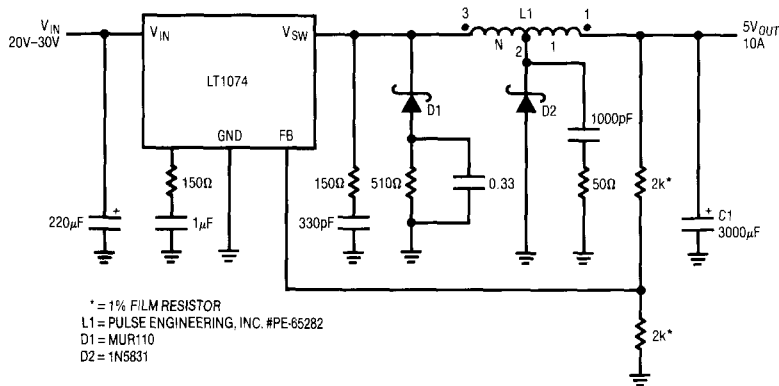


Figure 12. "Current Boosted" Step Down Regulator. Boost Current is Supplied by Energy Stored in the Tapped Inductor.

through C1 and D2 (trace E), somewhat increasing output voltage ripple. Not all the energy is transferred to the "1" winding. Current (trace C) will continue to flow in the "N" winding due to leakage inductance. A snubber network suppresses the effects of this leakage inductance. For lowest snubber losses the specified tapped inductor is bifilar wound for maximum coupling.

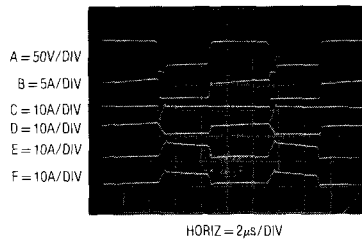
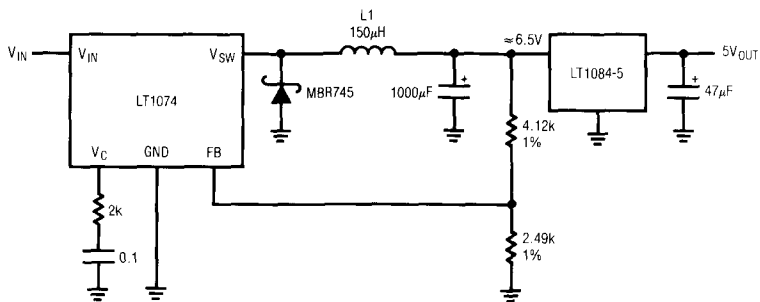


Figure 13. AC Current Flow for the Boosted Regulator

Post Regulation-Fixed Case

In most instances the LT1074 output will be applied directly to the load. Those cases requiring faster transient response or reduced noise will benefit from linear post regulation. In Figure 14 a three terminal regulator follows the LT1074 output. The LT1074 output is set to provide just

enough voltage to the LT1084 to maintain regulation. The LT1084's low dropout characteristics combined with a high circuit input voltage minimizes the overall efficiency penalty.



L1 = PULSE ENGINEERING, INC. #PE-51516

Figure 14. Linear Post-Regulator Improves Noise and Transient Response

Post Regulation-Variable Case

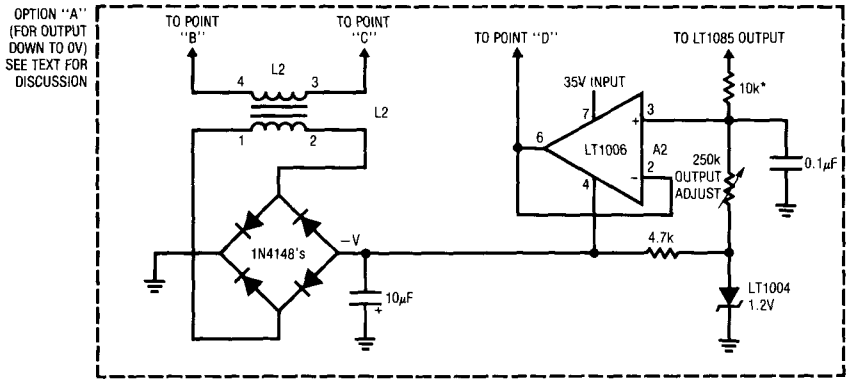
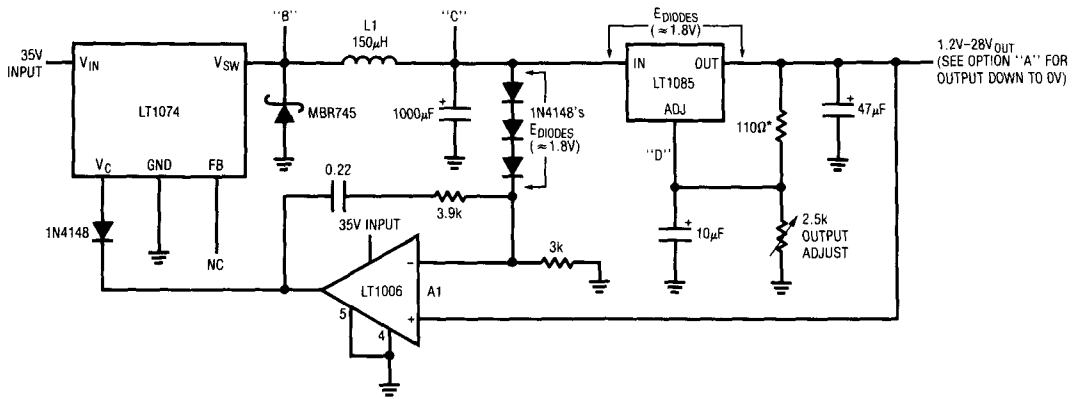
Some situations require variable linear post regulation. Figure 15 does this with little efficiency sacrifice. The LT1085 operates in normal fashion, supplying a variable 1.2V–28V output. The remainder of the circuit forms a switched mode pre-regulator which maintains a small, fixed voltage across the LT1085 regardless of its output voltage. A1 biases the LT1074 to produce whatever voltage is necessary to maintain the “E diodes” potential across the LT1085. A1’s inputs are balanced when the LT1085 output is “E diodes” above its input. A1 maintains this condition regardless of line, load or output voltage conditions. Thus, good efficiency is maintained over the full range of output voltages. The RC network at A1 compensates the loop. Loop start-up is assured by deliberately introducing a positive offset to A1. This is done by grounding A1’s appropriate balance pin (5), resulting in a positive 6mV offset. This increases amplifier drift, and is normally considered poor practice, but causes no measurable error in this application.

As shown, the circuit cannot produce outputs below the LT1085’s 1.2V reference. Applications requiring output adjustability down to 0V will benefit from option “A” shown on the schematic. This arrangement replaces L1 with L2. L2’s primary performs the same function as L1 and its coupled secondary winding produces a negative bias output (–V). The full wave bridge rectification is necessitated by widely varying duty cycles. A2 and its attendant circuitry replace all components associated with the

LT1085 V_{ADJ} pin. The LT1004 reference terminates the 10k–250k feedback string at –1.2V with A2 providing buffered drive to the LT1085 V_{ADJ} pin. The negative bias allows regulated LT1085 outputs down to 0V. The –V potential derived from L2’s secondary varies considerably with operating conditions. The high feedback string values and A2’s buffering ensure stable circuit operation for “starved” values of –V.

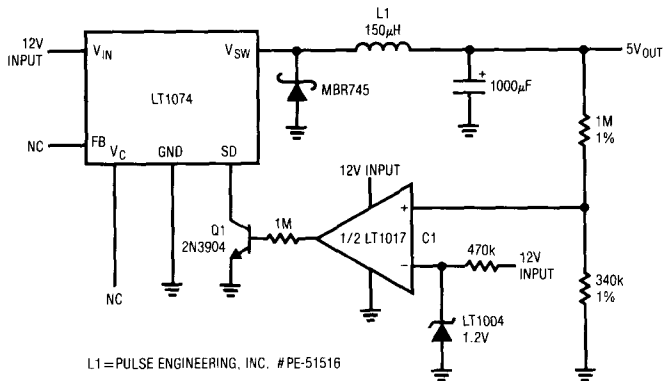
Low Quiescent Current Regulators

Many applications require very wide ranges of power supply output current. Normal conditions require currents in the ampere range, while standby or “sleep” modes draw only microamperes. A typical lap-top computer may draw 1 to 2 amperes running while needing only a few hundred microamps for memory when turned off. In theory, any regulator designed for loop stability under no-load conditions will work. In practice, a converter’s relatively large quiescent current may cause unacceptable battery drain during low output current intervals. Figure 16’s simple loop effectively reduces circuit quiescent current from 6mA to only 150µA. It does this by utilizing the LT1074’s shutdown pin. When this pin is pulled within 350mV of ground the IC shuts down, pulling only 100µA. Comparator C1 combines with the LT1004 reference and Q1 to form a “bang-bang” control loop around the LT1074. The LT1074’s internal feedback amplifier and voltage reference are bypassed by this loops operation. When the circuit output (trace C, Figure 17) falls slightly below 5V C1’s output (trace A) switches low, turning off Q1 and enabling the



L1 = PULSE ENGINEERING, INC. #PE-51516
 L2 = PULSE ENGINEERING, INC. #PE-65050

Figure 15. Adjustable Linear Post-Regulator Maintains Efficiency Over Widely Varying Operating Conditions



L1 = PULSE ENGINEERING, INC. #PE-51516

Figure 16. A Simple Loop Reduces Quiescent Current to 150µA

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LT1074. The V_{SW} pin (trace B) pulses at full duty cycle, forcing the output back above 5V. C1 then biases Q1 again, the LT1074 goes into shutdown, and loop action repeats. The frequency of this on-off control action is directly load dependent, with typical repetition rates of 0.2Hz at no load. Short on-times keep duty cycle low, resulting in the small effective quiescent current noted. The on-off operation combines with the LC filtering action in the regulator's V_{SW} line to generate an output hysteresis of about 50mV (again, see Figure 17, trace C).

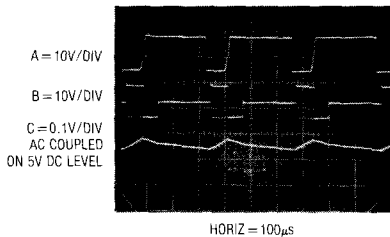


Figure 17. The Low Quiescent Current Loop's Waveforms

The loop performs well, but has two potential drawbacks. At higher output currents the loop oscillates in the 1kHz-10kHz range, causing audible noise which may be objectionable. This is characteristic of this type of loop, and is the reason that IC's employing gated oscillators invariably produce such noise. Additionally, the control loops operation causes about 50mV of ripple on the output. Ripple frequency ranges from 0.2Hz to 10kHz depending upon input voltage and output current.

Figure 18's more sophisticated circuit eliminates these problems with some increase in complexity. Quiescent current is maintained at 150µA. The technique shown is particularly significant, with broad implication in battery powered systems. It is easily applied to a wide variety of regulator requirements, meeting an acknowledged need across a wide spectrum of applications.

Figure 18's signal flow is similar to Figure 16, but additional circuitry appears between the feedback divider and the LT1074. The LT1074's internal feedback amplifier and reference are not used. Figure 19 shows operating wave-

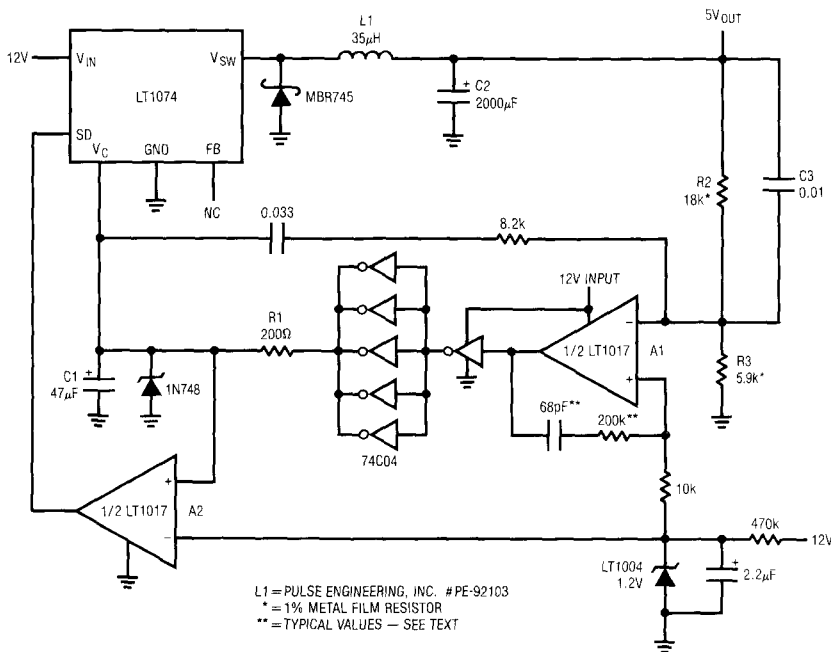


Figure 18. A More Sophisticated Loop Gives Better Regulation While Maintaining 150µA Quiescent Current

forms under no load conditions. The output (trace A) ramps down over a period of seconds. During this time comparator A1's output (trace B) is low, as are the 74C04 paralleled inverters. This pulls the V_C pin (trace D) low, forcing the regulator to zero duty cycle. Simultaneously, A2 (trace C) is low, putting the LT1074 in its $100\mu\text{A}$ shutdown mode. The V_{SW} pin (trace E) is off, and no inductor current flows. When the output drops about 60mV, A1 triggers and the inverters go high, pulling the V_C pin up and biasing the regulator. The zener diode prevents V_C pin overdrive. A2 also rises, taking the IC out of shutdown mode. The V_{SW} pin pulses the inductor at the 100kHz clock rate, causing the output to abruptly rise. This action trips A1 low, forcing the V_C pin back low and shutting off V_{sw} pulsing. A2 also goes low, putting the LT1074 into shutdown.

This "bang-bang" control loop keeps the 5V output within the 60mV ramp hysteresis window set by the loop. Note

that the loop oscillation period of seconds means the $R1-C1$ time constant at V_C is not a significant term. Because the LT1074 spends almost all of the time in shutdown, very little quiescent current ($150\mu\text{A}$) is drawn.

Figure 20 shows the same waveforms with the load increased to 2mA. Loop oscillation frequency increases to keep up with the loads sink current demand. Now, the V_C pin waveform (trace D) begins to take on a filtered appearance. This is due to $R1-C1$'s 10ms time constant. If the load continues to increase, loop oscillation frequency will also increase. The $R1-C1$ time constant, however, is fixed. Beyond some frequency, $R1-C1$ must average loop oscillations to DC. At 7mA loading (Figure 21) loop frequency further increases, and the V_C waveform (trace D) appears heavily filtered.

Figure 22 shows the same circuit points at 2A loading. Note that the V_C pin is at DC, as is the shutdown pin. Repetition rate has increased to the LT1074's 100kHz clock

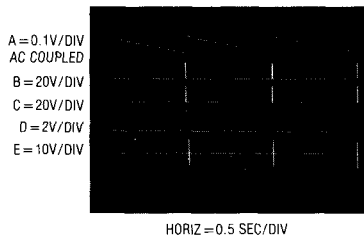


Figure 19. Low Quiescent Current Regulator's Waveforms With No Load (Traces B, C, and E Retouched for Clarity)

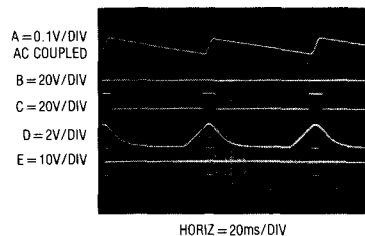


Figure 20. Low Quiescent Current Regulator's Waveforms at 2mA Loading

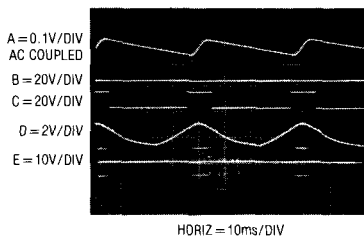


Figure 21. Low Quiescent Current Regulator's Waveforms at 7mA Loading

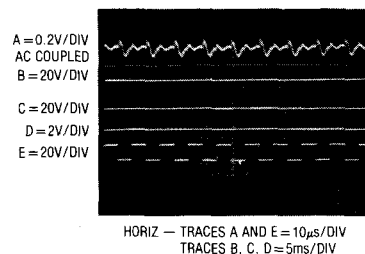


Figure 22. Low Quiescent Current Regulator's Waveforms at 2A Loading

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frequency. Figure 23 plots what is occurring, with a pleasant surprise. As output current rises, loop oscillation frequency also rises until about 23Hz. At this point the R1-C1 time constant filters the V_C pin to DC and the LT1074 transitions into "normal" PWM operation. With the V_C pin at DC it is convenient to think of A1 and the inverters as a linear error amplifier with a closed loop gain set by the R2-R3 feedback divider. In fact, A1 is still duty cycle modulating, but at a rate far above R1-C1's break frequency. The phase error contributed by C2 (which was selected for low loop frequency at low output currents) is dominated by the R1-C1 roll off and the C3 lead into A1. The loop is stable and responds linearly for all loads beyond 10mA. In this high current region the LT1074 is desirably "fooled" into behaving like a conventional step down regulator.

A formal stability analysis for this circuit is quite complex, but some simplifications lend insight into loop operation. At $250\mu\text{A}$ loading (20k Ω) C2 and the load form a decay time constant exceeding 30 seconds. This is orders of magnitude larger than R2-C3, R1-C1, or the LT1074's 100kHz commutation rate. As a result, C2 dominates the loop. Wideband A1 sees phase shifted feedback, and very low frequency oscillations similar to Figure 19's occur⁵. Although C2's *decay* time constant is long, its *charge* time constant is short because the circuit has low sourcing impedance. This accounts for the ramp nature of the oscillations.

Increased loading reduces the C2-load decay time constant. Figure 23's plot reflects this. As loading increases,

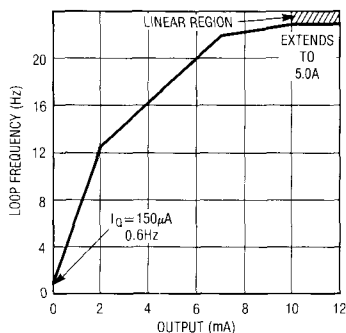


Figure 23. Figure 18's Loop Frequency vs Output Current. Note Linear Loop Operation Above 10mA.

the loop oscillates at a higher frequency due to C2's decreased decay time. When the load impedance becomes low enough C2's decay time constant ceases to dominate the loop. This point is almost entirely determined by R1 and C1. Once R1 and C1 "take over" as the dominant time constant the loop begins to behave like a linear system. In this region (e.g. above about 10mA, per Figure 23) the LT1074 runs continuously at its 100kHz rate. Now, C3 becomes significant, performing as a simple feedback lead⁶ to smooth output response. There is a fundamental trade-off in the selection of the C3 lead value. When the converter is running in its linear region it must dominate the loops time lag generated hysteretic characteristic. As such, it has been chosen for the best compromise between output ripple at high load and loop transient response.

Despite the complex dynamics transient response is quite good. Figure 24 shows performance for a step from no load to 1A. When trace A goes high a 1A load appears across the output (trace C). Initially, the output sags almost 200mV due to slow loop response time (the R1-C1 pair delay V_C pin (trace B) response). When the LT1074 comes on response is reasonably quick and surprisingly well behaved considering circuit dynamics. The multi-time constant recovery⁷ ("rattling") is perhaps more appropriate is visible in trace C's response.

Note 5: Some layouts may require substantial trace area to A1's inputs. In such cases the optional RC network around A1 ensures clean transitions at A1's output.

Note 6: "Zero Compensation" for all you technosnobs out there.

Note 7: Once again, "multi-pole settling" for those who adore jargon.

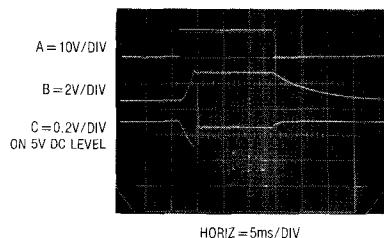


Figure 24. Load Transient Response for Figure 18

Figure 25 plots efficiency vs. output current. High power efficiency is similar to standard converters. Low power efficiency is somewhat better, although poor in the lowest ranges. This is not particularly bothersome, as power loss is very small.

The loop provides a controlled, conditional instability instead of the usually more desirable (and often elusive) unconditional stability. This deliberately introduced characteristic dramatically lowers converter quiescent current without sacrificing high power performance.

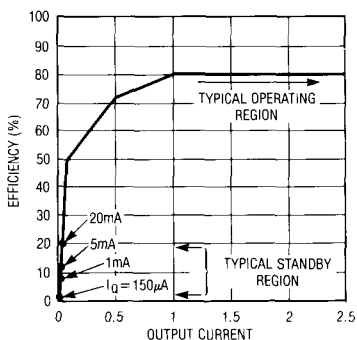


Figure 25. Efficiency vs Output Current for Figure 18. Standby Efficiency is Poor, But Power Loss Approaches Battery Self-Discharge

Wide Range, High Power, High Voltage Regulator

BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF THIS CIRCUIT. HIGH VOLTAGE. LETHAL POTENTIALS ARE PRESENT IN THIS CIRCUIT. EXTREME CAUTION MUST BE USED IN WORKING WITH AND MAKING CONNECTIONS TO THIS CIRCUIT. REPEAT: THIS CIRCUIT CONTAINS DANGEROUS, HIGH VOLTAGE POTENTIALS. USE CAUTION.

Figure 26 is an example of the LT1074 making a complex function practical. This regulator provides outputs from millivolts to 500V at 100W with 80% efficiency. A1 compares a variable reference voltage with a resistively scaled version of the circuit's output and biases the LT1074 switching regulator configuration. The switcher's DC output drives a toroidal DC-DC converter comprised of L1, Q1

and Q2. Q1 and Q2 receive out of phase square wave drive from the 74C74 + 4 flip-flop stage and the LT1010 buffers. The flip-flop is clocked from the LT1074 V_{SW} output via the Q3 level shifter. The LT1086 provides 12V power for A1 and the 74C74. A1 biases the LT1074 regulator to produce the DC input at the DC-DC converter required to balance to loop. The converter has a voltage gain of about 20, resulting in high voltage output. This output is resistively divided down, closing the loop at A1's negative input. Frequency compensation for this loop must accommodate the significant phase errors generated by the LT1074 configuration, the DC-DC converter and the output LC filter. The $0.47\mu\text{F}$ roll-off term at A1 and the 100Ω - $0.15\mu\text{F}$ RC lead network provide the compensation, which is stable for all loads.

Figure 27 gives circuit waveforms at 500V output into a 100W load. Trace A is the LT1074 V_{SW} pin while trace B is its current. Traces C and D are Q1 and Q2's drain waveforms. The disturbance at the leading edges is due to cross-current conduction, which lasts about 300ns — a small percentage of the cycle. Transistor currents during this interval remain within reasonable values, and no over-stress or dissipation problems occur. This effect could be eliminated with non-overlapping drive to Q1 and Q2⁸, although there would be no reliability or significant efficiency gain. The 500kHz ringing on the same waveforms is due to excitation of transformer resonances. These phenomena are not deleterious, although L1's primary RC damper is included to minimize them.

All waveforms are synchronous because the flip-flop drive stage is clocked from the LT1074 V_{SW} output. The LT1074's maximum 95% duty cycle means that the Q1-Q2 switches can never see destructive DC drive. The only condition allowing DC drive occurs when the LT1074 is at zero duty cycle. This case is clearly non-destructive, because L1 receives no power.

Figure 28 shows the same circuit points as Figure 27, but at only 5mV output. Here, the loop restricts drive to the DC-DC converter to small levels. Q1 and Q2 chop just 70mV into L1. At this level L1's output diode drops look large, but loop action forces the desired 0.005V output.

Note 8: For an example of this technique see LTC Application Note 29, Figure 1.

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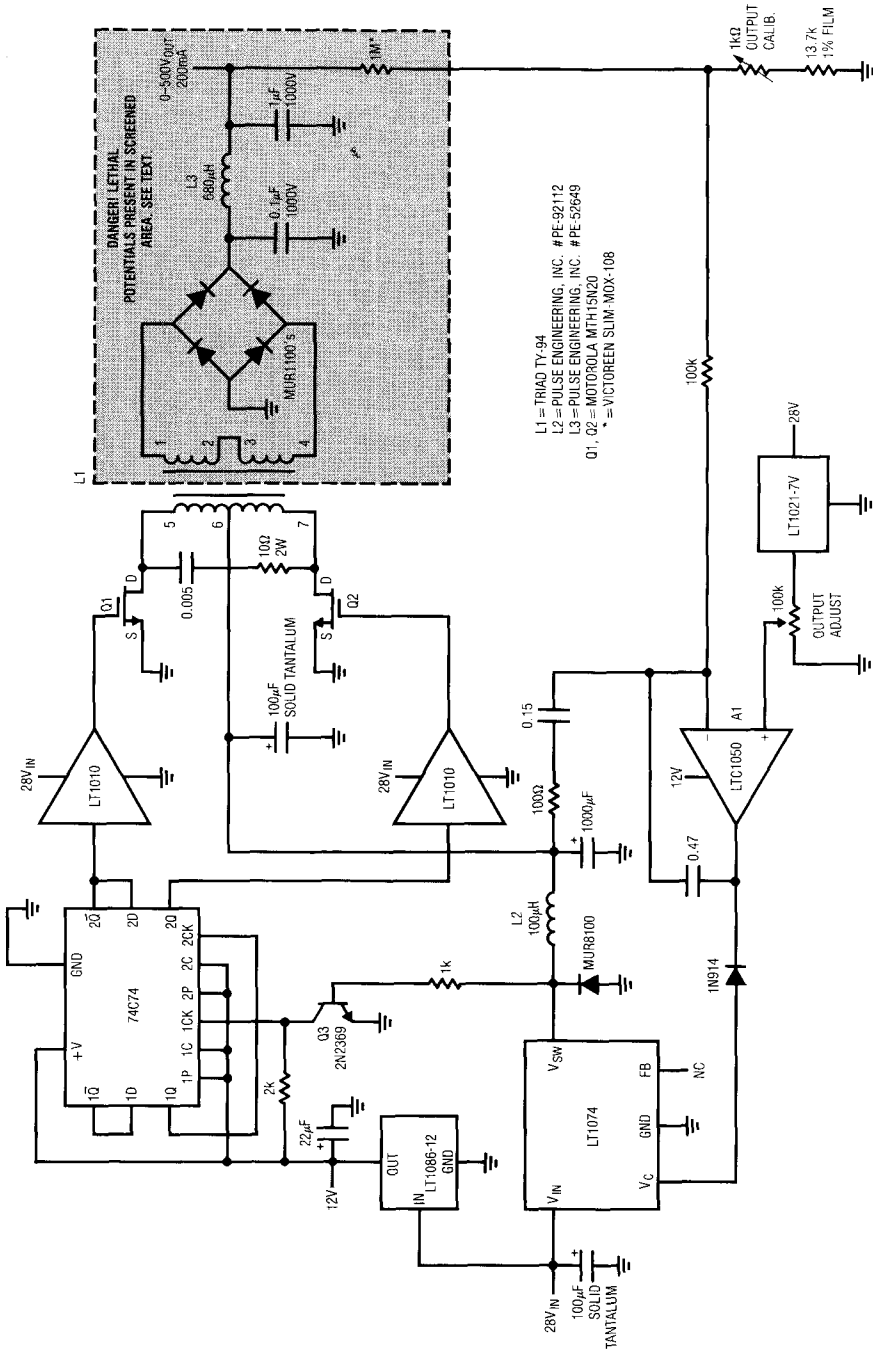


Figure 26. LT1074 Permits High Voltage Output Over 100dB Range with Power and Efficiency. **DANGER! Lethal Potentials Present — See Text.**

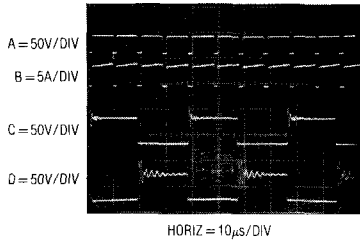


Figure 27. Figure 26's Operating Waveforms at 500V Output Into a 100W Load

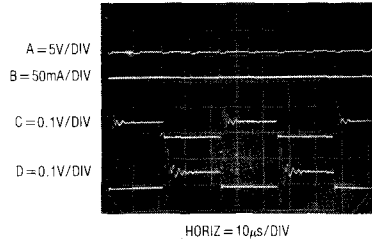


Figure 28. Figure 26's Operating Waveforms at 0.005V Output

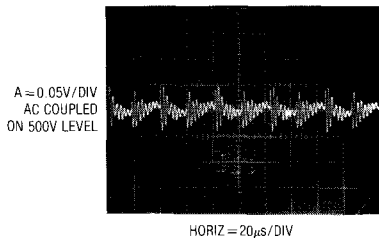


Figure 29. Figure 26's Output Noise at 500V into a 100W Load. Residue is Composed of Q1-Q2 Chopping Artifacts and Transformer Related Ringing. **DANGER! Lethal Potentials Present — See Text.**

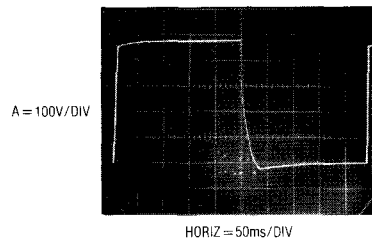


Figure 30. 500V Step Response with 100W Load (Photo Retouched for Clarity). **DANGER! Lethal Potentials Present — See Text.**

The LT1074's switched mode drive to L1 maintains high efficiency at high power, despite the circuits wide output range⁹.

Figure 29 shows output noise at 500V into a 100W load. Q1-Q2 chopping artifacts and transformer related ringing are clearly visible, although limited to about 80mV. The coherent noise characteristic is traceable to the synchronous clocking of Q1 and Q2 by the LT1074.

A 50V to 500V step command into a 100W load produces the response of Figure 30. Loop response on both edges is

clean, with the falling edge slightly underdamped. This slew asymmetry is typical of switching configurations, because the load and output capacitor determine negative slew rate. The wide range of possible loads mandates a compromise when setting frequency compensation. The falling edge could be made critically or even over damped, but response time for other conditions would suffer. The compensation used seems a reasonable compromise.

Note 9: A circuit related to the one presented here appears in LTC Application Note 18 (Figure 13). Its linear drive to the step-up DC-DC converter forces dissipation, limiting output power to about 15W. Similar restrictions apply to Figure 7 in Application Note 6.

Application Note 35

Regulated Sinewave Output DC-AC Converter

BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF THIS CIRCUIT. HIGH VOLTAGE, LETHAL POTENTIALS ARE PRESENT IN THIS CIRCUIT. EXTREME CAUTION MUST BE USED IN WORKING WITH AND MAKING CONNECTIONS TO THIS CIRCUIT. REPEAT: THIS CIRCUIT CONTAINS DANGEROUS, HIGH VOLTAGE POTENTIALS. USE CAUTION.

Figure 31 is another example of the LT1074 permitting the practical implementation of a complex function. It converts a 28V DC input to a regulated 115V_{AC} 400Hz sinewave output with 80% efficiency. Waveform distortion is below 1.6% at 50W output. This design shares similarities with the previous circuit. The LT1074 supplies efficient drive to a high voltage converter despite large line and load variations. An amplifier (A1) controls the input to the high voltage converter via A2 and the LT1074 switching regulator. The high voltage output is divided down and fed back to the amplifier where it is compared to a reference to close a loop. In the previous circuit the output is DC; here the output is AC. As such, A1's reference (trace A, Figure 32) is an amplitude and frequency stabilized 800Hz half-sine¹⁰. The high voltage converter is driven from a flip-flop clocked by a reference synchronized pulse (negative going excursions just visible in trace B) via level shift transistor Q3. The reference synchronized pulse occurs at the zero voltage point of the half-sine. The flip-flop outputs (traces C and D, respectively) drive the Q1 and Q2 gates. RC filters in the gate line retard the drive's slew rate.

A1 biases the LT1074's V_C pin via A2 to produce an 800Hz half-sine signal at L2's center tap (trace E). Because Q1 and Q2 are synchronously driven with the reference half-sine their drain waveforms (traces F and G) reveal alternate chopping of complete half cycles. L2 receives balanced drive and its secondary recombines the chopped half-sines into a 115V_{AC} 400Hz sinewave output (trace H). The diode bridge rectifies L2's output back to an 800Hz half-sine which is fed to A1 via the resistor divider. A1 balances this signal against the reference half-sine to close a loop. Transmitting the 800Hz waveform around the loop requires attention to available bandwidth. The LT1074's 100kHz switching frequency is theoretically high enough to permit this, but the bandwidth attenuation of its output

LC filter must be considered. The unusually low output filter capacitor value allows the necessary frequency response. A1's 330k-0.01 μ F components combine with the RC lead network across the 16k feedback resistor to stabilize the loop.

A2 closes a local loop around the LT1074 configuration. This is necessary because L2 blocks DC information from being conducted around A1's loop. This is a concern because the waveform presented to L2's primary center tap must have no DC component. DC content at this point will cause waveform distortion, transformer power dissipation or both. The LT1074's V_C pin operates with substantial and uncertain DC bias, making A1's inability to control DC errors unacceptable. A2 corrects this by biasing the LT1074 V_C pin at its DC threshold so that no DC component is presented to L2. A1's output represents the difference between the AC coupled circuit output and the half-sine reference. A2's output contains this information in addition to DC restoration information. L2 and A1 contribute essentially no DC error, so A2's loop may be closed at the LT1074 configuration's output. A2's feedback capacitor stabilizes this local loop.

The drive to L2 cannot sink current. This means that any residual energy stored in L2 when the drive waveform goes to zero sees no exit path. This is a relatively small effect, but can cause output crossover distortion. The synchronous switch option shown on the schematic provides such a path, and is recommended for lowest output distortion. This optional circuitry is detailed in Appendix E.

Figure 33A and 33B show waveforms in the "turnaround" region of circuit operation. This is the most critical part of the converter, and its characteristics directly determine output waveform purity. Figure 33A (trace A), a highly amplitude and time expanded version of L2's center tap drive, arrives at 0V (upper cross-etched horizontal line) and turns around cleanly. This action is just slightly time skewed from the reference synchronized pulse (trace B). The aberration on the rising edge is due to the optional synchronous switch's operation. This switch is shorted during the on-time of trace C's pulse (see Appendix E for operating details of this option). Trace D, Q2's gate drive,

Note 10: Complete operating details of the half-sine reference generator appear in Appendix E.

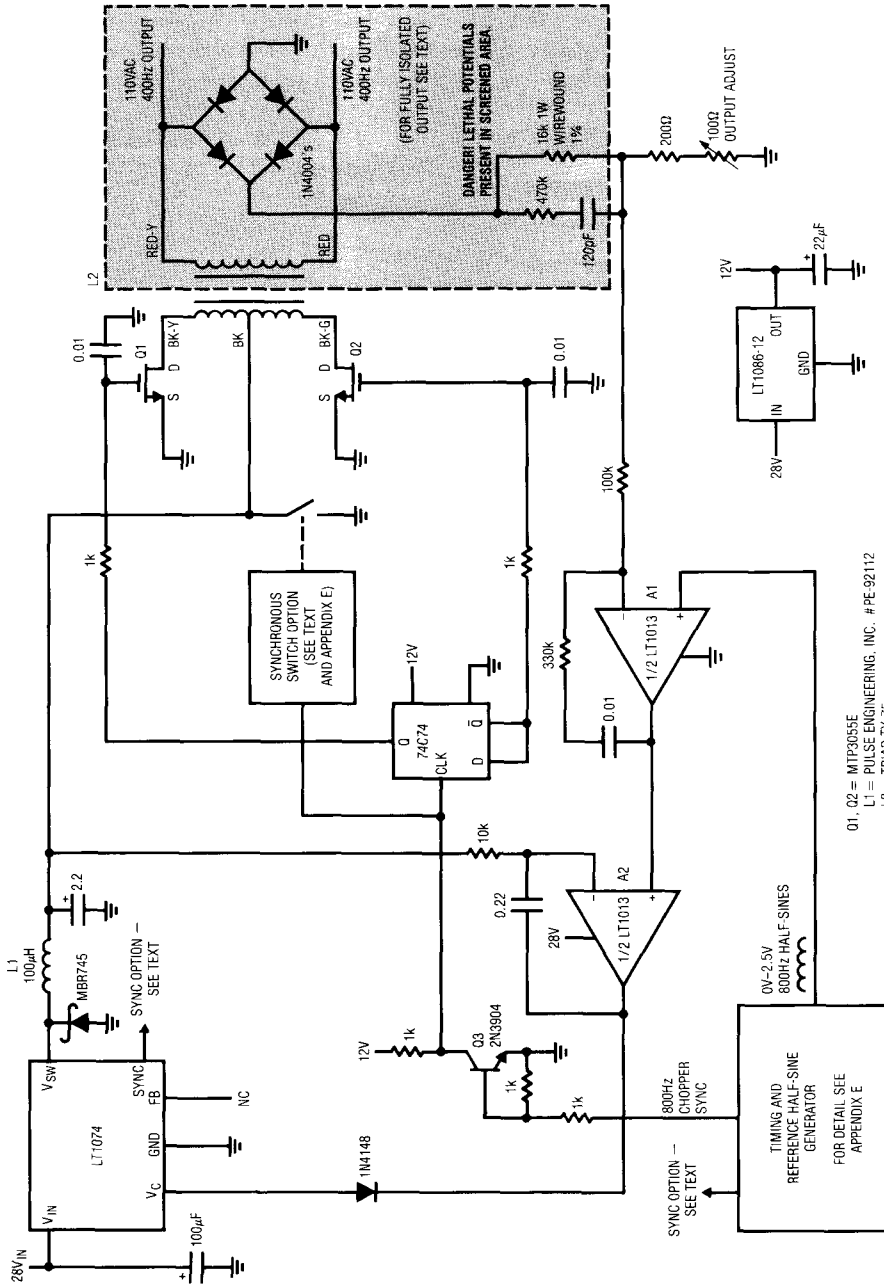


Figure 31. LT1074 Based +28-110VAC 400Hz Converter. Sinewave Output Shows Only 1.6% Distortion. **DANGER! Lethal Potentials Present — See Text.**

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aligns with trace B's pulse. The slew reduction caused by the $1k-0.01\mu F$ filter is clearly visible, and contributes to trace A's low noise turnaround. The LT1074's 100kHz chopping related components are easily observed in trace A. Waveforms at the next half cycle's zero point (e.g. Q1's gate driven) are identical.

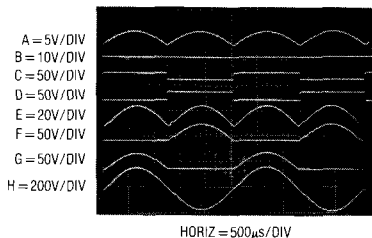


Figure 32. +28--110VAC, 400Hz Converter's Waveforms. The Optional Synchronous Switch is Disabled in this Photo, Resulting in Relatively High Crossover Distortion (Trace H). DANGER! Lethal Potentials Present -- See Text.

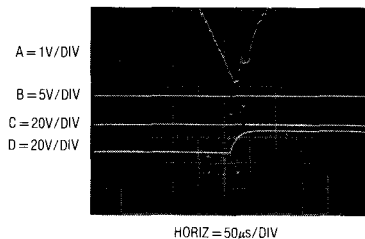


Figure 33A

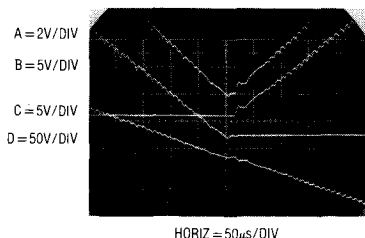


Figure 33B

Figure 33A and 33B. Details of "Turnaround" Sequence. Switching Characteristics Directly Determine Output Crossover Distortion. DANGER! Lethal Potentials Present -- See Text.

Figure 33B shows additional details at highly expanded amplitude and time scales. L2's center tap is trace A, Q1's drain is trace B and Q2's drain trace C. The output sinewave (trace D) is shown as it crosses through zero.

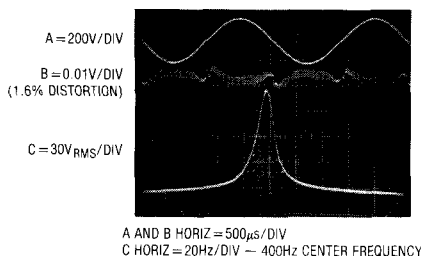


Figure 34. Distortion and Spectral Characteristics for the Sinewave Output Converter. Distortion Trace (B) Shows Crossover Aberrations and LT1074 Wideband Chopping Residue. The Synchronous Switch Option is Employed in This Photo for Lowest Distortion. DANGER! Lethal Potentials Present -- See Text.

Figure 34 studies waveform purity. Trace A is the sinewave output at 50W loading. Trace B shows distortion products, which are dominated by turnaround related crossover aberrations and LT1074 100kHz chopping residue. Although not strictly necessary, the LT1074's switching can be synchronized to the reference half-sine for coherent noise characteristics. This option is discussed in Appendix E, along with other reference generator details. Trace C is a spectrum analysis centered at 400Hz¹¹. In this photo the optional synchronous switch is used, accounting for improved crossover characteristics over Figure 32.

If a fully floating output is desired the output diode bridge can be isolated by a simple 1:1 ratio transformer. To calibrate this circuit trim the "output adjust" potentiometer for a 115V_{AC} output. Regulation remains within 1% over wide variations of input and load.

Note 11: Test equipment aficionados may wish to consider how this picture was taken. Hint: Double exposure techniques were not used. This photograph is a real time, simultaneous display of frequency and time domain information.

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Note: This application note was derived from a manuscript originally prepared for publication in EDN magazine.

APPENDIX A

Physiology of the LT1074

The LT1074 uses standard (as opposed to current mode) pulse width modulation, with two important differences. First, it is a clocked system with a maximum duty cycle of approximately 95%. This allows a controlled start-up when it is used as a positive to negative converter or a negative boost converter. Second, duty cycle is an inverse function of input voltage ($DC \approx 1/V_{IN}$), without any change in error amplifier output. This greatly improves line transient response and ripple rejection, especially for designs which have the control loop over-damped.

Referring to the block diagram, the heart of the LT1074 consists of the oscillator, the error amplifier A1, an analog multiplier, comparator C6, and an RS flip-flop. A complete switching cycle begins with the reset (down ramp) period of the oscillator. During this time ($\approx 0.7\mu s$), the RS flip-flop is set and the switch driver Q104 is kept off via the "and" gate G1. At the end of the reset time, Q104 turns on and drives the output switch Q111, Q112, and Q113. The oscillator ramp starts upward, and when it is equal to the output voltage of the analog multiplier, C6 resets the RS flip-flop, turning off the output switch. Duty cycle is therefore controlled by the output of the multiplier which in turn is controlled by the output of the error amplifier, A1.

A multiplier is used in the LT1074 to provide a perfect "feed forward" function. Conventional switching regulators sometimes use a simple form of feed forward to adjust duty cycle immediately when input voltage changes. This reduces the requirement for voltage swing at the output of the error amplifier as it tries to correct for line variations. Bandwidth of switching regulator error amplifiers must be fairly low to maintain loop stability, so rather large output perturbations occur when the output of the error amplifier must move quickly to correct for line variations. Conventional feed forward schemes typically operate well over a restricted input voltage range or are effective only at certain frequencies. The multiplier technique is very effective over the full range of input voltage and at all frequencies. The basic function is to compensate for the generalized buck regulator transfer function; $V_{OUT} = (V_{IN}) (DC)$, where $DC =$ switch duty cycle. This transfer function has two implications. First, it is obvious that to maintain a constant output, duty cycle must change inversely with input voltage. Second, input voltage appears in the loop transfer function, i.e., a fixed variation in duty cycle gives different variations in output voltage depending on input voltage. Loop gain is directly proportional to input voltage, and this can cause loop instability or slow loop response

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if input voltage varies over a wide range. The multiplier takes out all input voltage effects by automatically adjusting loop gain inversely with input voltage. The multiplier output (V_O) is equal to error amplifier output (V_E) divided by input voltage (V_{IN}); $V_O = (V_R) \cdot (V_E) / (V_{IN})$. V_R is a fixed voltage required by all analog multipliers to define multiplier gain. It has an effective value of approximately 20V in the LT1074.

The error amplifier used in the LT1074 is a transconductance type. It has high output impedance ($\approx 500k\Omega$), so that its AC voltage gain is defined by the impedance of external shunt frequency compensation components (Z_C) and the transconductance (gm) of the amplifier, $A_V = (gm) (A_C)$. gm is $\approx 3500\mu mho$. The error amplifier has its non-inverting input committed to an internal 2.3V reference. The inverting input (fb) is brought out for connection to an external voltage divider that establishes regulator output voltage.

Two other connections are made internally to the fb pin. A window comparator consisting of C4, C5, and some logic provides an "output status" function. It monitors the voltage on the fb pin and gives a "high" output only when the fb voltage is within $\pm 5\%$ of the internal reference voltage. This status output can be used to alert external circuitry that the regulator output is "in" or "out" of regulation. The delay and one shot circuits ensure that switching EMI will not cause spurious outputs, and that the minimum time for an "out-of-bounds" (low) status output is $\approx 20\mu s$. Also tied to the fb pin is a frequency shift circuit consisting of R15 and Q36. The base of Q36 is biased at $\approx 1V$ so that Q36 turns on when the fb pin drops below $\approx 0.6V$. Current through Q36 smoothly decreases oscillator frequency. This is necessary for maintaining control of current limit at high input voltages. A "dead short" on the output of a switching regulator requires that switch "on" time reduce to $(V_D) / (V_{IN}(f))$, where V_D is the forward voltage of the output catch diode and f is switching frequency. V_D is typically 0.5V for a Schottky catch diode, forcing switch "on" time to shrink to a theoretical 0.1 μs for a 50V input and 100kHz switching frequency with a shorted output. In practical circuits, effective "on" time can stretch to 0.3 μs under these conditions due to losses in the inductor wire resistance and switch rise and fall time. The LT1074 can-

not reduce switch "on" time to less than $\approx 0.6\mu s$ in current limit because it has true pulse-by-pulse switch current limiting. The current limit circuitry must sense switch current *after* the switch turns on, and then send a signal to turn the switch off. Minimum time for this signal path is 0.6 μs . Full control of current limit is maintained by reducing switching frequency when the output falls to less than approximately 15% of its regulated value. This has no effect on normal operation and does not change the selection of external components such as the inductor or output capacitor.

True pulse-by-pulse current limiting is performed by comparator C7. It monitors the voltage across sense resistor R52 and resets the RS flip-flop. Current limit threshold is set by the voltage across R47 which in turn is set by the voltage on the I_{LIM} pin. The I_{LIM} voltage is determined by an external resistor or by an internal clamp of 5V if no external resistor is used. To compensate for the temperature coefficient of R47 ($\approx +0.25\%/^{\circ}C$), the internal current source I_L has a matching positive temperature coefficient. Its nominal value is 300 μA at 25 $^{\circ}C$. Current limit can be set from 1A to 6A with one external resistor between I_{LIM} and ground. If no resistor is used, the I_{LIM} pin will self clamp at $\approx 5V$ and current limit will be $\approx 6.5A$. A small pre-bias is added to the negative input of C7 to ensure that current limit will go to zero (no switching) when the I_{LIM} pin is pulled to 0V, either by an external short or via Q11 during under-voltage lockout. Soft start can be achieved by connecting a capacitor to the I_{LIM} pin. Fold-back current limiting can also be implemented by connecting a resistor from I_{LIM} to the regulated output.

Switching frequency of the LT1074 is internally set at 100kHz, but can be increased by connecting a resistor from the frequency pin to ground. This resistor biases on Q79 and feeds extra current into the oscillator. Maximum suggested frequency is 200kHz. A comparator, C3, is also connected to the frequency pin and allows this pin to be used for synchronizing the oscillator to an external clock, even when the pin is also being used to boost oscillator frequency. R35 keeps the frequency pin biased correctly in a no-function state when it is left open and R36 limits Q79 current if the frequency pin is accidentally shorted to ground.

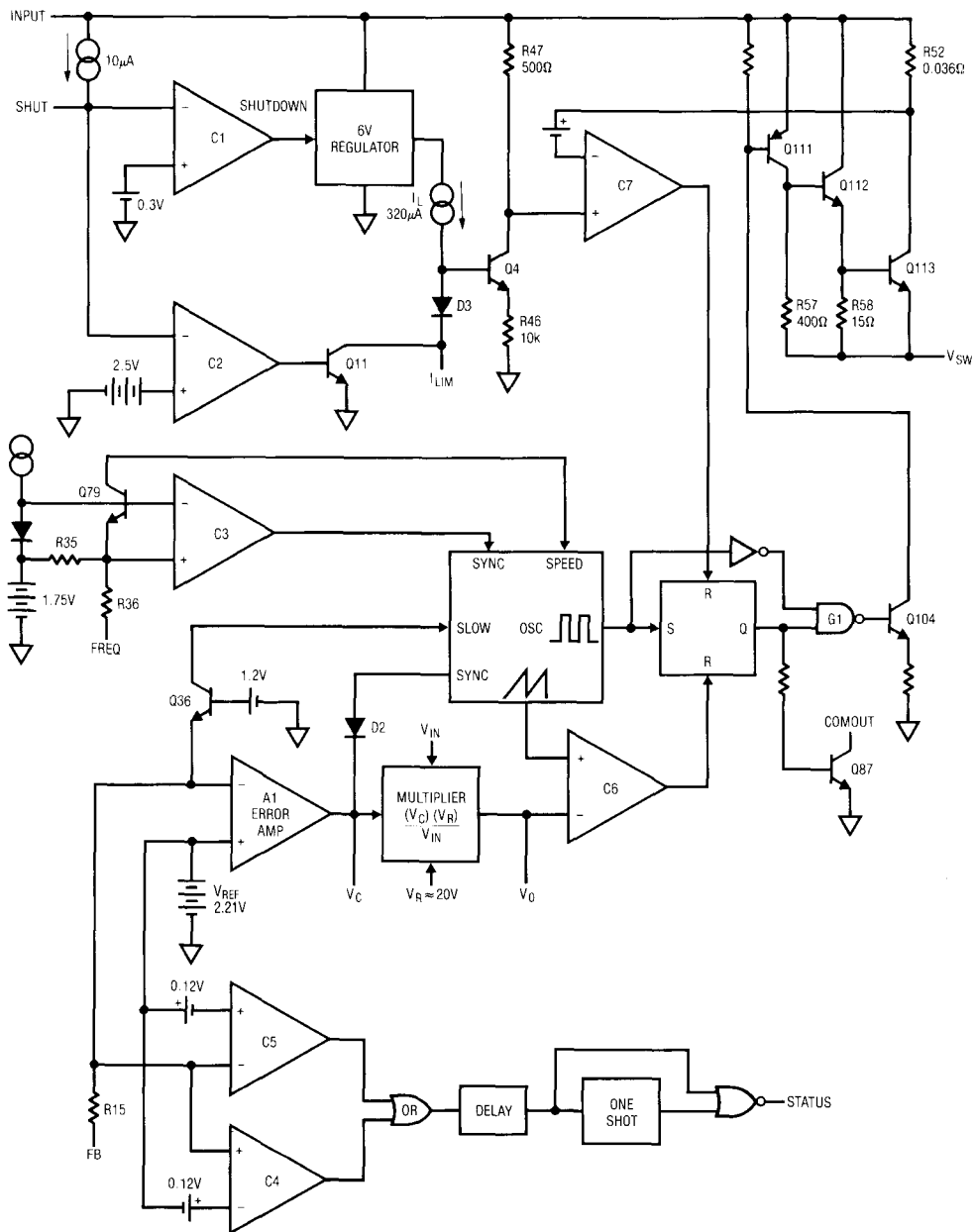


Figure A1. Simplified LT1074 Internal Details

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The shutdown pin on the LT1074 can be used as a logic control of output switching, as an under-voltage lockout, or to put the regulator into complete shutdown with $I_{SUPPLY} \approx 100\mu A$. Comparator C2 has a threshold of 2.5V. It forces the output switch to a 100% "off" condition by pulling the I_{LIM} pin low via Q11. Under-voltage lockout is implemented through C2 by connecting the tap of an input voltage divider to the shutdown pin. Full micropower shutdown of the regulator is achieved by pulling the shutdown pin below the 0.30V threshold of C1. This turns off the chip by shutting down the internal 6V bias supply. An internal $10\mu A$ current source pulls the shutdown pin high (inactive) if it is left open.

The Comout pin is an open-collector NPN whose collector voltage is the complement of the switch output (V_{SW}). Q87 is specified to drive up to 10mA and 30V. It is intended to drive the gate of an external N-channel MOS switch which is in parallel with the catch diode. The MOS switch then acts as a synchronous rectifier, which can significantly improve converter efficiency in low output voltage applications. The Comout pin can also be used to drive the gate of

an external P-channel MOS switch in parallel with the internal bipolar switch to provide ultra-high efficiency switching at lower input voltages. A slight time-shift in the Comout signal prevents switch overlap problems.

The combination of these features produces a DC-to-DC converter with the electrical characteristics shown in Figure A2.

PARAMETER	CONDITIONS	UNITS
Input Voltage Range		4.5V to 60V
Output Voltage Range		2.5V to 50V
Output Current Range	Standard Buck Tapped Buck	0A to 5A 0A to 10A
Quiescent Input Current		7mA
Switching Frequency		100kHz to 200kHz
Switch Rise/Fall Times		50ns
Switch Voltage Loss	1A 5A	1.6V 2V
Reference Voltage		$2.35V \pm 1.5\%$
Line/Load Regulation		0.05%
Efficiency	$V_{OUT} = 15V$ $V_{OUT} = 5V$	90% 80%

Figure A2. LT1074 Electrical Characteristics

APPENDIX B

GENERAL CONSIDERATIONS FOR SWITCHING REGULATOR DESIGN

Inductor Selection

Magnetic considerations are easily the most common problem area in switching regulator design. Ninety percent of the difficulties encountered are traceable to the inductive components in the circuit. The overwhelming level of difficulty associated with magnetics mandates a judicious selection process. The most common difficulty is saturation. An inductor is saturated when it cannot hold any more magnetic flux. As an inductor arrives at saturation it begins to look more resistive and less inductive. Under these conditions current flow is limited only by the inductor's DC copper resistance and the source capacity. This is why saturation often results in destructive failures.

While saturation is a prime concern, cost, heating, size, availability and desired performance are also significant. Electromagnetic theory, although applicable to these issues, can be confusing, particularly to the non-specialist.

Practically speaking, an empirical approach is often a good way to address inductor selection. It permits real-time analysis under actual circuit operating conditions using the ultimate simulator — a breadboard. If desired, inductor design theory can be used to augment or confirm experimental results.

Figure B1 shows a typical step down converter utilizing the LT1074 switching regulator. A simple approach may be employed to determine the appropriate inductor. A very useful tool is the #845 inductor kit¹² shown in Figure B2. This kit provides a broad range of inductors for evaluation in test circuits such as Figure B1.

Note 12: Available from Pulse Engineering, Inc., P.O. Box 12235, San Diego, California 92112, 619-268-2400.

Figure B3 was taken with a $450\mu\text{H}$ value, high core capacity inductor installed. Circuit operating conditions such as input voltage and loading are set at levels appropriate to the intended application. Trace A is the LT1074's V_{SW} pin voltage while trace B shows its current. When V_{SW} pin voltage is high, inductor current flows. The high inductance means current rises relatively slowly, resulting in the shallow slope observed. Behavior is linear, indicating no saturation problems. In Figure B4, a lower value unit with equivalent core characteristics is tried. Current rise is steeper, but saturation is not encountered. Figure B5's selected inductance is still lower, although core characteristics are similar. Here, the current ramp is quite pronounced, but well controlled. Figure B6 brings some informative surprises. This high value unit, wound on a low capacity core, starts out well but heads rapidly into saturation, and is clearly unsuitable.

The described procedure narrows the inductor choice within a range of devices. Several were seen to produce

acceptable electrical results, and the "best" unit can be further selected on the basis of cost, size, heating and other parameters. A standard device in the kit may suffice, or a derived version can be supplied by the manufacturer.

Using the standard products in the kit minimizes specification uncertainties, accelerating the dialogue between user and inductor vendor.

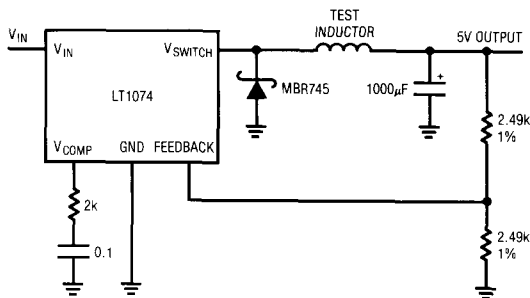


Figure B1. Basic LT1074 Test Circuit

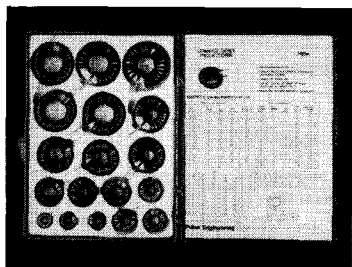


Figure B2. Model 845 Inductor Selection Kit from Pulse Engineering, Inc. Includes 18 Fully Specified Devices

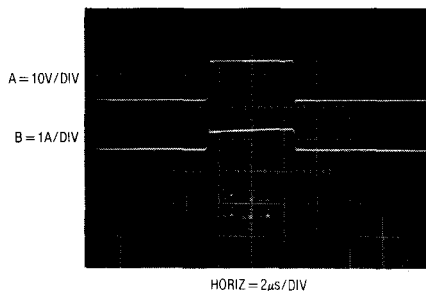


Figure B3. Waveforms for $450\mu\text{H}$, High Capacity Core Unit

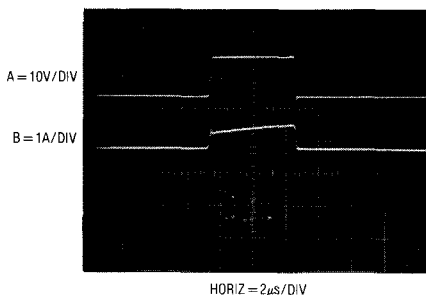


Figure B4. Waveforms for $170\mu\text{H}$, High Capacity Core Unit

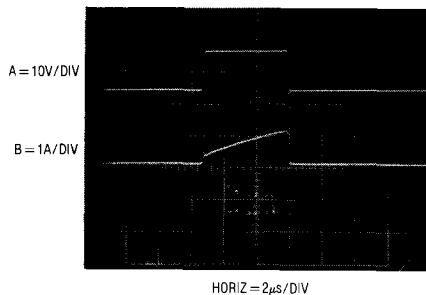


Figure B5. Waveforms for $55\mu\text{H}$, High Capacity Core Unit

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Inductor Selection - Alternate Method

There are alternate inductor selection methods to the one described. One of the most popular is utilized by those devoid of the recommended inductor kit, time or adequate instrumentation. What is usually desired is to get a prototype LT1074 circuit running *NOW*. What is often available is limited to a drawer of inductors (see Figure B7) of unknown or questionable lineage. Selection of an appropriate inductor is (hopefully) made by simply inserting one of these drawer dwellers into an unsuspecting LT1074 circuit. Although this methods theoretical premise is perhaps questionable, its seemingly limitless popularity compels us to address it. We have developed a two step procedure for screening inductors of unknown characteristics. Inductors passing both stages of the test have an excellent chance (75% - based on our sample of randomly selected

inductors) of performing adequately in a prototype LT1074 circuit. The only instrumentation required is an ohmmeter and a scale.

Test 1 consists of weighing the candidate inductor. Acceptable limits range between 0.01 and 0.25 pounds. This test is best performed at an Inductor Test Facility (see Figure B8), where precision scales are readily available. To save time the quick checkout line is recommended (but only if you have nine¹³ inductors or less — no cheating).

Figure B9 shows an inductor under test. The 0.13 pound weight indicated by the scale places this unit well within acceptable limits.

Note 13: The maximum permitted number of items in the quick checkout line varies from facility to facility. Please be familiar with and respect local regulations.

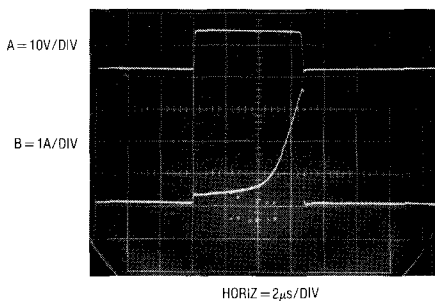


Figure B6. Waveforms for 500 μ H, Low Capacity Core Inductor (Note Saturation Effects)

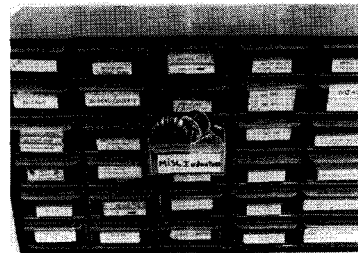


Figure B7. "Yeah, We Got Some Inductors in a Drawer. I'm Sure They'll Work ..."



Figure B8. Typical Inductor Test Facility

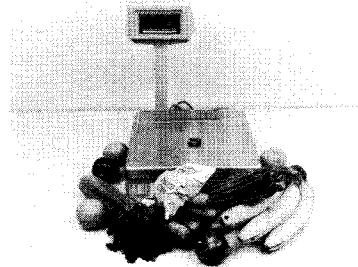


Figure B9. Inductor Under Test (Don't Forget to Pick-Up a Loaf of Bread and a Dozen Eggs)

The second test involves measuring the inductors DC resistance. Acceptable limits are usually between 0.01Ω and 0.25Ω . Inductors passing both tests will probably function in a prototype LT1074 circuit. Figures B10 and B11 show typical acceptable and unacceptable inductors. Graduates tend to be relatively dense, with (where visible) thick wire. Flunkers are usually less dense, with small (again, where visible) wire sizes.

When using an inductor selected with this method try low power first, then gradually increase loading. Observe inductor and LT1074 heating, making sure their dissipation is reasonable (warm to the touch). Disproportionate increases in heating as load is increased probably indicate inductor saturation. Either reduce the load, or go back to the drawer and try again.

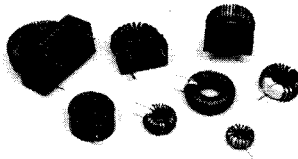


Figure B10. Typical Acceptable Inductors

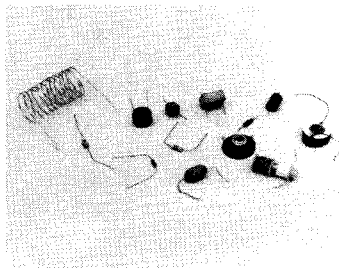


Figure B11. Typical Unacceptable Inductors

While these two tests are somewhat lacking in rigor they do increase the chances of quickly getting a circuit to run with available components. In the longer term, the appropriate inductor can be decided upon and specified.

For the theoretically minded, test 1 grades out inductors which are unlikely to have enough flux storage capability (core mass) to avoid saturation. Test 2 eliminates units with too high a resistance to efficiently support typical LT1074 operating currents. Expanded discussion and design considerations for inductors will be found in Reference 4.

Capacitors

Think about requirements in capacitors. All operating conditions should be accounted for. Voltage rating is the most obvious consideration, but remember to plan for the effects of equivalent series resistance (ESR) and inductance. These specifications can have significant impact on circuit performance. In particular, an output capacitor with high ESR can make loop compensation difficult or decrease efficiency.

Layout

Layout is vital. Don't mix signal, frequency compensation, and feedback returns with high current returns. Arrange the grounding scheme for the best compromise between AC and DC performance. In many cases, a ground plane may help. Account for possible effects of stray inductor-generated flux on other components and plan layout accordingly.

Diodes

Diode breakdown and switching ratings must be thought through. Account for all conditions. Transient events usually cause the most trouble, introducing stresses that are often hard to predict. Study the datasheet breakdown, current capacity, and switching speed ratings carefully. Were these specifications written under the same conditions that your circuit is using the device in? If in doubt, consult the manufacturer.

Switching diodes have two important transient characteristics — reverse recovery time and forward turn-on time.

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Reverse recovery time occurs because the diode stores charge during its forward conducting cycle. This stored charge causes the diode to act as a low impedance conductive element for a short period of time after reverse drive is applied. Reverse recovery time is measured by forward biasing the diode with a specified current, then forcing a second specified current backwards through the diode. The time required for the diode to change from a reverse conducting state to its normal reverse non-conducting state is reverse recovery time. Hard turn-off diodes switch abruptly from one state to the other following reverse recovery time. They therefore dissipate very little power even with moderate reverse recovery times. Soft turn-off diodes have a gradual turn-off characteristic that can cause considerable diode dissipation during the turn-off interval.

Fast diodes can be useless if stray inductance is high in the diode, output capacitor or LT1074 loop. 20-gauge hook-up wire has 30nH/inch inductance. Switching currents on the order of 10^8 A/sec are typical in regulator circuits. They can easily generate volts per inch in wiring.

Keep the diode, capacitor and LT1074 input/switch lead lengths *SHORT!*

Frequency Compensation

The basic LT1074 step down configuration is relatively free of frequency compensation difficulties. The simple RC damper networks shown from the V_C pin to ground will usually suffice. Things become more complex when gain and phase contributing elements are added to the basic loop. In these cases it is often useful to look at the LT1074 as a low bandwidth power stage. The delays are due to the sampled data nature of power delivery (100kHz switching frequency) and the output LC filter. In general, complex loops can be stabilized by limiting the gain-bandwidth of the LT1074 below that of the added elements. This is in accordance with well known feedback theory. A discussion of practical techniques for stabilizing such loops, "The Oscillation Problem (Frequency Compensation Without Tears)," appears at the end of LTC Application Note 18. Other pertinent comments appear in the "Frequency Compensation" sections of LTC Application Notes 19 and 25.

APPENDIX C

Techniques and Equipment for Current Measurement

Accurate measurement of current flow under rapidly changing circuit conditions is essential to switching regulator design. In many cases current waveforms contain more valuable information than voltage measurements. The most powerful and convenient current measuring tool is the clip-on current probe. Several types appear in Figure C1. The Tektronix P-6042, shown bottom left, is a Hall effect stabilized current transformer which responds from DC to 50MHz. The more recent Tektronix AM-503 (not shown) has similar specifications. The combination of convenience, broad bandwidth and DC response make Hall effect stabilized current probes the instrument of choice for converter design. The DC response allows determination of DC content in high speed current waveforms. The clip-on probe contains a current transformer and a Hall effect device. The Hall device senses at DC and low frequency while the transformer simultaneously processes high frequency content. Careful roll-off

matching allows a composite output with no peaking or response aberrations at the two sensors bandwidth crossover. Sensitivity ranges from fractions of a milliampere to amperes and is switch selectable.

Transformer based clip-on current probes are also available. These types lack the DC response of their Hall effect augmented cousins, but are still quite useful. The Tektronix type 131 (and the more modern 134) responds from hundreds of hertz to about 40MHz. AC current probes (type 131 appears in C1, upper left) are as convenient to use as Hall types, but cannot respond at low frequency. AC current probes are also available with a simple termination (left foreground, Figure C1). These types are more difficult to use than the actively terminated models (e.g. type 131 shown) because of complex gain switching. Their low frequency limitations are also poorer, although their high frequency response exceeds 100MHz.

A final form of AC current probe is the simple transformer shown in Figure C1's foreground. These are not clip-on devices, and usually have significant performance limitations compared to the instruments discussed. However, they are inexpensive and can provide meaningful measurement results when used according to manufacturers recommendations. In use, the conductor is threaded through the opening provided and the signal monitored at the output pins.

Figure C1 also shows a wide-ranging DC clip-on current probe. The Hewlett-Packard 428B (upper right) responds from DC to only 400Hz, but features 3% accuracy over a 100 μ A to 10A range. This instrument obviously cannot discern high speed events, but is invaluable for determining overall efficiency and quiescent current.

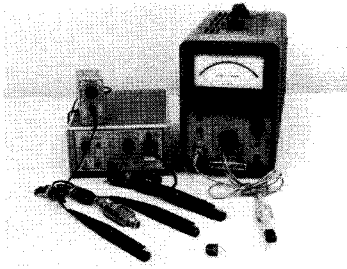


Figure C1. Various Current Probe Types Provide Different Capabilities. Selection Criteria is Application Dependent.

A great strength of the probes described is that they take a fully floating measurement. The extraction of current information by magnetic connection eliminates common mode voltage considerations. Additionally, the clip-on convenience makes the probes as easy to use as a standard voltage mode probe. As good as they are, current probes have limitations and characteristics which must be remembered to avoid unpleasant surprises. At high currents, probe saturation limits may be encountered. Resultant CRT waveforms will be corrupted, rendering the measurement useless and confusing the unwary. For Hall types, measurement below a few hundred microamperes is limited by noise, which is much more obvious on the display. Keep in mind that current probes have different signal transit delay times than voltage probes or dissimilar current probes. At high sweep speeds this effect shows

up in multi-trace displays as time skewing between individual channels. The current probes transit time delay can be mentally factored in to reduce error when interpreting the display. Note that active probes have the longest signal transit times, on the order of 25ns.

The AC probes low frequency bandwidth restriction must be kept in mind when interpreting CRT displays. Figure C2 clearly demonstrates this by showing the AC probes inability to follow low frequency. Similarly, remember that the probes stated bandpass is a -3dB figure, meaning signal information is not entirely present in the display at this frequency. When working in regions approaching either end of the probe bandpass consider that displayed information may be distorted or incomplete.

There are other ways, albeit less convenient and desirable than clip-on current probes, to measure wideband current signals. Ohm explains that measuring voltage across a resistor gives current. Current shunts (Figure C3 foreground)

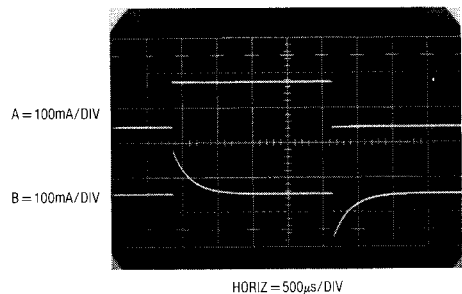


Figure C2. Hall Stabilized (Trace A) and Transformer (Trace B) Based Current Probes Responding to Low Frequency

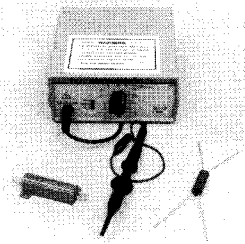


Figure C3. Typical Current Shunts and an "Isolated" Probe

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are low value (for LT1074 circuits 0.1Ω to 0.01Ω is typical) resistors with four terminal connections for accurate measurement. In theory, measuring voltage across a current shunt should yield accurate information. In practice, common mode voltages introduce measurement difficulties, particularly at speed. Making this measurement requires an isolated probe or a high speed differential plug-in. The Signal Acquisition Technologies SL-10 (Figure C3) has 10MHz bandwidth, a galvanically floating input and 600V common mode capability. This probe allows any oscilloscope to take a floating measurement across a shunt.

Differential oscilloscope plug-in's, while not galvanically floating, can measure across a shunt. Tektronix types W, 1A5 and 7A13 have 1mV sensitivity with up to 100MHz bandwidth and excellent common mode rejection. Types 1A7 and 7A22 have 10μV sensitivity, although bandwidth is limited to 1MHz. All differential plug-in's have bandwidth and/or common mode voltage restrictions that vary with sensitivity. These trade-offs must be reviewed when selecting the optimal shunt value for a particular measurement. In general the smallest practical shunt value is desirable. This minimizes the inserted resistances parasitic effects on circuit operation.

APPENDIX D

Optimizing Switching Regulators for Efficiency

Squeezing the utmost efficiency out of a switching regulator is a complex, demanding design task. Efficiency exceeding 80%-85% requires some combination of finesse, witchcraft and just plain luck. Interaction of electrical and magnetic terms produces subtle effects which influence efficiency. A detailed, generalized method for obtaining maximum converter efficiency is not readily described but some guidelines are possible.

Losses fall into several loose categories including junction, ohmic, drive, switching, and magnetic losses.

Semiconductor junctions produce losses. Diode drops increase with operating current and can be quite costly in low voltage output converters. A 700mV drop in a 5V output converter introduces more than 10% loss. Schottky devices will cut this nearly in half, but loss is still appreciable. Germanium (rarely used) is lower still, but switching losses negate the low DC drop at high speeds. In very low power converters Germanium's reverse leakage may be equally oppressive. Synchronously switched rectification is more complex, but can sometimes simulate a more efficient diode (see LTC Application Note 29, Figure 32). The LT1074's "Com Out" pin is intended to drive external synchronous switches. See Appendix A for details.

When evaluating synchronous rectification schemes remember to include both AC and DC drive losses in efficiency estimates. DC losses include base or gate current

in addition to DC consumption in any driver stage. AC losses might include the effects of gate (or base) capacitance, transition region dissipation (the switch spends some time in its linear region) and power lost due to timing skew between drive and actual switch action.

The LT1074's output switch is composed of a PNP driving a power NPN (Figure D1). The switch drop can reach 2V at high currents. This will usually be the major loss in the circuit. Its effect on efficiency can be mitigated by using the highest possible input voltage. Text Figure 7 shows 5V regulator efficiency improving almost 10% for higher input voltages. Higher output voltages will further minimize the switch losses.

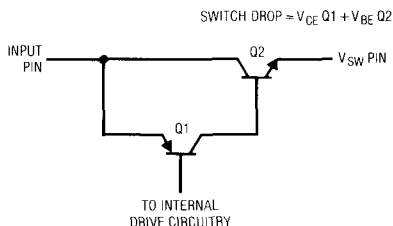


Figure D1. Simplified LT1074 Output Switch

Actual losses caused by switch saturation effects and diode drops are sometimes difficult to ascertain. Changing duty cycles and time variant currents make determination tricky. One simple way to make relative loss

judgements is to measure device temperature rise. Appropriate tools here include thermal probes and (at low voltages) the perhaps more readily available human finger. At lower power (e.g. less dissipation, even though loss percentage may be as great) this technique is less effective. Sometimes deliberately adding a known loss to the component in question and noting efficiency change allows loss determination.

Ohmic losses in conductors are usually only significant at higher currents. "Hidden" ohmic losses include socket and connector contact resistance and equivalent series resistance (ESR) in capacitors. ESR generally drops with capacitor value and rises with operating frequency, and should be specified on the capacitor datasheet. Consider the copper resistance of inductive components. It is often necessary to evaluate trade-offs of an inductor's copper resistance vs. magnetic characteristics.

Switching losses occur when the LT1074 spends significant amounts of time in its linear region relative to operating frequency. At higher switching frequencies transition times can become a substantial loss source. The LT1074's 100kHz pre-set switching frequency is a good compromise (for this device) and changes should be carefully considered. Raising the switching frequency to gain some desired benefit necessitates consideration of increased LT1074 losses. 200kHz is the maximum practical operating frequency.

Magnetics design also influences efficiency. Design of inductive components is well beyond the scope of this appended section, but issues include core material selection, wire type, winding techniques, size, operating frequency, current levels, temperature and other issues. Some of these topics are discussed in LTC Application Note 19, but there is no substitute for access to a skilled magnetics specialist. Fortunately, the other categories mentioned usually dominate losses, allowing good efficiencies to be obtained with standard magnetics. Custom magnetics are usually only employed after circuit losses have been reduced to lowest practical levels.

A Special Circuit

In cases where input voltage must be low, but may float, Figure D2's circuit may be preferable to an LT1074 based approach. This circuit uses the LT1070, a common emitter output device. With the emitter connected to the ground pin this device (LT1070 operating details are available in its datasheet, and in LTC Application Notes 19, 25 and 29) switch loss is significantly lower than the LT1074's. Although intended for voltage step-up in flyback configurations the LT1070 can be arranged to perform the step-down function. The advantage is the efficiency gain due to the reduced switch loss. The circuit's primary restriction is that the input must float with respect to the output. Q1 performs a level shift to get the feedback information

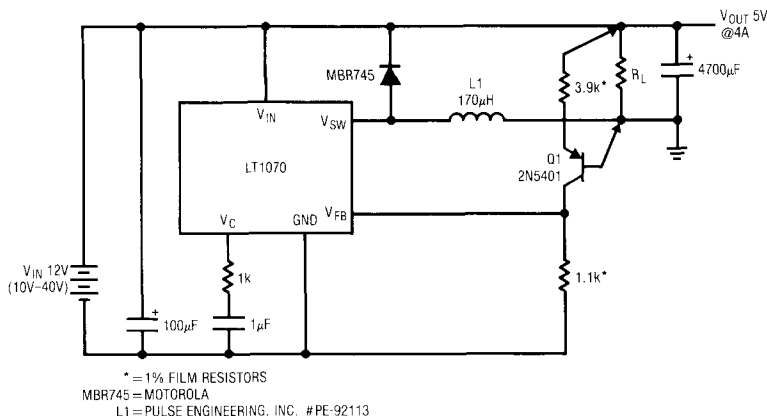


Figure D2. Floating Input Buck Regulator

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referenced to the LT1070 "ground" pin, which floats with the input. The LT1070 is effectively "fooled" and behaves like a flyback regulator. It is oblivious to the fact that the overall function is step-down, because the floating input is driven to the output potential. The negative side of the out-

put filter capacitor is connected to the ground (\oplus) of the powered system, and the LT1070 input rail becomes the 5V output. Other voltages are obtainable by altering the 3.9k-1.1k feedback ratio. Efficiency approaches 85%.

APPENDIX E

A Half-Sine Reference Generator

Text Figure 31's half-sine reference must be amplitude and frequency stabilized to a fairly high degree. It is not unreasonable to expect a 115V_{AC} 400Hz source to be within 1V and 0.1Hz. Additionally, Figure 31's reference requires a half-sine, as opposed to the more normal full-sine. These requirements are achievable by classical analog techniques, but a digital approach eases complexity with no performance trade-off¹⁴. Figure E3 shows such an approach. C1 forms a 1.024MHz crystal oscillator which is divided down by the 7490. The 7490's differentiated ÷10 output becomes the LT1074's 102.4kHz sync. option output. The 7490's ÷5 output (204.8kHz) is fed to the 74191 counters. These counters parallel load a 2716 EPROM which is programmed to produce an 8-bit (256 states) digitally coded half-sine. The program, developed by Sean Gold and Guy M. Hoover, appears in Figure E1. The 2716's

parallel output is fed to an 8-bit DAC, which produces 800Hz 2.5V (peak) half-sines.

Those wishing to utilize this reference for full-sines will find the appropriate software in Figure E2.

Figure E3 also shows the synchronous switch option discussed in the text. The 74C122 monostable forms a simple delayed pulse generator which drives the Q4 switch. The 20 μ s delay and 6 μ s pulse width set at the 74C122 were empirically determined to produce lowest overall crossover distortion in Figure 31's output.

Note 14: The sinewave is probably the paramount expression of the analog world. The Old Man Himself, George A. Philbrick, once elegantly discussed analog functions as "those which are continuous in excursion and time." He might have viewed digital production of a sinewave with considerable suspicion, or simply labeled it blasphemous. Such are the wages of progress.

Line	10801	Column	Wrap	APL2/PC
	GENCODES			
00	03	06	09	0D 10 13 16 19 1C 1F 22 26 29 2C 2F
32	35	38	3B	3E 41 44 47 4A 4D 50 53 56 59 5C 5F
62	65	68	6B	6D 70 73 76 79 7B 7E 81 84 86 89 8C
8E	91	93	96	98 9B 9D A0 A2 A5 A7 A9 AC AE B0 B3
B5	B7	B9	BB	BE C0 C2 C4 C6 C8 CA CB CD CF D1 D3
D5	D6	D8	DA	DB DD DE E0 E1 E3 E4 E6 E7 E8 EA EB
EC	ED	EE	EF	F1 F2 F3 F3 F4 F5 F6 F7 F8 F9 FA
FA	FB	FC	FD	FE FE FE FE FE FE FE FE FE FE FE FE
FF	FF	FF	FF	FF FE FE FE FE FD FC FC FC FB FB FA
FA	F9	F8	F7	F6 F5 F4 F3 F2 F1 EF EE ED EC
EB	EA	E9	E7	E6 E4 E3 E1 E0 DE DD DA DB DC DS
D3	D1	CF	CD	CB CA C8 C5 C4 C2 C0 BE BB BA B7 B5
B3	B0	AE	AC	A9 A7 A5 A2 A0 9D 9B 98 96 93 91 8E
8C	89	86	84	81 7E 7B 79 76 73 70 6B 68 65 62
5F	5C	59	56	53 50 4D 4A 47 44 41 3E 3B 38 35 32
2F	2C	29	26	22 1F 1C 19 16 13 10 0D 09 06 03 00

Figure E1. Half-Sine Software Code for the 2716 EPROM

Line	10736	Column	Wrap	APL2/PC
	GENCODES			
FF	FF	FF	FF	FE FE FE FD FC FC FB FA F9 F8 F7 F6
F5	F4	F3	F1	F0 EE ED EB E9 E8 E6 E4 E2 E0 DE DC
D9	D7	D5	D2	D0 CE C8 C9 C6 C3 C1 BE BB BA B6 B3
B0	AD	AA	A7	A4 A1 9E 9B 98 95 92 8E 8B 88 85 82
7F	7C	78	75	72 6F 6C 69 66 63 60 5D 5A 57 54 51
4E	48	48	45	42 40 3D 3A 38 35 33 30 2E 2B 29 27
25	22	20	1E	1C 1A 18 17 15 13 11 10 0E 0D 0C 0A
09	08	07	06	05 04 03 03 02 02 01 01 00 00 00 00
00	00	00	00	01 01 02 02 03 03 04 05 06 07 08 09
0A	0C	0C	0E	10 11 13 15 17 1B 1A 1C 1E 20 22 25
27	29	28	2E	30 33 35 38 3A 3D 40 42 45 48 4B 4E
S1	S4	S7	S4	S0 60 63 66 69 6C 6F 72 75 78 7C 7F
82	85	88	8B	8E 92 95 98 9B 9E A1 A4 A7 AA AD B0
B3	B6	B8	8B	BE C1 C3 C6 C9 CB CE D0 D2 D5 D7 D9
DC	DE	E0	E2	E4 E6 E8 E9 EB ED EE F0 F1 F3 F4 F5
F6	F7	F9	F9	FA FB FC FD FE FE FE FE FF FF FF FF

Figure E2. Full-Sine Software Code for the 2716 EPROM (Bonus)

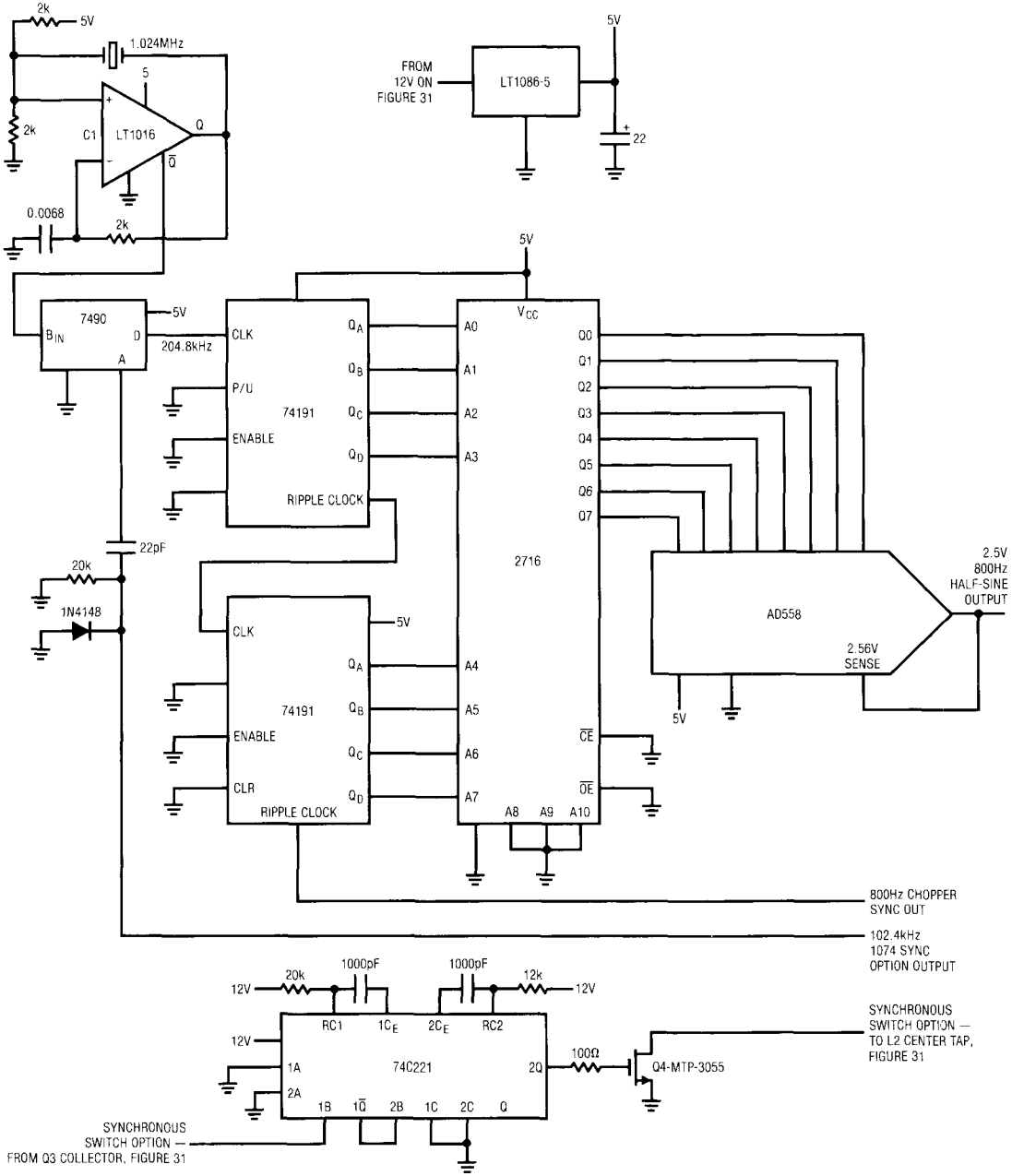


Figure E3. Timing and Reference Half-Sine Generator for Figure 31

Application Note 35

APPENDIX F

The Magnetics Issue

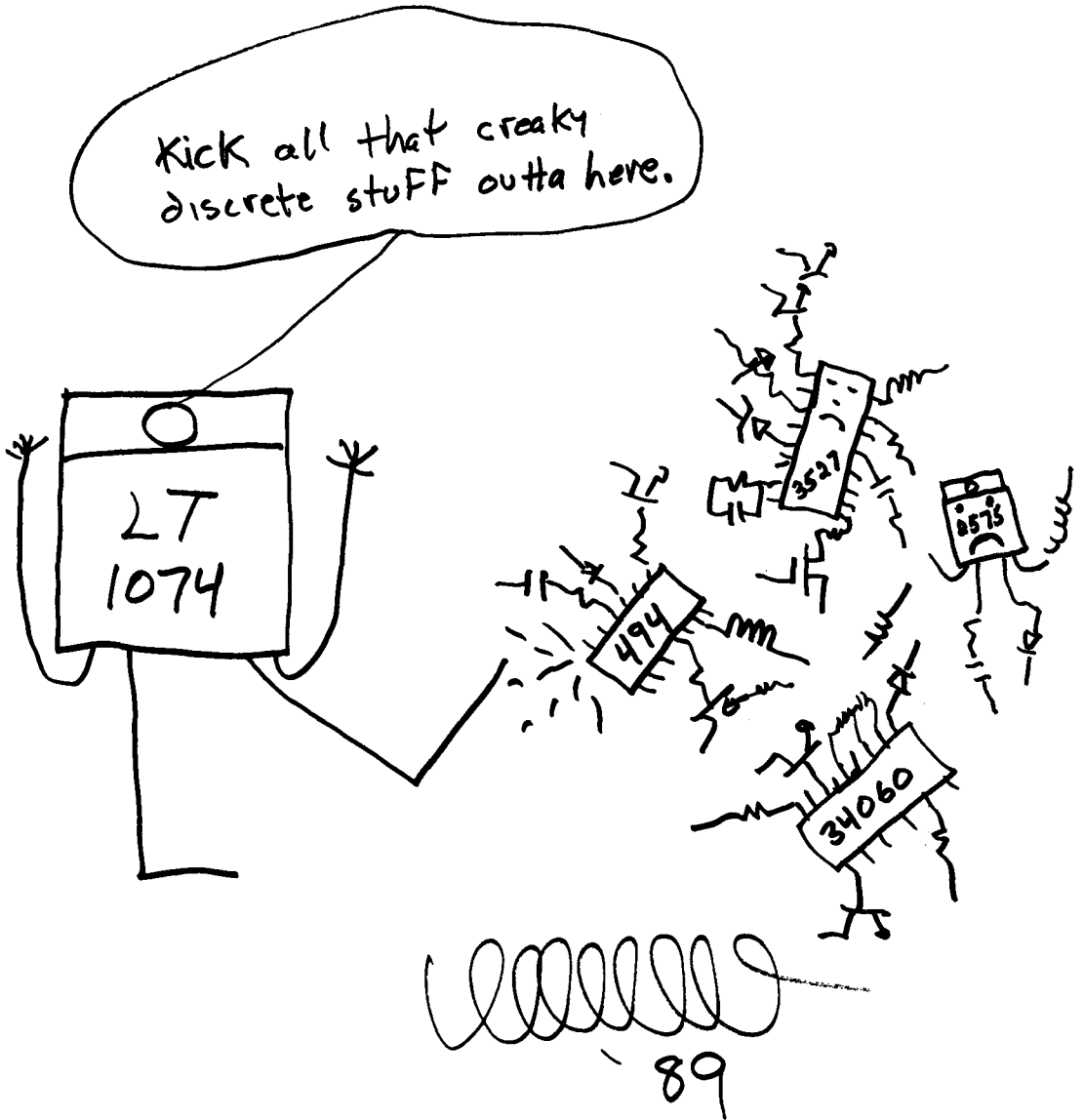
Magnetics is probably the most formidable issue in converter design. Design and construction of suitable magnetics is a difficult task, particularly for the non-specialist. It is our experience that the majority of converter design problems are associated with magnetics requirements. This consideration is accentuated by the fact that most converters are employed by non-specialists. As a purveyor of switching power IC's we incur responsibility towards addressing the magnetics issue (our publicly spirited attitude is, admittedly, capitalistically polluted). As such, it is LTC's policy to use off-the-shelf magnetics in our circuits. In some cases, available magnetics serve a particular design. In other situations the magnetics have been specially designed, assigned a part number and made available as standard product.

In many circumstances a standard product is suitable for production. Other cases may require modifications or changes which the manufacturer can provide or advise on. Hopefully, this approach serves the needs of all concerned.

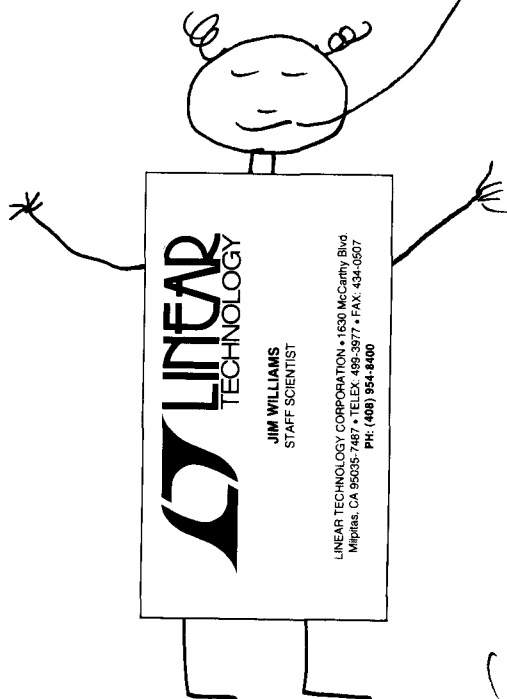
Recommended magnetics manufacturers include the following;

Pulse Engineering, Inc.
P.O. Box 12235
7250 Convoy Court
San Diego, California 92112
619-268-2400

Coiltronics
984 Southwest 13th Court
Pompano Beach, FL 33069
305-781-8900



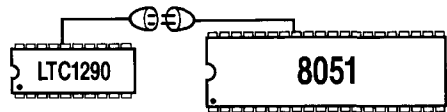
Call me & lets discuss your switching regulator requirements.



Jim Williams '89

Interfacing the LTC1290 to the 8051 MCU

Sammy Lum
Tim Rust



Introduction

This application note describes the hardware and software required for communication between the LTC1290 12-bit data acquisition system and the MCS-51 family of microcontrollers (e.g., 8051). The four wire interface is capable of completing a 12-bit conversion and transferring the data to the 8051 in 116 μ s. Configuration of the 8051 and the LTC1290 will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be discussed. Finally, a summary of results including data throughput rates will be provided.

Interface Details

The serial port of the 8051 does not support the synchronous, full duplex format used by the LTC1290. Therefore it is necessary for the user to construct a serial port

using four lines from one of the parallel ports available on the 8051. The lines are set or cleared using the bit manipulation features of the 8051. This provides a very flexible serial port but the data shift rate is three to four times slower than that available from microcontrollers with dedicated serial ports.

The LTC1290 has two clock lines: ACLK and SCLK. ACLK controls the A/D conversion rate while SCLK controls the data shift rate. These lines may be tied together or run separately. The 8051 provides a pin (ALE) which can be used to drive the ACLK of the LTC1290 (option 1). Alternatively, tying the clocks together saves one line that has to go between the LTC1290 and the 8051 (option 2). However, this implementation slows the data throughput rate due to additional code. The schematic of Figure 1 shows both of these options.

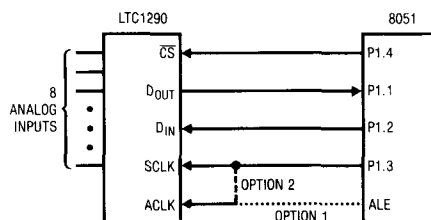


Figure 1. Schematic

Application Note 36A

Hardware Description

The code for this interface was developed on an 8051 evaluation board.

Due to the weak pullups of the 8051, excess loading should be avoided when examining the output of the microcontroller.

The timing diagram of Figure 2 was obtained with an HP1631A logic analyzer using separate ACLK and SCLK (option 1). The 8051 clock rate was 12MHz, producing a 2.0MHz clock on the ALE pin.

The analog section of the schematic in Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1290 please see the data sheet.

Software Description

The software simulates a serial port through bit manipulation instructions of the 8051. Additionally, the software generates a delay during which time the A/D conversion takes place.

The code sets up bit one of port one as an input by setting it high. (Due to the weak pullup of the 8051, the DOUT pin of the LTC1290 can then drive the pin high or low.)

SCLK is initialized to a low state and \overline{CS} is initialized to a high state. A D_{IN} word of \$0E is then loaded into the ac-

cumulator. An examination of Figure 3 and the data sheet will show that this configures the LTC1290 for CH0 with respect to CH1, unipolar, MSB first and a 12-bit word length. Next \overline{CS} goes low. If the user is tying ACLK and SCLK together (option 2) it is then necessary to generate two clock pulses to meet the deglitcher requirements. With separate clocks (option 1) the NOP is necessary to allow sufficient time for the deglitcher before starting to shift the data. Data is moved from the P1.1 pin (D_{OUT} of the LTC1290) to the carry register and shifted one bit at a time into the accumulator. At the same time, the 8-bit D_{IN} word is shifted from the accumulator into the carry register and output on P1.2 (D_{IN} of the LTC1290).

After the eight MSBs have been shifted, the contents of the accumulator are stored in R2. The final four bits are then shifted into the accumulator, placed in the most significant bits and stored in R3. The data is left justified at this point with the MSBs in R2 and the LSBs in R3. \overline{CS} is then raised and time (52 ACLK cycles) for the LTC1290 to do its next conversion must be allowed before the next read can be performed. If separate clocks are being used (option 1), quite often the microcontroller will have other tasks to accomplish and this time can be used productively. Otherwise, a routine such as the one labeled DELAY can be used. With the clocks tied together (option 2), it is necessary for the 8051 to manually clock the LTC1290 52 times and this free time is then lost as shown in Figure 7. An example of this routine is labeled LOOP 1.

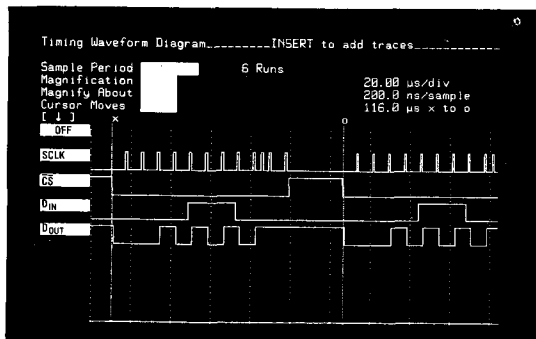


Figure 2. Timing Diagram for Option 1

If right justified data is required, the MSBF bit of the D_{IN} word could be cleared and the bits reversed (in this case producing a D_{IN} word of \$0A). Also it would be necessary to swap the rotate left and rotate right instructions.

0	0	0	0	1	1	1	0
S/D	O/S	S1	S2	UNI	MSBF	WL1	WL0

Figure 3. D_{IN} Word for LTC1290

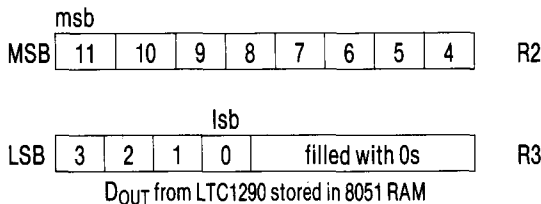


Figure 4. Memory Map

Power Shutdown

Figure 8 shows what occurs during a power shutdown and subsequent power up of the LTC1290. In ① a dummy conversion is performed prior to power shutdown in order to obtain the data from the previous conversion. In this example we are requesting a 12-bit word length MSB first. In ② power shutdown is requested by inputting the appropriate D_{IN} word (\$0D). The bottom trace is the LTC1290 supply current which shows the current going from a nominal value of 5mA to 5 μ A. In ③ power up occurs and the device is ready for conversion. The D_{OUT} word is not valid until the next cycle, ④. The analog input to the LTC1290 was a constant DC voltage. As one would expect the D_{OUT} word in ④ is the same as in ①.

Summary

A four wire interface between the LTC1290 and the 8051 with a combined data conversion and transfer time of 116 μ s was demonstrated. It was shown that the ACLK of the LTC1290 can be run separately from the SCLK by tying the ACLK to the ALE of the 8051. Alternatively, the two clock pins can be tied together (saving one line at the expense of speed). The data can be either left justified or right justified in the microcontroller's memory through the

proper choice of software and LTC1290 data format. The code shown applies to all MCS-51 family members. The same technique can be used on any parallel port processor.

Reference

Hoover, Guy and Rempfer, William, "Interfacing the LTC1090 to the 8051 MCU," Application Note 26A, Linear Technology Corp.

LABEL	MNEMONIC	COMMENTS
	MOV P1, #02H	BIT 1 PORT 1 SET AS INPUT
	CLR P1.3	SCLK GOES LOW
	SETB P1.4	CS GOES HIGH
CONT	MOV A, #0EH	D_{IN} WORD FOR LTC1290
	CLR P1.4	CS GOES LOW
	MOV R4, #08H	LOAD COUNTER
	NOP	DELAY FOR DEGLITCHER
LOOP	MOV C, P1.1	READ DATA BIT INTO CARRY
	RLC A	ROTATE DATA BIT INTO ACC
	MOV P1.2, C	OUTPUT D_{IN} BIT TO LTC1290
	SETB P1.3	SCLK GOES HIGH
	CLR P1.3	SCLK GOES LOW
	DJNZ R4, LOOP	NEXT BIT
	MOV R2, A	STORE MSBs IN R2
	MOV C, P1.1	READ DATA BIT INTO CARRY
	CLR A	CLEAR ACC
	RLC A	ROTATE DATA BIT INTO ACC
	SETB P1.3	SCLK GOES HIGH
	CLR P1.3	SCLK GOES LOW
	MOV C, P1.1	READ DATA BIT INTO CARRY
	RLC A	ROTATE DATA BIT INTO ACC
	SETB P1.3	SCLK GOES HIGH
	CLR P1.3	SCLK GOES LOW
	MOV C, P1.1	READ DATA BIT INTO CARRY
	RLC A	ROTATE DATA BIT INTO ACC
	SETB P1.3	SCLK GOES HIGH
	CLR P1.3	SCLK GOES LOW
	MOV C, P1.1	READ DATA BIT INTO CARRY
	RRC A	ROTATE RIGHT INTO ACC
	RRC A	ROTATE RIGHT INTO ACC
	RRC A	ROTATE RIGHT INTO ACC
	RRC A	ROTATE RIGHT INTO ACC
	MOV R3, A	STORE LSBs IN R3
	SETB P1.3	SCLK GOES HIGH
	CLR P1.3	SCLK GOES LOW
	SETB P1.4	CS GOES HIGH
DELAY	MOV R5, #0BH	LOAD COUNTER
	DJNZ R5, DELAY	GO TO DELAY IF NOT DONE

Figure 5. 8051 Code for Option 1 (ACLK Tied to ALE)

Application Note 36A

LABEL	MNEMONIC	COMMENTS
	MOV P1, #02H	BIT 1 PORT 1 SET AS INPUT
	CLR P1.3	SCLK GOES LOW
	SETB P1.4	\overline{CS} GOES HIGH
CONT	MOV A, #0EH	D_{IN} WORD FOR LTC1290
	CLR P1.4	\overline{CS} GOES LOW
	SETB P1.3	SCLK GOES HIGH
	CLR P1.3	SCLK GOES LOW
	SETB P1.3	SCLK GOES HIGH
	CLR P1.3	SCLK GOES LOW
	MOV R4, #08H	LOAD COUNTER
LOOP	MOV C, P1.1	READ DATA BIT INTO CARRY
	RLC A	ROTATE DATA BIT INTO ACC
	MOV P1.2, C	OUTPUT D_{IN} BIT TO LTC1290
	SETB P1.3	SCLK GOES HIGH
	CLR P1.3	SCLK GOES LOW
	DJNZ R4, LOOP	NEXT BIT
	MOV R2, A	STORE MSBs IN R2
	MOV C, P1.1	READ DATA BIT INTO CARRY
	CLR A	CLEAR ACC
	RLC A	ROTATE DATA BIT INTO ACC
	SETB P1.3	SCLK GOES HIGH
	CLR P1.3	SCLK GOES LOW
	MOV C, P1.1	READ DATA BIT INTO CARRY
	RLC A	ROTATE DATA BIT INTO ACC
	SETB P1.3	SCLK GOES HIGH
	CLR P1.3	SCLK GOES LOW
	MOV C, P1.1	READ DATA BIT INTO CARRY
	RRC A	ROTATE RIGHT INTO ACC
	RRC A	ROTATE RIGHT INTO ACC
	RRC A	ROTATE RIGHT INTO ACC
	RRC A	ROTATE RIGHT INTO ACC
	MOV R3, A	STORE LSBs IN R3
	SETB P1.3	SCLK GOES HIGH
	CLR P1.3	SCLK GOES LOW
	SETB P1.4	\overline{CS} GOES HIGH
	MOV R4, #34H	LOAD COUNTER
LOOP 1	SETB P1.3	SCLK GOES HIGH
	CLR P1.3	SCLK GOES LOW
	DJNZ R4, LOOP 1	GO TO LOOP 1 IF NOT DONE

Figure 6. 8051 Code for Option 2 (ACLK Tied to SCLK)

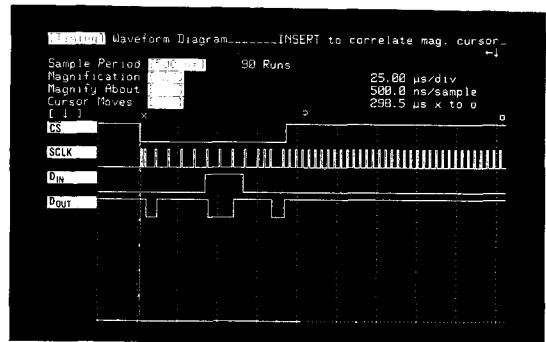


Figure 7. Timing Diagram for Option 2

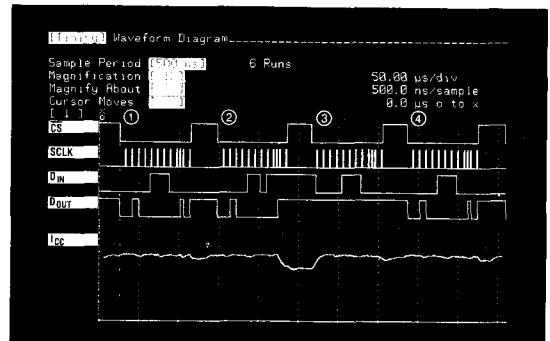


Figure 8. Power Shutdown

Interfacing the LTC1290 to the MC68HC05 MCU

Sammy Lum
 Tim Rust

Introduction

This application note describes an interface between the LTC1290 12-bit data acquisition system and the Motorola SPI family of single chip microcomputers (e.g., 68HC05). The simple four wire interface is capable of completing a 12-bit conversion and shifting the data to the 68HC05 in 40 μ s. Configuration of the LTC1290 and the 68HC05 will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be shown. Finally, a summary of the key points of this interface will be given, including data throughput rates.

Interface Details

The LTC1290 has two clock lines: ACLK and SCLK. ACLK controls the A/D conversion rate while SCLK controls the data shift rate. Data is transferred in a synchronous, full duplex format over D_{IN} and D_{OUT}.

The Motorola Serial Peripheral Interface (SPI) is a synchronous, full duplex, serial port built into the 68HC05 that allows the user to construct a simple communication path to the LTC1290. SPI provides clock, data in and data out lines that are compatible with the LTC1290. The only additional line required is one programmable output pin (CO) to control \overline{CS} on the LTC1290. The schematic of Figure 1 shows how the two devices are connected.

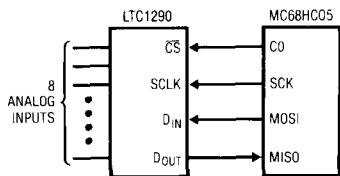
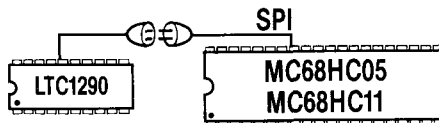


Figure 1. Schematic



Hardware Description

The 68HC05 was emulated and the code for this interface was developed on a Motorola M68HC05 EVM.

\overline{SS} (Pin 34) of the 68HC05 must be held high to enable the SPI properly for this interface.

The timing diagram of Figure 2 was obtained with an HP1631A logic analyzer using a 4MHz ACLK. The 68HC05 clock was 4MHz.

The analog section of the schematic in Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1290 please see the data sheet.

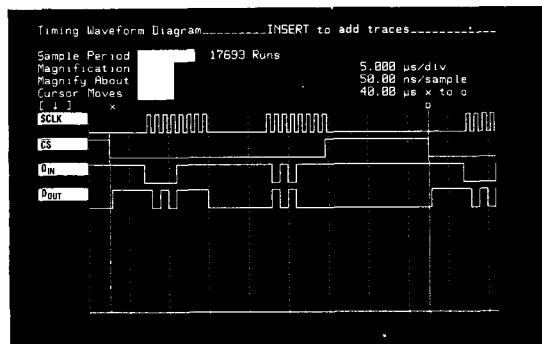


Figure 2. Timing Diagram

Software Description

The software configures and controls the SPI of the 68HC05. Additionally, the software manipulates CO (\overline{CS} of the LTC1290) and generates a delay during which time the LTC1290 performs a conversion.

The code first configures the Serial Peripheral Control Register (SPCR) of the SPI. The SPI interrupt is disabled. The SPI outputs are enabled. The SPI is configured as a master. Finally, the SPI clock is set to normally low, for

Application Note 36B

data transfer on the rising edge and for a frequency equal to half the internal processor clock (one fourth the crystal frequency).

Port C is configured as all outputs by placing ones in the data direction register of port C. A D_{IN} word that configures the LTC1290 for CH0 with respect to CH1, unipolar, MSB first and a 16-bit word length is stored in memory location \$50. Figure 3 shows how the D_{IN} word is composed.

CO is made to go low. D_{IN} for the LTC1290 is loaded into the SPI data register. Storing D_{IN} in the data register causes the transfer to begin. After waiting for the first eight bits to be transferred (8 NOPs) the status register of the SPI is examined. This clears the SPIF bit of the status register and allows the data register to be read, which is the next step. The first eight bits containing the MSBs from the LTC1290 are then stored in \$61 of the 68HC05 as shown in Figure 4. The LSBs are transferred in the same manner and stored in \$62 of the 68HC05. Notice in Figure 5 that only 6 NOPs are used in transferring the LSBs. This is because after 6 NOPs, time is consumed by the BSET command which sets the CO pin of the 68HC05. The data at this point is left justified.

0	0	0	0	1	1	1	1
S/D	O/S	S1	S2	UNI	MSBF	WL1	WLO

Figure 3. D_{IN} Word for LTC1290

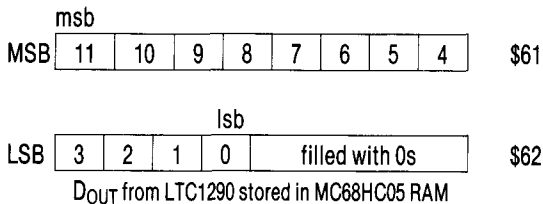


Figure 4. Memory Map

At this time 52 ACLK cycles must be allowed for the A/D to perform its next conversion. Usually the processor will have other tasks to perform during this time. If this is not the case a string of NOPs or a simple delay loop can be used to generate this delay.

The code was written for the 68HC05. By changing the addresses of the special function registers however, the code should run on all of Motorola's SPI processors including the 68HC11.

Power Shutdown

The LTC1290 can be shutdown by inputting the appropriate D_{IN} word (0D). A dummy conversion prior to a request for power shutdown is required because the data from the previous conversion will be shifted out as a 10-bit word during the power shutdown request. Upon power up the LTC1290 is ready for conversion and the D_{OUT} word will be valid on the second request for conversion.

Summary

A four wire interface between the LTC1290 and the 68HC05 with a combined data conversion and transfer time of 40 μ s was demonstrated. The interface used the serial (SPI) port of the 68HC05. The 12 data bits of the LTC1290 are shifted MSB first in two 8-bit transfers. The data is stored left justified in the 68HC05's internal RAM.

Reference

Hoover, Guy and Rempfer, William, "Interfacing the LTC1090 to the MC68HC05," Application Note 26B, Linear Technology Corp.

LABEL	MNEMONIC	COMMENTS	
LDA	#\$50	CONFIGURATION DATA FOR SPCR	
STA	\$0A	LOAD DATA INTO SPCR (\$0A)	
LDA	#\$FF	CONFIG. DATA FOR PORT C DDR	
STA	\$06	LOAD DATA INTO PORT C DDR	
LDA	#\$0F	LOAD LTC1290 D_{IN} DATA INTO ACC	
STA	\$50	LOAD LTC1290 D_{IN} DATA INTO \$50	
START	BCLR	0,\$02	CO GOES LOW (\overline{CS} GOES LOW)
LDA	\$50	LOAD D_{IN} INTO ACC FROM \$50	
STA	\$0C	LOAD D_{IN} INTO SPI. START SCK	
NOP		8 NOPs FOR TIMING	
LDA	\$0B	CHECK SPI STATUS REG	
LDA	\$0C	LOAD LTC1290 MSBs INTO ACC	
STA	\$61	STORE MSBs IN \$61	
STA	\$0C	START NEXT SPI CYCLE	
NOP		6 NOPs FOR TIMING	
BSET	0,\$02	CO GOES HIGH (\overline{CS} GOES HIGH)	
LDA	\$0B	CHECK SPI STATUS REGISTER	
LDA	\$0C	LOAD LTC1290 LSBs INTO ACC	
STA	\$62	STORE LSBs IN \$62	

Figure 5. 68HC05 Code

Interfacing the LTC1290/LTC1090 to the TMS370 MCU

Guy Hoover
 Sammy Lum
 Tim Rust

Introduction

This application note describes an interface between the LTC1290 12-bit data acquisition system and the TMS370 family of microcontrollers (e.g., TMS370C050). The simple four wire interface is capable of completing a 12-bit conversion and shifting data to the TMS370C050 in 42 μ s. Configuration of the LTC1290 and the TMS370C050 will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be shown. The LTC1090 10-bit data acquisition system is also compatible with this interface. Next the power shutdown feature of the LTC1290 will be discussed and a summary of the key points of this interface will be given, including data throughput rates.

Interface Details

The LTC1290 has two clock lines; ACLK and SCLK. ACLK controls the A/D conversion rate while SCLK controls the data shift rate. Data is transferred in a synchronous, full duplex format over D_{IN} and D_{OUT}.

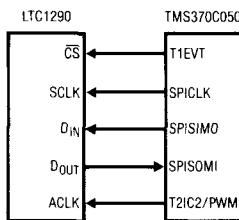
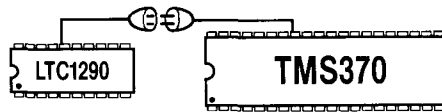


Figure 1. Schematic



The TMS370C050 has a Serial Peripheral Interface (SPI) which is a synchronous, full duplex, serial port that allows the user to construct a simple communication path to the LTC1290. SPI provides clock, data in and data out lines that are compatible with the LTC1290. The only additional line required is one programmable output pin (T1EVT) to control CS on the LTC1290. The TMS370C050 has two on board timers and one of them can be used to provide ACLK through pin T2IC2/PWM. The schematic of Figure 1 shows how the two devices are connected.

Hardware Description

The code for this interface was developed on a TMS370 application board. The TMS370C050 was used in the micro-processor mode which requires MC (pin 6) be tied high. External memory was used to store the program.

The timing diagram of Figure 2 was obtained with an HP1631A logic analyzer using a 2.5MHz ACLK. The TMS370C050 clock was 20MHz.

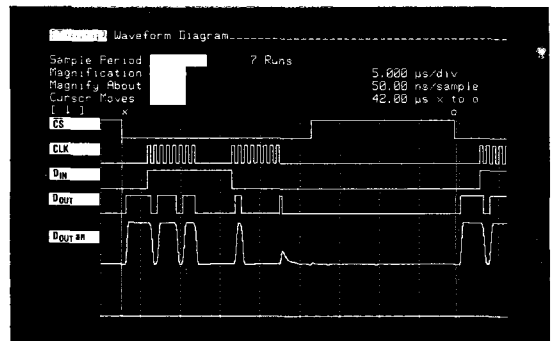


Figure 2. Timing Diagram

Application Note 36C

The analog section of the schematic in Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1290 please see the data sheet.

Software Description

The software configures and controls the SPI of the TMS370C050. Additionally, the software manipulates T1EVT (\overline{CS} of the LTC1290), generates ACLK via pin T2IC2/PWM and generates a delay during which time the LTC1290 performs a conversion.

The System Control and Configuration Control Register 2 (SCCR2) is first configured so the system is operating in the privilege mode. Next the code configures the Timer 2 module to generate a 2.5MHz ACLK. The T2 Compare Registers are loaded with a one. This will generate an ACLK with a frequency equal to one half the internal processor clock (one fourth the crystal frequency). Next the T2IC2/PWM pin is enabled to toggle. Then the pin is configured as an output with the T2IC2/PWM function.

Next the SPI clock is enabled then the SOMI and SIMO functions are enabled. The SPI Configuration Control Register (SPICCR) is set for eight bit character length, an

SPI clock that is 1/16 of the crystal frequency, input data transfer on the rising edge, output data transfer on the falling edge and initialization of the SPI. The SPI Operation Control Register (SPICTL) is set to disable the SPI interrupt, enable transmission and place the SPI in the master mode. Finally the SPI is enabled.

The T1EVT pin on Timer Module 1 is configured as an output pin and \overline{CS} is made to go low or high by placing a "0" or "1" in the T1EVT DATA OUT bit of the Timer 1 Port Control Register 1 (T1PC1). A D_{IN} word that configures the LTC1290 for CH7 with respect to COM, unipolar, MSB first and a 16-bit word length is shown in Figure 3.

T1EVT is made to go low. D_{IN} for the LTC1290 is loaded into the serial data register (SPIDAT). Storing D_{IN} in SPIDAT causes the transfer to begin. After waiting for the first eight bits to be transferred (3 NOP's) the first eight bits containing the MSB's of the LTC1290 are read from the receive data buffer register (SPIBUF) and stored in register 20 as shown in Figure 4. The SPI INT FLAG in the SPICTL register is reset when the data is read from the SPIBUF. The LSB's are transferred in the same manner and are stored in register 21. The data at this point is stored left justified.

1	1	1	1	1	1	1	1
S/D	O/S	S1	S2	UNI	MSBF	WL1	WLO

Figure 3. D_{IN} Word for LTC1290

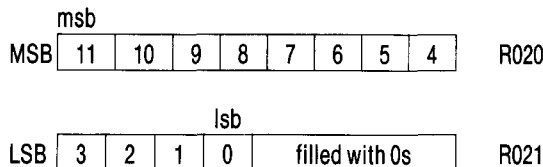


Figure 4. Memory Map

At this time 52 ACLK cycles must be allowed for the A/D to perform its next conversion. Usually the processor will have other tasks to perform during this time. If this is not the case a string of NOP's or a simple delay loop can be used to generate this delay. The code is shown in Figure 5 and a delay loop has been chosen for the A/D conversion.

LABEL	MNEMONIC	COMMENTS
	MOV #001h,P012	;CONFIGURATION DATA FOR SCCR2
		;CONFIGURE T2IC2/PWM PIN FOR ACLK
	MOV #000h,P062	;LOAD MSB DATA FOR COMPARE REG
	MOV #001h,P063	;LOAD LSB DATA FOR COMPARE REG
	MOV #070h,P06C	;CONFIGURATION DATA FOR T2CTL3
	MOV #030h,P06E	;CONFIGURATION DATA FOR T2PC2
	MOV #002h,P03D	;ENABLE SPI CLOCK
	MOV #032h,P03E	;ENABLE SOMI AND SIMO
	MOV #0CFh,P030	;CONFIGURATION DATA FOR SPICCR
	MOV #006h,P031	;CONFIGURATION DATA FOR SPICTL
	MOV #00Fh,P030	;ENABLE SPI
START	MOV #001h,P04D	;T1EVT GOES LOW (\overline{CS} GOES LOW)
	MOV #0FFh,P039	;LOAD D_{IN} INTO SPIDAT START SCLK
	NOP	;3 NOP'S FOR TIMING
	MOV P037,R020	;STORE MSB'S IN REGISTER 20
	MOV #000h,P039	;START NEXT SPI CYCLE
	NOP	;3 NOP'S FOR TIMING
	MOV P037,R021	;STORE LSB'S IN REGISTER 21
	MOV #005h,P04D	;T1EVT GOES HIGH (\overline{CS} GOES HIGH)
		;A/D CONVERSION DELAY LOOP
DELAY	MOV #002h,R023	;LOAD DATA IN DELAY COUNTER
	DEC R023	;DECREMENT COUNTER
	CMP #000h,R023	;COMPARE COUNTER WITH ZERO
	JNZ DELAY	;IF NOT ZERO RETURN TO DELAY
	JMPL START	;RETURN FOR NEXT SPI CYCLE

Figure 5. TMS370C050 Code

Power Shutdown

The TMS370C050 can be placed in one of three power reduction modes by configuring the SCCR2 register and issuing the IDLE command. Placing the TMS370C050 in the HALT mode reduces the supply current to its minimum power down value of 50 μ A. Therefore incorporating this with the power shutdown feature of the LTC1290 (typically 5 μ A in shutdown) it is possible to build a system that draws very low current when not in use. Figure 6 shows such a sequence. An external interrupt is required for the TMS370C050 to exit from the HALT mode. Then three conversion cycles are required to obtain the required data from a measurement and then enter the power shutdown mode again. The data is valid on the second conversion.

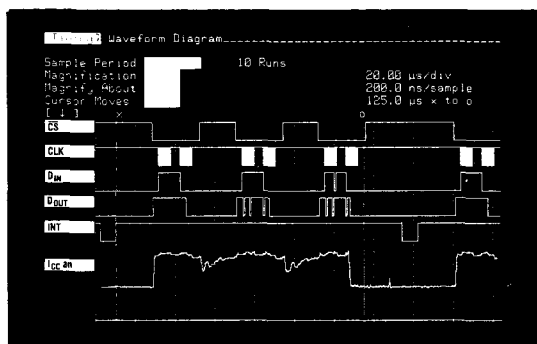


Figure 6. Power Shutdown

Application Note 36C

The third conversion is required because when power shutdown is requested ($D_{IN} = \#0FD$) the data from the previous conversion is output as a 10-bit word. The bottom trace shows the supply current for the LTC1290 during shutdown and then during conversion. Note there is no wait required for the LTC1290 to start a conversion after exiting from the shutdown mode. The time required for applying an external interrupt, making a measurement, storing the data and entering the shutdown mode is approximately 125 μ s. The code is shown in Figure 7.

Summary

A four wire interface between the LTC1290 and the TMS370C050 with a combined data conversion and data transfer rate of 42 μ s was demonstrated. The interface used the serial (SPI) port of the TMS370C050. The 12 data bits of the LTC1290 are shifted MSB first in two 8-bit transfers. The data is stored left justified in the TMS370C050's internal registers. By using the power reduction mode of the TMS370C050 and the power shutdown feature of the LTC1290 a low power system was shown to make a measurement in 125 μ s when active.

LABEL	MNEMONIC	COMMENTS	LABEL	MNEMONIC	COMMENTS
	.DATA 7F8h	;SET INTERRUPT 3 VECTOR WHEN		NOP	;3 NOP'S FOR TIMING
	.BYTE 70h,00h	;PROCESSOR COMES OUT OF HALT MODE		MOV P037,R021	;STORE LSB'S IN REGISTER 21
	.TEXT 7000h		MOV #005,P04D	;T1EVT GOES HIGH (\overline{CS} GOES HIGH)	
		;INTERRUPT SERVICE ROUTINE EXECUTED			;A/D CONVERSION DELAY LOOP
		;WHEN PROCESSOR COMES OUT OF HALT	MOV #002h,R023	;LOAD DATA IN DELAY COUNTER	
		;MODE	DELAY DEC R023	;DECREMENT COUNTER	
MOV #005h,P019		;CLEAR INTERRUPT FLAG	CMP #000h,R023	;COMPARE COUNTER WITH ZERO	
RTI		;RETURN FROM INTERRUPT	JNZ DELAY	;IF NOT ZERO RETURN TO DELAY	
BEGIN		;MAIN PROGRAM	DJNZ R025,LOOP	;RETURN FOR NEXT CONVERSION	
EINT		;ENABLE INTERRUPTS			;START POWER SHUTDOWN CONVERSION
MOV #005h,P04D		;CS GOES HIGH	MOV #001h,P04D	;T1EVT GOES LOW (\overline{CS} GOES LOW)	
MOV #001h,P012		;CONFIGURATION DATA FOR SCCR2	MOV #0FDh,P039	;LOAD D_{IN} FOR POWER SHUTDOWN	
		;CONFIGURE T2IC2/PWM PIN FOR ACLK			;3 NOP'S FOR TIMING
MOV #000h,P062		;LOAD MSB DATA FOR COMPARE REG.	MOV P037,R022	;CLEAR SPIBUF	
MOV #001h,P063		;LOAD LSB DATA FOR COMPARE REG.	MOV #000,P039	;START NEXT SPI CYCLE	
MOV #070h,P06C		;CONFIGURATION DATA FOR T2CTL3			;3 NOP'S FOR TIMING
MOV #030h,P06E		;CONFIGURATION DATA FOR T2PC2			
			MOV P027,R022	;CLEAR SPIBUF	
MOV #002h,P03D		;ENABLE SPI CLOCK	MOV #005h,P04D	;T1EVT GOES HIGH (\overline{CS} GOES HIGH)	
MOV #032h,P03E		;ENABLE SOMI AND SIMO			
MOV #0CFh,P030		;CONFIGURATION DATA FOR SPICCR	MOV #0C0h,P012	;PUT TMS370C050 IN HALT MODE	
MOV #006h,P031		;CONFIGURATION DATA FOR SPICTL	IDLE		
MOV #00Fh,P030		;ENABLE SPI	JMPL START	;AFTER EXTERNAL INTERRUPT JUMP TO ;START	
START EINT		;ENABLE INTERRUPTS			
MOV #002h,R025		;SET LOOP REG. TO 2 (WILL LOOP 2 TIMES)			
LOOP MOV #001h,P04D		;T1EVT GOES LOW (\overline{CS} GOES LOW)			
MOV #0FFh,P039		;LOAD D_{IN} INTO SPIDAT START SCLK			
					;3 NOP'S FOR TIMING
MOV P037,R020		;STORE MSB'S IN REGISTER 20			
MOV #000h,P039		;START NEXT SPI CYCLE			

Figure 7. Power Shutdown Code

Interfacing the LTC1290 to the COP820C MCU

Sammy Lum
 Tim Rust

Introduction

This application note describes the hardware and software required for communication between the LTC1290 12-bit data acquisition system and the National Semiconductor COP800 microcontroller family which uses the MICROWIRE/PLUS serial interface. The simple four wire interface is capable of completing a 12-bit conversion and shifting the data in 37 μ s. Configuration of the LTC1290 and the COP820C will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be shown. Finally, a summary of the key points of this interface will be given including data throughput rates.

Interface Details

The LTC1290 has two clock lines: ACLK and SCLK. ACLK controls the A/D conversion rate while SCLK controls the data shift rate. Data is transferred in a full duplex format over D_{IN} and D_{OUT}.

The National Semiconductor MICROWIRE/PLUS is a synchronous, full duplex, serial port built into the COP800 family that allows easy interface to the LTC1290. MICROWIRE/PLUS provides clock, data in and data out lines that are compatible with the LTC1290. One additional line (G1) is required to control the \overline{CS} pin on the LTC1290. The schematic of Figure 1 shows how the two devices are connected.

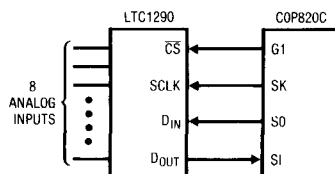
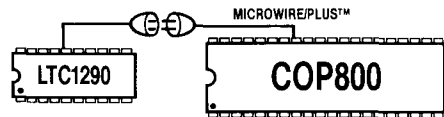


Figure 1. Schematic



Hardware Description

The actual interface was done using the COP820C, a member of the COP800 family. All code shown here should work with any of the COP800 family.

The code for this interface was developed on a COP820 evaluation board operated in the emulation mode.

The timing diagram of Figure 2 was obtained with an HP1631A logic analyzer using a 4MHz ACLK. The COP820C clock was 10MHz. To obtain a 37 μ s transfer time it is necessary to run the COP820C at 20MHz which requires a high speed version of the part.

The analog section of the schematic in Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1290 please see the data sheet.

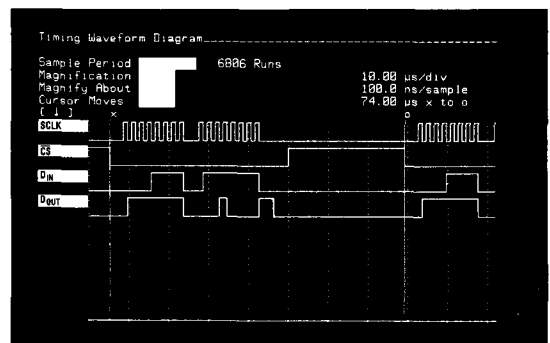


Figure 2. Timing Diagram

Software Description

The software configures and controls the MICROWIRE/PLUS serial interface of the COP820C. Additionally, the software manipulates G1 (\overline{CS} of the LTC1290) and generates a delay during which time the LTC1290 performs a conversion.

Application Note 36D

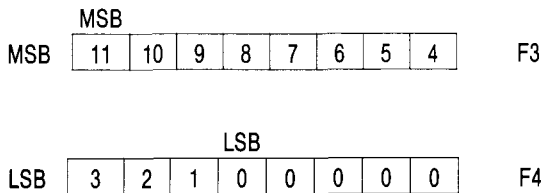
The code first loads the LTC1290 D_{IN} word into memory location \$F0. This D_{IN} word configures the LTC1290 for CH0 with respect to CH1, MSB first, unipolar and 16 bits as shown in Figure 3. Next port G is configured for MICROWIRE™ master mode and G1 is configured as an output. The control register is initialized so that SO and SK are outputs. The port G data register address is loaded into the B register. At this point the COP820C is initialized and the data transfer process is ready to begin.

The D_{IN} word for the LTC1290 is then loaded into the ACC from location \$F0. G1 (\overline{CS}) is cleared and D_{IN} is transferred into the MICROWIRE shift register. The BUSY bit of the PSW register is set which starts the transfer of the first eight bits. A delay consisting of 15 NOPs waits for the data shift to finish at which time the D_{OUT} word from the LTC1290 is loaded into the ACC. The busy bit is set again which causes the transfer to continue. Then, the D_{OUT} word in the ACC is stored in location \$F3. The busy bit is cleared which halts the transfer. G1 (\overline{CS}) is set and the contents of the MICROWIRE shift register are swapped with those of the ACC. The contents of the ACC are then stored in \$F4. The data at this point is left justified as shown in Figure 4.

52 ACLK cycles must be allowed between transfers for the A/D to perform its next conversion. The instructions, after G1 is set, take enough time so that no additional delay is required by this program.

0	0	0	0	1	1	1	1
S/D	O/S	S1	S2	UNI	MSBF	WL1	WLO

Figure 3. D_{IN} Word for LTC1290



D_{OUT} from LTC1290 stored in COP820C RAM

Figure 4. Memory Map

LABEL	MNEMONIC	COMMENTS
	LD (F0)—0F	LOAD 0F INTO F0 (D_{IN})
	LD (D5)—32	CONFIGURE PORT G
	LD (EE)—8	CONFIGURE CONTROL REG.
	LD (B)—D4	PORT G DATA REG. INTO B
LOOP	LD (A)—(F0)	LOAD D_{IN} INTO ACC
	RBIT 1	G1 RESET (\overline{CS} GOES LOW)
	X (A)—(E9)	LOAD D_{IN} INTO SHIFT REG.
	LD (B)—EF	LOAD PSW REG ADDR IN B
	SBIT 2	TRANSFER BEGINS
	NOP	15 NOPs FOR TIMING
	X (A)—(E9)	LOAD D_{OUT} INTO ACC
	SBIT 2	TRANSFER CONTINUES
	NOP	15 NOPs FOR TIMING
	X (A)—(F3)	LOAD D_{OUT} IN ADDR F3
	LD (B)—D4	PUT PORT G ADDR IN B
	SBIT 1	G1 SET (\overline{CS} GOES HIGH)
	X (A)—(E9)	LOAD D_{OUT} INTO ACC
	X (A)—(F4)	LOAD D_{OUT} IN ADDR F4

Figure 5. COP820C Code

Power Shutdown

The LTC1290 can be shutdown by inputting the appropriate D_{IN} word (0D). A dummy conversion prior to a request for power shutdown is required because the data from the previous conversion will be shifted out as a 10-bit word during the power shutdown request. Upon power up the LTC1290 is ready for conversion and the D_{OUT} word will be valid on the second request for conversion.

Summary

A four wire interface between the LTC1290 and the COP820C with a combined data conversion and transfer time of $37\mu s$ was demonstrated. The interface used the MICROWIRE/PLUS serial port of the COP820C. The 16 data bits of the LTC1290 are shifted MSB first in two 8-bit transfers. The data is stored left justified in the COP820C's internal RAM.

Reference

Hoover, Guy and Rempfer, William, "Interfacing the LTC1090 to the COP820C MCU," Application Note 26D, Linear Technology Corp.

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Interfacing the LTC1290 to the TMS7742 MCU

Sammy Lum
Tim Rust

Introduction

This application note describes an interface between the LTC1290 12-bit data acquisition system and the TMS7000 family of microcomputers (e.g., TMS7742). The simple four wire interface is capable of completing a 12-bit conversion and shifting the data to the TMS7742 in 102 μ s. Configuration of the LTC1290 and the TMS7742 will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be shown. Finally, a summary of the key points of this interface will be given including data throughput rates.

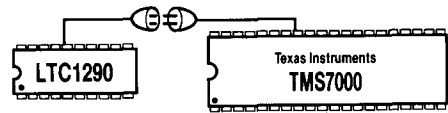
Interface Details

The LTC1290 has two clock lines: ACLK and SCLK. ACLK controls the A/D conversion rate while SCLK controls the data shift rate. Data is transferred in a full duplex format over D_{IN} and D_{OUT}.

The TMS7742 contains a synchronous, full duplex, serial port that allows the user to construct a simple communication path to the LTC1290. The serial port provides clock, transmit, and receive lines that are compatible with the LTC1290. The only additional line required is one programmable output pin (A0) to control \overline{CS} on the LTC1290. The schematic of Figure 1 shows how the two devices are connected.

Hardware Description

The TMS7742 was chosen because it contains 4k of EPROM which can be programmed using a standard



EPROM programmer. Any member of the TMS7000 family which contains a serial port should be able to use this code with only modifications to the peripheral register numbers.

The timing diagram of Figure 2 was obtained using an HP1631A logic analyzer. ACLK of the LTC1290 was 4MHz and the TMS7742 clock was 5MHz.

The analog section of the schematic of Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1290 please see the data sheet.

Software Description

The software configures and controls the serial port of the TMS7742. Additionally, the software manipulates A0 (\overline{CS} of the LTC1290) and generates a delay during which time the LTC1290 performs a conversion.

The code first disables all interrupts and initializes the stack. Next the serial port is configured. Tx is enabled, the serial port is reset, and the SMODE register is configured for eight bits, no parity, and one stop bit. The SCLK rate is

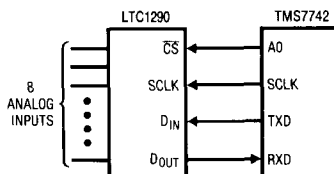


Figure 1. Schematic

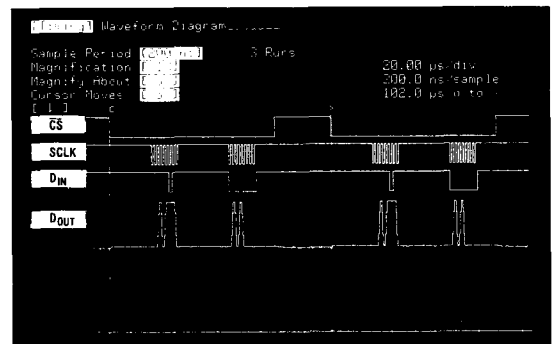


Figure 2. Timing Diagram

Application Note 36E

set to the processor clock frequency divided by 4. The D_{IN} word of the LTC1290 is next loaded into the ACC. This D_{IN} word (\$DF) configures the LTC1290 for CH7 with respect to COM, unipolar mode, LSB-first and a 16-bit word length. Examine Figure 3 to see how this is constructed keeping in mind that the TMS7742 transmits data LSB-first.

A subroutine SXTNBIT is called next. This is a routine that does the actual data shifting. A0 (\overline{CS}) is cleared. Then, the LTC1290 D_{IN} word is placed into the transmit buffer. The serial port is turned on and the data is shifted while the processor idles in a loop. The first eight bits containing the LSBs are then placed in the B register. The procedure is repeated for the next eight bits which contain the four MSBs and the result is placed in the A register. A0 (\overline{CS}) is then set and the subroutine returns to the original program. The data in the A and B registers is then stored in R5 and R6.

At this time 52 ACLK cycles must be allowed for the A/D to perform its next conversion. Enough time is consumed by this program however that no additional delay for the conversion is required. Branching back to the label LOOP starts the next conversion.

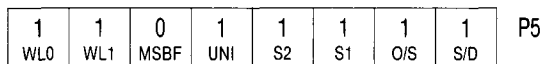
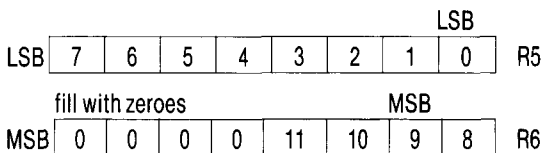


Figure 3. D_{IN} Word for LTC1290 Stored in TMS7742 RAM



D_{OUT} from LTC1290 stored in TMS7742 RAM

Figure 4. Memory Map

Power Shutdown

The LTC1290 can be shutdown by inputting the appropriate D_{IN} word (9F). A dummy conversion prior to a request for power shutdown is required because the data from the previous conversion will be shifted out as a 10-bit word during the power shutdown request. Upon power up the LTC1290 is ready for conversion and the D_{OUT} word will be valid on the second request for conversion.

Summary

A four wire interface between the LTC1290 and the TMS7742 with a combined data conversion and transfer time of 102μs was demonstrated. The interface used the serial port of the TMS7742. Because the serial port transfers data LSB-first, care must be taken to properly construct the D_{IN} word so that the bits are transmitted in the proper order to the LTC1290. The 12 data bits of the LTC1290 are shifted LSB-first in two 8-bit transfers. The data is stored right justified in the TMS7742's internal RAM.

Reference

Hoover, Guy and Rempfer, William, "Interfacing the LTC1090 to the TMS7742 MCU," Application Note 26E, Linear Technology Corp.

LABEL	MNEMONIC	COMMENTS	
START	DINT	DISABLES ALL INTERRUPTS	
	MOVP % > 2A, P0	DISABLE INTERRUPT FLAGS	
	MOVP % > 02, P16	DISABLE INTERRUPT FLAGS	
	MOV % > 60, B	ADDRESS OF STACK	
	LDSP	PUT ADDRESS INTO POINTER	
	MOVP % > DF, P5	CONFIGURE PORT A	
	MOVP % > 08, P6	ENABLE Tx BY SETTING B3 = 1	
	MOVP % > 00, P17	P17 POINTS TO SCTL0	
	MOVP % > 40, P17	RESET THE SERIAL PORT	
	MOVP % > 0C, P17	CONFIGURE THE SERIAL PORT	
	MOVP % > 00, P21	TURN START BIT OFF	
	MOVP % > 00, P17	ENABLE THE SERIAL PORT	
	MOVP % > 00, P20	SET SCLK RATE (TIMER 3)	
MOVP % > C0, P21	START TIMER		
LOOP	MOV % > DF, A	LOAD LTC1290 D _{IN} WORD IN A	
	CALL SXTNBIT	ROUTINE THAT SHIFTS DATA	
	MOV B, R5	PUT FIRST 8 LSBs IN R5	
	MOV A, R6	PUT MSBs IN R6	
BR @LOOP	NEXT CONVERSION		
SXTNBIT	ANDP % > FE, P4	A0 CLEARED (\overline{CS} GOES LOW)	
	MOVP A, P23	PUT LTC1290 D _{IN} INTO TXBUF	
	MOVP % > 40, P21	SCLK OFF (TIMER 3 DISABLED)	
	MOVP % > 17, P17	ENABLE SERIAL PORT	
	MOVP % > C0, P21	SCLK ON (TRANSFER BEGINS)	
	MOVP % > 14, P17	TXEN GOES LOW	
	MOV % > 02, A	LOAD COUNTER	
	WAIT1	LOOP WHILE SHIFT OCCURS	
WAIT1	NOP	DELAY	
	MOVP P22, B	PUT D _{OUT} FROM LTC1290 IN B	
	MOVP A, P23	LOAD TXBUF	
	MOVP % > 40, P21	SCLK OFF (TIMER 3 DISABLE)	
	MOVP % > 17, P17	ENABLE SERIAL PORT	
	MOVP % > C0, P21	SCLK ON (TRANSFER BEGINS)	
	MOVP % > 14, P17	TXEN GOES LOW	
	MOV % > 02, A	LOAD COUNTER	
	WAIT2	LOOP WHILE SHIFT OCCURS	
	WAIT2	NOP	DELAY
		MOVP P22, A	PUT D _{OUT} FROM LTC1290 IN A
		ORP % > 01, P4	A0 SET (\overline{CS} GOES HIGH)
RETS		RETURN TO MAIN PROGRAM	

Figure 5. TMS7742 Code

Interfacing the LTC1290 to the COP402N MCU

Sammy Lum
 Tim Rust

Introduction

This application note describes the hardware and software required for communication between the LTC1290 12-bit data acquisition system and the National Semiconductor COP400 microcontroller family which uses the MICROWIRE serial interface. The simple four wire interface is capable of completing a 12-bit conversion and shifting the data in 100 μ s. Configuration of the LTC1290 and the COP402N will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be shown. Finally, a summary of the key points of this interface will be given including data throughput rates.

Interface Details

The LTC1290 has two clock lines: ACLK and SCLK. ACLK controls the A/D conversion rate while SCLK controls the data shift rate. Data is transferred in a full duplex format over D_{IN} and D_{OUT}.

The National Semiconductor MICROWIRE interface is a synchronous, full duplex, serial port built into the COP400 family that allows the user to easily interface to the LTC1290. MICROWIRE provides clock, data in and data out lines that are compatible with the LTC1290. One additional line (G0) is required to control the \overline{CS} pin on the LTC1290. The schematic of Figure 1 shows how the two devices are connected.

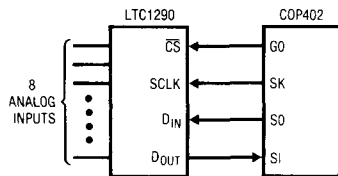
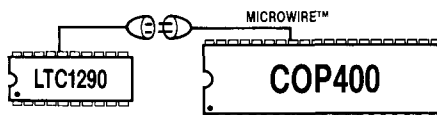


Figure 1. Schematic



Hardware Description

The actual interface will involve using the COP402N, a member of the COP400 family. All code shown here should work with any of the COP400 family.

The code for this interface was developed on a COP400 evaluation board which allows an external EPROM to be used in place of the internal processor ROM.

The timing diagram of Figure 2 was obtained with an HP1631A logic analyzer using a 4MHz ACLK. The COP402N clock was 4MHz.

The analog section of the schematic in Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1290 please see the data sheet.

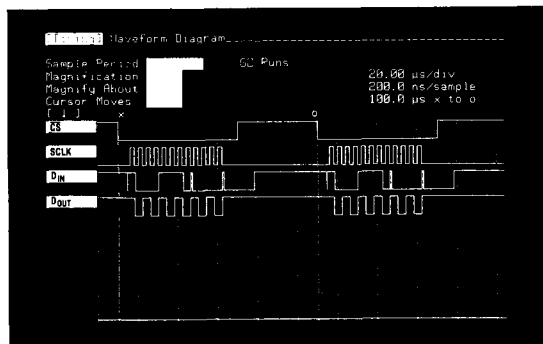


Figure 2. Timing Diagram

Software Description

The software configures and controls the MICROWIRE serial interface of the COP402N. Additionally, the software manipulates G0 (\overline{CS} of the LTC1290) and generates a delay during which time the LTC1290 performs a conversion.

The code first initializes the B register and then loads the LTC1290 D_{IN} word into the RAM of the COP402 one nibble at a time. As shown in Figure 3 the D_{IN} word configures the

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LTC1290 for CH0 with respect to COM, unipolar, MSB first, and 12 bits. SO is configured as an output. The carry is set so that when an XAS instruction is generated the shift clock (SK) will begin clocking data.

The first nibble of the D_{IN} word is loaded into the ACC and $G0$ (\overline{CS}) is cleared. The D_{IN} nibble is loaded into the shift register and the data begins to shift. The second nibble of the D_{IN} word is loaded into the ACC. One NOP is allowed for timing and then the contents of the ACC are swapped with those of the shift register. The MSBs of the LTC1290 D_{OUT} word are now in the ACC. This data is then stored in memory location \$13. The ACC is loaded with null data from RAM and another swap between the ACC and the shift register is executed. The next D_{OUT} nibble is stored in \$14. The carry is cleared so that on the next XAS instruction the shift clock will stop. The XAS instruction is executed and the final nibble of the LTC1290 D_{OUT} word containing the LSBs is loaded into the ACC. $G0$ (\overline{CS}) is taken high and the A/D begins its next conversion cycle. The third D_{OUT} nibble is stored in location \$15. The B register is then reinitialized so that when the loop is run again the data will always be stored in the same memory locations. The D_{OUT} data from the LTC1290 is now in a left justified format as shown in Figure 4.

52 ACLK cycles must be allowed between transfers for the A/D to perform its next conversion. The instructions, after $G0$ is set, take enough time so that no additional delay is required by this program.

\$10				\$11			
1	0	0	0	1	1	1	0
S/D	O/S	S1	S2	UNI	MSBF	WL1	WLO

Figure 3. D_{IN} Word for LTC1290

MSB				
11	10	9	8	\$13
7	6	5	4	\$14
LSB				
3	2	1	0	\$15

D_{OUT} from LTC1290 stored in COP402 RAM

Figure 4. Memory Map

LABEL	MNEMONIC	COMMENTS
	CLRA	MUST BE FIRST INSTRUCTION
	LBI	BR = 1 BD = 0 INITIALIZE B REG.
	STII	8 FIRST D_{IN} NIBBLE IN \$10
	STII	E SECOND D_{IN} NIBBLE IN \$11
	STII	0 NULL DATA IN \$12, B = \$13
	LEI	C SET EN TO (1100) BIN
LOOP	SC	CARRY SET
	LDD	1,0 LOAD FIRST D_{IN} NIBBLE IN ACC
	OGI	0 $G0$ (\overline{CS}) CLEARED
	XAS	ACC TO SHIFT REG. BEGIN SHIFT
	LDD	1,1 LOAD NEXT D_{IN} NIBBLE IN ACC
	NOP	TIMING
	XAS	NEXT NIBBLE, SHIFT CONTINUES
	XIS	0 FIRST NIBBLE D_{OUT} TO \$13
	LDD	1,2 PUT NULL DATA IN ACC
	XAS	SHIFT CONTINUES, D_{OUT} TO ACC
	XIS	0 NEXT NIBBLE D_{OUT} TO \$14
	RC	CLEAR CARRY
	CLRA	CLEAR ACC
	XAS	THIRD NIBBLE D_{OUT} TO ACC
	OGI	1 $G0$ (\overline{CS}) SET
	XIS	0 THIRD NIBBLE D_{OUT} TO \$15
	LBI	1,3 SET B REG. FOR NEXT LOOP

Figure 5. COP402 Code

Power Shutdown

The LTC1290 can be shutdown by inputting the appropriate D_{IN} word (D for the second nibble). A dummy conversion prior to a request for power shutdown is required because the data from the previous conversion will be shifted out as a 10-bit word during the power shutdown request. Upon power up the LTC1290 is ready for conversion and the D_{OUT} word will be valid on the second request for conversion.

Summary

A four wire interface between the LTC1290 and the COP402N with a combined data conversion and transfer time of 100 μ s was demonstrated. The interface used the MICROWIRE serial port of the COP402N. The 12 data bits of the LTC1290 are shifted MSB first in three 4-bit transfers. The data is stored left justified in the COP402N's internal RAM. The code demonstrated will work on any member of the COP400 family.

Reference

Hoover, Guy and Rempfer, William, "Interfacing the LTC1090 to the COP402N MCU," Application Note 26F, Linear Technology Corp.

MICROWIRE is a trademark of National Semiconductor Corp.

Interfacing the LTC1290 to the Z-80 MPU

Sammy Lum
 Tim Rust

Introduction

This application note describes an interface between the LTC1290 12-bit data acquisition system and the Z-80 microcomputer. The interface is capable of completing a 12-bit conversion and shifting the data to Z-80 in 260 μ s. Configuration of the LTC1290 and the Z-80 will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be shown. Finally, a summary of the key points of this interface will be given, including data throughput rates.

Interface Details

The LTC1290 has two clock lines: ACLK and SCLK. ACLK controls the A/D conversion rate while SCLK controls the data shift rate. Data is transferred serially in a synchronous, full duplex format over D_{IN} and D_{OUT}.

The Z-80 does not have a serial port. Therefore it is necessary for the user to construct a serial port with TTL gates as shown in the schematic of Figure 1.

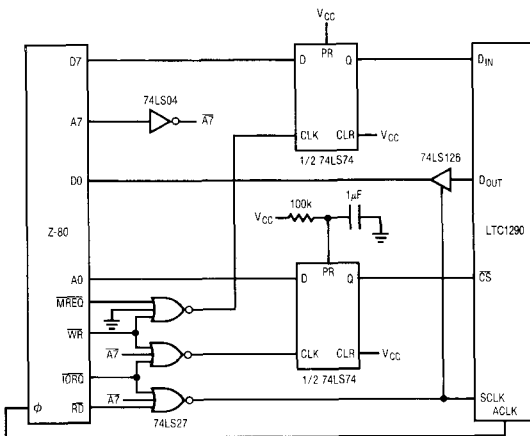
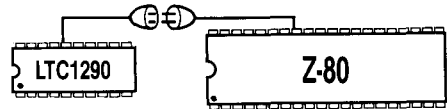


Figure 1. Serial Interface Requires Four 74LS Chips



Hardware Description

\overline{CS} is set or cleared by placing a 1 or a 0 on address line A0 and writing to an I/O port that has an even address of 128 or higher. The LTC1290 SCLK is generated by reading from an I/O port that has an address greater than 128. Data is clocked into the LTC1290 one bit at a time by placing the desired bit on D7 of the Z-80 and writing to any memory location. The serial data output of the LTC1290 is fed into D0 of the Z-80 through the 74LS126. The 74LS126 prevents the LTC1290 from writing to the data bus of the Z-80 except when the microprocessor requires data from the A/D. The ACLK of the LTC1290 is also the clock for the Z-80.

The code for this interface was developed on a Multitech MPF-1 single board development system.

The timing diagram of Figure 2 was obtained with an HP1631A logic analyzer. The Z-80 clock rate was 1.79MHz. Using a Z-80B and running it at a 6MHz clock rate, it is possible to reduce this time to approximately 100 μ s. This would require generating ACLK externally or dividing down the ϕ signal.

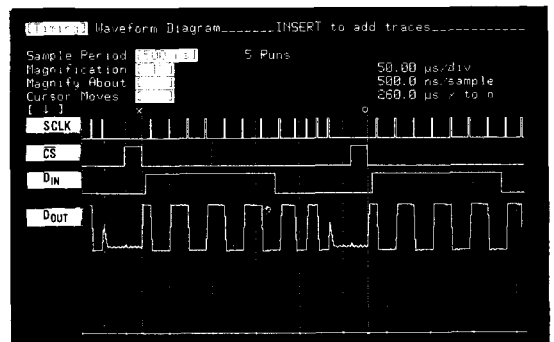


Figure 2. Throughput Time is Limited by the Z-80 MPU. A 12-Bit Conversion Result is Transmitted Every 260 μ s.

Fast Charge Circuits for NiCad Batteries

Jim Williams

Safe, fast charging of NiCad batteries is attractive in many applications. Short charge time requires high current. A potential difficulty with high current charging is battery heating. Excessive internal heating degrades the battery and can cause gas venting to the outside atmosphere. Fast charge schemes based on monitoring cell voltage during charge suffer because cell voltage is not necessarily indicative of the battery's charge state. Additionally, the battery's charge-voltage relationship may alter over life and temperature. Similarly, open loop charging techniques involving high charge rates for a fixed time do not account for battery charge state or characteristic shifts over life and temperature.

One way to charge batteries without abuse is to measure cell temperature and taper the charge accordingly. This method is based on the fact that a discharged battery converts charging current to stored electrochemical energy, with relatively little heat produced. When the battery arrives at full charge the cell is saturated and cannot hold any more energy. As such, heat is produced, raising battery temperature. One way to detect this point is to measure cell surface temperature referred to ambient. An absolute temperature measurement is undesirable

because cell temperature represents the summation of excess charging energy and ambient temperature. Additionally, the ambient and battery temperatures must be measured in phase. The thermal time constant of a battery pack can easily exceed one hour. If battery temperature is referred to a quickly responding ambient temperature poor charging characteristics can result. Consider the case of a portable computer retrieved from a locked automobile on a summer day. Passenger compartment temperature can exceed 120°F. The computer is brought inside, where the ambient temperature sensor quickly settles to 73°F. The battery pack temperature is sitting at 120°F looking through a one hour thermal time constant. Under these conditions the system is fooled into believing the battery has just received a full charge, and no charge is delivered. The opposite effect occurs if the computer is in a car parked overnight in Minneapolis in January. These effects are avoidable by lagging the ambient temperature information with a time constant similar to the battery packs. Figure 1 shows a simple analog. The resistors represent thermal resistance while the capacitors correspond to thermal capacitance. Ambient temperature appears as a common mode term, while charger energy affects the battery only. Note that the ambient and battery

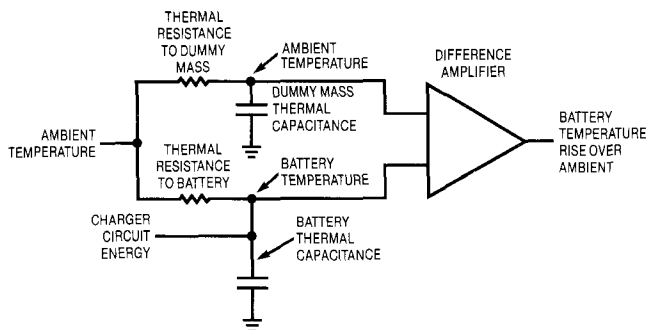


Figure 1. Simplified Thermal Analog. Matched Thermal RC Terms Provide Immunity to Ambient Temperature Shifts.

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temperatures do not require the same individual R-C values to present phased information to the difference amplifier. Rather, their RC products must be matched. A massive battery pack with relatively low thermal resistance to ambient can be matched by the time constant of a well insulated (e.g., high thermal resistance) small thermal mass.

Practical Thermally Based NiCad Charger

Figure 2 shows a practical circuit. Thermocouples sense cell and ambient temperatures. The LT1006 amplifier furnishes the low level capability necessary to work with the microvolt level thermocouple signals. To understand the circuit's operation, assume a discharged battery pack in the transistor collector line. The battery and ambient thermocouples are at the same temperature. The battery thermocouple is directly mounted to one of the cells in the pack. The ambient thermocouple is thermally insulated and mounted to a mass, perhaps a frame member of the equipment. Under these conditions the sensors are phase matched, their outputs cancel and A1 sees 0V. The offset adjustment deliberately introduces enough input offset for A1 to swing positively, turning on the transistor. Current flows from the supply, through the battery pack and to ground via the $250\mu\Omega$ shunt. The low impedance shunt minimizes losses, cost, and complexity. The voltage across the shunt rises to about $625\mu\text{V}$ (the amount of offset forced by the potentiometer), and the amplifier servo controls about 2.5A through the battery pack. As the battery charges, it heats. This heat is picked up by the

*See Appendix A for construction information on low resistance shunts.

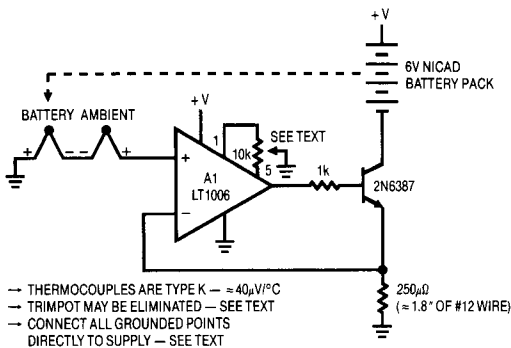


Figure 2. Thermally Controlled NiCad Battery Charger

battery-mounted thermocouple. The temperature difference between the two thermocouples determines the voltage which appears at the amplifier's positive input. As battery temperature rises, this small negative voltage (1°C difference between the thermocouples equals $40\mu\text{V}$) becomes larger. The amplifier gradually reduces the current through the battery to maintain its inputs at balance. The effect of this action is shown in Figure 3. The battery charges at a high rate until heating occurs and the circuit then tapers the charge. The values given in the circuit limit the battery surface temperature rise over ambient to about 15°C .

Figure 4's circuit is arranged for use with batteries which are committed to ground. The common emitter output necessitates exchanging amplifier input assignments, but circuit operation is identical to Figure 2. In both circuits the trimpot may be eliminated by specifying an LT1006 set at manufacture to the desired offset value.

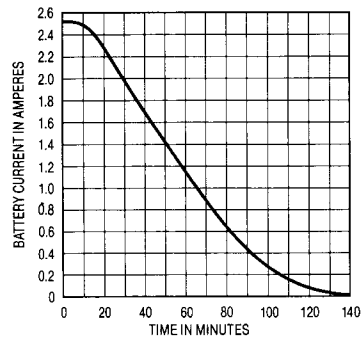


Figure 3. Figure 2's Charge Characteristics

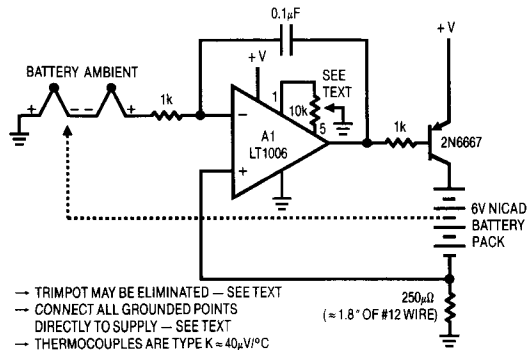


Figure 4. Figure 2's Circuit Arranged for a Grounded Battery

The small shunt sense voltage requires a high quality ground for accurate results. This ensures that the large current flow through the transistor does not combine with ground return impedances to create errors. In practice, all returns should be brought directly back to the supply common terminal. Similarly, parasitic thermocouple effects should be avoided (see LTC Application Note 9 for a discussion on minimizing parasitic thermocouple effects).

Both circuits force the transistor to dissipate some power, particularly in the middle of the charge curve. The heat produced may be a problem in a very small enclosure. Figure 5's circuit eliminates this problem. This design is similar to the others, except that the A2 duty cycle modulator configuration is interposed between A1 and the output transistor. The transistor, in this case a power FET, operates in switched mode, delivering duty cycle modu-

lated current pulses to the battery pack. R7-C4 filters the switching waveform to DC. R6 and R7 present a balanced source impedance to A1. C2 sets gain roll-off. This design relies on the source impedance of the wall transformer to limit the current through Q1 and the battery pack. This parameter may be set when specifying the transformer. Figure 6 should be used in cases where the charging source has low impedance. Here, the circuit's output is reconfigured as a simple step down switching regulator (basic operation of step down switching regulators is described in LTC Application Note 35). The 74C04's provide phase inversion and drive for Q1, a P-channel MOSFET. Figure 7 shows waveforms. Trace A is A2's output with trace B showing Q1's gate drive. Trace C is Q1's drain voltage and trace D its current. Trace E is the MR850 catch diode current. Trace F is L1's current. L1 smooths current flow, resulting in low loss operation.

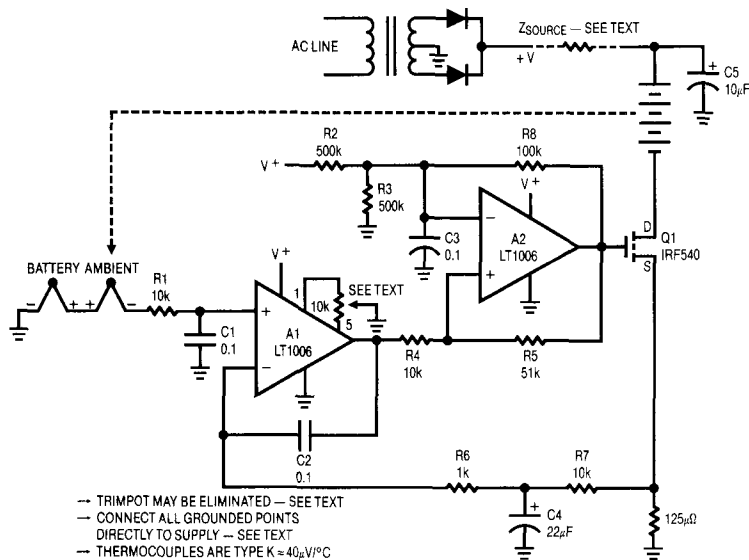


Figure 5. Switched Mode Thermal NiCad Charger

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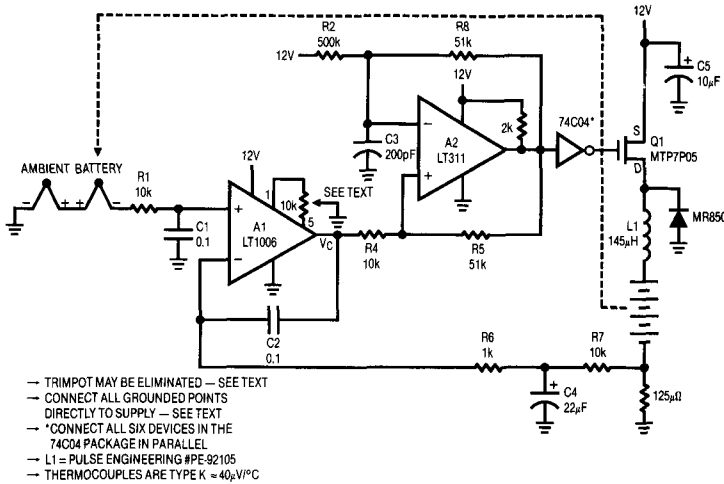
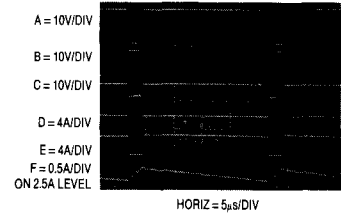


Figure 6. Switched Mode Thermal NiCad Charger

Figure 7. Figure 6's Switching Waveforms



Note — This application note was derived from a manuscript originally prepared for publication in EDN magazine.
 Acknowledgement — The contributions of William Cho towards the completion of this Application Note are gratefully acknowledged.

APPENDIX A

Construction of Low Resistance Shunts

A simple, inexpensive way to construct low resistance shunts is to use a small length of wire or PC trace. The type and length of wire determine shunt resistance, which will vary with desired charging characteristics. Figure A1

WIRE GAUGE	$\mu\Omega/\text{INCH}$
10	83
11	100
12	130
13	160
14	210
15	265
16	335
17	421
18	530
19	670
20	890
21	1000
22	1300
23	1700
24	2100
25	2700

Figure A1. Resistance vs Size for Various Copper Wire Types

gives resistance vs length characteristics for various wire sizes. The shunt should have separate connections for sensing (Kelvin style) so that the high current does not corrupt readings. Figure A2 shows a typical configuration.

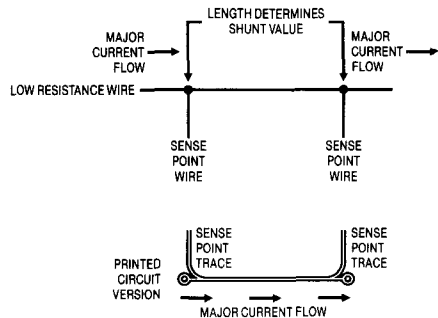


Figure A2. Detail of a Low Resistance Current Shunt

FilterCAD User's Manual, Version 1.00

Software Written By: Richard Zarr
Colin Hsi

Applications and
Algorithms: Nello Sevastopoulos
Philip Karantzalis
Richard Markell

Manual Written By: David Doty
Edited By: Richard Markell

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PART 1—GETTING STARTED

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WHAT IS FILTERCAD?

FilterCAD is a computer-aided design program for use in conjunction with the Linear Technology Corporation family of switched-capacitor filter i.c.'s. Devices supported by this version of FilterCAD include the LTC1059, 1059A, 1060, 1060A, 1061, 1061A, 1064, 1064A and 1164. Future Linear Technology Corporation devices may be added when available by means of the FilterCAD Device Parameter Editor (see Appendix 1).

FilterCAD is designed to help users without special expertise in filter design to design good filters with a minimum of effort. It can also help experienced filter designers achieve better results by providing the ability to play "what if" with the values and configuration of various components.

With FilterCAD, you can design any of the four major filter types (lowpass, highpass, bandpass, and notch), with Butterworth, Chebyshev, Elliptic, or custom-designed response characteristics. (Bessel filters can be realized by manually entering pole and Q values, but FilterCAD cannot synthesize a Bessel response in this version.) FilterCAD is limited to designs which can be achieved by cascading state-variable second-order sections. FilterCAD plots amplitude, phase and group-delay graphs, selects appropriate devices and modes, and calculates resistor values. Device selection, cascade order, and modes can be edited by the user.

LICENSE AGREEMENT/DISCLAIMER

This copy of FilterCAD is provided as a courtesy to the customers of Linear Technology Corporation. It is licensed for use in conjunction with Linear Technology Corporation products only. The program is not copy protected and you may make copies of the program as required, provided that you do not modify the program, and that said copies are used only with Linear Technology Corporation products.

While we have made every effort to ensure that FilterCAD operates in the manner described in this manual, we do not guarantee operation to be error free. Upgrades, modifications, or repairs to this program will be strictly at

the discretion of Linear Technology Corporation. If you encounter problems in installing or operating FilterCAD, you may obtain technical assistance by calling our applications department, at (408) 432-1900, between 8:00 a.m. and 5:00 p.m. Pacific time, Monday through Friday. Because of the great variety of IBM-compatible computer systems, operating-system versions, and peripherals currently in use, we do not guarantee that you will be able to use FilterCAD successfully on all such systems. If you are unable to use FilterCAD, Linear Technology Corporation does guarantee to provide design support for LTC filter products by whatever means necessary.

Linear Technology Corporation (LTC) makes no warranty, either expressed or implied, with respect to the use of FilterCAD or its documentation. Under no circumstances will LTC be liable for damages, either direct or consequential, arising from the use of this product or from the inability to use this product, even if we have been informed in advance of the possibility of such damages.

INVENTORY

Please check to be sure you have received the following items:

This Manual
FilterCAD Program Disk
LTC Filter Application Notes and Data Sheets may be included or, if they are not, may be requested from LTC.

The FilterCAD Diskette

Your FilterCAD distribution diskette includes the following files. If, after installing the program, you have difficulty in running FilterCAD, check your disk to be sure all of the necessary files are present.

README.DOC	(Optional) if present, includes updated information on FilterCAD not included in this manual
INSTALL.BAT	Automatic installation program — installs FilterCAD on hard drive
FCAD.EXE	Main program file for FilterCAD

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FCAD.OVR	Overlay file for FilterCAD — used by FCAD.EXE
FCAD.ENC	Encrypted copyright protection file — DO NOT TOUCH!
FDPF.EXE	Device-parameter file editor — used to update FCAD.DPF (see Appendix 1)
FCAD.DPF	Device-parameter file — holds data for all device types supported by FilterCAD
ATT.DRV	AT&T graphics adapter driver
CGA.DRV	IBM CGA or compatible graphics driver
EGAVGA.DRV	EGA and VGA graphics drivers
HERC.DRV	Hercules monochrome graphics driver
ID.DRV	Identification file for all driver specifications

A 3 1/2" diskette available upon special request contains the following files in addition to those just mentioned:

IBM8514.DRV	IBM8514 color graphics adapter driver
PC3270.DRV	IBM PC3270 color graphics adapter driver

Note: Once you have configured FilterCAD and selected your display type, you can delete unnecessary drivers if you need to conserve disk space. (Be sure not to delete any drivers from your original FilterCAD distribution diskette.)

Before You Begin

Please check the FilterCAD program disk to see if it contains the README.DOC file. This file, if present, will contain important information about FilterCAD not included in this manual. Please read this file before attempting to install and use FilterCAD. To display the README file on your screen, place the FilterCAD diskette in drive A and type:

```
TYPE    README.DOC    [Enter]
```

Press

[Ctrl] S

to pause scrolling. Press any key to resume scrolling. To print a hardcopy of the README file on your printer type:

```
TYPE    README.DOC >PRN    [Enter]
```

HARDWARE REQUIREMENTS

FilterCAD runs on an IBM PC, XT, AT, or PS/2, or a compatible system, equipped with one floppy drive or one hard drive and one floppy drive, at least 256k bytes of system memory, an appropriate graphics adapter and monitor, and DOS 2.0 or later. A list of the graphics adapters and modes supported by FilterCAD will be found in the "Configuration" section. FilterCAD is a calculation-intensive program, and should, therefore, be run on the most powerful system available. A floating-point math coprocessor (8087, 80287, or 80387, as appropriate for your system) is not required, but will significantly increase the operating speed of the program.

INSTALLATION

Floppy Disk Systems

Use the DOS DISKCOPY command to make a copy of the FilterCAD distribution disk. Place a diskette with the DOS DISKCOPY.COM program in drive A and type:

```
DISKCOPY  A:    B:    [Enter]
```

Following the messages that appear on your screen, place the FilterCAD distribution disk in drive A, place a blank floppy disk in drive B, and press any key to begin copying. When the copy is completed, put the original FilterCAD disk away in a safe place, and label your copy. You will use your copy to run FilterCAD.

Note: If you have only one floppy drive, DISKCOPY will prompt you when to swap diskettes. Just follow the messages that appear on the screen.

Hard Disk Systems

To install FilterCAD on a hard disk system, you should first make a floppy disk backup of the FilterCAD distribution disk, as indicated. Then, put your working copy of the FilterCAD diskette in drive A and type:

```
INSTALL      N: (path)      [Enter]
```

Where

```
"N:"
```

is the drive letter and

```
(path)
```

is an optional path specification. The INSTALL.BAT program will create a sub-directory called "FCAD" on the drive and below the optional path you have specified, and copy the FilterCAD program files into that directory. For example, if you typed

```
INSTALL      C: [Enter]
```

the program files will be installed in C:\FCAD. If you typed

```
INSTALL      C: \ FILTERS [Enter]
```

the program files will be installed in C:\FILTERS\FCAD.

FilterCAD is now installed on your hard disk and ready to run.

Note: If the directory you specify already exists, the install program will issue an error message saying that it was unable to create the specified directory. It will then copy the FilterCAD files into the existing directory, overwriting the earlier version of FilterCAD. However, before installing this version of FilterCAD over an existing version, you should delete the earlier version of FCAD.CFG from your hard disk to avoid problems.

STARTING AND CONFIGURING FILTERCAD

To start FilterCAD, place your working copy of the FilterCAD diskette in drive A or log on to the directory on your hard disk where FilterCAD's program files have been installed, and type:

```
FCAD        [Enter]
```

When you see FilterCAD's sign-on screen, press

```
[Enter]
```

again to start the program. When you run FilterCAD for the first time, select item 6 on the MAIN MENU, "CONFIGURE FilterCAD," before attempting to use the program. This will open the HARDWARE CONFIGURATION MENU, which offers the following eight options:

1. Install DISPLAY
2. Install PRINTER
3. Install PLOTTER
4. Install MOUSE
5. Configure I/O PORTS
6. Configure DISPLAY PARAMETERS
7. Set PATH to DRIVERS

9. RETURN to MAIN MENU

Installing the Display

The first step is to tell FilterCAD what video display adapter is installed in your system and what graphics mode you wish to use. To access the DISPLAY INSTALLATION MENU, press

```
1
```

The DISPLAY INSTALLATION MENU offers fourteen options, supporting all of the popular PC display adapters, including the IBM Color Graphics Adapter (CGA), the MCGA (the built-in graphics controller in IBM's PS/2 models 25 and 30), the Enhanced Graphics Adapter (EGA), the Video Graphics Array (VGA, the built-in graphics controller in IBM's PS/2 models 50-80, also available as an add-in card for PC/XT/AT family machines), Hercules Monochrome Graphics, the AT&T Graphics Adapter, and the IBM 8514 Graphics Adapter (IBM's high resolution graphics add-in for the PS/2 models 50-80). To install the driver for your display adapter and desired graphics mode, simply type the number of your selection and press

```
[Enter]
```

Several of the supported display adapters offer more than one option for different resolutions or color selections. The resolution and number of colors you will be able to obtain from a particular display adapter may depend on

the type of monitor connected to it. For example, the Enhanced Graphics Adapter will display 640 pixels by 200 lines with 16 colors on a standard RGB monitor (option 4), 640 pixels by 350 lines with 16 colors on an enhanced RGB monitor (item 5), or 640 pixels by 350 lines in monochrome on a TTL monochrome monitor (item 6). Obviously it is desirable to choose the highest resolution and greatest color selection available from your system. If you are uncertain what option to select for your particular monitor/display adapter combination, consult the documentation for your computer system, display adapter, and/or monitor.

Note: When you install your display and exit back to FilterCAD's main menu, you will be asked whether you want to save your changes to the FCAD.CFG file. Answer "YES." This will create the configuration file which will be used every time you start FilterCAD.

Installing Your Printer and Plotter

FilterCAD has been equipped with a text printer driver for a standard-ASCII text printer, which is used for printing reports, and a plotter driver for an HPGL-compatible plotter. These selections cannot be modified by the user. In addition, you can select a printer driver for a graphics screen dump. Press

2

to access the printer installation menu. The options at this time are limited to the Epson FX-80 or a compatible dot-matrix printer, the Hewlett-Packard ThinkJet, and the Hewlett-Packard LaserJet or a compatible laser printer. The last can be configured to print at a number of different resolutions, including 75, 100, 150, or 300 dots-per-inch. Note that FilterCAD performs a true pixel-for-pixel screen dump, so the size of the image depends on the resolution. At 300 d.p.i., the image is approximately the size of a large postage stamp.

Configuring Display Parameters

Item 6 on the HARDWARE CONFIGURATION MENU, "Configure Display Parameters" has two functions: "Change SCREEN COLORS," and "Change GRAPH Window." The first option, obviously, allows you to select the colors used for the various text messages and graphic

elements displayed by the program. Of course, if you are using a display option that only supports two colors (e.g., the IBM Color Graphics Adapter or Hercules Monochrome Graphics) this item will not allow you to select different colors for the graphic elements, but it will allow you to select different attributes (underline, high-intensity, reverse-video, etc.) for the different classes of text messages. Use the arrow keys to select the items that you wish to modify, and use the

F

and

B

keys to step through the available color options. Press

D

if you wish to restore the default colors (the colors that were displayed when you started the program). Press

ESC

to exit the COLOR CONFIGURATION MENU and save your changes. When you configure FilterCAD for the first time, it is recommended that you select the colors for the text messages only. Delay changing the options for the graphic elements until you have had a chance to explore the program and see how the various graphic elements interact.

The second option under Configure DISPLAY Parameters, "Change GRAPH Window," allows you to modify the frequency and gain ranges of the filter frequency response graphs generated by FilterCAD, as well as the number of data points that will be plotted. Whereas most of the configuration settings can be set once and then forgotten, the parameters of the graph window may have to be modified regularly as you design different types of filters with different frequency ranges. Until you have explored the graphing features of FilterCAD, you should probably leave the default parameters of the graph window unmodified.

WHAT IS A FILTER?

A filter is a circuit that selectively passes a certain range of the frequencies present at its input to its output, while blocking (attenuating) other frequencies. Filters are normally described in terms of the frequencies that they pass.

Most filters conform to one of four common types. Low-pass filters pass all frequencies below a specified frequency (called the cutoff frequency) and progressively attenuate frequencies above the cutoff frequency. High-pass filters do exactly the opposite; they pass frequencies above the cutoff frequency while progressively attenuating frequencies below the cutoff frequency. Bandpass filters pass a band of frequencies around a specified center frequency, attenuating frequencies above and below. Notch or bandstop filters attenuate the frequencies around the center frequency, passing frequencies above and below. The four basic filter types are illustrated in Figures 1.1–1.4. There are also allpass filters, which, not surprisingly, pass all of the frequencies present at their input.¹ In addition, it is possible to create filters with more complex responses which are not easily categorized.

The range of frequencies that a filter passes is known, logically enough, as its “passband.” The range of frequencies that a filter attenuates is known as its “stopband.” Between the passband and stopband is the “transition region.” An ideal filter might be expected to pass all of the frequencies in its passband without modification while infinitely attenuating frequencies in its stopband. Such a response is shown in Figure 1.5. Regrettably, real-world filters do not meet these imaginary specifications. Different types of filters have different characteristics, less-than-infinite rates of attenuation vs. frequency in the

Note 1: While allpass filters don't affect the relative amplitudes of signals with different frequencies, they do selectively affect the phase of different frequencies. This characteristic can be used to correct for phase shifts introduced by other devices, including other types of filters. FilterCAD cannot synthesize allpass filters.

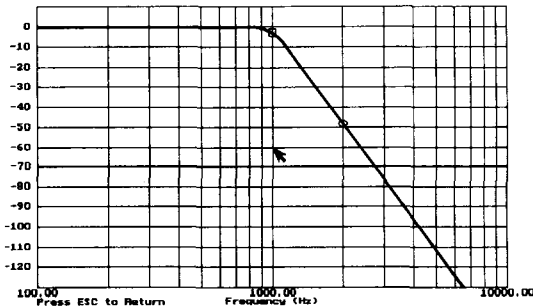


Figure 1.1. Lowpass Response

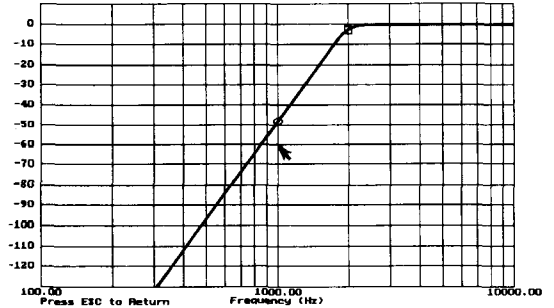


Figure 1.2. Highpass Response

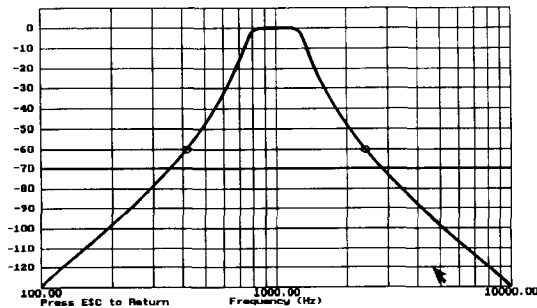


Figure 1.3. Bandpass Response

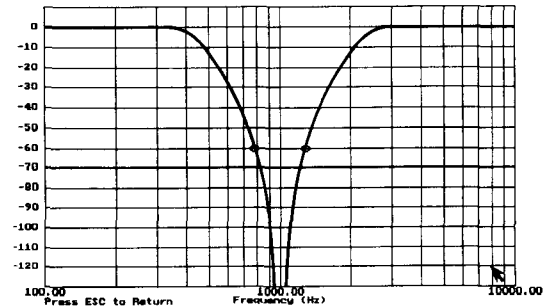


Figure 1.4. Notch Response

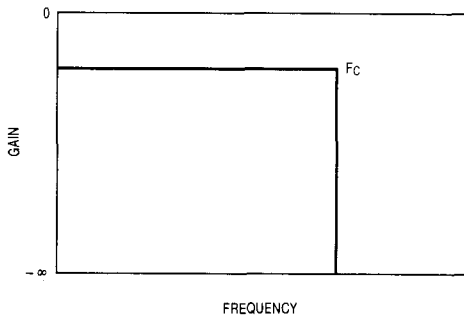


Figure 1.5. Ideal Lowpass Response

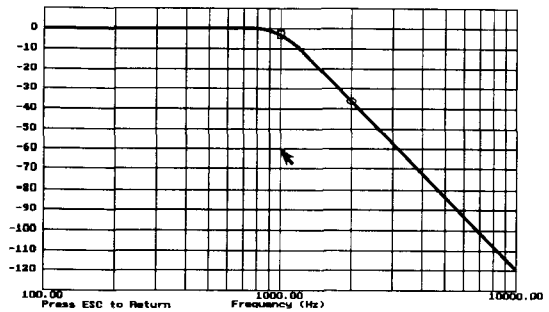


Figure 1.6. 6th Order Butterworth Lowpass Response

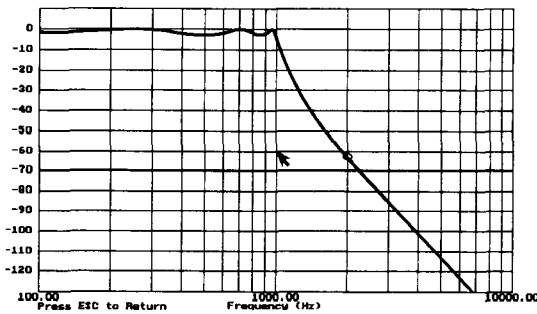


Figure 1.7. 6th Order Chebyshev Lowpass Response

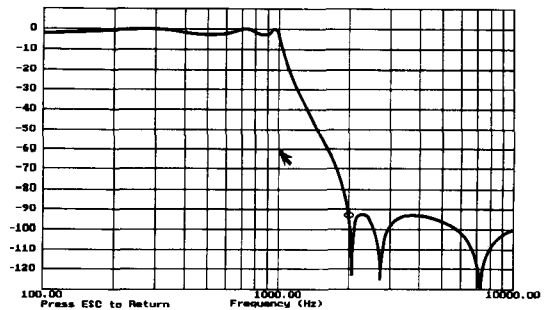


Figure 1.8. 6th Order Elliptic Lowpass Response

transition region. In other words, the amplitude response of a given filter has a characteristic slope. Frequencies in the passband may also be modified, either in amplitude ("ripple") or in phase. Real-world filters all represent compromises: steepness of slope, ripple, and phase shift (plus, of course, cost and size).

FilterCAD permits the design of filters with one of three response characteristics (plus custom responses). These three response types, which are known as "Butterworth," "Chebyshev," and "Elliptic," represent three different compromises among the previously described characteristics. Butterworth filters (Figure 1.6) have the optimum flatness in the passband, but have a slope that rolls off more gradually after the cutoff frequency than the other two types. Chebyshev filters (Figure 1.7) can have a steeper initial roll off than Butterworths, but at the expense of more than 0.4dB of ripple in the passband. Ellip-

tic filters (Figure 1.8) have the steepest initial roll off of all, but exhibit ripple in both the passband and the stopband. Elliptic filters have higher Q 's which may (if not carefully implemented) translate to a noisier filter. These high Q 's have made elliptic filters difficult to implement with active RC filters because of the increased stability and center frequency accuracy requirements. Elliptic filters can be implemented with SCF's due to their inherently better stabilities and center frequency accuracies when compared to active RC filters. Chebyshev and elliptic designs can achieve greater stopband attenuation for a given number of 2nd order sections than can Butterworths.

Filters are typically built up from basic building blocks known as 1st order and 2nd order sections. Each LTC filter contains circuitry which, together with an external clock and a few resistors, closely approximates 2nd order filter functions. These are tabulated in the frequency domain.

- 1. Bandpass function:** available at the bandpass output pin, refer to Figure 1.9.

$$G(s) = H_{OBP} \frac{s\omega_0/Q}{s^2 + (s\omega_0/Q) + \omega_0^2}$$

H_{OBP} = Gain at $\omega = \omega_0$

$f_0 = \omega_0/2\pi$; f_0 is the center frequency of the complex pole pair. At this frequency, the phase shift between input and output is -180° .

Q = Quality factor of the complex pole pair. It is the ratio of f_0 to the -3dB bandwidth of the 2nd order bandpass function. The Q is always measured at the filter BP output.

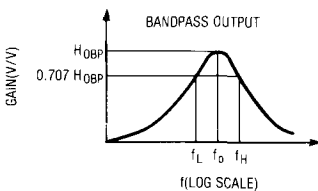
- 2. Lowpass function:** available at the LP output pin, refer to Figure 1.10.

$$G(s) = H_{OLP} \frac{\omega_0^2}{s^2 + s(\omega_0/Q) + \omega_0^2}$$

H_{OLP} = DC gain of the LP output.

- 3. Highpass function:** available only in mode 3 at the HP output pin, refer to Figure 1.11.

$$G(s) = H_{OHP} \frac{s^2}{s^2 + s(\omega_0/Q) + \omega_0^2}$$

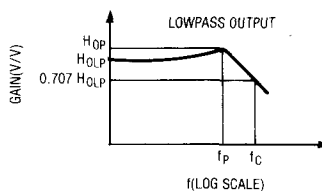


$$Q = \frac{f_0}{f_H - f_L}; f_0 = \sqrt{f_L f_H}$$

$$f_L = f_0 \left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1} \right)$$

$$f_H = f_0 \left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1} \right)$$

Figure 1.9. 2nd Order Bandpass Section

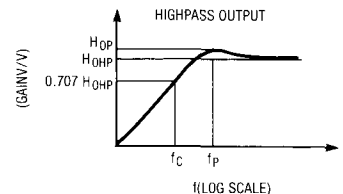


$$f_c = f_0 \times \sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}$$

$$f_p = f_0 \sqrt{1 - \frac{1}{2Q^2}}$$

$$H_{OP} = H_{OLP} \times \frac{1}{Q \sqrt{1 - \frac{1}{4Q^2}}}$$

Figure 1.10. 2nd Order Lowpass Section



$$f_c = f_0 \times \left[\sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}} \right]^{-1}$$

$$f_p = f_0 \times \left[\sqrt{1 - \frac{1}{2Q^2}} \right]^{-1}$$

$$H_{OP} = H_{OHP} \times \frac{1}{Q \sqrt{1 - \frac{1}{4Q^2}}}$$

Figure 1.11. 2nd Order Highpass Section

H_{OHP} = gain of the HP output for $f \rightarrow \frac{f_{CLK}}{2}$

- 4. Notch function:** available at the N output for several modes of operation.

$$G(s) = (H_{ON2}) \frac{(s^2 + \omega_n^2)}{s^2 + s(\omega_0/Q) + \omega_0^2}$$

H_{ON2} = gain of the notch output for $f \rightarrow \frac{f_{CLK}}{2}$

H_{ON1} = gain of the notch output for $f \rightarrow 0$

$f_n = \omega_n/2\pi$; f_n is the frequency of the notch occurrence.

These sections are cascaded (the output of one section fed to the input of the next) to produce higher-order filters which have steeper slopes. Filters are described as being of a certain "order," which corresponds to the number and type of cascaded sections they comprise. For example, an 8th order filter would require four cascaded 2nd order sections, whereas a 5th order filter would require two 2nd order sections and one 1st order section. (The order of a filter also corresponds its number of poles, but an explanation of poles is outside the scope of this manual.)

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PART 2—THE BASIC STEPS

Application Note 38

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STEP ONE, THE BASIC DESIGN

The first item on FilterCAD's MAIN MENU is "DESIGN Filter." To access the DESIGN Filter screen, press

1

On the DESIGN Filter screen, you make several basic decisions about the type of filter you're going to design. First, you must select your basic filter type (lowpass, highpass, bandpass, or notch). Press the

Spacebar

to step through the options. When the filter type that you want is displayed, press

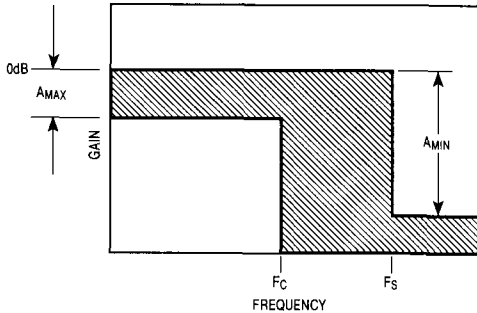


Figure 2.1. Lowpass Design Parameters: A_{MAX} = Maximum Passband Ripple, F_C = Corner Frequency, F_S = Stopband Frequency, A_{MIN} = Stopband Attenuation

[Enter]

Next, you must select the type of response characteristic you want (Butterworth, Chebyshev, Elliptic, or Custom). Again, use the

Spacebar

to step through the options and press

[Enter]

when the response type you want is displayed.

Next, you will enter the most important parameters for your filter. Exactly what these parameters will be depends on the type of filter you have chosen. If you have selected

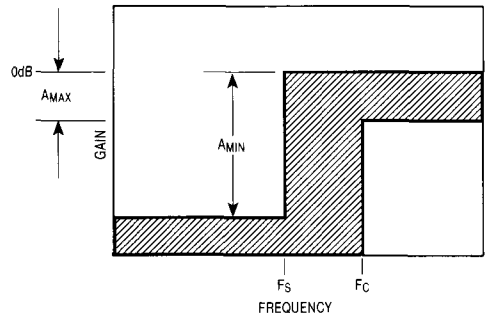


Figure 2.2. Highpass Design Parameters: A_{MAX} = Maximum Passband Ripple, F_C = Corner Frequency, F_S = Stopband Frequency, A_{MIN} = Stopband Attenuation

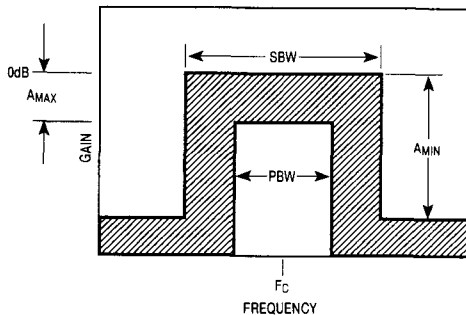


Figure 2.3. Bandpass Design Parameters: A_{MAX} = Maximum Passband Ripple, F_C = Center Frequency, PBW = Pass Bandwidth, SBW = Stop Bandwidth, A_{MIN} = Stopband Attenuation

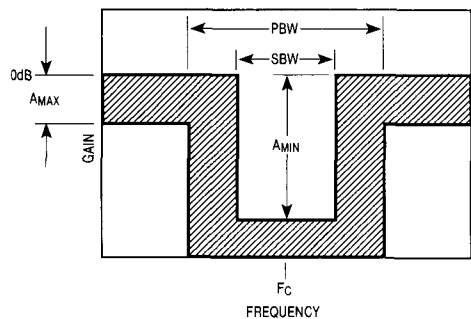


Figure 2.4. Notch Design Parameters: A_{MAX} = Maximum Passband Ripple, F_C = Center Frequency, PBW = Pass Bandwidth, SBW = Stop Bandwidth, A_{MIN} = Stopband Attenuation

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lowpass or highpass, you must enter the maximum passband ripple, in dB (must be greater than zero, or, in the case of Butterworth response, must be 3dB); the stopband attenuation, in dB; the corner frequency (also known as the cutoff frequency), in Hz; and the stopband frequency. If you chose a bandpass or notch filter, you must enter the maximum passband ripple and the stopband attenuation, followed by the center frequency, in Hz; the pass bandwidth, in Hz; and the stop bandwidth, in Hz. (The meanings of these various parameters in the different design contexts are illustrated in Figures 2.1-2.4.) If you chose a custom response, you're in an entirely different ball game, which will be described later.

Type in the parameters for your chosen filter, pressing

[Enter]

after each parameter. If you want to go back and alter one of the parameters you have previously entered, use the

Up-Arrow

and

Down-Arrow

keys to move to the appropriate location and retype the parameter. When you have entered all of the correct parameters, move the cursor to the last parameter in the list and press

[Enter]

FilterCAD will now calculate and display additional parameters of the filter you have designed, including its order, actual stopband attenuation, and gain, and will display a list of the 2nd order and 1st order sections needed to realize the design, along with their F_0 , Q , and F_n values (as appropriate). These numbers will be used later to implement your filter design and calculate resistor values.

FilterCAD will, in many cases, prevent you from entering inappropriate values. For instance, in the case of a low-pass filter, the program will not permit you to enter a stopband frequency that is lower than the corner frequency. Similarly, in the case of a highpass filter, the stopband frequency must be lower than the corner frequency. In addition, you cannot enter a maximum passband ripple value that is greater than the stopband attenuation, nor can you enter a set of values that will lead to a filter of an order greater than 28.

Custom Filters

The custom-response option on the DESIGN screen can be used in two ways. It can be used to modify filter designs created by the method previously described, or it can be used to create filters with custom responses from scratch, by specifying a normalization value and manually entering the desired F_0 , Q , and F_n values for the necessary 2nd order and 1st order sections. To edit the response of a filter that has already been designed, press

ESC

to exit the DESIGN screen, then press

1

to re-enter the DESIGN screen. Move the cursor to "FILTER RESPONSE" and use the

Spacebar

to select "CUSTOM." You can now edit the F_0 , Q , and F_n values for the 2nd order and 1st order sections in the window at the bottom of the screen. When you customize an existing design, the normalization frequency is automatically set to the previously-specified corner/center frequency. It can, however, be edited by the user.

To design a custom filter from scratch, simply select "CUSTOM" as your response type upon first entering the DESIGN screen, then type in the appropriate F_0 , Q , and F_n values for the desired response. By default, the normalization value for custom filters is 1Hz. Once you have entered your values, you can change the normalization frequency to any desired value and FilterCAD will scale the F_0 , and F_n frequencies accordingly. To change the normalization frequency, press

N

type in the new value, and press

[Enter]

By alternately graphing the resulting response and modifying the F_0 , Q , and F_n values, almost any kind of response shape can be achieved by successive approximations.

It should be understood that true custom filter design is the province of a small number of experts. If you have a

“feel” for the type of pole and Q values that produce a particular response, then FilterCAD will allow you to design by this “seat of the pants” method. If you lack such erudition, however, it is beyond the scope of the program or this manual to supply it. Nevertheless, novice designers can make productive use of FilterCAD’s custom-response feature by entering design parameters from published tables. An example of this technique will be found in the following section.

STEP TWO, GRAPHING FILTER RESPONSE

After you have designed your filter, the next step is item two on the MAIN MENU, GRAPH Filter Response. You can graph the amplitude, phase, and/or group-delay characteristics of your filter, and you can plot your graph on either a linear or logarithmic scale. The graph also highlights the 3dB-down point(s) (for Butterworth filters only) and the point(s) where the calculated attenuation is achieved. An additional option on the Graph Menu is called “Reduced View.” This option displays a reduced view of your graph in a window in the upper right-hand corner of the full-sized graph. This feature is useful in conjunction with the “Zoom” option.

Your graph can be displayed on the screen, output to a Hewlett-Packard 74XX or compatible plotter, or written to disk as an HPGL file or an ASCII text file for later output to a plotter or transfer to a presentation-graphics or desktop publishing program. The screen graph can also be dumped to an Epson dot-matrix or Hewlett-Packard ThinkJet or LaserJet Printer. Use the

Up-Arrow

and

Down-Arrow

keys to move through the list of graph parameters and press the

Spacebar

to step through the selections for each parameter that you wish to modify. When all of the graph parameters have been set correctly, press

[Enter]

to begin plotting the graph.

Plotting to the Screen

If you chose the screen as your output device, FilterCAD will immediately begin plotting the graph. Generating the graph is a calculation-intensive process. It is here that the speed and power of your CPU and the presence or absence of a math coprocessor will become evident. On a fast '386 system with a math coprocessor, the graph will be generated in a matter of seconds. On a PC/XT-class machine, with an 8088 processor and no math coprocessor, you can easily make and consume a cup of coffee, if not a light lunch, while waiting for the graph of a complex response to be plotted. Note, however, that the speed of calculation and plotting can be increased by reducing the number of data points to be plotted. To modify this parameter, use the “Change GRAPH Window” option, found under item 6, “Configure DISPLAY Parameters,” on the Configuration Menu. The number of points can range from 50 to 500. Of course, choosing a smaller number of points will result in a coarser graph, but this may be an acceptable trade-off for quicker plotting.

The Zoom Feature — When you display the graph on the screen, you have the additional option of magnifying or “zooming in” on areas of the graph that are of particular interest. (Before using the zoom feature, it is a good idea to enable the “Reduced View” option on the graph menu. When you zoom in, the area of the zoom will be indicated by a box on the reduced view of the full-sized graph.) Note the arrow in the lower right-hand corner of the graph. This arrow can be used to select the region of the graph to zoom in on. It can also be used to pinpoint the frequency and gain values of any given point on the graph. (These values are displayed at the upper right-hand corner of the screen.) The location of the arrow is controlled by the arrow keys (the cursor control keys) on the numeric key pad. The arrow can move in either fine or coarse increments. To select coarse movement, press the

+

key. To select fine movement, press the

-

key. Move the arrow to one corner of the area that you wish to magnify, and press

[Enter]

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Next, move the arrow to the opposite corner of the area of interest. As you move the arrow, you will see a box expand to enclose the area to be magnified. If you want to relocate the box, you must press

ESC

and restart the selection process. When the box encloses the desired area, press

[Enter]

and the screen will be redrawn and a new graph will be plotted within the selected range. Note that the program actually calculates new points as appropriate for the higher precision of the magnified section.

It is possible to zoom in repeatedly to magnify progressively smaller areas of the graph. There is a limit to this process, but the available magnification is more than adequate for any practical purpose. If you want to output the magnified graph to the plotter or a disk file, you can do so. Just press

ESC

once to return to the GRAPH MENU screen, change the output device to plotter or disk, press

[Enter]

and then proceed with the plotting process as described later. To zoom out to the previous graph, press

L

(for Large). You can zoom out as many times in succession as you have zoomed in. Note, however, that for each successive zoom out the graph is recalculated and replotted. If you have done several successive zooms and you want to get back to the full-sized graph without the intermediate steps, it will be quicker to press

ESC

twice to return to the MAIN MENU, then re-enter the GRAPH screen.

Printing the Screen — If you have an Epson-FX compatible dot-matrix printer, a Hewlett-Packard ThinkJet, or a Hewlett-Packard LaserJet compatible laser printer, and

you have installed the appropriate print driver, you can dump your screen graph to your printer at any time by pressing

[Alt] P

This same feature can be used from the Device Screen (see the Implementation section) to print FilterCAD's mode diagrams. The screen-print routine will check to see whether your printer is connected and turned on, and will warn you if it is not. If your printer is connected and turned on, but off line, FilterCAD will put it on line and begin printing. Once printing begins, however, FilterCAD does no error checking, so turning off your printer or taking it off line to stop printing may cause the program to "hang up."

Plotting to a Plotter, HPGL File, or Text File

If you choose to send your graph to a plotter or to an HPGL disk file, you will first be shown the PLOTTER STATUS MENU. First, you will be asked "GENERATE CHART (Y/N)." You are not being asked here whether you want to plot a graph, but whether, when you plot to disk or plotter, you want to draw the grid or only plot the data. This may seem like an absurd choice, but it is here for a reason. If you are plotting to a plotter, you could overlay the response graphs of several different filter designs on one sheet of paper for comparison. If you drew the grid every time, you would end up with a mess. This option allows you to draw the grid on the first pass, then plot only the data on successive passes. This same process can be used, albeit with slightly more effort, when plotting to a disk file. The procedure here is to plot two (or more) separate files, the first with the grid turned on, and the remainder with the grid turned off. Then exit FilterCAD and use the DOS COPY command to concatenate the files. For example, if you wanted to concatenate three HPGL files named SOURCE1, SOURCE2, and SOURCE3 into a single file called TARGET, you would use the following syntax:

```
COPY/B SOURCE1 + SOURCE2 + SOURCE3  
TARGET [Enter]
```

After you have answered the question

GENERATE CHART (Y/N)

the remainder of the PLOTTER STATUS MENU will be displayed. Here, you can select the dimensions of your graph,

the pen colors to be used, and whether to print the design parameters below the graph. When you have determined that the plotter options are set correctly, press

P

to begin plotting. If you wish to exit the PLOTTER STATUS MENU without plotting, press

ESC

You can also plot your graph as a set of data points for gain, phase and group delay plotted to disk in ASCII text format. Select

DISK/TEXT

as the output device. Then select which parameters to plot and press

[Enter]

You will then be prompted for a file name into which the data will be placed. To plot onto a disk in drive "A" type

A: [YOUR FILE] [Enter]

These points may then be imported to a spreadsheet program, for example, for data manipulation.

If your graph consists mostly of straight horizontal lines or slopes, this indicates that the frequency and amplitude ranges of the graph are probably not set appropriately for the particular filter you are graphing (e.g., a graph frequency range of 100Hz to 10,000Hz for a highpass filter with a corner frequency of 20Hz). To adjust the frequency and gain ranges of your graph, use the "Change GRAPH Window" option, found under item 6, "Configure DISPLAY Parameters," on the Configuration Menu.

IMPLEMENTING THE FILTER

The third item on the MAIN MENU, "IMPLEMENT Filter," is where we transform the numbers generated in step one into practical circuitry. There are several steps to this process.

Optimization

The first step is to optimize your filter for one of two characteristics.² You can optimize for lowest noise or lowest harmonic distortion. When you optimize for noise, the

cascaded sections are ordered in such a way as to produce the lowest output noise when the filter input is grounded. In the absence of any other, conflicting design criteria, this is the most obvious characteristic for optimization. When you optimize for harmonic distortion, the sections are cascaded so as to minimize the internal swings of the respective amplifiers, resulting in reduced harmonic distortion. *Note, however, that optimizing for harmonic distortion will result in the worst noise performance.*

The Optimization screen also allows you to select the ratio of the internal clock frequency to F_0 (50:1 or 100:1) and the clock frequency in Hz, and to turn automatic device selection on and off. It should be understood that the clock frequency ratio represents the state of a particular pin on the device, and does not *necessarily* correspond to the actual ratio of the clock frequency to F_0 . Thus, if you change the clock frequency to a value other than that automatically selected by FilterCAD, the frequency ratio *will not change accordingly*. Novice filter designers are advised to use the clock frequency selected by FilterCAD unless there is a compelling reason to do otherwise, and to leave automatic device selection "ON." Clock frequencies and frequency ratios are not arbitrary, but have a relationship to the corner or center frequency that depends upon the selected mode. For more information on clock frequencies, frequency ratios, and modes, consult LTC product data sheets.

When you have selected the characteristic for optimization and adjusted the other options to your satisfaction, move the cursor back to "OPTIMIZE FOR" and press

O

FilterCAD will respond by displaying the selected device and mode(s) and its rationale for selecting a particular cascade order. If you want to re-optimize for some other characteristic, press

O

again and repeat the process previously described.

Note 2: FilterCAD will not optimize custom filter designs, nor will it select the modes for such designs. This is just another indication that custom designs are the province of experienced designers.

Implementation

When you are satisfied with the optimization, press

I

to proceed with the implementation. This won't do anything obvious except to clear the window where the optimization information is displayed, so press

D

to view the selected device, cascade order, and modes. When the Device screen is first displayed, it will show detailed specifications of the selected part. To see the mode diagrams of the 2nd and 1st order sections that implement the design, press the

Down-Arrow

key to move the cursor through the cascade-order list on the left-hand side of the screen.

You will have probably observed that, on the implementation menu, this screen is entitled "Edit DEVICE/MODEs," and you can, in fact, manually edit both the device selection and the modes of the 2nd and 1st order sections. This capability, however, is one that the novice user would be best advised to ignore. If you manually edit the device selection or the modes, you are essentially ignoring the expertise that is built into the program in favor of your own judgement. Experienced designers may choose to do this under some circumstances, but if you want to get from a specification to a working design with the least time and effort, accept the device and modes that FilterCAD selects. To complete the implementation process, press

ESC

to exit the device screen, then press

R

to calculate the resistor values. You can calculate absolute values by pressing

A

or the nearest 1% tolerance values by pressing

P

There is one more option on the implementation menu that we have not yet examined, "Edit CASCADE ORDER." This option allows you to exchange poles and zeros among and edit the cascade order of the 2nd order sections that make up your filter. This represents one of the most arcane and esoteric aspects of filter design — even the experts are sometimes at a loss to explain the benefits to be gained by tweaking these parameters. So, once again, we must recommend that the novice leave this feature alone.³

SAVING YOUR FILTER DESIGN

Item 4 on the MAIN MENU, "SAVE Current Filter Design," allows you to save your design to disk. Press

4

to save your design. By default, a new file will be saved with the name "NONAME," while a file that was previously saved and loaded will be saved under its previous name. If you want to save the file under a different name, just type it in at the cursor position. Type the file name only, eight characters or fewer; do not type an extension. All files are saved with the extension .FDF (*Filter Design File*).

By default, the file will be stored in the current directory (the directory that was active when FilterCAD was started). This directory will be displayed at the top of the screen. If you want to save the file to a different directory, press

Home

then type in a new path. When the file name and path are correct, press

[Enter]

to save the file. If there is already a file on the disk with the name that you have selected, FilterCAD will ask whether you want to overwrite the file. Press

Y

to overwrite the file or press

N

to save the file under a different name.

Note 3: Of course, there is no harm in the novice experimenting with the advanced features of FilterCAD, provided he or she realizes that the results of such experiments will not necessarily be useful filter designs.

LOADING A FILTER DESIGN FILE

To load a Filter Design File that you have previously saved, select

5

on the main menu. The LOAD FILE MENU screen will display a directory of all of the .FDF files in the current directory. Use the cursor keys to move the pointer to the name of the file you want to load and press

[Enter]

If there are more .FDF files than can be displayed on the screen at one time, press the

PgDn

key to see additional files. If you want to load a file from a different directory, press

P

then type in the new path. You can also enter a mask to restrict the file names which will appear on the screen. This mask can consist of any of the characters that DOS allows for file names, including the DOS wildcards "*" and "?". By default, the mask is "*", allowing all file names to be displayed. To change the mask, press

M

then type in a new mask of up to eight characters. For example, if you named your .FDF files in such a way that the first two letters of the file name represented the filter type (LP for lowpass, HP for highpass, etc.), you could change the mask to LP* to display only the lowpass filter design files.

Note: If you attempt to load an .FDF file created with an earlier version of FilterCAD, the program will issue a warning and ask you whether you want to abort loading or proceed at your own risk. Differences between .FDF files from different versions of FilterCAD are minor, and you should be able to load and use earlier .FDF files without difficulty.

Caution: When you load a filter design file, FilterCAD DOES NOT prompt you to save any design currently in memory, so when a new file is loaded, any unsaved work in memory will be lost.

CONFIGURING FILTERCAD

Item 6 on the MAIN MENU, "CONFIGURE FilterCAD," is explained in Part 1, "Getting Started."

PRINTING A REPORT

Item 7 on the MAIN MENU, "SYSTEM Status/Reports," displays a varied collection of information on your system, such as the date and time, your DOS version, the presence or absence of a math coprocessor, and the status of your printer and communications ports. It also shows the state of progress of the current design, including the total design time. (Gosh, a 6th order Butterworth lowpass in 00:05:23, only five seconds shy of the record!) The main function of this screen, however, is to print a design report. This report will include all of the information about your filter available on the design, optimization and implementation screens, except for the mode diagrams. You can also print the gain, phase and group delay of your filter design by pressing

P

Note that if you have not completed the design process by implementing the design and calculating resistor values, the "REPORT AVAILABLE" line will say "PARTIAL." A partial report, lacking modes and resistor values, can be printed, but for a complete report you must implement and calculate resistor values.

AND NOW, A WORD FROM OUR SPONSOR

The eighth item on the MAIN MENU displays Linear Technology Corporation's address and phone, fax, and telex numbers, followed by a list of our other products.

QUITTING FILTERCAD

The ninth and final item on FilterCAD's MAIN MENU, "END FilterCAD," is self-explanatory. If you haven't saved your current design before attempting to exit the program, FilterCAD will ask you if you wish to do so. Press

Y

to exit the program or press

N

to remain in FilterCAD.

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PART 3—SOME PRACTICAL EXAMPLES

Application Note 38

Part 3— Some Practical Examples	3-1
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Now that we have examined the principal features of FilterCAD, let's walk through a few typical filter designs to get a better idea of how the program works.

A BUTTERWORTH LOWPASS EXAMPLE

First, we'll design a Butterworth lowpass filter, one of the most basic filter types. Load FilterCAD, if you haven't already done so, and press

1

to go to the design screen. Select lowpass as the design type and Butterworth as the response type. Now we have four additional parameters to enter. The passband ripple *must* be specified as 3dB; this places the cutoff frequency - 3dB down with respect to the filters DC gain. Should you desire a Butterworth response with other than 3dB passband ripple you can do so by going to the custom menu. Let's select an attenuation of 45dB, a corner frequency of 1000Hz, and a stopband frequency of 2000Hz. Press

[Enter]

after each parameter. When the last parameter is entered, FilterCAD will synthesize the response. We soon see that the result is an 8th order filter with an actual attenuation of 48.1442dB at 2000Hz. It is composed of four 2nd order lowpass sections, all with corner frequencies of 1000Hz and modest Q's. (Having the same corner frequency for all of the cascaded sections is a characteristic of Butterworth filters.) This is a good time to experiment with some of the filter's parameters to see how they affect the resulting design. Try increasing the attenuation or lowering the stopband frequency. You'll discover that any modification that results in a significantly steeper rolloff will increase the order of the filter proportionally. For instance, reducing the stopband frequency to 1500Hz changes results in a filter of order 13! If a very steep rolloff is required and some ripple in the passband is acceptable, a response type other than Butterworth would probably be preferable.

Next, we'll graph the amplitude and phase characteristics of our Butterworth lowpass filter. Press

ESC

to return to the MAIN MENU, then press

2

to go to the graph menu. We're going to output this graph to the screen, so press

[Enter]

to begin graphing immediately. In a few seconds or a few minutes, depending on the type of computer system you're using, you should see a graph very much like the one in Figure 3.1A. Amplitude (in dB's) is indicated on the left side of the graph and phase (in degrees) is indicated on the right side. (If you have your graph parameters set differently than FilterCAD's defaults, your graph may show less of the frequency and amplitude range than the figure. If you don't see a graph substantially like the one in Figure 3.1A, you may need to adjust the graph's ranges. Exit the graph screen, go the the MAIN MENU, and select 6, CONFIGURE FilterCAD. Next, select item 6, "Configure DISPLAY Parameters," followed by item 2, "Change GRAPH Window.")

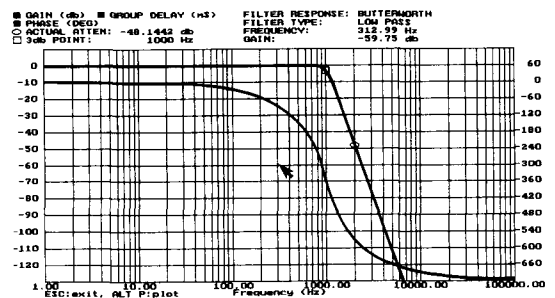


Figure 3.1A. Butterworth Lowpass Filter Response

Observe the characteristic amplitude and phase-response curves of the Butterworth response. (The amplitude curve is the one that begins at 0dB and begins to fall off sharply around 1000Hz — of course, if you have a color display you can make the amplitude and phase curves easily distinguishable by assigning them different colors.) The amplitude in the passband is extremely flat (you could magnify a small segment of the passband many times and still find no observable ripple), and the slope of the rolloff begins just before the corner frequency, reaching the 3dB down point (which, in a Butterworth response is synonymous with the corner frequency) at 1000Hz, and continues to rolloff at the same constant rate to the stopband and beyond. (In theory, the slope will continue to rolloff at this

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same rate all the way to an infinite attenuation at an infinite frequency.) The phase response begins at 0, slopes exponentially to near -360° as it approaches the corner frequency, then continues down until it asymptotes to -720° in the filter's stopband. Butterworth filters offer the most linear phase response of any type except the Bessel. Figure 3.1B shows the phase response of the Butterworth lowpass filter using a linear phase scale.

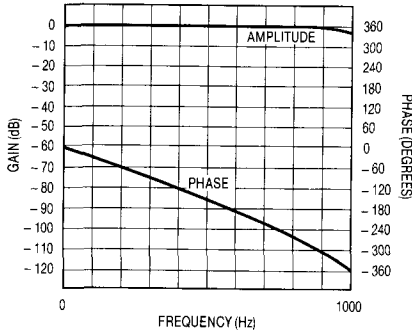


Figure 3.1B. Butterworth Lowpass Phase Response

Having graphed our filter's response, we will next go to the implementation screen to transform it into a practical design. Press

ESC

twice to exit the graph display, then press

3

to go to the implementation screen. The first step is to optimize. Lacking any other pressing need, we'll optimize for noise (the default optimization strategy). We'll use a clock frequency ratio of 50:1 and we'll leave auto device selection ON. Press

O

to execute optimization. FilterCAD selects the LTC1164 and indicates that the Q's have been intermixed for the lowest noise. Next, press

I

for implement and then

D

to display the device screen. This screen shows detailed specs of the LTC1164, and, in the window on the left-hand

side of the screen, indicates that **all four of the 2nd order sections in the design will use mode 1**. Press the

Down-Arrow

key and you'll see a diagram of a mode 1 network like the one in Figure 3.2 in place of the LTC1164 specs. Press the

Down-Arrow

three more times, and you'll see three more examples of the same network, differing only in their Q values. This configuration would be fine except for one thing: the LTC1164 has four 2nd order sections, but the fourth lacks an accessible summing node, and therefore cannot be configured in mode 1. You must manually change the mode of the last stage to mode 3. This illustrates the limitations of the present version of FilterCAD.

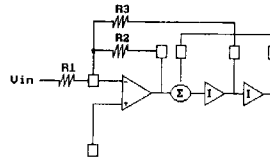


Figure 3.2. Mode 1 Network

Each mode 1 section requires three resistors, and the final mode 3 section requires four. To calculate the resistor values, press

ESC

to exit the Device screen, then press

R

On pressing

P

to select 1% tolerance resistors, FilterCAD displays the values in Table 3.1. This completes the implementation of our Butterworth lowpass example.

Table 3.1. Resistors for Butterworth Lowpass Example

STAGE	R1	R2	R3	R4
1	16.50k	15.50k	10.00k	
2	10.00k	10.00k	25.50k	
3	11.00k	11.00k	10.00k	
4	20.50k	20.50k	10.00k	20.50k

A CHEBYSHEV BANDPASS EXAMPLE

For our next example, we'll design a bandpass filter with a Chebyshev response. (We'll assume you know your way around the program reasonably well at this point, so we'll dispense with telling you specific keys to press unless we introduce a new feature.) For our Chebyshev design, we'll select a maximum passband ripple of 0.05dB, an attenuation of 50dB, and a center frequency of 5000Hz. We'll specify a pass bandwidth of 600Hz and a stop bandwidth of 3000Hz. This results in another 8th order filter, consisting of four 2nd order bandpass sections, with their corner frequencies staggered around 5000Hz and moderate Q's illustrated in Table 3.2.⁴

Table 3.2. F_o , Q, and F_n Values for 8th Order Chebyshev Bandpass

STAGE	F_o	Q	F_n
1	4657.8615	27.3474	0.0000
2	5367.2699	27.3474	INFINITE
3	4855.1190	11.3041	0.0000
4	5149.2043	11.3041	INFINITE

The Q's of the sections have been kept within reasonable limits by specifying the very low minimum passband ripple of 0.05dB. That this should be the case may not be obvious until you consider that the passband ripple consists of the product of the resonant peaks of the 2nd order sections. By keeping the passband ripple to a minimum, the Q's of the individual sections are reduced proportionally. You can verify this fact by changing the passband ripple to a higher value and observing the effect on the Q's of the 2nd order sections.

Next we'll graph the response of our design. The result appears in Figure 3.3. (We have reset the frequency range of the graph to focus on the area of interest.) Observe that the slope of the amplitude response rolls off quite steeply in the transition region and that the slopes become more gradual well into the stopband. In other words, the slope is not constant. This is a characteristic of Chebyshev filters. The characteristic passband ripple is not observable at the current scale, but we can see it by zooming in on the passband.

Note 4: It is possible to design a bandpass filter from a mixture of highpass and lowpass or highpass, lowpass, and bandpass sections, but FilterCAD will not do this. When you specify a particular filter type, all of the sections used to realize the design will be of that same type.

To zoom, first press

+

to select coarse motion, then use the arrow keys on the cursor keypad to move the arrow to one corner of the rectangle you want to zoom in on (just outside the passband), then press

[Enter]

Now move the arrow again and you'll see a box expand to enclose the area to be magnified. When the box encloses the passband, press

[Enter]

again and the new graph will be calculated and plotted. It may require two or three consecutive zooms, but eventually you'll get a closeup of the passband that shows the 0.05dB ripple quite clearly, as in Figure 3.4. (Note that in this figure, the graph style has been reset to "linear.") To return to the full-scale graph, press

L

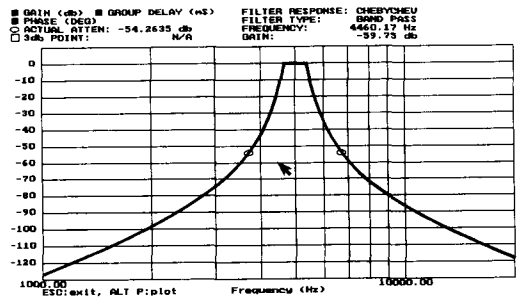


Figure 3.3. Chebyshev Bandpass Response

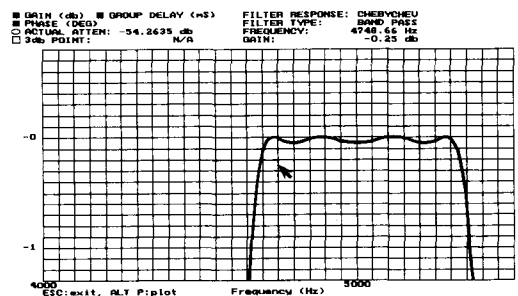


Figure 3.4. Closeup of Passband

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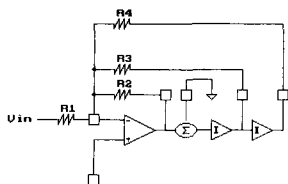


Figure 3.5A. Mode 3 Network

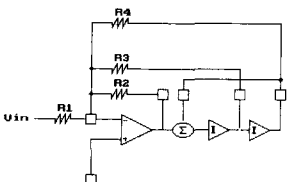


Figure 3.5B. Mode 2 Network

Now, we'll implement our design, optimizing, as before, for lowest noise. We will select clock to F_0 ratio equal to 50:1 and clock frequency equal to 250,000Hz. Once again the LTC1164 is selected and the Q's of the sections are intermixed for the lowest noise. This time mode 3 has been chosen for the first two stages (where $F_0 < F_{CLK}/50$) and mode 2 has been selected for the remaining two stages (where $F_0 > F_{CLK}/50$). The overall gain of 27.29dB has been evenly distributed among stages two through four and the gain of stage one has been set to 1 for improved dynamics. When we view the Device screen, we'll see the specs of the LTC1164 and two diagrams of the mode 3 network followed by two diagrams of the mode 2 network with different F_0 , Q, and F_n values (see Figures 3.5A and 3.5B). Calculating the 1% resistor values produces the results in Table 3.3.

Table 3.3. Resistors for Chebyshev Bandpass Example

STAGE	R1	R2	R3	R4
1	10.20k	10.00k	68.10k	10.70k
2	10.00k	12.70k	147.0k	14.70k
3	10.00k	154.0k	3.160M	1.000M
4	10.00k	12.40k	130.0k	205.0k

TWO ELLIPTIC EXAMPLES

For our next example, we will design a lowpass filter with an elliptic response. We'll specify a maximum passband ripple of 0.1dB, an attenuation of 60dB, a corner frequency

of 1000Hz, and a stopband frequency of 1300Hz. In the case of an elliptic response, we have one additional question to answer before the response is synthesized. When we have entered the other parameters, FilterCAD asks "Remove highest F_n ?" (Y/N). This question requires a bit of explanation. An elliptic filter creates notches by summing the highpass and lowpass outputs of 2nd order stages. To create a notch from the last in a series of cascaded 2nd order stages, an external op amp will be required to sum the highpass and lowpass outputs. Removing the last notch from the series eliminates the need for the external op amp, but does change the response slightly, as we will see.

Note: The last notch can be removed only from an even-order elliptic filter. If you are synthesizing an elliptic response for the first time and you are uncertain what order of response will result, answer "NO" when asked if you want to remove the last notch. If an even-order response results you can go back and remove the last notch if you wish.

For comparison, we will synthesize both responses. The F_0 , Q, and F_n values for both designs (both are 8th order) are shown in Table 3.4. Observe that the removal of the highest F_n produces slight variations in all of the other values.

Table 3.4. F_0 , Q, and F_n Values for Lowpass Elliptic Examples

STAGE	F_0	Q	F_n
Highest F_n Not Removed			
1	478.1819	0.6059	5442.3255
2	747.3747	1.3988	2032.7089
3	939.2728	3.5399	1472.2588
4	1022.0167	13.3902	1315.9606
Highest F_n Removed			
1	466.0818	0.5905	INFINITE
2	723.8783	1.3544	2153.9833
3	933.1712	3.5608	1503.2381
4	1022.0052	13.6310	1333.1141

When we graph our two elliptic examples, (Figures 3.6A and 3.6B) we see that the response of the filter without the highest F_n removed shows four notches in the stopband and a gradual slope after the last notch, whereas the filter with the highest F_n removed exhibits only three notches

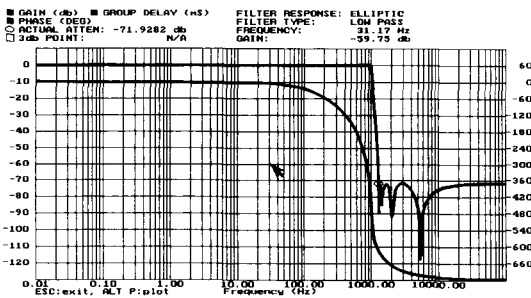


Figure 3.6A. Lowpass Elliptic, Highest F_n Not Removed

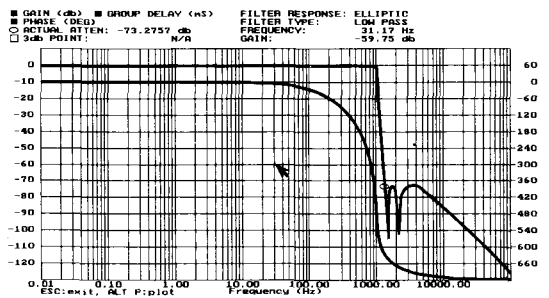


Figure 3.6B. Lowpass Elliptic, Highest F_n Removed

followed by a steeper slope. Both examples have the steep initial rolloff and extremely non-linear phase response in the vicinity of the corner frequency that are essential characteristics of the elliptic response. If your only goal is stopband attenuation greater than 60dB, either implementation would be satisfactory, and the version with the highest F_n removed would probably be selected due to its lower parts count.

When we optimize our two elliptic filters for noise, FilterCAD selects the LTC1164 and specifies mode 3A for all four stages. Mode 3A is the standard mode for elliptic and notch filters, as it sums the highpass and lowpass outputs of the 2nd order sections as described previously. When we go to the Device screen, we see four mode 3A diagrams, each showing the external op amp, as in Figure 3.7. In practice, this external summing amp is not needed in every case. When cascading sections, the highpass and lowpass outputs of the previous section can be summed into the inverting input of the next section, an external

summing amp being required only for the last section. If the highest F_n is removed, external op amps can be dispensed with entirely.

Calculating 1% resistor values (for clock to F_0 ratio 50:1, clock frequency equals 50,000Hz) for our two elliptic variations yields the results in Table 3.5. RH and RL are the resistors which sum the highpass and lowpass outputs of the successive stages, and RG is the resistor that sets the gain of the external op amp. Therefore, there is one fewer

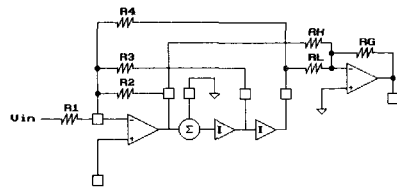


Figure 3.7. Mode 3A Network

Table 3.5. Resistor Values for Lowpass Elliptic Examples

STAGE	R1	R2	R3	R4	RG	RH	RL
Highest F_n Not Removed							
1	24.90k	10.00k	17.40k	17.80k		237.0k	57.60k
2		10.50k	73.20k	10.00k		21.50k	12.70k
3		10.00k	30.90k	11.30k		21.50k	10.00k
4		19.60k	24.30k	86.60k	10.20k	294.0k	10.00k
Highest F_n Removed							
1	26.10k	10.00k	17.40k	19.10k		261.0k	56.20k
2		10.50k	75.00k	10.00k		23.20k	13.00k
3		10.00k	31.60k	11.50k		22.60k	10.00k
4		18.70k	23.20k	86.60k			

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RH/RL pair in the version with the last F_n removed, and RG is found only in the last stage of the first example. Also, R1, the resistor connected to the inverting input of the input amplifier, is used only for the first stage. **The RH/RL pair takes the place of R1 in subsequent stages.**

A CUSTOM EXAMPLE

For a simple example of how the custom design option works, we'll design a 6th order lowpass Bessel filter by manually entering pole and Q values. When you set the response on the Design screen to "Custom" and press

[Enter]

the usual parameter-entry stage is bypassed and you go directly to the F_o , Q, and F_n section, where you can enter any values you want. We'll use values from Table 3.6, for a filter normalized to $-3\text{dB} = 1\text{Hz}$. The published table from which these values were taken didn't mention F_n values at all, so when the author typed them in initially, he left the F_n values as he found them, as zeros. The result was not the desired lowpass filter, but its highpass mirror image. This shows the kind of trap that awaits the unwary.

Once the values have been entered, they can be re-normalized for any desired corner frequency. Just press

[Enter]

In this case we will re-normalize to 1000Hz, which simply multiplies the F_o values in the table by 1000.

Table 3.6. F_o , Q, and F_n Values for 6th Order Lowpass Bessel, Normalized for 1Hz

STAGE	F_o	Q	F_n
1	1.606	0.510	INFINITY
2	1.691	0.611	INFINITY
3	1.907	1.023	INFINITY

Looking at the graph of the resulting response (Figure 3.8), we see the characteristic Bessel response, with its droopy passband and very gradual initial rolloff. When we go to the implementation stage, the process is a little different than we are accustomed to. FilterCAD won't optimize a custom design, nor will it specify the mode(s). It will, however, select the device, (the envelope please...) the LTC1164. Now we need to go to the device screen and manually select the mode for each of the three 2nd order sections. We will select mode 3 for all sections, because the three sections each have different corner frequencies, and mode 3 provides for independent tuning of the individual sections by means of the ratio $R2/R4$. (We've seen what the mode 3 network looks like before, so we won't duplicate it here.) Having selected the mode, we can calculate resistor values. The results are shown in Table 3.7.

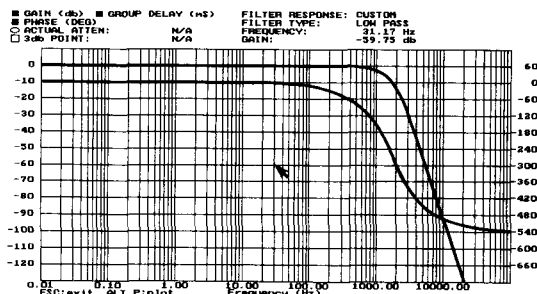


Figure 3.8. 6th Order Lowpass Bessel Response

Table 3.7. Resistors for 6th Order Bessel Lowpass Example

STAGE	R1	R2	R3	R4
1	13.00k	33.20k	10.00k	13.00k
2	10.50k	29.40k	10.00k	10.50k
3	10.00k	36.50k	17.40k	10.00k

PART 4—ADVANCED APPLICATIONS

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EDITING CASCADE ORDER

As stated earlier in this manual, optimizing performance by editing cascade order and/or swapping pole and Q values is among the most arcane and esoteric aspects of active filter design. Although certain aspects of this process are understood by experienced designers, current knowledge is not sufficiently systematic to guarantee the success of algorithmic optimization. Hence the need for manual editing. In the discussion that follows, we will consider briefly the underlying principals of optimization for minimizing noise or harmonic distortion. This will be followed by some concrete examples illustrating the effect of these principles on real-world filter designs. It should be emphasized that the fine-tuning process described here may or may not be necessary for a particular application. If you need assistance in maximizing performance of a filter using LTC parts, do not hesitate to contact our applications department for advice and counsel.

Optimizing for Noise

The key to noise optimization is the concept of band limiting. Band limiting of noise is achieved by placing the 2nd order section with the lowest Q and lowest F_0 (in the case of a lowpass filter) *last* in the cascade order. To understand why this works, we must consider the response shapes of 2nd order sections. A 2nd order section with a low Q begins rolling off before F_0 (Figure 4.1). The lower the Q, the farther into the passband the rolloff begins. 2nd order sections with high Q's, on the other hand, have reso-

nance peaks centered at F_0 (Figure 4.2). The higher the Q, the higher the resulting peak. The most noise in cascaded filters is contributed by the stages with the highest Q's, the noise being greatest in the vicinity of the resonance peaks. By placing the stage with the lowest Q and the lowest F_0 last in the cascade order, we place much of the noise contributed by previous stages *outside* the passband of this final stage, resulting in a reduction of the overall noise. Also, because the final stage is the lowest in Q, it contributes relatively little noise of its own. This technique allows the realization of selective elliptic lowpass filters with acceptable noise levels.

Optimizing for Harmonic Distortion

Distortion in switched-capacitor filters can be caused by three factors. First, distortion can be produced by loading. The CMOS amplifiers that are used in LTC switched-capacitor filter devices are not suited to driving heavy loads. For best results, no node should see an impedance of less than 10k Ω , and you will observe that FilterCAD never calculates a resistor value below this limit. Further, it may be desirable, when trying to obtain optimal distortion performance, to scale up resistor values calculated by FilterCAD by a factor of two or three to minimize loading.

The second factor that affects distortion performance is the clock frequency. Each LTC switched capacitor filter device has an optimum clock frequency range. Using a clock frequency significantly above the optimal range will result in increased distortion. For information on acceptable

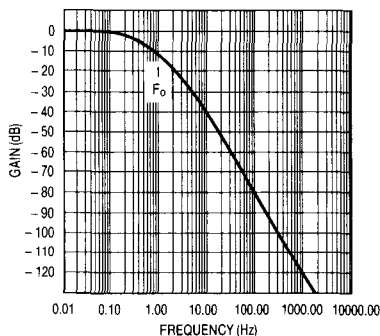


Figure 4.1. Low Q 2nd Order Lowpass Response

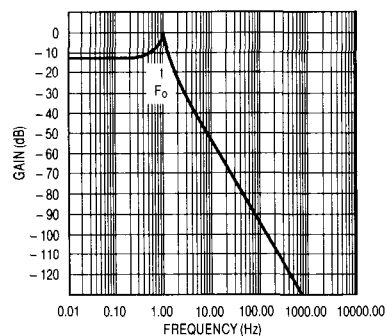


Figure 4.2. High Q 2nd Order Lowpass Response

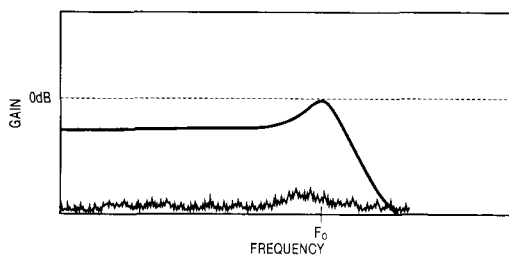
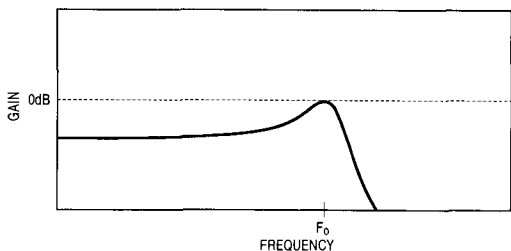
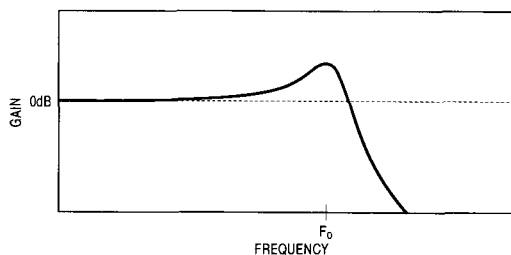
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clock frequency ranges, consult LTC data sheets and application notes. If you do not observe these two design factors, any attempt to optimize THD performance by editing cascading order will likely be wasted.

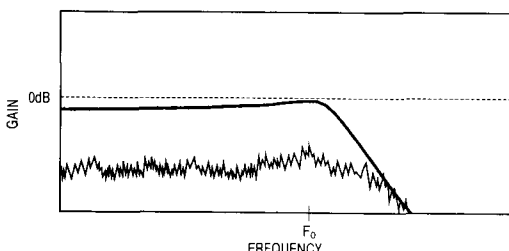
The third factor is distortion introduced by the non-linear effects of the internal op amps when they swing close to their rails.

Both the gain and the position of the highest Q section are significant factors in this process. As previously discussed, high Q 2nd order sections ($Q > 0.707$) have a resonance peak in the vicinity of F_0 . In order to maintain an overall gain of 1 for the circuit, and to minimize distortion, it is necessary to give high Q stages a **DC gain** of less than 1 and proportionally increase the gain of subsequent stages. (Note that FilterCAD automatically performs dynamic optimization for designs based exclusively on mode 3A, independent of the cascading order of the 2nd order sections.) If each stage were given a gain of 1, the overall gain for the circuit would, of course, be 1. However, when a high Q section has a gain of 1 at DC, the frequencies in the vicinity of F_0 will receive an additional boost

from the resonance peak, resulting in a gain greater than 1 for those frequencies (see Figure 4.3 and the LTC1060 data sheet). Depending on the strength of the input signal, the output from the high Q stage may saturate the following input stage, driving it into its non-linear region and thereby creating distortion. Setting the gain of the high Q stage so that the peak at F_0 does not exceed 0dB results in a DC gain of less than 1 for the stage. This has the effect of significantly attenuating most of the frequencies in the passband, thereby minimizing the excursions of the input amplifier. Although this strategy reduces harmonic distortion, it can create noise problems, because the noise generated by a 2nd order stage increases with Q. (As a rule of thumb, noise can be regarded as increasing at approximately the square root of Q.) When the output from the high Q stage is amplified by subsequent stages in order to bring the overall passband gain up to 1, its noise component is amplified proportionally (Figure 4.4). Thus, as we stated previously, THD optimization is inimical to noise optimization, so the “best” cascade is a compromise between the two.



HIGH Q, LOW GAIN SECTION



SUBSEQUENT SECTION WITH LOWER Q, HIGHER GAIN. NOISE FROM PREVIOUS SECTION IS BOOSTED.

Figure 4.3. DC Gain of 1 Results in Amplitude Greater than 0dB at F_0 ; DC Gain is Reduced, Attenuating Frequencies in the Passband

Figure 4.4. Noise Generated by a High Q, Low-Gain Stage is Amplified by a Subsequent Low Q, High-Gain Stage

MORE PRACTICAL EXAMPLES

To illustrate how the sorting of cascade order can affect performance, we will examine two concrete examples. The first is an 8th order Butterworth lowpass filter, normalized to 1Hz. The maximum passband ripple is 3dB, the stopband attenuation is 48dB, the corner frequency is 1Hz, and the stopband frequency is 2Hz. Two different versions of this design were implemented, one with the cascade order sorted for decreased harmonic distortion (THD), and the other sorted for lowest noise. Table 4.1 shows the F_o , Q , and F_n values for both versions of our example. Of the four stages, three have Q 's of less than 1, and one has a Q greater than 2.5. The two cascade orders differ only in the position of this high Q section. Observe that in the first case, the highest Q stage was placed in the second position, rather than the first, as the previous discussion indicated. This is a compromise to minimize harmonic distortion while maintaining acceptable noise performance. In the second case, the highest Q section is placed in the third position, followed immediately by the section with the lowest Q . Since this is a Butterworth filter, all of the sections have the same F_o . Nevertheless, because the low Q section has a droopy passband (see Figure 4.2) it still has the effect of band-limiting the noise from the preceding section.

Mode 3 was selected for all stages because it produces lower harmonic distortion than mode 1. The clock-frequency ratio is 50:1, with an actual clock frequency of 400kHz giving an actual F_o value of 8kHz. These two designs were breadboarded, using the resistor values given in Table 4.2. All of the resistor values calculated by FilterCAD were multiplied by 3.5 to minimize loading, except for the R_1 values, which were selected to set the gains for the various sections so that no node will go above 0dB (lowpass gain for mode 3 = R_4/R_1).

The harmonic distortion performance was measured, yielding the results in Figures 4.5 and 4.6. The graphs indicate total harmonic distortion as a percentage of the input voltage. Each graph shows THD performance for inputs of 1V and 2.5V_{RMS}. The difference between the two designs with a 1V_{RMS} input is negligible, but with a 2.5V input, a clear improvement in harmonic distortion is visible in Figure 4.5. In both examples, the distortion takes a

Table 4.1. F_o , Q , and F_n Values for 8th Order Butterworth Lowpass

STAGE	F_o	Q	F_n
Sorted for Reduced Harmonic Distortion			
1	1.0000	0.6013	INFINITE
2	1.0000	2.5629	INFINITE
3	1.0000	0.9000	INFINITE
4	1.0000	0.5098	INFINITE
Sorted for Low Noise			
1	1.0000	0.6013	INFINITE
2	1.0000	0.9000	INFINITE
3	1.0000	2.5629	INFINITE
4	1.0000	0.5098	INFINITE

Table 4.2. Resistor Values for 8th Order Butterworth Lowpass

STAGE	R_1	R_2	R_3	R_4	DC GAIN
Optimized for Reduced Harmonic Distortion					
1	61.90k	60.90k	35.00k	60.90k	0.98
2	57.60k	35.00k	77.35k	35.00k	0.61
3	43.20k	42.35k	35.00k	42.35k	0.96
4	39.20k	71.75k	35.00k	71.75k	1.83
(Total)					1.05
Optimized for Low Noise					
1	60.20k	60.90k	35.00k	60.90k	1.01
2	41.60k	42.35k	35.00k	42.35k	1.00
3	56.20k	35.00k	77.35k	35.00k	0.60
4	43.20k	71.75k	35.00k	71.75k	1.66
(Total)					1.05

significant dip as we approach the corner frequency. This is somewhat deceptive, however, since in this region the third and higher harmonics begin to be attenuated by the filter. While giving better harmonic distortion performance, Figure 4.5 has a wideband noise spec of 90 μ V_{RMS}, whereas Figure 4.6 yielded a wideband noise spec of 80 μ V_{RMS}.

Our second example is a 6th order elliptic lowpass filter, again normalized to 1Hz and realized in two versions, one optimized for noise, and the other optimized for harmonic distortion. This example has a maximum passband ripple of 1dB, a stopband attenuation of 50dB, a corner frequency of 1Hz, and a stopband frequency of 1.20Hz. The

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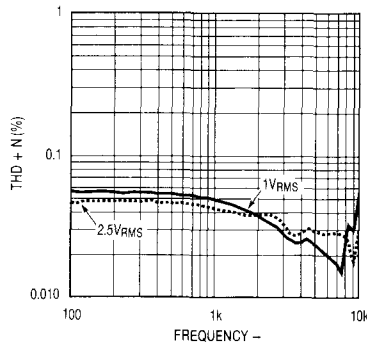


Figure 4.5. THD Performance, 8th Order Butterworth Sorted for Reduced THD

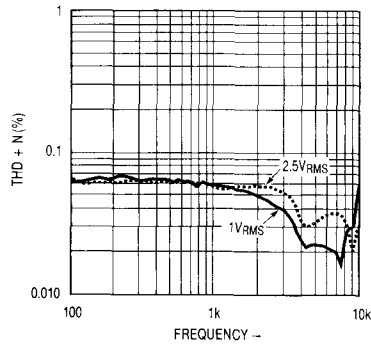
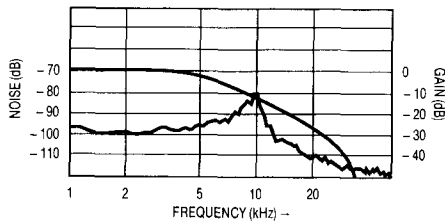
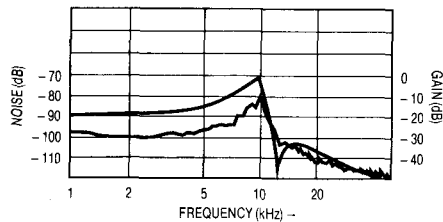


Figure 4.6. THD Performance, 8th Order Butterworth Sorted for Reduced Noise



GAIN AND NOISE OF SECOND ORDER ELLIPTIC SECTION BANDLIMITING NOISE FROM PREVIOUS SECTION. $Q = 0.79$, $F_0 = 4.6\text{kHz}$, $F_n = 36\text{kHz}$.



GAIN AND NOISE OF SECOND ORDER ELLIPTIC SECTION. $Q = 15$, $F_0 = 10\text{kHz}$, $F_n = 12.2\text{kHz}$.

Figure 4.7. Using Cascade-Order to Band-Limit Noise

clock to filter cutoff frequency ratio is 100:1. The cascade orders for the two sections are given in Table 4.3. The case of an elliptic filter is more complex than the Butterworth in that the 2nd order responses have F_n values (notches or 0's) as well as F_0 's and Q 's. The ratio of F_n to F_0 in a particular section affects the height of the resonance peaks resulting from high Q 's. The closer F_n is to F_0 , the lower the peak.

Table 4.3. F_0 , Q , and F_n Values for 6th Order Elliptic Lowpass

STAGE	F_0	Q	F_n
Sorted for Reduced Harmonic Distortion			
1	0.9989	15.0154	1.2227
2	0.8454	3.0947	1.4953
3	0.4618	0.7977	3.5990
Sorted for Low Noise			
1	0.8454	3.0947	1.4953
2	0.9989	15.0154	1.2227
3	0.4618	0.7977	3.5990

In the first instance, the section with the highest F_0 and the highest Q is paired with the lowest F_n , and placed first in the cascade order. The second-highest Q is paired with the second-lowest F_n , and so on. This pairing minimizes the difference between the highest peak and the lowest gain in each second order section. Referring to Table 4.4, which gives the resistor values and lowpass gains for the stages, we see that the first stage has a very low gain of 0.067, and that most of the gain is provided by stage three, which has the lowest Q . Thus, the input swings of the individual stages are minimized, input-induced distortion is reduced, and an overall gain of 1 for the circuit is obtained. (In the case of mode 3A sections, lowpass gain for the first section is determined by $R4/R1$, and lowpass gain for subsequent stages is determined by $R4$ divided by R_L of the previous stage. The final gain stage is provided by the external op amp, and is determined by R_G/R_L . Highpass gain is not taken into account here.)

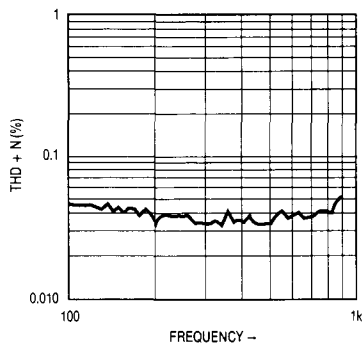


Figure 4.8. THD Performance, 6th Order Elliptic Sorted for Reduced THD

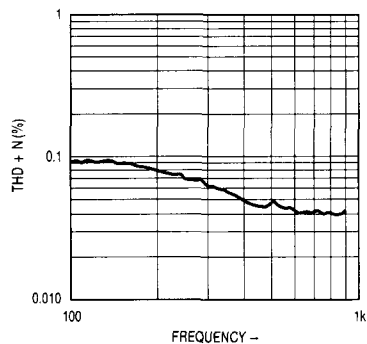


Figure 4.9. THD Performance, 6th Order Elliptic Sorted for Reduced Noise

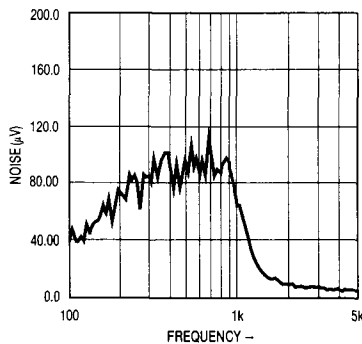


Figure 4.10. Noise Performance, 6th Order Elliptic Sorted for Reduced THD

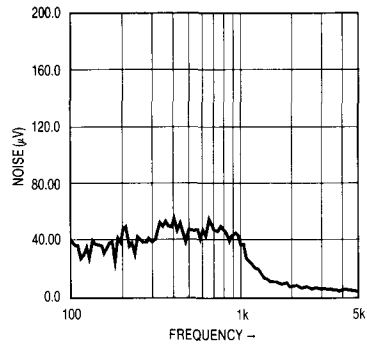


Figure 4.11. Noise Performance, 6th Order Elliptic Sorted for Reduced Noise

In the second example, 2nd order stages have been sorted for reduced noise. In this case, the stage with the highest Q and F_0 is placed in the middle of the cascade order and is followed immediately by the stage with the lowest Q and F_0 . Most of the gain is provided by stage three, which would tend to boost the noise generated by the previous stage, but the greater-than-2:1 ratio between the F_0 's of the two sections causes much of the noise generated by stage two to fall outside of stage three's passband (See Figure 4.7). This produces the band-limiting effect described previously, and improves the overall noise performance of the circuit significantly. Figures 4.8 through 4.11 detail noise and THD performance of the two 6th order elliptic examples.

NOTCHES...THE FINAL FRONTIER

Notch filters, especially those with high Q 's and/or high attenuations, are the most difficult to implement with universal switched-capacitor filter devices. You may design a notch filter with FilterCAD, with specifications that purport to yield a stopband attenuation of greater than 60dB, and find that in practice an attenuation of 40dB or less is the result. This is primarily due to the sampled data nature of the universal filter blocks; signals of equal amplitude and opposite phase do not ideally cancel when summed together as they would do in a purely analog system. Notches of up to 60dB *can* be obtained, but to do so requires techniques not covered by this version of FilterCAD. Some of these techniques will be examined here.

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Table 4.4. Resistor Values for 6th Order Lowpass Elliptic (100:1, F_{CLK} to F_c)

STAGE	R1	R2	R3	R4	RG	RH	RL	LOWPASS GAIN
Sorted for Low THD								
1	150.0k	10.00k	150.0k	10.00k		15.00k	10.00k	0.067
2		11.80k	43.20k	16.50k		22.60k	10.00k	1.650
3		16.90k	28.70k	78.70k	11.50k	130.0k	10.00k	7.870
External Op Amp								1.150
(Total)								1.000
Sorted for Low Noise								
1	43.20k	10.00k	36.50k	14.00k		110.0k	48.70k	0.324
2		10.00k	150.0k	10.00k		15.00k	10.00k	0.205
3		28.00k	48.70k	130.0k	11.50k	130.0k	10.00k	13.00
External Op Amp								1.150
(Total)								0.993

Table 4.5. F_o , Q, and F_n Values for 40kHz, 60dB Notch

STAGE	F_o	Q	F_n
1	35735.6793	3.3144	39616.8585
2	44773.1799	3.3144	40386.8469
3	35242.9616	17.2015	39085.8415
4	45399.1358	17.2105	40935.5393

We will start by using FilterCAD to enter the parameters for an elliptic notch response. We'll specify a maximum passband ripple of 0.1dB, an attenuation of 60dB, a center frequency of 40kHz, a stop bandwidth of 2kHz, and a pass bandwidth of 12kHz. Given these parameters, FilterCAD synthesizes the response shown in Table 4.5. This 8th order filter claims an actual stopband attenuation of greater than 80dB, a level of performance that would be exceedingly difficult to achieve in the real world. A working filter with an attenuation of 60dB can be achieved, but only by deviating significantly from the advice provided by FilterCAD.

Switched-capacitor filter devices give the best performance when certain operating parameters are kept within particular ranges. Those conditions which produce the best results for a particular parameter are called its "figure of merit." For example, in the case of the LTC1064, the best specs for clock to center frequency ratio (F_{CLK}/F_o) accuracy are published for a clock frequency of 1MHz and a Q of 10. As we depart from this "figure of merit" (as we must do to produce the 40kHz notch in our example), per-

Table 4.6. F_o , Q, and F_n Values for 40kHz, 60dB Notch

STAGE	F_o (kHz)	Q	F_n (kHz)	MODE
1	40.000	10.00	40.000	1
2	43.920	11.00	40.000	2
3	40.000	10.00	40.000	1
4	35.920	8.41	40.000	3

formance will gradually deteriorate. One of the problems that we will encounter is "Q-enhancement." That is, the Q's of the stages will appear slightly greater than those set by resistors. (Note that Q-enhancement is mostly a problem in modes 3 and 3A and is *not* limited to notches but occurs in LP, BP and HP filters as well.) This results in peaking above and below the notch. Q-enhancement can be compensated for by placing small capacitors (3pF-30pF) in parallel with R4 (mode 2 or 3). With this modification, Q-enhancement can be compensated for in notch filters with center frequencies as high as 90kHz. The values suggested here are compromise values for a wide-range clock-tunable notch. If you want to produce a fixed-frequency notch, you can use larger caps at higher frequencies. At least in the case of the LTC1064, Q-enhancement is unlikely to be a problem below 20kHz. Adding capacitors at lower frequencies will have the effect of widening the notch.

As mentioned previously, the other problem in implementing notch filters is inadequate attenuation. For low frequency notches, stopband attenuation may be increased

by boosting the clock to notch frequency up to 250:1. Attenuation may also be improved by adding external capacitors, this time in parallel with R2 (modes 1, 2, and 3A). Capacitors of 10pF–30pF in this position can increase stopband attenuation by 5dB–10dB. Of course, this capacitor/resistor combination constitutes a passive 1st order lowpass stage with a corner frequency at $1/(2\pi RC)$. In the case of the values indicated above, the corner frequency will appear so far out in the passband that it is unlikely to be significant. However, if the notch is needed at a frequency below 20kHz, the capacitor value will need to be increased and the corner frequency of the 1st order stage will be lowered proportionally. For a capacitor of 100pF and an R2 of 10k, the corner frequency will be 159kHz, a value that is still unlikely to cause problems in most applications. For a capacitor of 500pF (a value that might prove necessary for a deep notch at a low center frequency) and an R2 of 20k, the corner frequency drops down to 15.9kHz. If maximum stopband attenuation is more important than a wide passband, such a solution may prove acceptable. Adding resistors in parallel with R2

produces one additional problem: it increases the Q that we just controlled with the capacitors across R4. Resistor values must be adjusted to bring the Q down again.

Table 4.6 contains the parameters for a *real* notch filter which actually meets our 60dB attenuation spec using the techniques previously outlined. This is essentially the clock-tunable 8th order notch filter described in the LTC1064 data sheet. Note the mixture of modes used. This is a solution that FilterCAD is incapable of proposing.

It should be apparent that the methods for notch filters described here are primarily empirical at this point, and that the account given here is far from comprehensive. We have not even touched on optimizing these filters for noise or distortion, for instance. No simple rules can be given for this process. Such optimization is possible, but must be addressed on a case-by-case basis. If you need to implement a high-performance notch filter and the tips above prove inadequate, please call the LTC applications department for additional assistance.

PART 5—APPENDICES

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APPENDIX 1

The FilterCAD Device-Parameter Editor

The FilterCAD Device-Parameter Editor (FDPF.EXE) allows you to modify the FilterCAD Device-Parameter File (FCAD.DPF). This file contains the data about LTC switched-capacitor filter devices which FilterCAD uses in making device selections in its implementation phase. The Device-Parameter Editor is a menu-driven program that has a similar command structure to FilterCAD. Its main menu includes the following entries:

1. ADD New Device
2. DELETE Device
3. EDIT Existing Device
4. SAVE Device Parameter File
5. LOAD Device Parameter File
6. CHANGE Path to Device Parameter File

9. END Device Parameter Editor

The principle reason for editing the Device-Parameter File is to add data for new LTC devices that were released after this revision of FilterCAD. To enter data for a new device, press

1

You will see a blank form with fields for the necessary parameters. Use the arrow keys to move through the fields and type in the appropriate values from the LTC data sheet. Press

[Enter]

to accept the data in each field, then press

ESC

when you have finished entering the data. Don't forget to SAVE the new .DPF file. The program will inform you that the FCAD.DPF already exists and ask you whether you want to overwrite it. Press

Y

to save your file.

Another possible reason for using the Device-Parameter Editor is to delete some devices from the Device-Parameter File so that FilterCAD could only select devices that you have on hand. To delete a device, press

2

When it shows you a device name on the screen, press

Y

to delete the device from the file or press

N

to cycle through the list of devices until it displays the one that you wish to delete.

You can also use the Device-Parameter Editor to edit the data for a device supported by this version of FilterCAD in the event that the specifications for that device are revised. To edit a device already in the Device-Parameter File, press

3

You will see a form, like the one described previously for adding new devices, except the fields will contain data. Use the

PgDn

and

PgUp

keys to page through the devices to find the one you wish to edit, move the cursor to the fields that you want to modify and type in the new data. You must press

[Enter]

to accept the new value in each field. Press

ESC

when you have finished editing.

The remainder of the options on the Device-Parameter File Editor's main menu are self explanatory.

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APPENDIX 2

Bibliography

For more information on the theory of filter design, consult one of the works listed below.

1. Daryanani, Gobind, "Principles of Active Network Synthesis and Design." New York: John Wiley and Sons, 1976.
2. Ghausi, M.S., and K.R. Laker, "Modern Filter Design, Active RC and Switched Capacitor." Englewood Cliffs, New Jersey: Prentice-Hall, Inc., 1981.
3. Lancaster, Don, "The Active Filter Cookbook." Indianapolis, Indiana: Howard W. Sams & Co., Inc., 1975.
4. Williams, Arthur B., "Electronic Filter Design Handbook." New York: McGraw-Hill, Inc., 1981.

Parasitic Capacitance Effects in Step-Up Transformer Design

Brian Huffman

One of the most critical components in a step-up design like Figure 1 is the transformer. Transformers have parasitic components that can cause them to deviate from their ideal characteristics, and the parasitic capacitance associated with the secondary can cause large resonating current spikes on the leading edge of the switch current waveform. These spikes can cause the regulator to exhibit erratic operating conditions that manifests itself as duty cycle instability. This effect is exacerbated in very high voltage designs. Attention to transformer design will cure this problem.

Figure 2 shows the high-frequency current paths of the parasitic capacitors. In the analysis of operation assume the input and output voltages are at AC ground. Thus, the parasitic capacitors are all in parallel. The transformer's secondary provides the AC current path for these capacitors. The current flowing through the secondary produces N times the current in the primary. As the parasitic capacitance and turns ratio increase, the primary current becomes progressively larger.

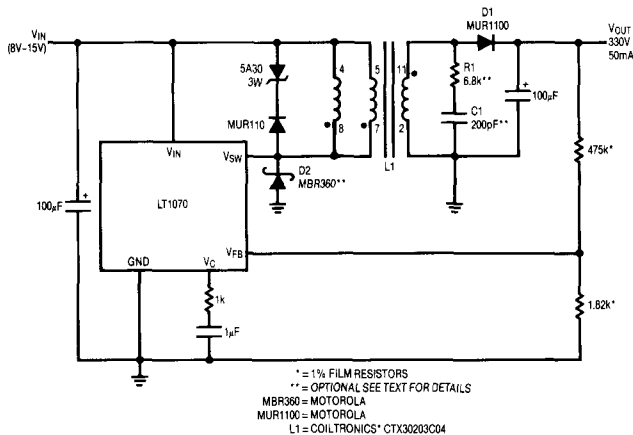


Figure 1. High Voltage Power Supply

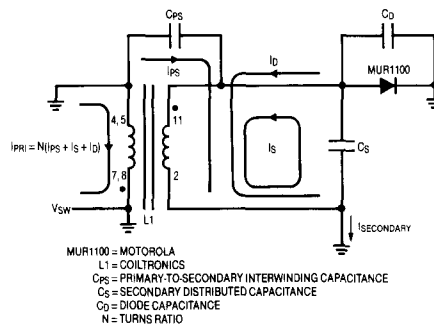


Figure 2. AC Current Paths for Parasitic Capacitors

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The operation waveforms for this circuit are shown in Figure 3. When the switch (V_{SW} pin — trace A) is turned “on” the primary is pulled to ground. The secondary cannot instantly follow this action because of the loading effects of its parasitic capacitances. The effects of the parasitic capacitance can easily be seen in the leading edge of the switch current waveform (trace B). This current spike is caused by the loading effect of the secondary parasitic capacitances. The secondary output (trace D) swing can exceed 600V. As such, a large amount of charge ($Q = C \cdot V$) is needed to swing this node during the switching transients.

The secondary current is amplified by the turns ratio and produces a primary current; $I_{PRI} = N(I_{PS} + I_S + I_D)$. This amplifying effect can be observed by comparing the secondary current (trace C), which does not include the effects of I_S , with the switch current (trace B). The result is a rather large current spike.

The oscillatory nature of the response is formed by a series combination of the leakage inductance and reflected secondary capacitance (Figure 4). Any impedance placed across the secondary appears at the primary

terminals reduced in magnitude by a factor of the turns ratio squared. For example, if $N = 10$, then a 200Ω resistor looks like 2Ω and a 100pF capacitor looks like $0.01\mu\text{F}$, so even a small secondary capacitance can heavily load the primary. The series LC forms a self-resonating circuit that rings at the resonant frequency of the transformer.

The output switching diode, D1, can also cause narrow spikes on the current waveform. In this case, the reverse recovery time of the diode is the important parameter. Reverse recovery time occurs because the diode “stores” charge during its forward conducting cycle. This stored charge causes the diode to act like a low impedance conductive element for a short period of time after reverse drive is applied.

There is a short period of time (blanking time) following switch turn “on” during which the LT1070 ignores the switch current waveform. This blanking time eliminates premature termination of the “on” pulse caused by the leading edge current spike in the current waveform. Once this blanking time has elapsed the output switch will turn “off” when the peak switch current reaches the threshold level established by the error amplifier output (V_C pin).

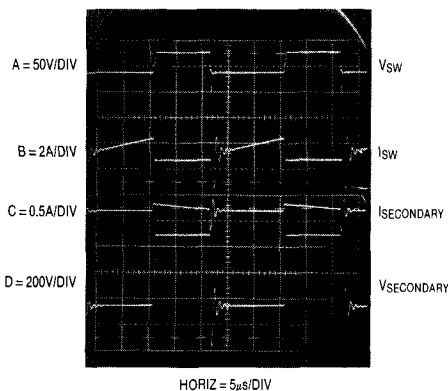


Figure 3. Operating Waveforms for High Voltage Converter

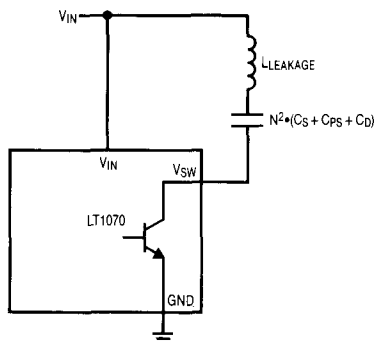


Figure 4. Simplified Primary Model During Transient Conditions

This internally fixed blanking time, 400ns, is appropriate for typical applications. However, for high voltage applications the blanking time becomes a critical parameter. The effects of the transformer's parasitic capacitance is to extend the "spike" width past the blanking time causing the LT1070 to mistrigger, as shown in Figure 5. The duty cycle variations in the switch pin (trace A) and switch current (trace B) waveforms are the result of this problem. Figure 6 details the interaction between blanking time and peak switch current. Notice that the switch is turned "off" as soon as the LT1070 samples the switch current. For the LT1070 to function properly, the spike current must be below the normal peak switch current before the 400ns blanking period is over.

Another problem induced by the parasitic capacitance can also be seen in Figure 3. High reverse current can flow in the V_{SW} pin (trace B) due to the oscillatory nature of the transformer. This will forward bias the LT1070's substrate diode, which is inherent in the output transistor (see Appendix A). Unwanted current can flow almost anywhere within the IC's circuitry when the substrate diode is forward biased, causing unpredictable duty cycle behavior.

The substrate diode current can be eliminated by placing a Schottky diode, D2, between the V_{SW} pin and ground (Figure 1). The reverse primary current will flow through the Schottky diode instead of the LT1070. Another way to prevent the substrate diode from conducting is to place an RC snubber, R1-C1, on the secondary. This will attenuate the ringing.

Well-known transformer winding techniques can be used to minimize parasitic capacitance in step up transformers. The basic technique is to wind the secondary layers in a manner that minimizes the voltage difference between adjacent layers. A standard way of accomplishing this is to wind several separate secondary "stacks" on a split bobbin. This and other techniques will cause a dramatic reduction in secondary capacitance.

For transformer information contact:

Coiltronics
 984 Southwest 13th Court
 Pompano Beach, FL 33069
 305-781-8900

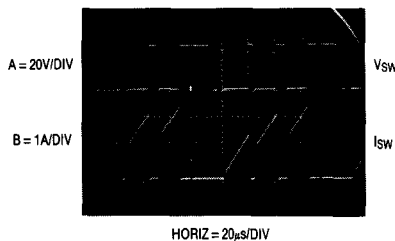


Figure 5. Duty Cycle Instability Due to Current Spike

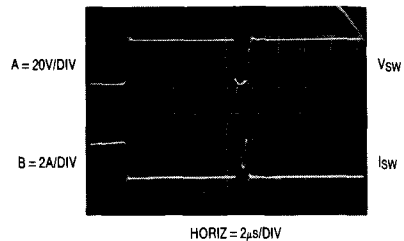


Figure 6. Detail Waveforms of Switch Current Spike

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APPENDIX A

In a junction isolated IC the monolithic transistors are surrounded by an isolating P-N junction, as illustrated in Figure A1. When this junction is reverse biased, it electrically isolates one device from another on the chip. However, this device structure also forms parasitic lateral NPN transistors (see Figure A2). The P substrate is the base, the N-epi region is the emitter and the collector is any other N-epi pocket. A simplified schematic diagram of the NPN cell is shown in Figure A3.

If the vertical NPN output switch transistor is operating in its normal mode, either "on" or "off," the parasitic transistor is off and will have no effect. The parasitic becomes active when the vertical collector is pulled to a potential below that of the substrate by the reverse switch current. This forward biases the collector substrate junction, which is commonly called the substrate diode. As a result, the parasitic NPN draws current from other portions of the circuit. This current will add to the base drive of lateral PNP's and to the collector current of NPN's, causing the IC to behave in mysterious and unpredictable ways (see Figure A2).

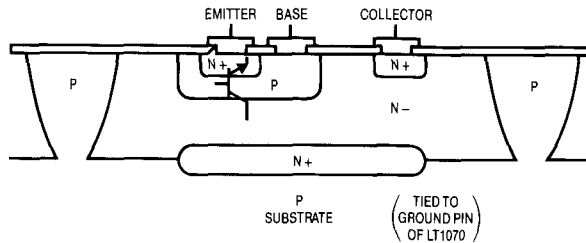


Figure A1. Junction Isolated NPN Structure

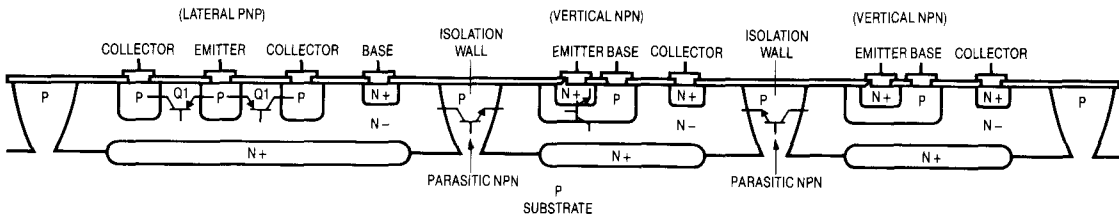


Figure A2. Locations Where the Lateral NPN Occur

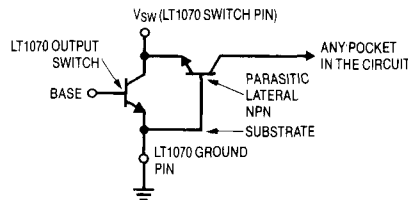


Figure A3. Schematic Diagram of LT1070's Output Switch with Parasitic

Take the Mystery Out of the Switched Capacitor Filter: The System Designer's Filter Compendium

Richard Markell

INTRODUCTION

Overview

This Application Note presents guidelines for circuits utilizing Linear Technology's switched capacitor filter family. Although the switched capacitor filter has been designed into "telecom" circuits for over 20 years, the newer devices are faster, quieter, and lower in distortion. These filters now achieve total harmonic distortion (THD) below -76dB (LTC1064-2), wideband noise below $55\mu\text{V}_{\text{RMS}}$ (LTC1064-3), high frequency of operation (LTC1064-2, -3, and -4 to 100kHz) and steep rolloffs from passband to stopband (LTC1064-1: -72dB at $1.5 \times f_{\text{CUTOFF}}$). These specifications make the new generation of switched capacitor filters from LTC candidates to replace all but the most esoteric of active RC filter designs.

Application Note 40 takes the mystery from the design of high performance active filters using switched capacitor filter integrated circuits. To help the designer get the highest performance available, this note covers most of the problems prevalent in system level switched capacitor filter design. The note covers both tutorial filter material and direct operating criteria for LTC's filter parts. Special attention is given to proper breadboarding techniques, proper power supply selection and design, filter response selection, aliasing, and optimization of dynamic range, noise and THD. These issues are presented after a short introduction to the switched capacitor filter.

The Switched Capacitor Filter

Why use switched capacitor filters? One reason is that sampled data techniques economically and accurately imitate continuous time functions. Switched capacitor filters can be made to model their active RC counterparts in the continuous time domain. The advantages of the

switched capacitor approach lie in the fact that a MOS integrated capacitor with a few switches replaces the resistor in the active RC biquad filter allowing full filter implementation on a chip. The building block for most filter designs, the integrator, appears in Figure 1. When implemented with resistors, capacitors and op amps it is expensive and sensitive to component tolerances. The switched capacitor integrator, as seen in Figure 2, eliminates the resistors and replaces them with switched capacitors. The dependency on component tolerances is virtually eliminated because the switched capacitor filter integrator depends on capacitor value ratios, and not on absolute

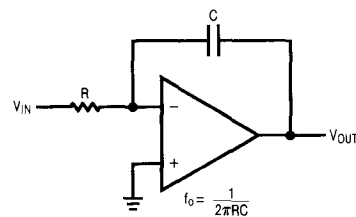


Figure 1. Active RC Inverting Integrator

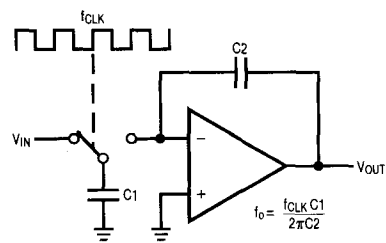


Figure 2. Inverting Switched Capacitor Integrator

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values. This provides very good accuracy in setting center frequencies and Q values. Additionally, this implementation allows the effective resistor value to be varied by the clock operating the switches. This allows the resistors (and therefore the filter center frequencies) to be varied over a wide range (typically 10,000:1 or more). Since existing integrated circuit technology can implement capacitor ratios much more accurately than resistor ratios (see Figure 2), the switched capacitor filter can provide filters with inherent accuracy and repeatability. Active RC configurations are limited by resistor and capacitor tolerances (and to a secondary extent, the accuracy and bandwidth of the op amps) and usually require trimming. Switched capacitor filters do have disadvantages compared to their active RC competitors. These include somewhat more noise in some circuit configurations and a phenomenon called clock feedthru. Clock feedthru is circuit clock artifacts feeding through to the filter output. It is present in virtually all sampled data systems to some degree. LTC has greatly improved this parameter over the past few years to the point where clock feedthru in the LTC1064 series is rarely a problem.

Present day switched capacitor filters include one to four 2nd order sections per packaged integrated circuit. Not long ago the switched capacitor filter was only considered for low frequency work where signal to noise ratio was non-critical. This has changed for the better in recent years. Recent switched capacitor filter designs allow up to 8th order switched capacitor filters to be implemented that compete successfully with the typical multiple operational amplifier designs in critical areas, including signal to noise ratios, stopband attenuation and maximum cutoff frequencies.¹

CIRCUIT BOARD LAYOUT CONSIDERATIONS

The most critical aspect of the testing and evaluation of any switched capacitor filter is a proper circuit board layout. Switched capacitor filters are a peculiar mix of analog and digital circuitry that require the user to take time to layout the circuit board, be it a breadboard or a board for the space station. All this hoopla is standard "do as I say,

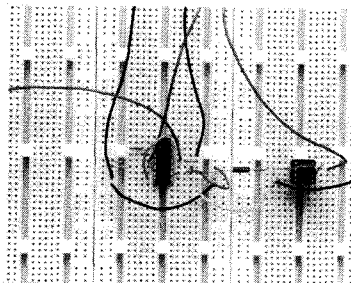
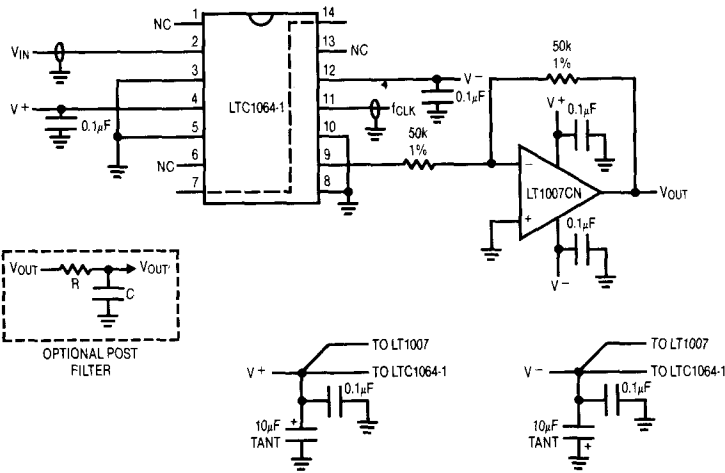


Figure 3. Improperly Constructed "Poor" Switched Capacitor Filter Breadboard

not as I do" in most data sheets. To give the issue its proper credibility, two breadboards were built of the same circuit. The first was built on a "protoboard." No bypass capacitors were used to isolate the power supply from the circuitry and, of course, there was no ground plane. The clock line consisted of flying wires as opposed to the coax used on the second or "recommended" breadboard. Additionally, when tests were run on the first breadboard, in most cases, no buffer operational amplifier at the filter output was used. A photograph of the first protoboard breadboard is shown as Figure 3. It should be emphasized here that the protoboard is a very good board for some types of breadboarding scenarios; it is just not very useful for the type of layout a switched capacitor filter circuit requires.

Figure 5 shows a photograph of a properly constructed switched capacitor filter breadboard. The circuit is built on a copper clad board which acts as a ground plane. The switched capacitor filter and buffer operational amplifier are well bypassed. All leads are kept as short as possible and the switched capacitor filter clock input is through a shielded cable. The second breadboard uses a single point ground in the form of the whole board. (Figure 4 shows the schematic for both breadboards.) Single point grounding techniques become more and more critical as switched capacitor filter parts are incorporated into large

Note 1: Sevastopoulos, Nello, and Markell, Richard, "Four-Section Switched-Cap Filter Chips Take on Discretes." *Electronic Products*, September 1, 1988.



NOTES:

1. $V_S = \pm 8V$
2. $V_{IN}/CLOCK$ PIN USED SHIELDED COAX ON COPPER-CLAD BREADBOARD; FLYING LEADS ON "POOR BREADBOARD."
3. THE BUFFER OP AMP SHOULD NOT SHARE POWER LINES WITH THE SCF.
4. $f_{CLK} = 2MHz/100:1 f_{CLK}/f_0$
5. GROUND PLANE ON RECOMMENDED BREADBOARD.
6. NO BYPASS CAPACITORS USED ON "POOR BREADBOARD."

Figure 4. Schematic of LTC1064-1 Breadboards

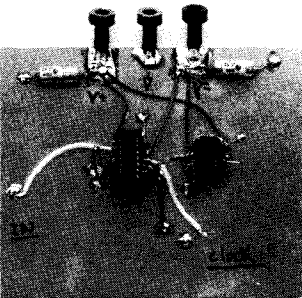


Figure 5. Properly Constructed "Good" Switched Capacitor Filter Breadboard

boards containing many analog and digital devices. In these large boards, and in larger multi-board systems, lots of design time should be spent on single point grounding techniques and noise abatement.²⁻⁶ It will be worthwhile in the long run.

Test results comparing the same circuit built on each breadboard are very interesting. Figure 6 shows the pass-

band response of an 8th order Elliptic lowpass filter, the LTC1064-1. The figure clearly illustrates the ripple in the passband that can be attributed not to the filter, but to the breadboarding technique. The good breadboard is a factor of 5 to 10 times better than the inadequate breadboard.

Figure 7 shows the two breadboard circuits measured in the filter stopband. The top trace is the inadequate breadboard while the bottom is the well constructed model.

Note 2: Brokaw, A. Paul, "An IC Amplifier User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change." Analog Devices Data-Acquisition Databook 1984, Volume I, Pgs. 20-13 to 20-20.

Note 3: Morrison, Ralph, "Grounding and Shielding Techniques in Instrumentation." Second Edition, New York, NY: John Wiley and Sons, Inc., 1977.

Note 4: Motchenbacher, C. D., and Fitchen, F. C., "Low-Noise Electronic Design." New York, NY: John Wiley and Sons, Inc., 1973.

Note 5: Rich, Alan, "Shielding and Guarding." Analog Dialogue, 17, No. 1 (1983), 8-13. Also published as an Application Note in Analog Devices Data-Acquisition Databook 1984, Volume I, Pgs. 20-85 to 20-90.

Note 6: Rich, Alan, "Understanding Interference-Type Noise." Analog Dialogue, 16, No. 3 (1982), 16-19. Also published as an Application Note in Analog Devices Data-Acquisition Databook 1984, Volume I, Pgs. 20-81 to 20-84.

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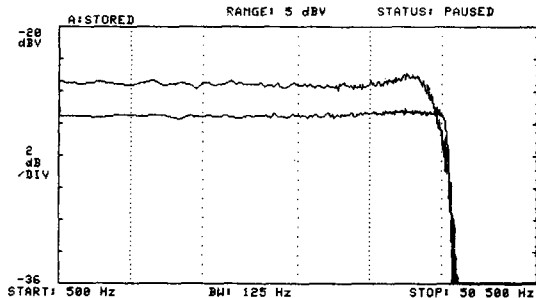


Figure 6. Passband Response — 8th Order Elliptic Lowpass Filter (LTC1064-1). Top Trace: Improperly Constructed Breadboard, No Buffer. Bottom Trace: Good Breadboard, with Buffer. Both: $f_{CLK} = 2\text{MHz}$, $f_{CUTOFF} = 20\text{kHz}$, $V_S = \pm 8\text{V}$. Note: Top Trace Was Offset to Increase Clarity.

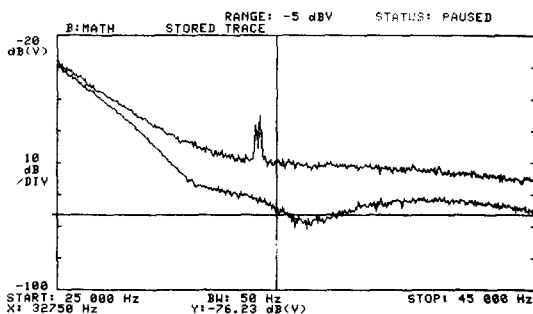


Figure 7. Stopband Response — 8th Order Elliptic Lowpass Filter (LTC1064-1). Top Trace: Improperly Constructed Breadboard, No Buffer. Bottom Trace: Good Breadboard, with Buffer. Both: $f_{CLK} = 2\text{MHz}$, $f_{CUTOFF} = 20\text{kHz}$, $V_S = \pm 8\text{V}$.

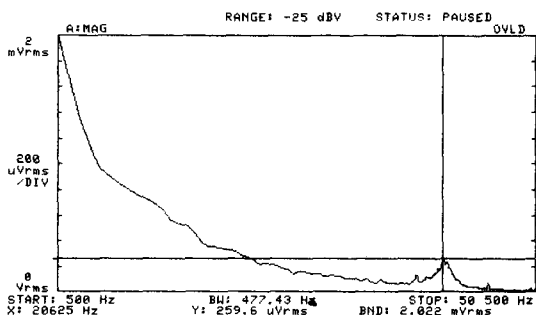


Figure 8. Wideband Noise Measurement — 8th Order Elliptic Lowpass Filter (LTC1064-1) Using Improper Breadboarding Techniques. $f_{CLK} = 2\text{MHz}$, $f_{CUTOFF} = 20\text{kHz}$, $V_S = \pm 8\text{V}$, Buffered with LT1007.

Note the loss of between 10dB and 20dB of attenuation. Also notice the notch, almost 80dB down from the input signal, which is clearly shown when using a good breadboard and which cannot be seen using the poorly constructed breadboard.

Figures 8 and 9 show the noise for the two different breadboards. Two plots were necessary as the noise was more than an *order of magnitude* greater when the poor breadboard was used. These tests were run using the identical switched capacitor filter part (LTC1064-1CN) which was moved from one breadboard to the next to ensure exactly the same measurement conditions, except for the breadboards themselves.

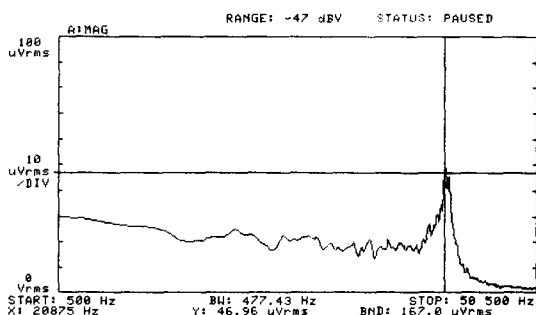


Figure 9. Wideband Noise Measurement — 8th Order Elliptic Lowpass Filter (LTC1064-1) Using Good Breadboarding Techniques. $f_{CLK} = 2\text{MHz}$, $f_{CUTOFF} = 20\text{kHz}$, $V_S = \pm 8\text{V}$, Buffered with LT1007.

Not shown graphically, but measured, was the offset voltage of the switched capacitor filter part in each breadboard. In the poorly constructed board the offset was a whopping 266mV, while in the other circuit board it was 40.7mV, almost a factor of seven times less.

Carefully note that all measurements in this Application Note (with a few noted exceptions) were performed with a good 10x, low capacitance, scope probe (i.e. Tektronix P6133) at the output of the buffer operational amplifier. The probe ground lead length was kept below 1" in length.

Moral of this section: Beware the breadboard that sits on your bench. It may not suffice to resurrect your old 741

breadboard to test today's switched capacitor filters. They require fast clocks, buffering and good breadboarding techniques to deliver their optimum specifications.

POWER SUPPLIES

Power supplies, proper bypassing of these supplies, and supply noise are usually given little attention in the broad spectrum of chaos called system design. Beware! Sampled data devices such as switched capacitor filters, A-to-D and D-to-A converters, chopper stabilized operational amplifiers and sampled data comparators require careful power supply design. Poorly chosen or poorly designed power supplies may induce noise into the system. Similarly, improper bypassing may impair even the most ideal of power supplies. Common complaints range from noise in the passband of a switched capacitor filter to spurious A-to-D outputs due to high frequency noise being aliased back into the signal bandwidth of interest. These effects are, at best, difficult to find and, at worst, worth a call to the local goblin extermination crew (LTC's Application Group!).

Figure 10 shows an example of how a switcher can cause problems. The figure was generated by using the breadboard in Figure 3. An industry standard +5V to ± 15 V switcher module was used to power the board. The switcher was unbypassed to better illustrate the potential problems.

Figure 10 can be compared directly with Figure 7 to see the switcher noise. The poor breadboard causes the stopband attenuation to be well above where it should be when proper breadboarding techniques are used but switcher harmonics are also evident. These appear in Figure 10. Some of these peaks are only -45 dB down from the signal of interest in the passband and could be confused with a legitimate signal. Clearly, if a filter is designed to be 80dB down in the stopband, using a noisy switcher will not do. Figure 11 shows the schematic diagram of a good, low noise switcher for system use. It produces ± 7.5 V with $200\mu\text{V}$ of noise. This switcher is an excellent example of good, low noise design techniques.⁷

All power supplies in a good system design should be properly bypassed. There are as many techniques for

Note 7: Williams, Jim, and Huffman, Brian, "Some Thoughts on DC-DC Converters," Linear Technology AN29.

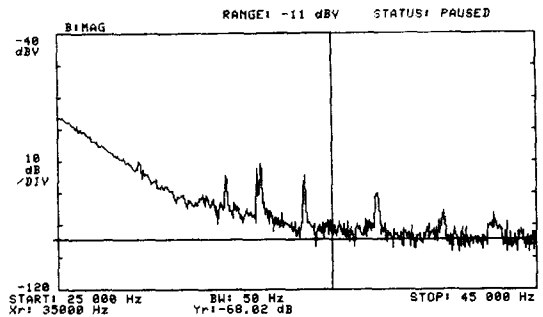


Figure 10. Stopband Response — 8th Order Elliptic Lowpass Filter (LTC1064-1). Power Supply Is Unbypassed Industry Standard Modular +5V to ± 15 V Switcher. The Improperly Constructed Breadboard Was Used For This Test. $f_{\text{CLK}} = 2\text{MHz}$, $f_{\text{CUTOFF}} = 20\text{kHz}$, $V_S = \pm 7.5\text{V}$, (Switcher Zenered to $\pm 7.5\text{V}$).

bypassing as voodoo curses, so we will not overly dwell on the subject. For switched capacitor filters, we recommend good, low ESR bypass capacitors ($0.1\mu\text{F}$ minimum, $0.22\mu\text{F}$ better) as close to the power supply pins of the part as possible. High quality capacitors are recommended for bypassing. For more details on how to identify an adequate capacitor see Appendix B. We recommend separate digital and analog grounds with the two only being tied together as close to supply common as practical. The ground lead to the bypass capacitors should go to the analog ground plane.

The prudent layout includes bypass capacitors on the pins of the switched capacitor filter which are tied to a circuit potential for programming, such as the 50/100 pins. Should spikes and/or transients appear on this pin, trouble will ensue. The summing junction pins SA, SB, etc. are also candidates for bypassing if they are tied to analog ground in a single supply system where lots of noise is present. This last issue is probably icing on the cake in most cases, but it will help lower the noise in some cases.

Last, but not least, the power supplies used to power the switched capacitor filters limit the maximum input and output signals to and from the filters. Thus, power supplies have a direct effect on the system dynamic range. For the LTC1064 type filter ± 7.5 V supplies provide ± 5 V output swing, while ± 5 V supplies provide ± 3.3 V of swing. For a filter with 450mVp-p of output noise these numbers translate to 87dB and 83dB of dynamic range respectively.

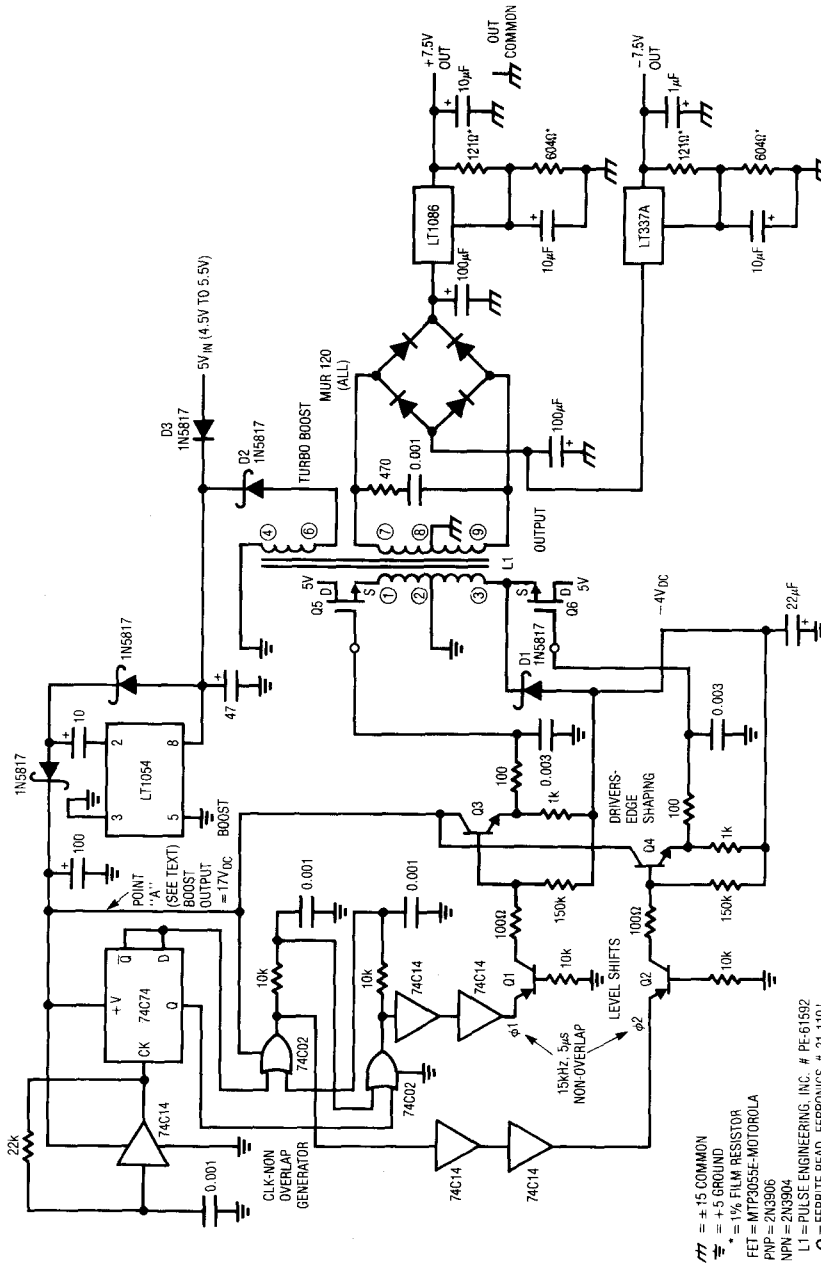


Figure 11. Low Noise 5V to ±7.5V Converter (200µV_{p-p} Noise)

INPUT CONSIDERATIONS

This section considers some aspects of switched capacitor filter design which are related to the input signal, the filter's input structure and the overall filter response.

Offset Voltage Nulling

Typical offset voltages for an LTC1064 or an LTC1064-X through the four sections may range up to 40mV or 50mV. While this may not be of concern for AC coupled systems, it becomes important in DC coupled applications. The anti-aliasing filter used before an A/D converter is a typical application where this is an important concern. For a 5V_{o-p} input signal, the least significant bit of an 8-bit A/D converter is approximately 20mV, and one half the LSB is approximately 10mV. This implies that use of a filter (or for that matter, any type of device other than a straight wire) before an 8-bit A/D converter requires offset voltages below 10mV. For a 12-bit converter this provision mandates stringent 600 μ V of offset at the A/D's input.

Several methods of offset cancellation are common. The usual method seen with operational amplifiers utilizes a potentiometer to inject a correction voltage. Figure 12 shows this arrangement with an LTC1064-1 Elliptic filter. This method can correct the initial offset, but both the adjustment circuit and the CMOS operational amplifiers in the switched capacitor filters have temperature coefficients that are not zero. Thus, if this circuit is used to correct the offset at 25°C, it will not fully correct the offset at another temperature. An advantage of this type of offset

nulling is that the filters frequency response is affected very little. Figure 13 shows the time domain response of Figure 12's filter circuitry. The rising and falling edge overshoot is typical of high Q filters be it switched capacitor or active RC. (This time domain performance parameter, the risetime, is treated separately in a latter section.) Compare Figure 13 with Figure 15 to observe the time domain response of an open loop offset correction scheme (the potentiometer) versus Figure 14's closed loop servo.

Figure 14 shows the circuit of an LTC1064-1 Elliptic filter with the same LT1007 output buffer amplifier used in Figure 13. An addition is the LT1012 operational amplifier used as a servo to zero the offset of the filter. This arrangement can provide offsets of less than 100 μ V which is quite acceptable for a 12-bit system. The servo generates a low

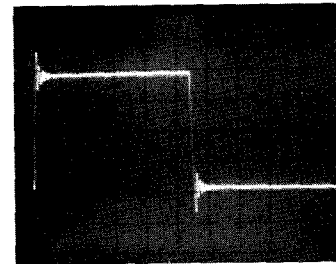


Figure 13. Time Domain Response of Elliptic Filter (LTC1064-1) Without Servo in Figure 12. Input Signal 1Hz Square Wave. LTC1064-1 Cutoff (f_c) = 100Hz. Horiz = 0.1s/Div., Vert = 0.5V/Div.

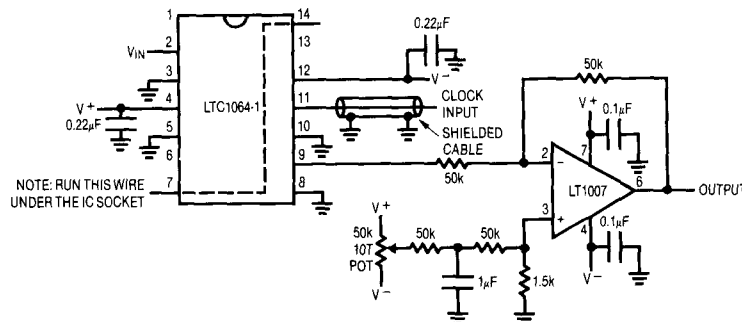


Figure 12. Elliptic Filter with Offset Adjustment Potentiometer

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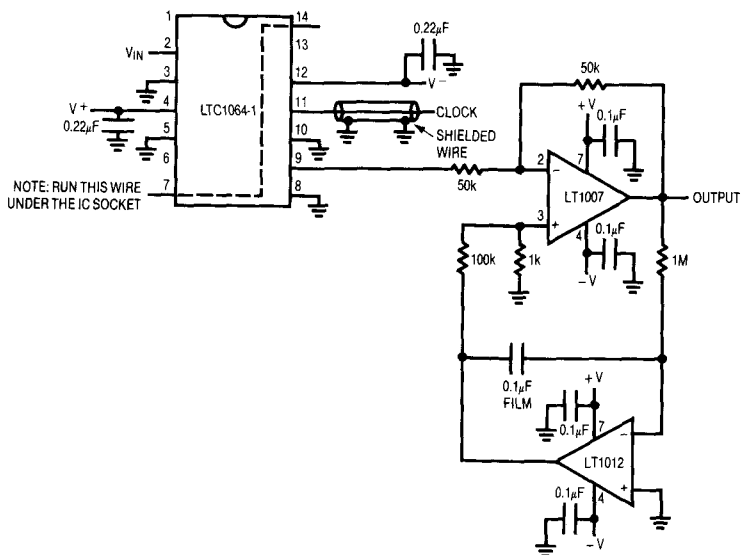


Figure 14. Elliptic Filter (LTC1064-1) with Servo Offset Adjustment

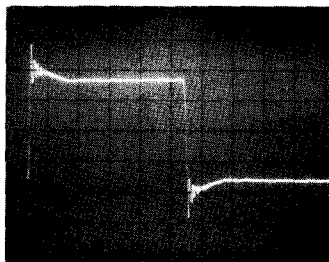


Figure 15. Time Domain Response of Elliptic Filter (LTC1064-1) With Servo per Figure 14. Input Signal 1Hz Square Wave. LTC1064-1 Cutoff (f_0) = 100Hz. Horiz = 0.1s/Div., Vert = 0.5V/Div.

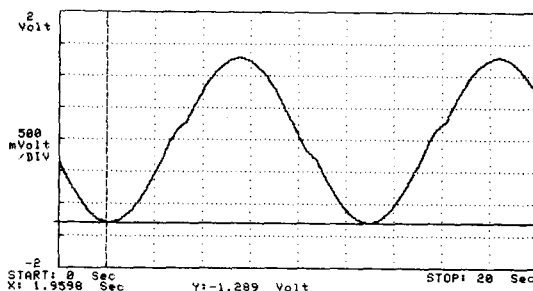


Figure 16. Large Signal Response — Output of Elliptic Filter (LTC1064-1) Plus Servo (Figure 14). Input: 1V_{RMS}, 0.092Hz Sine Wave. Filter f_{CUTOFF} = 100Hz.

frequency pole at about 0.16Hz which can interact with some signals of interest to some system users. Figure 15 shows the low frequency square wave response. Figure 16 shows the distortion introduced for large signal inputs at a frequency near the servo pole. Figure 17 shows a sine wave input to the servo system, but at lower amplitude and higher frequency. The small distortion introduced at this higher frequency is probably traceable to the servos high

frequency cutoff. Figure 19 shows the servo response to the small signal input at 0.092Hz shown in Figure 18. The servo tracks this input, but at a lower amplitude. The servo thus looks like a highpass filter to the input signal at input frequencies below the servo pole frequency. Servo offset nulling can be extremely useful in systems if the limitations described are tolerable.

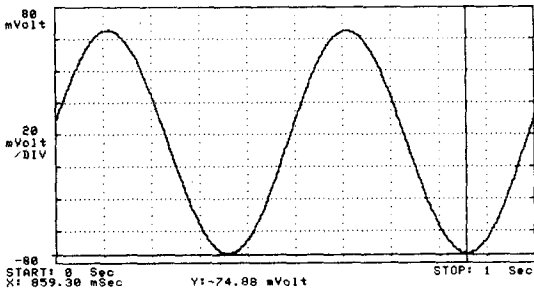


Figure 17. Small Signal Response — Output of Elliptic Filter (LTC1064-1) Plus Servo (Figure 14). Input: 50mV_{RMS}, 2Hz Sine Wave. Filter $f_{CUTOFF} = 100\text{Hz}$.

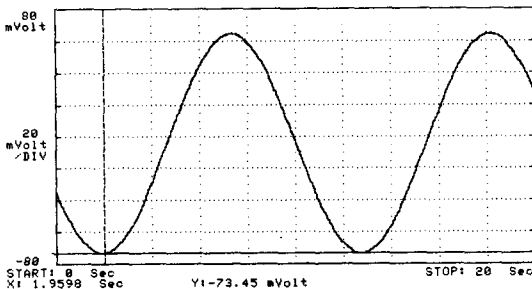


Figure 18. Input Signal (50mV_{RMS}, 0.092Hz) to Elliptic Filter (LTC1064-1) as Shown in Figure 14.

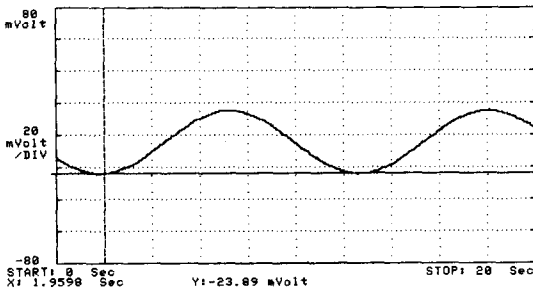


Figure 19. Small Signal Output Response of Elliptic Filter (LTC1064-1) Plus Servo to Input Shown as Figure 18. Filter $f_{CUTOFF} = 100\text{Hz}$.

Slew Limiting

The input stage operational amplifiers in active RC or switched capacitor filters can be driven into slew limiting if the input signal frequency is too high. Slew limiting is usually caused by a capacitance load drive limitation in the op amps internal circuitry. Contemporary switched capacitor filter devices are designed to avoid slew limiting in almost all cases.

As an example, the LTC1064 filter has a typical slew rate of 10V/ μs . Since slew rate is a large signal parameter, it also defines what is called the power bandwidth, given as

$$f_p = \frac{SR}{2\pi E_{op}} \quad (\text{See Note 8})$$

where f_p is the full power frequency and E_{op} is the peak amplifier output voltage.

For the LTC1064 operating at $V_S = \pm 7.5\text{V}$, the device can swing $\pm 5\text{V}$ or 10V peak. Based on the op amp slew rate performance *only*, the full power frequency is calculated as,

$$f_p = \frac{10\text{V}}{10^{-6}\text{s} \cdot 2\pi \cdot 10\text{V}} = 159\text{kHz}$$

This f_p is sufficient for all but the most stringent switched capacitor filter applications of the LTC1064.

Aliasing

Since the switched capacitor filter is based around a "switching capacitor" to generate variable filter parameters, it is by definition a sampled data device. Like all other such devices it is subject to aliasing. Aliasing is a complex subject with lots of mathematics involved. As such, its derivation is the subject of many paragraphs in textbooks.⁹ The system designer can get a meaningful handle on the subject by a series of spectrum analyzer views.

Note 8: Jung, Walter, "IC Op Amp Cookbook." Howard W. Sams, 1988.

Note 9: Schwartz, Misha, "Information Transmission, Modulation and Noise." New York, NY: McGraw Hill Book Co., 1980.

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Figure 20 through Figure 23 each show three spectrum segments while the switched capacitor filter's input signal varies from 100Hz to 49.9kHz. Each figure shows a different input frequency and spectrum plots of the filter's passband (10Hz–510Hz), the frequency spectrum around $f_{CLK}/2$ (25kHz) and the frequency spectrum around f_{CLK} (50kHz). The switched capacitor filter is a lowpass Elliptic filter (LTC1064-1) with a cutoff frequency set to 500Hz

($f_{CLK}/f_{CUTOFF} = 100:1$). The clock used for this cutoff is 50kHz. Thus, from sampled data theory, aliasing begins when the input signal passes the $f_{CLK}/2$ threshold (25kHz).

Figure 20 shows the LTC1064-1 in its normal mode of operation with the signal (100Hz) within the passband of the filter. Note the small second harmonic content (-80dB) component which also appears in the passband.

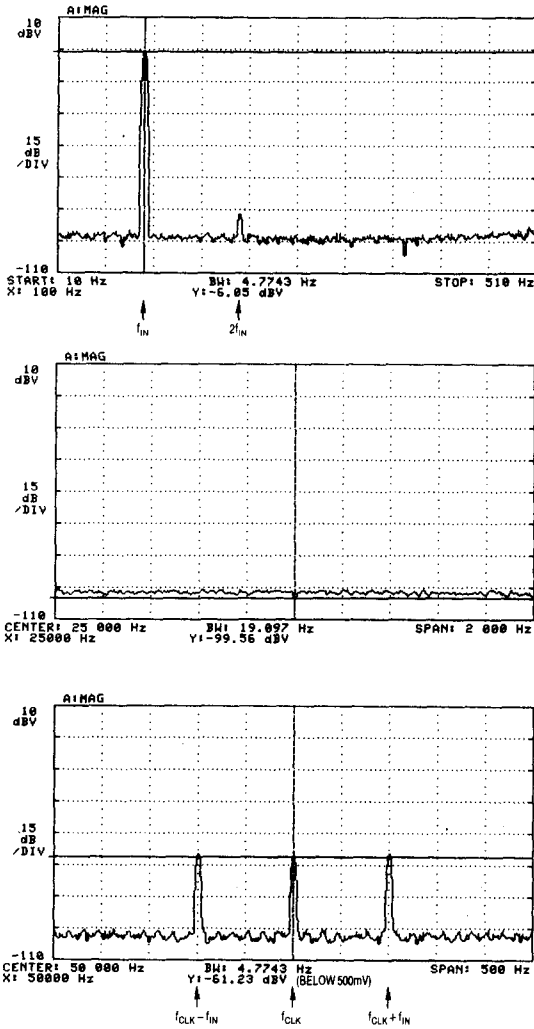


Figure 20. Elliptic Switched Capacitor Filter (LTC1064-1) Aliasing Study. $f_o = 500\text{Hz}$, $f_{CLK} = 50\text{kHz}$, $V_S = \pm 8\text{V}$, $V_{IN} = 100\text{Hz} @ 500\text{mV}_{RMS}$. Note Dynamic Range Limitation.

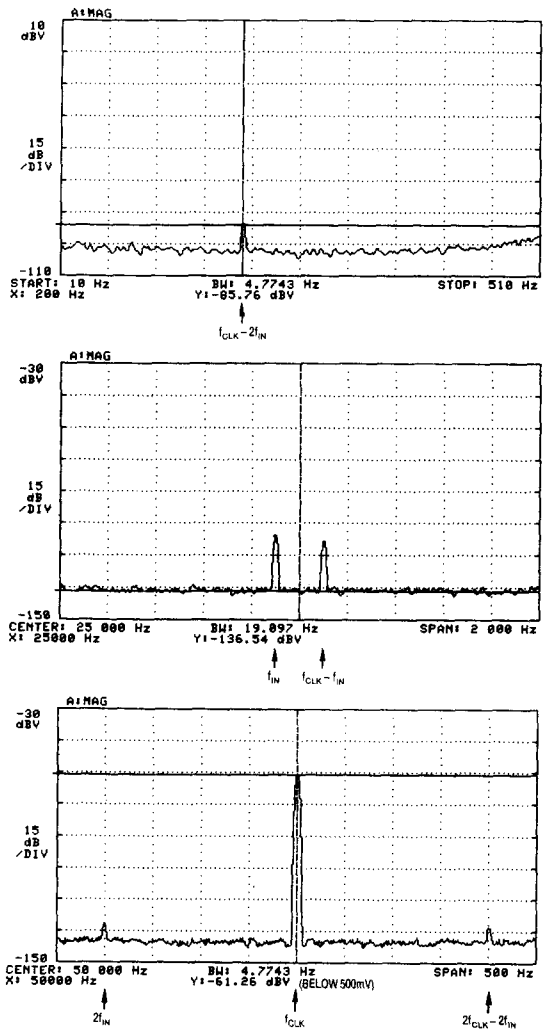


Figure 21. Elliptic Switched Capacitor Filter (LTC1064-1) Aliasing Study. $f_o = 500\text{Hz}$, $f_{CLK} = 50\text{kHz}$, $V_S = \pm 8\text{V}$, $V_{IN} = 24.9\text{kHz} @ 500\text{mV}_{RMS}$.

No signals are seen around $f_{CLK}/2$, however, the original signal (100Hz) appears attenuated (sin x/x envelope response) at 49.9kHz and 50.1kHz. This is consistent with sampled data theory and is a very important anomaly to be taken into consideration in some systems. Thus, for any signal input there will be side lobes at $f_{CLK} \pm f_{IN}$. These side lobes will be attenuated by the sin x/x envelope familiar to those who work with sampled data systems.

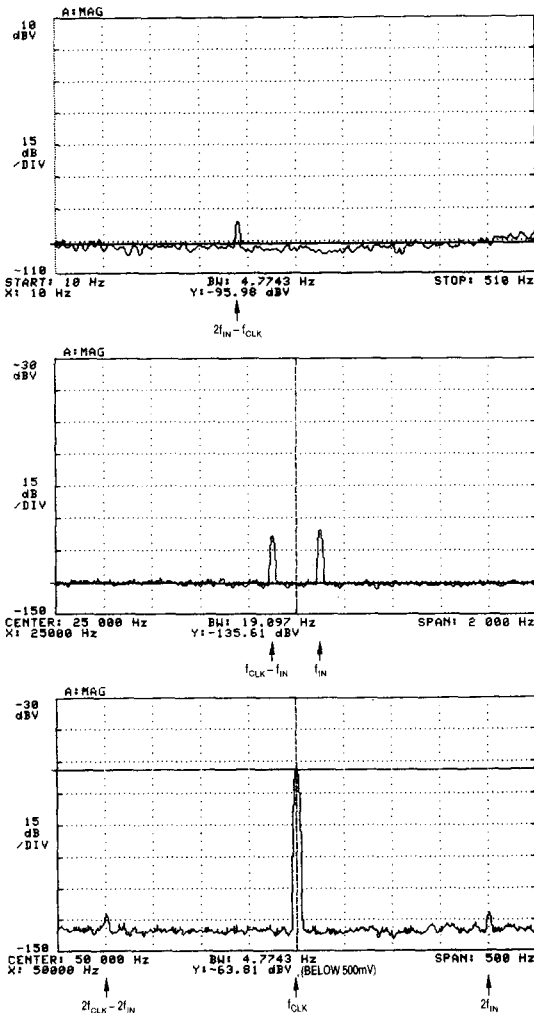


Figure 22. Elliptic Switched Capacitor Filter (LTC1064-1) Aliasing Study. $f_0 = 500\text{Hz}$, $f_{CLK} = 50\text{kHz}$, $V_S = \pm 8\text{V}$, $V_{IN} = 25.1\text{kHz} @ 500\text{mV}_{RMS}$.

Figure 21 shows the same series of spectral photos for an input signal of 24.9kHz. This signal is outside of the filter passband, so the signals are much attenuated. The signal seen at 200Hz in this series of plots is actually the alias of the 49.8kHz second harmonic of the input signal. The signals seen around 25kHz are the 24.9kHz input and the $f_{CLK} - f_{IN}$ signals (see your textbook!!) The signals around and at 50kHz are clock feedthru, and the second harmonic images of the 24.9kHz input signal around the clock frequency.

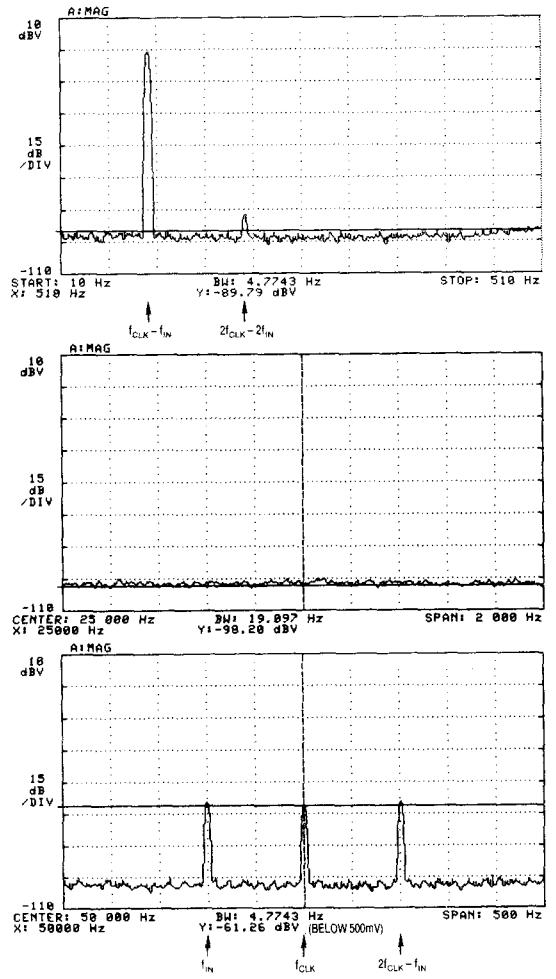


Figure 23. Elliptic Switched Capacitor Filter (LTC1064-1) Aliasing Study. $f_0 = 500\text{Hz}$, $f_{CLK} = 50\text{kHz}$, $V_S = \pm 8\text{V}$, $V_{IN} = 49.9\text{kHz} @ 500\text{mV}_{RMS}$. Note Dynamic Range Limitation.

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Similarly, Figure 22 shows spectral plots for an input signal of 25.1kHz. The signals appear in the same locations as Figure 21, but for different reasons. The 200Hz signal in this figure is the alias of the 50.2kHz. The signals around 25kHz are the input signal at 25.1kHz and its alias at 24.9kHz.

Figure 23 details aliasing at its very worst. The input signal here is 49.9kHz which aliases back, in the filter passband, to 100Hz and appears almost identical to Figure 20's 100Hz signal. The input signal appears at 49.9kHz with its 50.1kHz mirror image.

Of additional note to the system designer is the LTC1062 5th order dedicated Butterworth lowpass filter. This device makes use of a continuous time input stage (an R and C) to prevent aliasing, making it attractive in some applications.

FILTER RESPONSE

What Kind of Filter Do I Use? Butterworth, Chebyshev, Bessel or Elliptic

One of the questions most asked among system designers at the shopping malls of America is "how do I choose the proper filter for my application?" Aside from the often used retort, "call Linear Technology," a discussion of the types of filters and when to use them is appropriate.

A typical application could involve lowpass filtering of pulses. This filter might be in the IF section of a digital radio receiver. The received pulses must pass through the filter without large amounts of overshoot or ringing. A Bessel filter is most likely the filter of choice.

Another application may be insensitive to filter pulse response, but requires as steep a cutoff slope as possible. This might occur in the detection of a series of continuous tones as in an EEG system. If filter ringing is irrelevant, an Elliptic filter may be a good choice.

The trade-offs involved in filter design are critical to the system designers understanding of this topic. This means understanding what happens in both the time domain and in the frequency domain. At the risk of sounding pedantic, a discussion of this topic is appropriate. A time domain response can be viewed on an oscilloscope as amplitude

versus time. It is in the time domain that pulse overshoot, ringing and distortion appear. The frequency domain (amplitude versus frequency) is traditionally where the designer looks at the filter's response (on a spectrum analyzer). A wonderful response in the frequency domain often appears ugly in the time domain. The converse may also be true. It is crucial to examine both responses when designing a filter!

Figures 24 through 28 reprinted here from Zverev¹⁰ show the time domain step response for the Butterworth, two types of Chebyshev, a Bessel and a synchronously tuned filter. (The synchronously tuned filter is one that is made up of multiple identical stages, but contains no notches. See AN27A for more discussion on this topic.) Figure 29 shows the time domain response of the LTC1064-1 8th order Elliptic LP filter to a 10Hz input square wave. The photo shows that a system requiring good pulse fidelity cannot use this filter. Figure 30 shows a better filter for this application. It is the LTC1064-3, an 8th order Bessel LPF. The response has a nice, rounded off risetime with no overshoot. The trade-off appears in the frequency domain.

Figures 31 through 34 show the frequency domain response of four 8th order filters, the LTC1064-1 through LTC1064-4. (Figure 35 shows an expansion of the comparison of the LTC1064-1 and LTC1064-4 rolloff from the passband to the stopband.) The LTC1064-1 and LTC1064-4 are 8th order Elliptic filters, while the LTC1064-2 is a Butterworth and the LTC1064-3 is a Bessel. The rolloff from the passband to the stopband is least steep for the LTC1064-3 Bessel filter. This is the price paid for the linear phase response which enables the filter to pass a square wave with good fidelity. Similarly, the LTC1064-2 Butterworth trades slightly worse transient response for steeper rolloff.

The system designer must carefully consider a potential filtering solution in the time and frequency domains. Figures 24 through 34 are intended as examples to help the designer with this process. There are an infinite variety of filters that can be implemented with switched capacitor filters to obtain the precise response required for one's system.

Note 10: Zverev, "Handbook of Filter Synthesis." New York, NY: John Wiley and Sons, Inc., Copyright 1967.

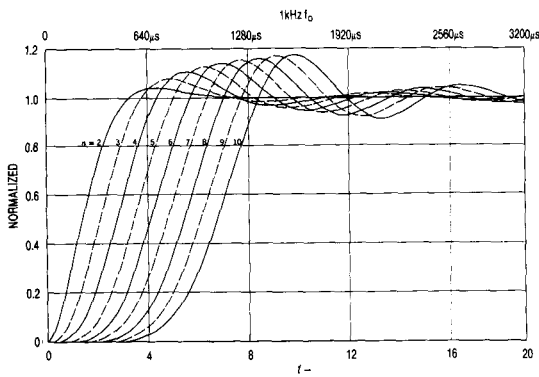


Figure 24. Step Response for Butterworth Filters*

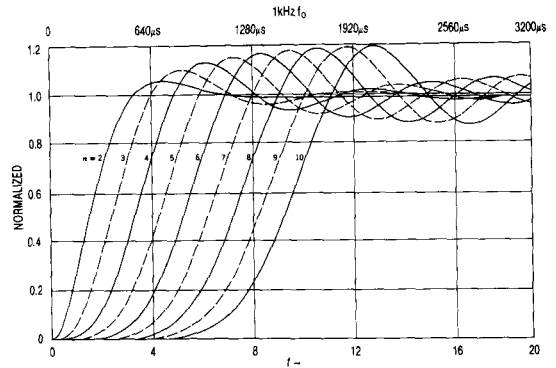


Figure 25. Step Response for Chebyshev Filters with 0.1dB Ripple*

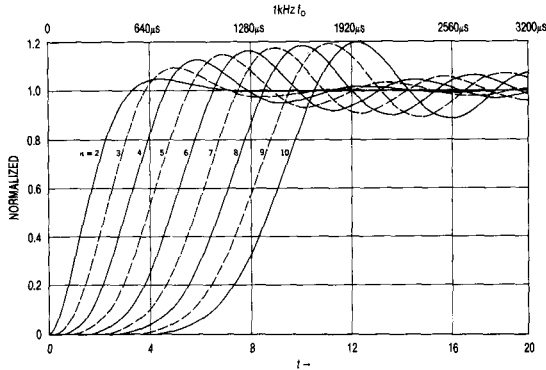


Figure 26. Step Response for Chebyshev Filters with 0.01dB Ripple*

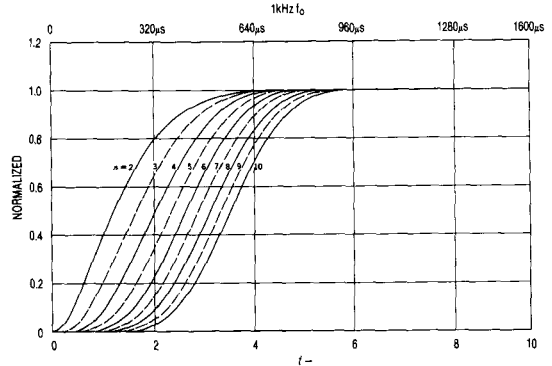


Figure 27. Step Response for Maximally Flat Delay (Bessel) Filters*

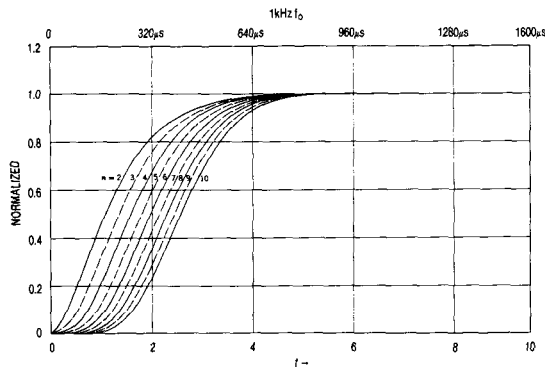


Figure 28. Step Response for Synchronously Tuned Filters*

*From Anatol I. Zverev, "Handbook of Filter Synthesis," Copyright © 1967 John Wiley and Sons, Inc., Reprinted by permission of John Wiley and Sons, Inc.

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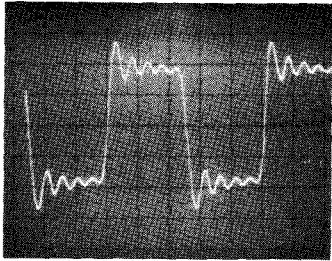


Figure 29. LTC1064-1 Time Domain Response. Filter $f_{CUTOFF} = 100\text{Hz}$. Input: 10Hz Square Wave. Horiz = 20ms/Div., Vert = 0.5V/Div.

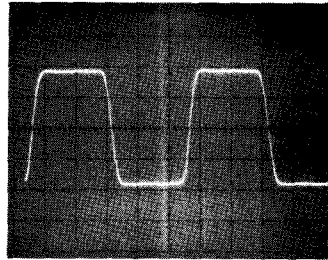


Figure 30. LTC1064-3 Time Domain Response. Filter $f_{CUTOFF} = 100\text{Hz}$. Input: 10Hz Square Wave. Horiz = 20ms/Div., Vert = 0.5V/Div.

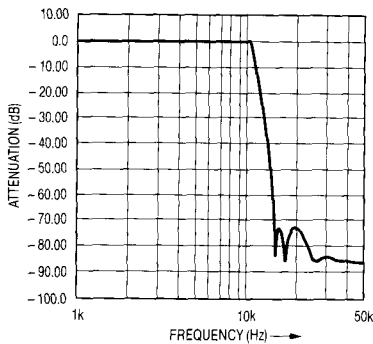


Figure 31. Frequency Domain Response of LTC1064-1 Elliptic Filter. $f_{CUTOFF} = 10\text{kHz}$, $V_S = \pm 7.5\text{V}$, LT1007 Output Buffer, 100:1.

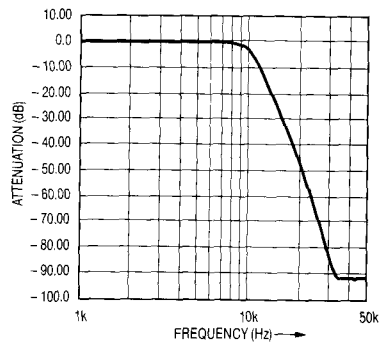


Figure 32. Frequency Domain Response of LTC1064-2 Butterworth Filter. $f_{CUTOFF} = 10\text{kHz}$, $V_S = \pm 7.5\text{V}$, LT1007 Output Buffer, 50:1.

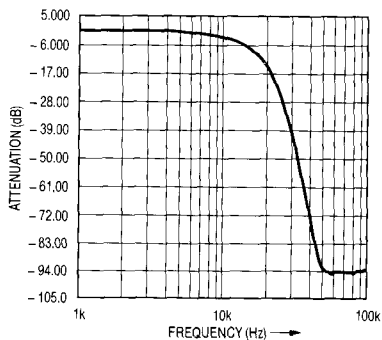


Figure 33. Frequency Domain Response of LTC1064-3 Bessel Filter. $f_{CUTOFF} = 10\text{kHz}$, $V_S = \pm 7.5\text{V}$, LT1007 Output Buffer, 75:1.

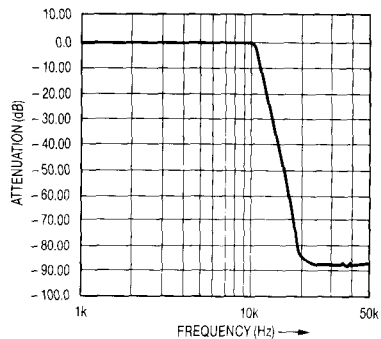


Figure 34. Frequency Domain Response of LTC1064-4 Elliptic Filter. $f_{CUTOFF} = 10\text{kHz}$, $V_S = \pm 7.5\text{V}$, LT1007 Output Buffer, 50:1.

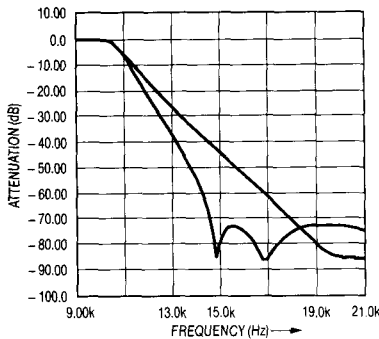


Figure 35. Frequency Domain Response of LTC1064-1 and LTC1064-4 Transition Region Blow-Up. $f_{CUTOFF} = 10\text{kHz}$, $V_S = \pm 7.5\text{V}$, LT1007 Output Buffer.

Call Linear Technology Applications at (408) 432-1900 for additional help in choosing and/or defining a particularly difficult filtering problem.

The perennial question, “how fast can I sweep?” a filter from one frequency to another can be answered by looking at the transient response curves and renormalizing them to the desired cutoff frequency. Then the settling time can be read off the curve. A frequency sweep is in many aspects like the settling time performance to a pulse input.

Table 1 details the four filters mentioned previously and some of their key parameters. Note the wide variation in the stopband attenuation specification. This specification is a measure of the filters steepness of attenuation. This is a key specification for anti-aliasing filters found at an A/D converter’s input. Note that for the LTC1064-1 in the figure (corner frequency set to 10kHz) the attenuation to a 15kHz signal would be about 72dB. The Butterworth gives approximately 27dB, while the Bessel only about 7dB attenuation. These latter two filters trade frequency domain rolloff for good time domain response.

Table 1. Filter Selection Guide

PART NUMBER	TYPE	PASSBAND RIPPLE	STOPBAND ATTENUATION	WIDEBAND NOISE 1Hz-1MHz	SNR	THD (1kHz) (NOTE 1)	SUPPLY VOLTAGE
LTC1064-1	Elliptic	$\pm 0.15\text{dB}$	72dB @ $1.5f_c$	$150\mu\text{V}_{\text{RMS}}$	1V_{RMS} Input = 76dB	-76dB	$V_S = \pm 5\text{V}$
				$165\mu\text{V}_{\text{RMS}}$	3V_{RMS} Input = 85dB	-70dB	$V_S = \pm 7.5\text{V}$
LTC1064-2	Butterworth	3dB	90dB @ $4f_c$	$80\mu\text{V}_{\text{RMS}}$	1V_{RMS} Input = 82dB	-76dB	$V_S = \pm 5\text{V}$
				$90\mu\text{V}_{\text{RMS}}$	3V_{RMS} Input = 90dB	-70dB	$V_S = \pm 7.5\text{V}$
LTC1064-3	Bessel	3dB	60dB @ $5f_c$	$55\mu\text{V}_{\text{RMS}}$	1V_{RMS} Input = 85dB	-76dB	$V_S = \pm 5\text{V}$
				$60\mu\text{V}_{\text{RMS}}$	3V_{RMS} Input = 94dB	-70dB	$V_S = \pm 7.5\text{V}$
LTC1064-4	Elliptic	$\pm 0.1\text{dB}$	80dB @ $2f_c$	$120\mu\text{V}_{\text{RMS}}$	1V_{RMS} Input = 78dB	-76dB	$V_S = \pm 5\text{V}$
				$130\mu\text{V}_{\text{RMS}}$	3V_{RMS} Input = 87dB	-70dB	$V_S = \pm 7.5\text{V}$

Note 1: These specifications from LTC data sheets represent typical values. Optimization may result in significantly better specifications. Call LTC for more details.

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FILTER SENSITIVITY

How Stable Is My Filter?

One of the great advantages of the switched capacitor filter is the lack of discrete capacitors with their inherent tolerance and stability limitations. The active RC filter designed with theoretical capacitor values has problems with repeatability and stability when real world capacitors are used. The switched capacitor filter has small errors in both the cutoff frequency, f_0 , and Q, but they are easier to deal with than those of the active RC filter.

Most universal switched capacitor filters are arranged in the so-called State-Variable-Biquad circuit configuration.¹¹ This configuration not only allows realization of all filter functions, LP, BP, HP, AP and notch, but also allows high Q filters to be realized with low sensitivity to component tolerances. (For a strict mathematical analysis of the sensitivity of the State-Variable-Biquad see reference 11, chapter 10.)

Manufacturing realities of the semiconductor business also affect the switched capacitor filter design. Though this inaccuracy is much less than the active RC design (do the math in Daryanani), it does exist. Thus, switched capacitor filters are available from manufacturers such as LTC with center frequency tolerances of generally 0.4% to 0.7%. This presumes an accurate stable clock. Operating the universal switched capacitor filter in mode 3 tends to make the center frequency error depend on the resistors since the equation for f_0 is

$$f_0 = \frac{f_{CLK} \sqrt{R2/R4}}{50 \text{ or } 100}$$

Thus the manufacturing inaccuracy of the switched capacitor filter is multiplied (and generally swamped) by the resistor inaccuracy. Mode 2 guarantees a filter designed with switched capacitor filters has lower f_0 sensitivity than Mode 3 by changing the equation for f_0 to

$$f_0 = \frac{f_{CLK}}{50 \text{ or } 100} \sqrt{1 + R2/R4}$$

Here resistor sensitivity is mitigated by the one under the radical, and thus the inaccuracy is, in most cases, only caused by the manufacturing tolerances of the switched capacitor filter. (See discussion of switched capacitor filter modes in the LTC1060 and/or LTC1064 data sheets).

An excellent method of minimizing the filter dependence on resistor tolerances, is to integrate the resistors directly on the semiconductor device. This can be done with the LTC1064 family of devices using silicon chrome resistors placed directly on the die.

Actual resistor values are generally better than 0.5%, but the important feature is that all thin film resistors track each other in both resistance and temperature coefficient. Thus, filters such as the LTC1064-1 through LTC1064-4 have virtually indistinguishable characteristics for each and every part.

The small tolerances in f_0 using the switched capacitor filter are trivial when compared to an active RC filter. An Elliptic filter like the LTC1064-1 requires no small amount of trimming when built with resistors, capacitors and op amps. Changing the f_0 is even more impractical.

OUTPUT CONSIDERATIONS

THD and Dynamic Range

Presently, one of the biggest uses of filters is before A/D converters for anti-aliasing. The filter bandlimits the signal at the input to a Digital Signal Processing system. A critical concern is the filter's signal to noise ratio (SNR). Thus, if a filter has a maximum output swing of $2V_{RMS}$ with noise of $100\mu V_{RMS}$ it can be said to have an SNR (signal to noise ratio) of 86dB. This certainly seems to make it a candidate for anti-aliasing applications before a 14-bit A/D (required SNR approximately 84dB). But, *is this the only consideration??* What is missing in this analysis is a discussion of total harmonic distortion. This is a frequently ignored subtlety of system design.

This filter example has an SNR of 86dB. But suppose its THD is only -47dB. What this means can be better understood by applying a 1kHz signal to the system. What is desired is to digitize this 1kHz to 14-bits of accuracy. What happens is quite different. The 1kHz signal, along with its harmonics, will be digitized. THD (total harmonic distortion)

Note 11: Daryanani, Gobind, "Principles of Active Network Synthesis and Design." New York, NY: John Wiley and Sons, Inc., Copyright 1976.

tion) is a measure of the unwanted harmonics that are introduced by non-linearities in the system. Thus, the 1kHz pure tone will come out looking like 1kHz + 2kHz + 3kHz, etc. The A/D converter will digitize these signals adding errors to the data acquisition process.

Figure 36 illustrates a good way to characterize this potential problem. This figure shows a THD plot of an LTC1064-2 8 pole Butterworth LPF (circuit as shown in Figure 37). The graph shows THD versus input amplitude. A second horizontal scale labels SNR. The graph clearly shows, for instance, that for a 1.5V_{RMS} input the THD is below -70dB and the SNR is below -85dB. Thus, all the harmonics of the input signal (in this case 4kHz) are below -70dB. Figure 38 shows a THD + N versus frequency curve for the same filter. At an input frequency of 2kHz the THD + N is approximately 0.018% or -74.9dB. Figure 39 shows good

correlation with a spectrum analyzer in the frequency domain. Of course, there are an unlimited number of these plots that can be taken, for an almost unlimited number of cutoff frequencies and input frequencies. What must be considered as the most important issue, is that *THD generally limits digitization accuracy, not SNR*. Figure 40 shows four units of the LTC1064-2 with a 1kHz input frequency. Here, as before, the -70dB THD specification is preserved up to 2.5V_{RMS} input.

Total harmonic distortion is a complicated phenomenon and it is difficult to analyze all its potential causes. Some of these causes in the switched capacitor filter are thought to be the charge transfer inherent in the SC process, the output drive and the swing internal to the switched capacitor filter state variable filter.

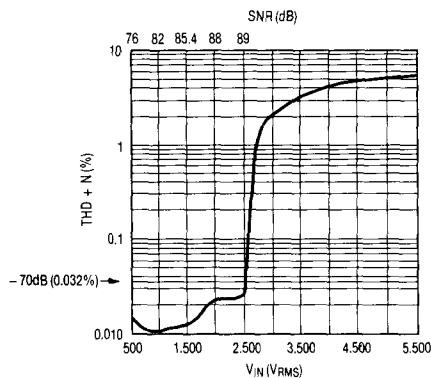


Figure 36. LTC1064-2 THD + Noise vs Input Amplitude and Signal to Noise Ratio. Filter $f_{CUTOFF} = 8\text{kHz}$, $f_{IN} = 4\text{kHz}$, $f_{CLK} = 800\text{kHz}$, $V_S = \pm 5\text{V}$. Inverting Buffer LT1006.

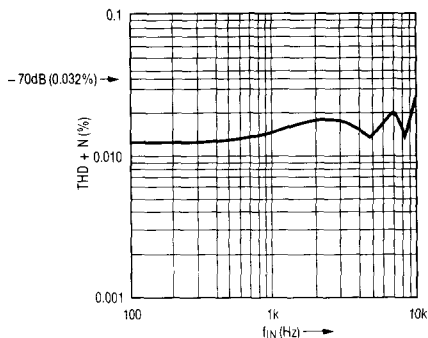


Figure 38. LTC1064-2 THD + Noise vs Input Frequency. Filter $f_{CUTOFF} = 8\text{kHz}$, $f_{CLK} = 800\text{kHz}$, $V_S = \pm 5\text{V}$, $V_{IN} = 1.5\text{V}_{RMS}$. Buffered Output Using LT1006.

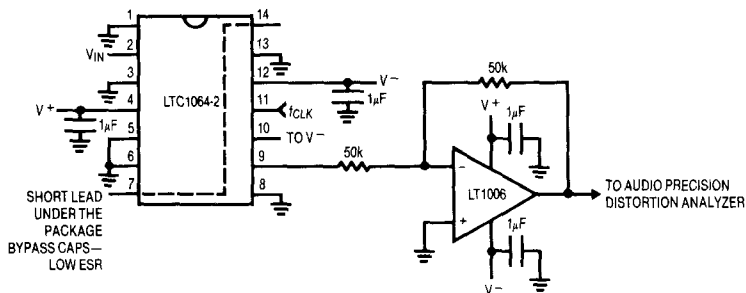


Figure 37. LTC1064-2 Circuit Used for THD Testing. $V_S = \pm 5\text{V}$.

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THD in Active RC Filters

THD in RC active filters is generally assumed to be superior to switched capacitor filters. Traditional filter textbooks seem to lack data on THD, either in a theoretical or a practical sense. The data presented here shows the RC active to be somewhat better than the switched capacitor filter, but at a tremendous cost in terms of board space, non-tunability and cost.

Figure 41 shows a THD versus amplitude plot of the RC active equivalent of the LTC1064-1 8th order Elliptic filter. This filter requires 16 operational amplifiers, 31 resistors and eight capacitors on a board approximately 2-1/2 x 6 inches in size. An equivalent THD plot for the LTC1064-1 is shown in Figure 42.

The Elliptic filters are the worst choice for good THD specifications because of their high Q sections. Butterworth and Bessel filters have very good THD specifications.

Linear Technology has done extensive research in comparing the THD and SNR aspects of our switched capacitor filters to those of active RC filters. In many cases, a filter may be optimized for THD by adjusting its design parameters. This process is specialized and thus data sheet THD specifications may not reflect the best achievable. Call us for more details.

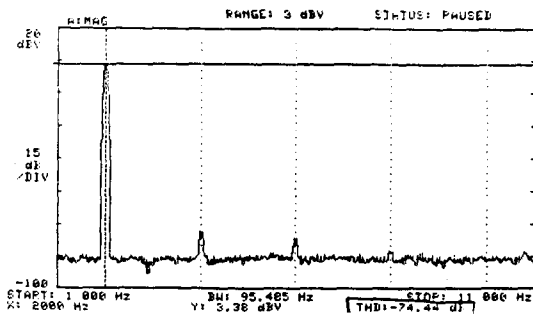


Figure 39. LTC1064-2 Spectrum Analyzer Plot for $V_{IN} = 1.5V_{RMS}$, $f_{IN} = 2kHz$, $V_S = \pm 5V$, Buffered Output Using LT1006

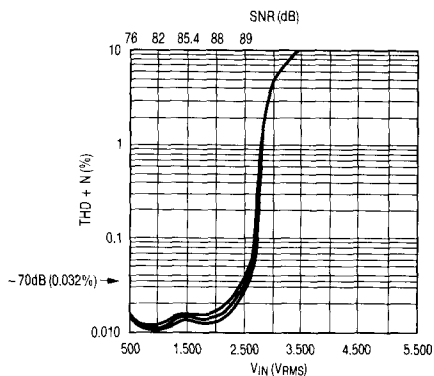


Figure 40. LTC1064-2 THD + Noise vs Input Amplitude and Signal to Noise Ratio. Filter $f_{CUTOFF} = 8kHz$, $f_{CLK} = 800kHz$, $f_{IN} = 1kHz$, $V_S = \pm 5V$, Inverting Buffer Using LT1006. Four Devices Superimposed.

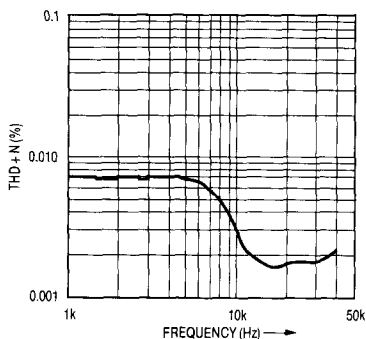


Figure 41. Active RC Implementation of LTC1064-1 8th Order Elliptic Filter. $V_{IN} = 3V_{RMS}$, $V_S = \pm 7.5V$, Op Amps = TL084, $f_c = 40kHz$.

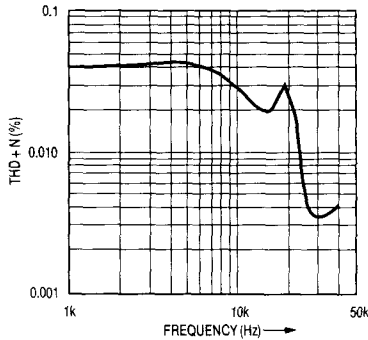


Figure 42. LTC1064-1 8th Order Elliptic Filter. $V_{IN} = 3V_{RMS}$, $V_S = \pm 7.5V$, $f_c = 40kHz$, Buffered Output.

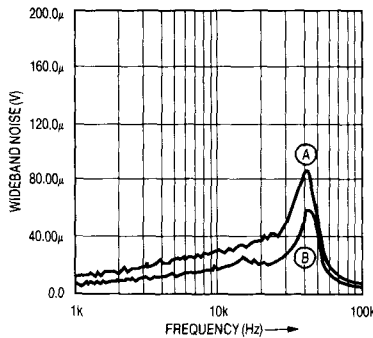


Figure 43. Noise Comparison Between Figure 41 Active RC Elliptic (B) and LTC1064-1 (A), Figure 42

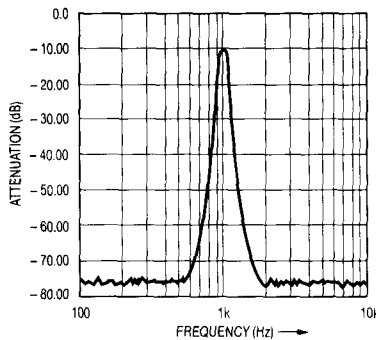


Figure 44. 8th Order Bessel Using LTC1064. $V_S = \pm 8V$, $V_{IN} = 1V_{RMS}$, $f_{CLK} = 50kHz$, $f_{CUTOFF} = 1kHz$, Buffered Output.

Noise in Switched Capacitor Filters

Noise in switched capacitor filters has been on the decline since the invention of the device. At this time many devices, like the LTC1064 family, have noise which competes with active RC filters. What is not immediately obvious is that the noise of the switched capacitor filter is *constant independent of bandwidth*. The LTC1064-2 Butterworth filter has approximately $80\mu V_{RMS}$ noise from 1Hz to 50kHz (f_0 equal to 50kHz), it also has $80\mu V_{RMS}$ noise from 1Hz to 10kHz (f_0 equal to 10kHz). Since the traditional RC active filter has noise specifications based on so many nV per $Hz^{1/2}$, the switched capacitor filter is a better competitor to the active RC as the filter cutoff frequency increases. Future LTC devices will have even better noise specifications than the LTC1064-2.

Figure 43 compares noise between an RC active equivalent of the LTC1064-1 and the switched capacitor filter. Both curves show typical peaking at the corner frequency. The illuminating feature seen in this figure is that the TL084 active filter noise is only slightly better than the LTC1064-1.

Bandpass Filters and Noise — An Illustration

Figure 44 is the frequency response of an 8th order Bessel bandpass filter implemented with an LTC1064 as shown in Figure 45. This filter has a Q of approximately nine and a very linear phase response (in the passband) as shown in Figure 47. As previously discussed, the Bessel response is very useful when signal phase is important.

Of particular interest to the present discussion is the noise of this bandpass filter (Figure 46). Note that the noise bandshape is identical to Figure 44. This is not unusual since the bandpass filter is letting only the noise at a particular f_c through the filter. This is **not** clock feedthru and it is **not** peculiar to the switched capacitor filter. In an active RC, or even an LC passive bandpass filter with these characteristics, noise appears “like a signal” at the center frequency of the BPF.

Note 12: Ghausi, M. S., and K. R. Laker, “Modern Filter Design, Active RC and Switched Capacitor.” Englewood Cliffs, New Jersey: Prentice-Hall, Inc., 1981.

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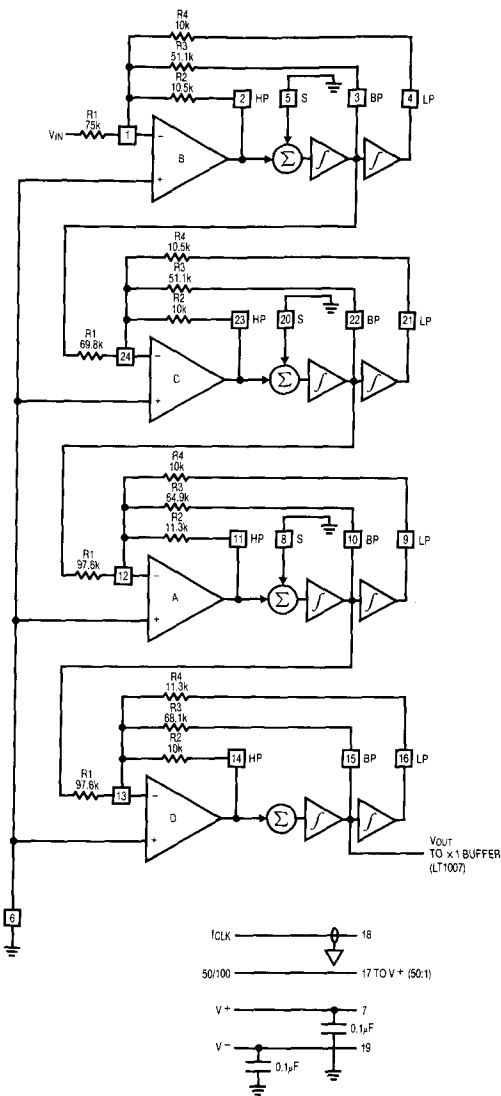


Figure 45. Implementation, Section by Section, of Bessel BPF as per Figure 43 Using LTC1064. For $f_{CUTOFF} = 1\text{kHz}$, $f_{CLK} = 50\text{kHz}$.

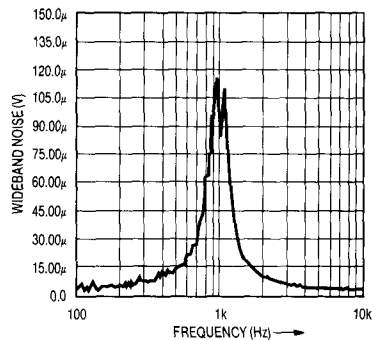


Figure 46. Noise Spectrum of Bessel BPF as Shown in Figure 43. Input Grounded. Total Wideband Noise = $130\mu\text{VRMS}$.

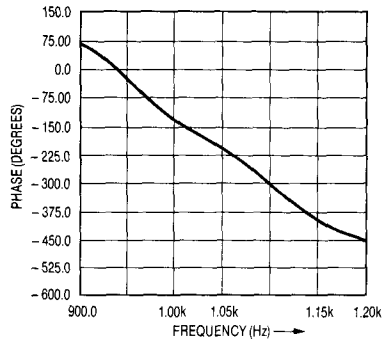


Figure 47. Passband Phase Response of Bessel BPF as Shown in Figure 43. Note the Linear Phase Through the Passband.

CLOCK CIRCUITRY

Jitter

Clocking of switched capacitor filters cannot be taken for granted. A good, stable clock is required to obtain device performance commensurate with the data sheet specifications. This implies that 555 type oscillators are verboten. Often, what appears as insufficient stopband attenuation or excessive passband ripple is, in fact, caused by poor clocking of the switched capacitor filter device.

Figure 48 shows an LTC1064-1 set up to provide cutoff frequency of 500Hz. The clock was modulated (in the top curve measurement) to simulate approximately 50% clock

jitter. The stopband attenuation at 750Hz is seen to be approximately 42dB instead of the specified (in the LTC1064-1 data sheet at $1.5 \times$ the cutoff frequency) 68dB. The second curve on the graph shows the situation when a good stable clock is used.

Similar graphs of the noise in Figures 49 and 50 show the effect of clock jitter on the noise. The wideband noise from 10Hz to 1kHz rises when a jittery clock is used from $156\mu\text{V}_{\text{RMS}}$ to $173\mu\text{V}_{\text{RMS}}$. This is an increase of approximately 11% due only to a poor clocking strategy.

LTC's Application Note 12 provides some good clock sources if none are available in the system.

Clock Synchronization with A/D Sample Clock

Synchronizing the A/D and switched capacitor filter clocks is highly recommended. This allows the A/D to receive filtered data at a constant time and to ensure that the system has settled to its desired accuracy.

Clock Feedthru

While clock feedthru has been greatly improved in the recent generation of switched capacitor filters, some users still want to further limit this anomaly.

The higher the clock to f_{CUTOFF} ratio, the easier it is to filter out clock feedthru.

Figure 20 in the aliasing study shows the clock feedthru at 50kHz to be -61dB . This is below 0dB , which in this case is 500mV . Clock feedthru here is approximately $400\mu\text{V}$. Inserting a simple RC filter (well outside the passband of the filter) at the output of the filter can reduce this by a factor of ten.

Figure 51 shows a similar set of curves with a simple RC on the output of the buffer amplifier (see Figure 4). The RC values were 9.64k and 3300pF . Figure 51 shows that clock feedthru has been reduced to -82dB below 500mV ($40\mu\text{V}$) when this post filter is used.

Post filtering is often unnecessary, as often-times the clock feedthru is out of the band of interest.

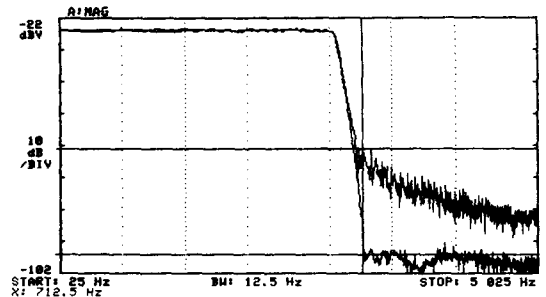


Figure 48. Clock Jitter of Approximately 50% (Top Curve in Stopband) and Jitter Free Clock (Bottom Curve in Stopband) Showing the Difference in Response. LTC1064-1, $f_{\text{CLK}} = 50\text{kHz}$, $f_0 = 500\text{Hz}$, Buffered Output.

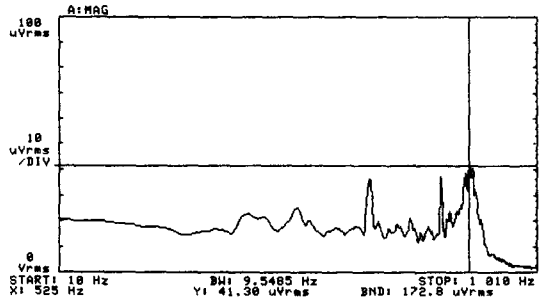


Figure 49. Noise of LTC1064-1 as per Figure 48 with $\approx 50\%$ Clock Jitter. $V_S = \pm 7.5\text{V}$, Input Grounded.

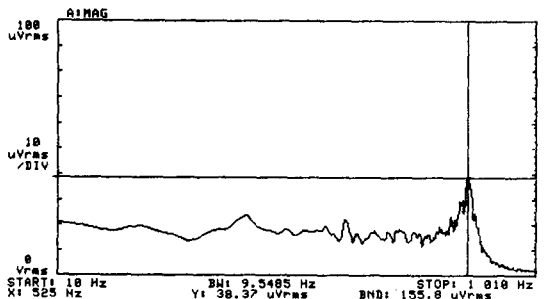


Figure 50. Noise of LTC1064-1 as per Figure 48 with Low Jitter ($< 1\text{ns}$). $V_S = \pm 7.5\text{V}$, Input Grounded.

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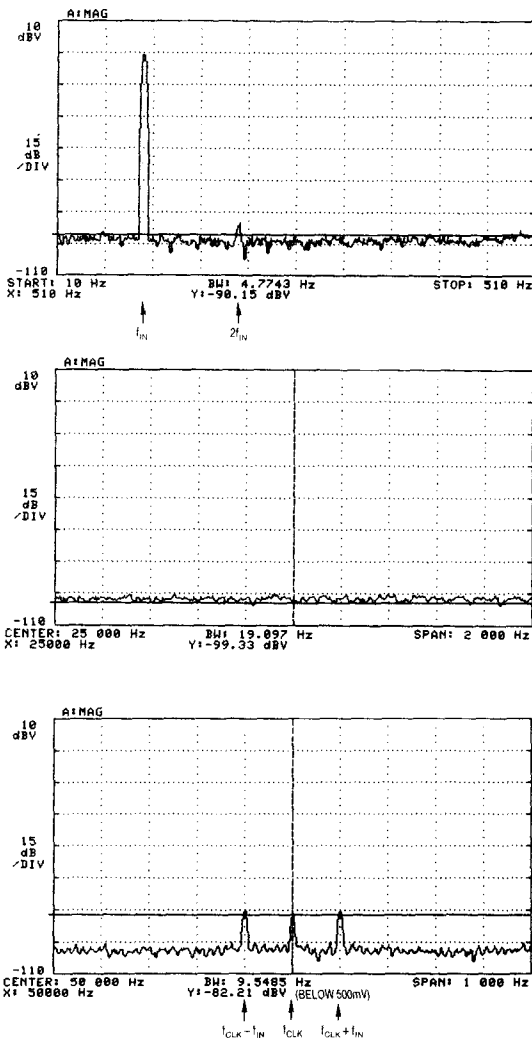


Figure 51. Elliptic Switched Capacitor Filter (LTC1064-1) Clock Feedthru Suppression. $f_0 = 500\text{Hz}$, $f_{CLK} = 50\text{kHz}$, $V_S = \pm 8\text{V}$, $V_{IN} = 100\text{Hz} @ 500\text{mV}_{RMS}$, RC Filter (9.64k, 3300pF) @ Buffer Output, $f_{RC FILTER} = 1/2\pi RC = 5\text{kHz}$.

CONCLUSIONS

Switched capacitor filters are an evolving technology which continues to improve. As this evolution progresses, the switched capacitor filter will replace greater numbers of active RC filters because of the switched capacitor filters inherent smaller size, better accuracy and tunability.

To best take advantage of this evolving technology the system designer must observe good engineering practices as described in this Application Note. More specifically, to properly evaluate and use the current crop of switched capacitor filters as well as parts on the drawing boards one must observe certain precautions:

- 1) Utilize good breadboarding techniques.
- 2) Use a linear power supply. If this is impossible use a clean switcher. Properly bypass the supply.
- 3) Be aware that sampled data systems can alias and be prepared to deal with this limitation. Bandlimit!
- 4) Be aware that the ultimate response in the frequency domain is not the ultimate response in the time domain and vice versa. Look at both responses on the bench before committing a filter to the PCB or silicon.
- 5) Understand THD and signal to noise ratio and where one limits the other.
- 6) Provide a good clean clock to the switched capacitor filter to avoid problems caused by too much clock jitter.

APPENDIX A

Square Wave to Sine Wave Conversion Graphically Illustrates the Frequency Domain, Time Domain and Aliasing Aspects of Switched Capacitor Filters

Figures 52 through 63 illustrate yet another use of the versatile switched capacitor filter. In the past it has been difficult to obtain a good clean sine wave locked to a square wave input, if the square wave varies in frequency. In this example a square wave is filtered by an Elliptic filter (the LTC1064-1) to produce an excellent sine wave which is phase locked to the input. A Butterworth filter (the LTC1064-2) will also work for this application, but the sine wave will not be quite as pure.

The series of figures illustrates a varied input square wave (from 1kHz to 7500Hz) to an LTC1064-1 Elliptic filter. Recall that a square wave consists of odd harmonics of the fundamental; that is, a 1kHz square wave should contain (in the mathematical world) 1kHz, 3kHz, 5kHz, 7kHz, 9kHz, 11kHz . . . spectral lines, *that is sine waves*, all added together to produce the 1kHz square wave.

Figure 53 and 54 show the Elliptic filter passing the 1kHz square wave with poor fidelity. As the input frequency increases, the fidelity decreases as fewer and fewer of the square waves' spectral lines are passed through the filter.

Figures 56 and 57 show the spectrum analyzer and oscilloscope response from the filter's output for an input square wave of 2.5kHz.

Figure 59 and 60 show the frequency and time domain responses from the filter's output for an input square wave of 5kHz. The 10kHz cutoff frequency of the filter passes only the first harmonic (5kHz) and the 10kHz second harmonic (which is a signal generator problem and should not be there at all). The output appears to be a nice clean sine wave as seen in Figure 60.

Figure 61 shows the input spectrum of a 7.5kHz square wave. Figure 62 is the output from the filter in the frequency domain. In addition to the 7.5kHz spectral line producing the sine wave shown in Figure 63, there are other lines. These lines at 2.5, 5, 10 and 12.5kHz are the result of the 132nd, 133rd, 134th and 135th (!!!!!) harmonics of the 7.5kHz fundamental frequency of the input square wave aliasing back into the passband of the filter. The perfect

square wave should not contain even harmonics but the 133rd and 135th harmonic would remain. Again, **WARNING: Bandlimit your input signal or risk aliasing!**¹³

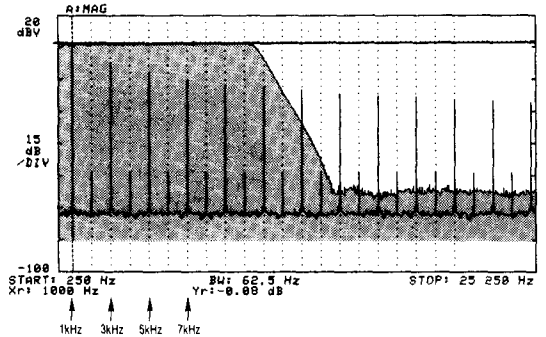


Figure 52. Frequency Domain (Spectrum Analyzer) Plot of 1kHz Square Wave (5Vp-p) Input to LTC1064-1 as Configured in Figure 4. $f_{CUTOFF} = 10\text{kHz}$. Shaded Area is the Frequency Response of the Filter.

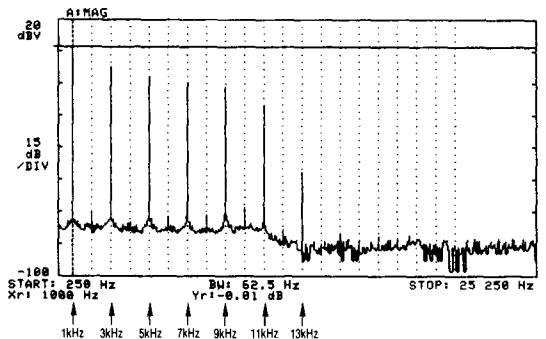


Figure 53. Filter Output (Shown in Frequency Domain) for 1kHz Input. Note Raised Noise Floor Due to LTC1064-1 Approx. 75dB Noise Level.

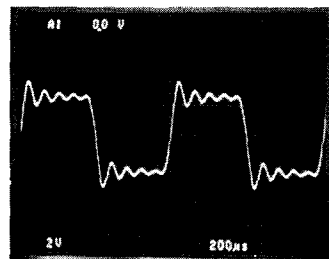


Figure 54. Filter Time Domain Output for Input 1kHz Square Wave

Note 13: Thanks to Lew Cronis for the inspiration to do this appendix.

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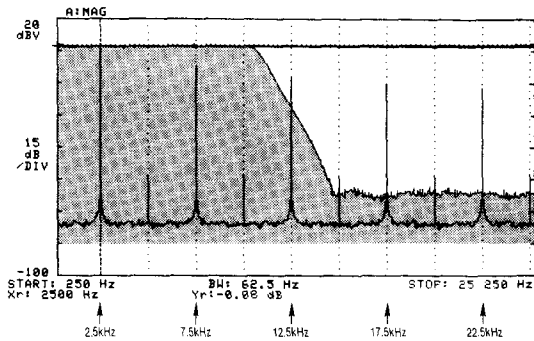


Figure 55. Frequency Domain (Spectrum Analyzer) Plot of 2500Hz Square Wave (5Vp-p) Input to LTC1064-1 as Configured in Figure 4. $f_{CUTOFF} = 10\text{kHz}$. Shaded Area is the Frequency Response of the Filter.

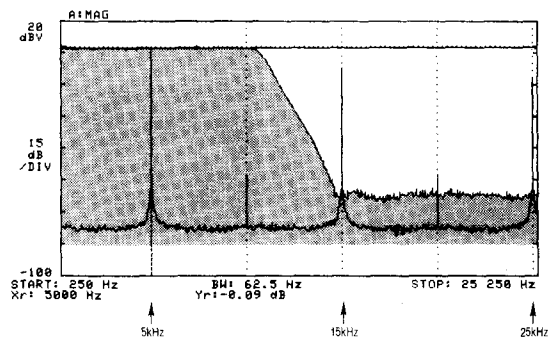


Figure 58. Frequency Domain (Spectrum Analyzer) Plot of 5kHz Square Wave (5Vp-p) Input to LTC1064-1 as Configured in Figure 4. $f_{CUTOFF} = 10\text{kHz}$. Shaded Area is the Frequency Response of the Filter.

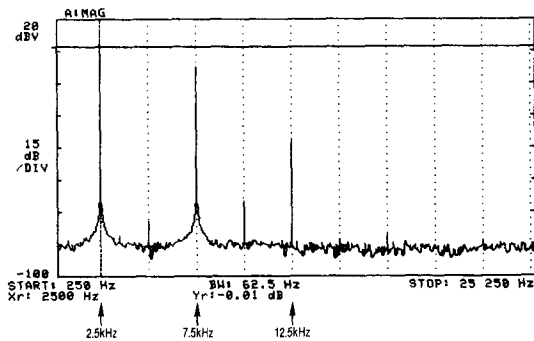


Figure 56. Filter Output (Shown in Frequency Domain) for 2500Hz Input. Note Raised Noise Floor Due to LTC1064-1 Approx. 75dB Noise Level.

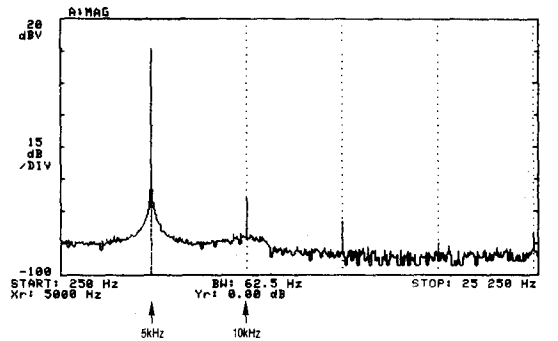


Figure 59. Filter Output (Shown in Frequency Domain) for 5kHz Input. Note Raised Noise Floor Due to LTC1064-1 Approx. 75dB Noise Level.

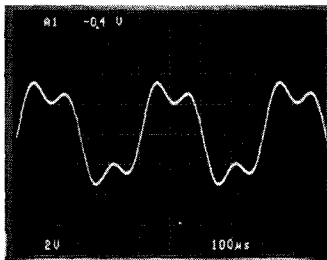


Figure 57. Filter Time Domain Output for Input 2500Hz Square Wave

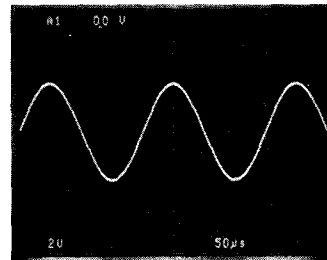


Figure 60. Filter Time Domain Output for Input 5kHz Square Wave

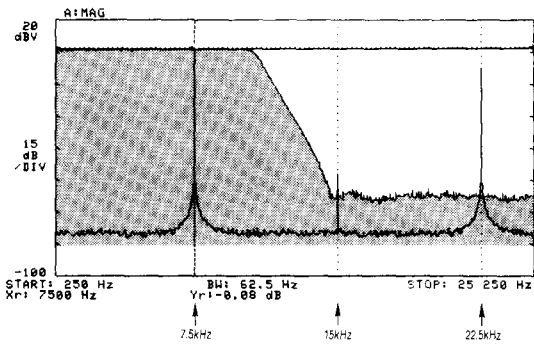


Figure 61. Frequency Domain (Spectrum Analyzer) Plot of 7500Hz Square Wave (5Vp-p) Input to LTC1064-1 as Configured in Figure 4. $f_{CUTOFF} = 10\text{kHz}$. Shaded Area is the Frequency Response of the Filter.

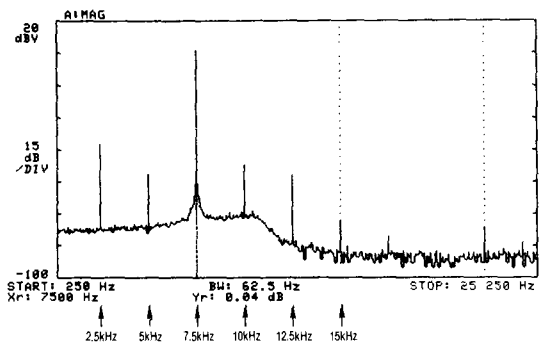


Figure 62. Filter Output (Shown in Frequency Domain) for 7500Hz Input. Note Raised Noise Floor Due to LTC1064-1 Approx. 75dB Noise Level.

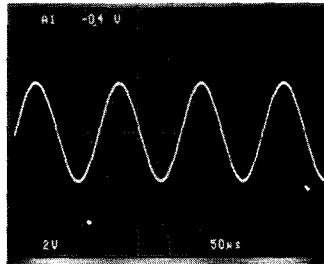


Figure 63. Filter Time Domain Output for Input 7.5kHz Square Wave

APPENDIX B

About Bypass Capacitors

Bypass capacitors are used to maintain low power supply impedance at the point of load. Parasitic resistance and inductance in supply lines mean that the power supply impedance can be quite high. As frequency goes up, the inductive parasitic becomes particularly troublesome. Even if these parasitic terms did not exist, or if local regulation is used, bypassing is still necessary because no power supply or regulator has zero output impedance at 100MHz. What type of bypass capacitor to use is determined by the application, frequency domain of the circuit, cost, board space and many other considerations. Some useful generalizations can be made.

All capacitors contain parasitic terms, some of which appear in Figure B1. In bypass applications, leakage and dielectric absorption are second order terms but series R and L are not. These latter terms limit the capacitor's ability to damp transients and maintain low supply impedance. Bypass capacitors must often be large values so they can absorb long transients, necessitating electrolytic types which have large series R and L.

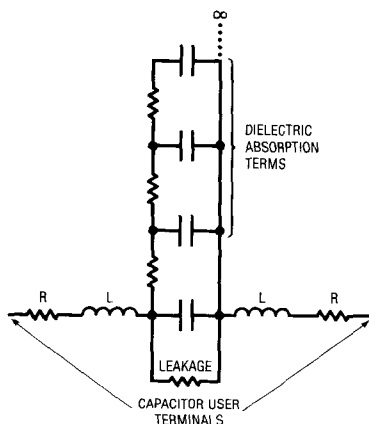


Figure B1. Parasitic Terms of a Capacitor

Different types of electrolytics and electrolytic-non-polar combinations have markedly different characteristics. Which type(s) to use is a matter of passionate debate in some circles and the test circuit (Figure B2) and accompanying photos are useful. The photos show the response of five bypassing methods to the transient generated by the test circuit. Figure B3 shows an unbypassed line which sags and ripples badly at large amplitudes. Figure B4 uses an aluminum $10\mu\text{F}$ electrolytic to considerably cut the disturbance, but there is still plenty of potential trouble. A tantalum $10\mu\text{F}$ unit offers cleaner response in B5 and the $10\mu\text{F}$ aluminum unit combined with a $0.01\mu\text{F}$ ceramic type is even better in B6. Combining electrolytics with non-polarized capacitors is a popular way to get good response but beware of picking the wrong duo. The right (wrong) combination of supply line parasitics and paralleled dissimilar capacitors can produce a resonant, ringing response, as in B7. Caveat!

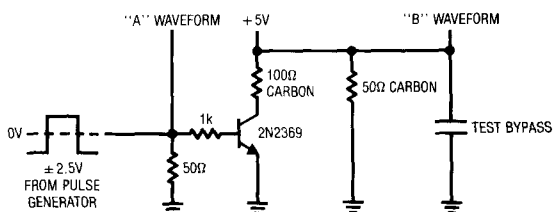


Figure B2. Bypass Capacitor Test Circuit

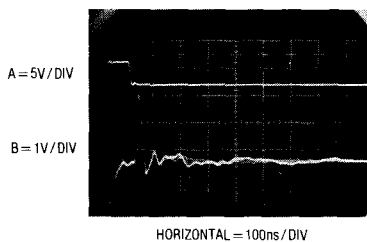


Figure B3. Response of Unbypassed Line

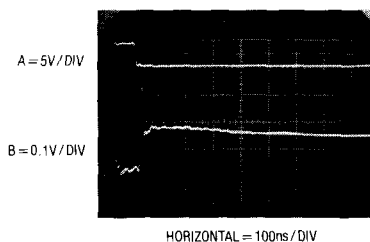


Figure B4. Response of 10 μ F Aluminum Capacitor

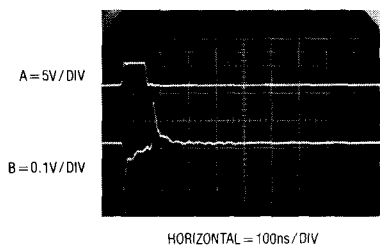


Figure B5. Response of 10 μ F Tantalum Capacitor

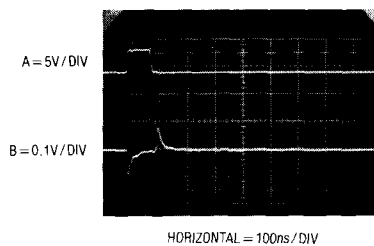


Figure B6. Response of 10 μ F Aluminum Paralleled by 0.01 μ F Ceramic

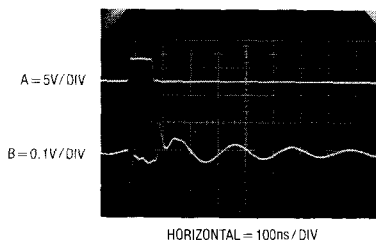


Figure B7. Some Paralleled Combinations Can Ring. Try Before Specifying!

Application Note 40

Thanks to Nello Sevastopoulos, Philip Karantzalis and Kevin Vasconcelos for their generous assistance with this Application Note. Thanks to Lew Cronis for the inspiration to do Appendix A.

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SECTION 2—DESIGN NOTES

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New Data Acquisition Systems Communicate with Microprocessors Over 4 Wires

As board space and semiconductor package pins become more valuable, serial data transfer methods between microprocessors (MPUs) and their peripherals become more and more attractive. Not only does this save lines in the transmission medium, but, because of the savings in package pins, more function can be packed into both the MPU and the peripheral. Users are increasingly able to take advantage of these savings as more MPU manufacturers develop serial ports for their products¹⁻³. However, peripherals which are able to communicate with these MPUs must be available in order for users to take full advantage. Also, MPU serial formats are not standardized so not all peripherals can talk to all MPUs.

The LTC1090 Family

A new family of 10-bit data acquisition circuits has been developed to communicate over just 4 wires to the recently developed MPU synchronous serial formats as well as to MPUs which do not have serial ports. These circuits feature software configurable analog circuitry including analog multiplexers, sample and holds, bipolar and unipolar conversion modes. They also have serial ports which can be software configured to communicate with virtually any MPU. Even the lowest grade device features guaranteed $\pm 0.5\text{LSB}$ linearity over the full operating temperature range. Reduced span operation (down to 200mV), accuracy over a wide temperature range and low power single supply operation make it possible to locate these circuits near remote sensors and transmit digital data back through noisy media to the MPU. Figure 1 shows a typical hookup of the LTC1090, the first member of this data acquisition family. For more detail, refer to the 24-page LTC1090 data sheet.

Included are eight analog inputs which can common-mode to both supply rails. Each can be configured for unipolar or bipolar conversions and for single-ended or differential inputs by sending a data input (D_{IN}) word from the MPU to the LTC1090 (Figure 1).

Both the power supplies are bypassed to analog ground. The V^- supply allows the device to operate with inputs which swing below ground. In single supply applications it can be tied to ground.

The span of the A/D converter is set by the reference inputs which, in this case, are driven by a 2.5V LT1009 which gives an LSB step size of 2.5mV. However, any reference voltage within the power supply range can be used.

The 4 wire serial interface consists of an active low chip select pin (\overline{CS}), a shift clock (SCLK) for synchronizing the data bits, a data input (D_{IN}) and a data output (D_{OUT}). Data is transmitted and received simultaneously (full duplex), minimizing the transfer time required.

The external ACLK input controls the conversion rate and can be tied to SCLK as in Figure 1. Alternatively, it can be derived from the MPU system clock (e.g., the 8051 ALE pin) or run asynchronously. When the ACLK pin is driven at 2MHz, the conversion time is 22 μ s.

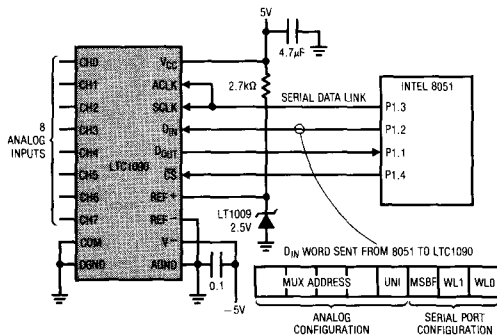


Figure 1. A Typical Hookup of the LTC1090

Advantages of Serial Communications

The LTC1090 can be located near the sensors and serial data can be transmitted back from remote locations through isolation barriers or through noisy media.

Several LTC1090s can share the serial interface and many channels of analog data can be digitized and sent over just a few digital lines (see Figure 2). This could, for example, be used to simplify the communications between an instrument and its front panel.

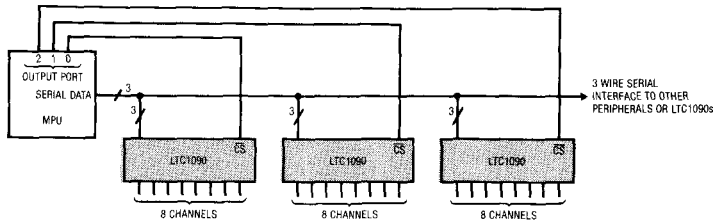


Figure 2. Several LTC1090s Sharing One 3 Wire Serial Interface

Using fewer pins for communication makes it possible to pack more function into a smaller package. LTC1090 family members are complete systems being offered in packages ranging from 20 pins to 8 pins (e.g., LTC1091).

Speed is Usually Limited by the MPU

A perceived disadvantage of the serial approach is speed. However, the LTC1090 can transfer a 10-bit A/D result in $10\mu\text{s}$ when clocked at its maximum rate of 1MHz. With the minimum conversion time of $22\mu\text{s}$, throughput rates of 30kHz are possible. In practice, the serial transfer rate is usually limited by the MPU, not the LTC1090. Even so, throughput rates of 20kHz are not uncommon when serial port MPUs are used. For MPUs without serial ports, the transfer time is somewhat longer because the serial signals are generated with software. For example, with the Intel 8051 running at 12MHz, a complete transfer takes $80\mu\text{s}$. This makes possible throughput rates of approximately 10kHz.

Talking to Serial Port MPUs

By accommodating a wide variety of transfer protocols, the LTC1090 is able to talk directly to almost all synchronous serial formats. The last 3 bits of the LTC1090 data input (D_{IN}) word define the serial format. The MSBF bit determines the sequence in which the A/D conversion result is sent to the processor (MSB or LSB first). The two bits WL1 and WLO define the word length of the LTC1090 data output word. Figure 3 shows several popular serial formats and the appropriate D_{IN} word for each. Typically a complete data transfer cycle takes only about 15 lines of processor code.

Talking to MPUs without Serial Ports

The LTC1090 talks to serial port processors but works equally well with MPUs which do not have serial ports. In these cases, \overline{CS} , SCLK and D_{IN} are generated with software on 3 port lines. D_{OUT} is read on a fourth. Figure 3 shows the appropriate D_{IN} word for communicating with MPU parallel ports. Figure 1 shows a 4 wire interface to the popular Intel 8051. A complete transfer takes only 33 lines of code.

Sharing the Serial Interface

No matter what processor is used, the serial port can be shared by several LTC1090s or other peripherals (see Figure 2). A sepa-

rate \overline{CS} line for each peripheral determines which is being addressed.

Conclusions

The LTC1090 family provides data acquisition systems which communicate via a simple 4 wire serial interface to virtually any microprocessor. By eliminating the parallel data bus they are able to provide more function in smaller packages, right down to 8 pin DIPs. Because of the serial approach, remote location of the A/D circuitry is possible and digital transmission through noisy media or isolation boundaries is made easier without a great loss in speed.

Hardware and software is available from the factory to interface the LTC1090 to most popular MPUs. The LTC1090 data sheet contains source code for several microprocessors. Further applications assistance is available by calling the factory.

LTC1090 D_{IN} Word						
Type of Interface	LTC1090 Data Format	Analog Configuration	MSBF	WL1	WLO	
All Parallel Port MPUs	MSB First 10 Bits	X X X X X X	1	0	1	
National MICROWIRE*	MSB First 12 Bits	X X X X X X X X	1	1	0	
MICROWIRE/PLUS*	MSB First 16 Bits	X X X X X X X X X X	1	1	1	
Motorola SPI	LSB First 16 Bits	X X X X X X X X	0	1	1	
Hitachi Synchronous SCI		X X X X X X X X	0	1	1	
TI TMS7000 Serial Port		X X X X X X X X	0	1	1	

Figure 3. The LTC1090 Accommodates Both Parallel and Serial Ports

*MICROWIRE and MICROWIRE/PLUS are trademarks of National Semiconductor Corp.

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For LTC1090 literature call 800-637-5545. For help with an application call (408) 432-1900, Ext. 361.

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Sampling of Signals for Digital Filtering and Gated Measurements

William Rempfer

Introduction

For many signal processing applications a sample and hold function is required in a data acquisition system. It is often critical for the processing system to know the exact value of an analog input at an exact time. In DSP applications such as digital filters the usable bandwidth of the system is limited by the Nyquist frequency and the sample and hold bandwidth need only be, and is often intentionally limited to, one half the sampling rate. However, another area of application requires infrequently capturing instantaneous values of relatively fast signals, sometimes referred to as gated measurements. In the extreme case of pulse height measurements, only one sample point is required. Here, the sample and hold bandwidth should be as high as possible even though the sampling rate is very low.

The LTC1090 excels in both environments. This note shows how the LTC1090 sample and hold can be synchronized to an external event and gives two simple applications: an 8 channel data acquisition system with digital filtering, and the gated measurement of a 1MHz sine wave.

The LTC1090 Sample and Hold

The LTC1090 provides a sample and hold which is fast, accurate and can be synchronized to an external event. Although the sampling rate is limited (by the A/D conversion and data transfer rate) to about 30kHz, the signal bandwidth of the sample and hold exceeds 1MHz. The acquisition time is less than $1\mu\text{s}$ to 0.1% (1LSB). Accuracy is so good, in fact, that it is possible to include all the sample and hold's error contributions (offset, gain, hold step, droop rate, etc.) into the converter specification and still maintain overall system accuracy of $\pm 0.05\%$ ($\pm 0.5\text{LSB}$) over temperature.

Sampling occurs on the falling edge of the last data transfer clock pulse as described in the LTC1090 data sheet. Figure 1 shows a typical application which includes circuitry to synchronize sampling to an external sample clock, f_s .

8-Channel Data Acquisition System with Digital Filter

The circuit of Figure 1 contains an LTC1090 providing multiplexing, sample and hold, A/D conversion and data transfer to the microcontroller (MCU). An MC68HC05C4 is used as the

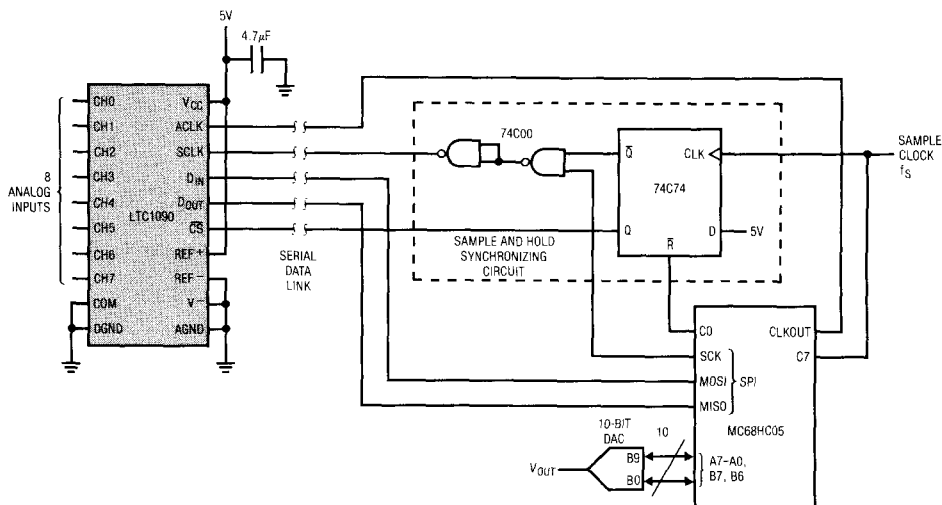


Figure 1. 8 Channel Data Acquisition System Showing Sample and Hold Synchronizing Circuitry

controller (much higher filter performance may be achieved with a dedicated DSP processor). The MCU communicates with the LTC1090 over the serial peripheral interface (SPI), performs the digital filtering algorithm and provides the filtered data on its output port. The DAC provides reconstruction of the filtered waveform for viewing on an oscilloscope or spectrum analyzer. The 74C74 and 74C00 synchronize the sampling of the LTC1090 to the externally applied sample clock, f_s .

In Figure 1, the MCU initiates a two byte serial data exchange with the LTC1090. This configures the LTC1090 for the next conversion, simultaneously reads back the previous conversion result and resets the 74C74. The LTC1090 will sample the analog input when the last shift clock (SCLK) pulse falls, so the MCU must end the data transfer by leaving the SCLK in a high state. This inhibits sampling of the selected analog input. When the sample clock, f_s , rises, it clocks the 74C74 which raises the CS and drops the SCLK. This falling SCLK causes the sample to be taken and starts the conversion. After the MCU senses the rising sample clock it waits for the conversion to be completed (44 ACLK cycles) and then initiates another data exchange, preparing the LTC1090 for the next sample. This cycle repeats.

4th Order Elliptic Filter

Using the circuit of Figure 1, a 4th order elliptic digital filter was implemented. 10 bit input and output data words and 14 bit coefficients were used with the same coefficients being used for each channel. A direct form II IIR filter was implemented according to the following equations:

$$D(n) = [7203 \times D(n-1) - 19209 \times D(n-2) + 6324 \times D(n-3) - 4383 \times D(n-4)] \times 2^{-14} + X(n)$$

$$Y(n) = [3069 \times D(n) + 5505 \times D(n-1) + 7824 \times D(n-2) + 5504 \times D(n-3) + 3066 \times D(n-4)] \times 2^{-14}$$

where: $X(n)$ = filter input value
 $Y(n)$ = filter output value
 $D(n)$ = delay node value

The filter frequency response is shown in Figure 2. The cutoff frequency is 175Hz, one fourth the sample frequency of 700Hz. The cutoff frequency of the filter can be tuned by varying the frequency of the sample clock.

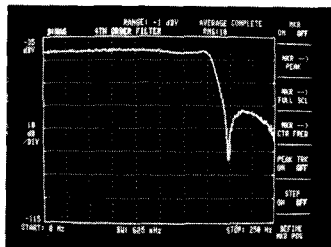


Figure 2. Spectrum of 4th Order Elliptic Digital Filter used in the Data Acquisition System, $f_c = 175\text{Hz}$

Because of 68HC05 speed and instruction set limitations, sample rate is limited by the MCU's ability to perform the DSP algorithm. Maximum sample rate was determined to be 700Hz for a single channel filter and 90Hz for eight channels. Using a high performance DSP would allow sample rates approaching the limit of 30kHz for one channel and 3.7kHz for all eight set by the LTC1090. Hopefully, this simple example will encourage the reader to pursue higher order, higher performance applications.

If large amplitude, unwanted AC signals are present on the inputs, a linear filter such as the LTC1062 can be used to remove them and prevent reduction in the dynamic range of the system.

Gated Measurements of Fast Signals

As an example of gated measurements, the circuit of Figure 1 was used with no filtering to repetitively sample a 5Vp-p 1MHz sine wave. The waveform was sampled at 15kHz (approximately one sample every 67 cycles of the 1MHz waveform). A 20ns pulse, triggered off the sample clock, was applied to the z-axis input of a storage scope to illuminate one dot on the CRT per sample. Samples were allowed to accumulate on the storage scope as shown in Figure 3. The upper waveform is the sampled input to the LTC1090 and the lower waveform is the sampled output of the DAC. (Remember that the waveforms are not real time: one dot was illuminated only every 67 cycles of the 1MHz sine wave.) With this technique the signal bandwidth of the LTC1090 sample and hold was determined to be 2MHz.

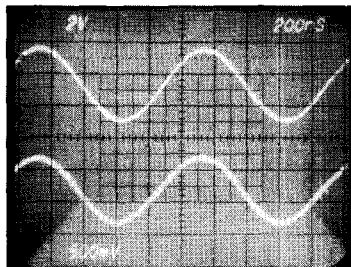


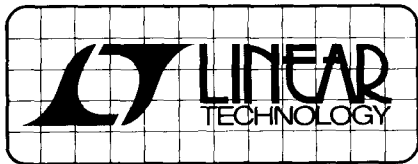
Figure 3. Input and Output Sample Points of a 1MHz Sine Wave Accumulated on a Storage Scope

Using the LTC1090 sample and hold, high speed circuits such as a 1MHz bandwidth AC to DC converter are possible. Because the acquisition time is less than $1\mu\text{s}$ it is also possible to make a gated measurement of the height of a pulse as narrow as $1\mu\text{s}$ to 0.1% accuracy.

For LTC1090 literature call 800-637-5545. For help with an application call (408) 432-1900, Ext. 361.

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DESIGN NOTES

Number 3 in a series from Linear Technology Corporation

October, 1987

Operational Amplifier Selection Guide for Optimum Noise Performance

George Erdi

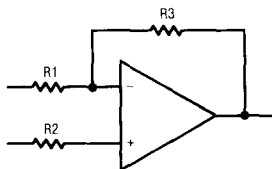
The LT1028 is the lowest noise op amp available today. Its voltage noise is less than that of a 50Ω resistor. In other words, if the LT1028 is operated with source resistors in excess of 50Ω, resistor noise will dominate. If the application requires large source resistors, the LT1028's relatively high current noise will limit performance, and other op amps will provide lower overall noise.

In general, the total noise of any op amp (referred to the input) is given by:

$$\text{total noise} = \sqrt{(\text{voltage noise})^2 + (\text{resistor noise})^2 + (\text{current noise} \times R_{eq})^2}$$

where,

$$\begin{aligned} \text{resistor noise} &= 0.13\sqrt{R_{eq}} \text{ in } nV/\sqrt{Hz} \\ \text{and } R_{eq} &= \text{equivalent source resistance} \\ &= R2 + R1//R3 \end{aligned}$$



Several conclusions can be reached by inspection of the equation:

- (a) To minimize noise, resistor values should be minimized to make the contribution of the second and third terms of the equation negligible. Don't forget, however, that feedback resistor R3 is a load on the output.
- (b) Total noise is dominated by:
 - (i) voltage noise at low R_{eq} ,
 - (ii) resistor noise at mid R_{eq} ,
 - (iii) current noise at high R_{eq} , because resistor noise is proportional to $\sqrt{R_{eq}}$, while the current noise contribution to total noise is proportional to R_{eq} .

The table below lists which op amp gives minimum total noise for a specified equivalent source resistance. A two step procedure should be followed to optimize noise:

- (1) Reduce equivalent source resistance to a minimum allowed by the specific application.
- (2) Enter the table to find the optimum op amp.

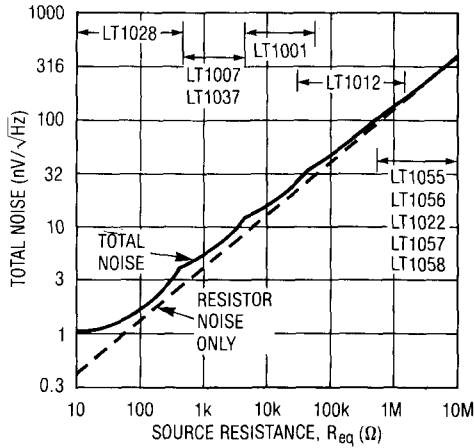
The table actually has two sets of devices: one for low frequency (instrumentation), one for wideband applications. The slight differences between the two columns occur because voltage and current noise increase at low frequencies (below the so-called 1/f corner) while resistor noise is flat with frequency.

Best Op Amp for Lowest Noise vs Source Resistance

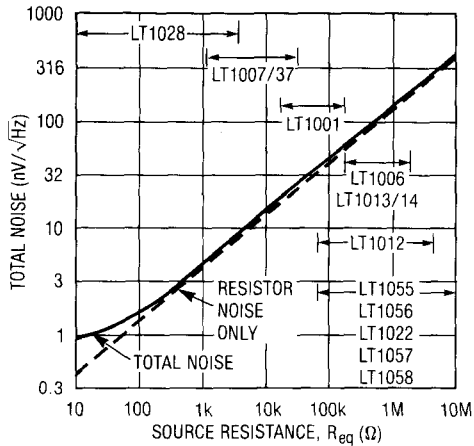
SOURCE R (R_{eq})	BEST OP AMP	
	@ LOW FREQ. (10Hz)	@ WIDEBAND (1kHz)
0Ω to 400Ω	LT1028	LT1028
400Ω to 1k	LT1007/37	LT1028
1k to 4k	LT1007/37	LT1028, LT1007/37
4k to 15k	LT1001	LT1007/37
15k to 30k	LT1001	LT1001, LT1007/37
30k to 70k	LT1001, LT1012	LT1001
70k to 150k	LT1012	LT1001, LT1012 LT1055/56/22, LT1057/58
150k to 600k	LT1012, LT1006/13/14	LT1012, LT1006/13/14 LT1055/56/22, LT1057/58
600k to 2M	LT1012 LT1055/56/22, LT1057/58	LT1012, LT1006/13/14 LT1055/56/22, LT1057/58
2M to 10M	LT1055/56/22, LT1057/58	LT1012 LT1055/56/22, LT1057/58
> 10M	LT1055/56/22, LT1057/58	LT1055/56/22, LT1057/58

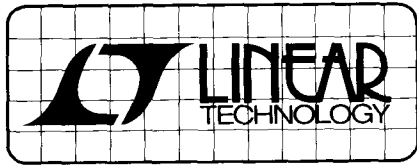
The actual achievable total noise is plotted at 10Hz and 1kHz. The striking feature of these plots is that with the proper selection of op amps total noise is dominated by equivalent source resistor noise over a five decade (100Ω to 10MΩ) range.

10Hz Total Noise vs Equivalent Source Resistance



1kHz Total Noise vs Equivalent Source Resistance





DESIGN NOTES

Number 4 in a series from Linear Technology Corporation

November, 1987

New Developments in RS232 Interfaces

Robert Dobkin

New RS232 interface chips have been developed that offer significant advantages over older devices such as the 1488 and 1489. The new RS232 interface ICs improve speed, power, voltage supply requirements, and protection over older devices. Further, the new chips are easier to use, requiring fewer external components and may be turned off to a "zero" power supply current condition for use in battery powered systems.

The new RS232 drivers are implemented in a monolithic bipolar technology. A unique output stage was designed that provides large output swings, minimizing power supply voltage requirements, while retaining outstanding overload protection features. The outputs can be driven beyond the power supply voltage without drawing excessive current or forcing current back into the power supplies. Of course, current limiting is included to protect against short circuit conditions.

Initial consideration of technologies for implementing RS232 interfacing might include CMOS as a possible technology for this type of application. Power supply requirements are low, output voltage swing is high, and higher voltage CMOS technologies are available to allow operation up to $\pm 15V$. Consideration of some of the problems associated with CMOS decreases its attractiveness for RS232 drivers.

Inherent in the CMOS structure, are diodes between the drain and source of the CMOS devices and the power supplies as is shown in Figure 1. A requirement of RS232 interfaces is the ability to withstand voltage applied to the output pins. With a CMOS output stage this is achieved with the inclusion of a 300Ω resistor in series with the output. (The resistor is similar to the resistors included in older drivers.) It protects the interface chip, but still allows damage to other devices powered by the same supply.

A problem occurs when the output of a driver which is powered from the 5V logic supply is connected to an external 12V or 15V source as is allowed by the RS232 specification. Ex-

ternal current flows through the 300Ω limiting resistor, through the diodes, which are a part of the CMOS structure, and into the power supply. This forces the power supply to 12V or 15V damaging the 5V logic that is connected to the supplies. This problem can even cause latchup if the logic supply is off when external RS232 signals feed voltage into the supply. This problem did not usually exist in the past, because the RS232 interfaces were powered by separate $\pm 12V$ supplies.

ESD damage is probably the most frequent cause of failure of interface chips. Bipolar devices are relatively rugged but still can be damaged by ESD. System requirements for ESD may be as high as 20kV. No IC can withstand that much voltage without external protection.

A requirement of the RS232 specification is the ability to withstand $\pm 25V$ input signals. The CMOS LTC1045 which is used as an RS232 receiver has been designed to operate with external resistors in series with the input. These resistors allow very large voltage swings at the input pins and provide ESD protection to the IC. Using on-chip resistors precludes the use of the optimum ESD protection structures, so CMOS devices may be more sensitive to ESD destruction at their inputs.

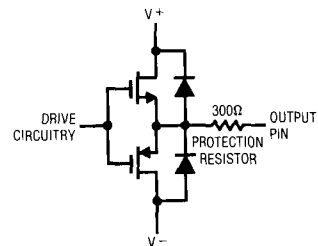


Figure 1. CMOS Line Driver Showing Parasitic Diodes to the Power Supplies

The output stage of the bipolar drivers is shown in Figure 2. Opposed collector NPN and PNP transistors give the widest possible output swings. The PNP transistor will swing to within 200mV of the positive supply while the NPN transistor with its associated Schottky diode will swing within about 900mV of the negative supply. If the output voltage is forced above the positive supply the emitter base junction of the PNP transistor reverse biases, and no current flows into the supply. The device is unaffected by external voltage up to the breakdown voltage of the transistor. If the output is forced below the negative supply, the Schottky diode reverse biases and prevents external current flow into the chip. Capacitor C1 is used to control the output slew rate so that no frequency compensation components are required to meet the RS232 specification of $4V/\mu s$ to $30V/\mu s$.

Typically the slew rate of these drivers is about $8-10V/\mu s$. This allows them to be used successfully up to about 64k baud. The output slew rate of the bipolar drivers is well controlled by an internal capacitor and relatively independent of load resistance or capacitance. The bipolar receiver is relatively straightforward utilizing a level detector with hysteresis to set the trip point. Nominally the trip point is set at about 1.5V with 200mV of hysteresis. The receivers go into a high output state with an open input. The receivers outputs are both TTL and CMOS compatible.

A recent advance in the drivers and receivers is on-chip power supply generation. Devices like the LT1080 and LT1081 include an oscillator, capacitive voltage doubler, and capacitive inverter to generate $\pm 9V$ from the 5V power supply. The charge-pump power supply generator requires only four $1\mu F$ capacitors to generate RS232 communication levels from a 5V logic supply. Figure 3 shows a typical hook-up for the

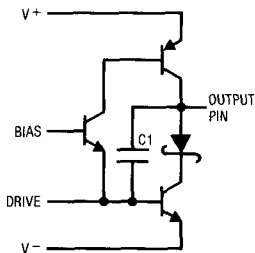


Figure 2. New Bipolar Driver Output Stage

LT1080. The on-chip power supply generators generate excess power over the LT1080 requirements, so another RS232 communication device such as the LT1039 can be powered from the same power supply generator. Table 1 gives typical performance of all Linear Technology driver/receiver devices for RS232 communication.

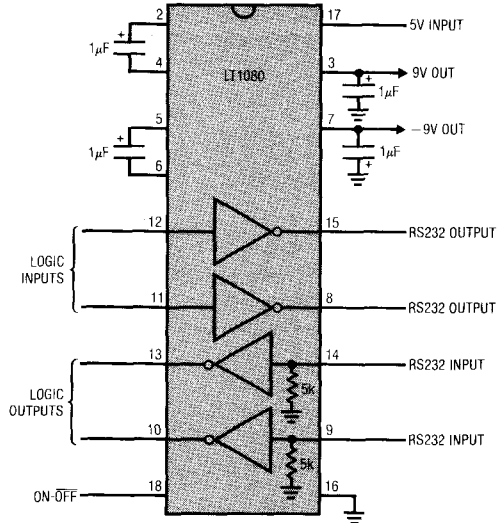
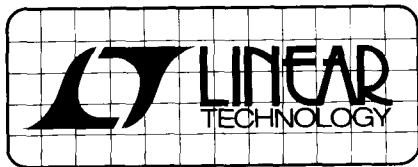


Figure 3. 5V Powered RS232 Driver/Receiver

Table 1. New Drivers and Receivers

DEVICE	DRVS	RECS	SHUT-DOWN	SUPPLY GENERATOR	REMARKS
LT1030	4		X		Low Cost
LT1032	4		X		RS423 Compatible
LT1039	3	3	X		
LT1039N16	3	3			MC145406 Compatible
LTC1045		6	X		Micropower
LT1080	2	2	X	X	
LT1081	2	2		X	MAX232 Compatible
LT1130	5	5		X	
LT1131	5	4	X	X	
LT1132	5	3		X	
LT1133	3	5		X	
LT1134	4	4		X	
LT1135	5	3			
LT1136	4	5	X	X	
LT1180	2	2	X		0.1µF Caps
LT1181	2	2			0.1µF Caps



DESIGN NOTES

Number 5 in a series from Linear Technology Corporation

March, 1989

Temperature Measurement Using the LTC1090/91/92 Series of Data Acquisition Systems

William Rempfer
Guy Hoover

Introduction

Accurate temperature measurement is a difficult and very common problem. Whether recording a temperature, regulating a temperature or modifying a process to accommodate a temperature, the LTC1090 family of data acquisition systems can provide an important link in the chain between the blast furnace temperature and the microcontroller. Features of the LTC1090 family can make temperature measurement easier, cheaper and more accurate.

High DC input resistance and reduced span operation allow direct connection to many standard temperature sensors. Multiplexer options allow one chip to measure up to 8 channels of temperature information. Single supply operation, modest power requirements (~5mW) and serial interfaces make remote location possible. Switching power on and off lowers power consumption (560 μ W) even more for battery applications. Finally, because few sensors have accuracies as good as 0.1%, the 10-bit resolution and 0.05% accuracy of

the LTC1090 family are just right for most temperature sensing applications.

Thermocouple Systems

The circuit of Figure 1 measures exhaust gas temperature in a furnace. The 10-bit LTC1091A gives 0.5°C resolution over a 0°C to 500°C range. The LTC1050 amplifies and filters the thermocouple signal, the LT1025A provides cold junction compensation and the LT1019A provides an accurate reference. The J type thermocouple characteristic is linearized digitally inside the MCU. Linear interpolation between known temperature points spaced 30°C apart introduces less than 0.1°C error. The code for linearizing is available from LTC. The 1024 steps provided by the LTC1091 (24 more than the required 1000) insure 0.5°C resolution even with the thermocouple curvature.

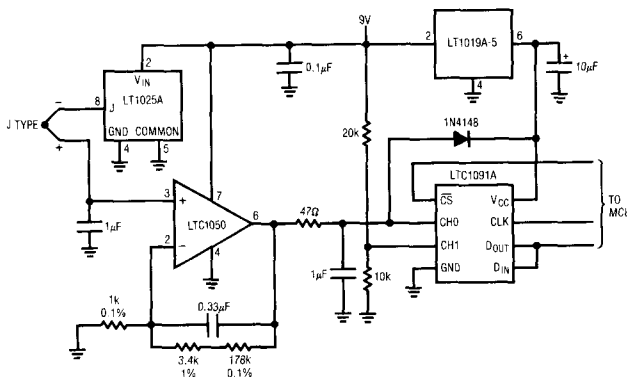


Figure 1. 0°C-500°C Furnace Exhaust Gas Temperature Monitor with Low Supply Detection

Offset error is dominated by the LT1025 cold junction compensator which introduces 0.5°C maximum. Gain error is 0.75°C max because of the 0.1% gain resistors and to a lesser extent the output voltage tolerance of the LT1019A and the gain error of the LTC1091A. It may be reduced by trimming the LT1019A or gain resistors. The LTC1091A keeps linearity better than 0.25°C. The LTC1050's 5 μ V offset contributes negligible error (0.1°C or less). Combined errors are typically 0.5°C or less. These errors don't include the thermocouple itself. In practice, connection and wire errors of 0.5°C to 1°C are not uncommon. With care, these errors can be kept below 0.5°C.

The 20k/10k divider on CH1 of the LTC1091 provides low supply voltage detection (the LT1019A reference requires a minimum supply of 6.5V to maintain accuracy). Remote location is easy, with data transferred from the MCU to the LTC1091 via the 3 wire serial port.

Thermilinear Networks

Figure 2 shows an 8 channel 0°C to 100°C temperature measurement system with 0.1°C resolution. The high DC input resistance and adjustable span of the LTC1090 allow it to measure the outputs of the YSI thermilinear components directly. Accuracy is limited by the sensor repeatability and precision resistors to 0.25°C.

Sensor input voltage (V_{IN}), not critical because of ratiometric operation, is set to around 1.5V to minimize self heating. The zero scale (COM pin) and full-scale (REF+ pin) of the LTC1090 are set by the precision resistor string to directly digitize the roughly 0.2V to 1V sensor output. The LT1006 buffers the 10k Ω reference resistance of the LTC1090. 0°C and 100°C

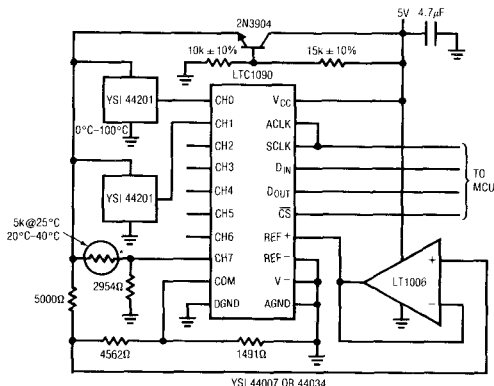


Figure 2. 0°C-100°C 0.25°C Accurate Thermistor Based Temperature Measurement System

correspond to unipolar output codes of 0 and 1000 (decimal), respectively with an overrange of 102.3°C.

Thermistors

A thermistor is a cheaper alternative to thermilinear components in narrower temperature range applications. In Figure 2, CH7 is being used to digitize the output of a 5k Ω thermistor. The resistor shown linearizes the output voltage around the 30°C point. The output remains linear to 0.1°C over a 20°C to 40°C range but gets nonlinear rapidly outside this range. By correcting for the non-linearity in software this range can be extended to 0°C to 60°C. Beyond that, the repeatability error of the thermistor increases above 0.2°C making correction difficult.

Silicon Sensors

Because of its high DC input impedance and reduced span capability, the LTC1090 family can directly measure the output of most industry standard silicon temperature sensors, both voltage and current mode. Popular sensors of this type include the LM134 and AD590 (current output) and silicon diodes.

Figure 3 shows a simple connection between the LTC1092 and industry standard 1 μ A/°K current output sensors. Resolution is 0.25°C and accuracy is limited by the sensor and resistors. Standard 10mV/°K voltage output sensors can also be connected directly to the LTC1092 input in a similar manner.

For LTC1090/91/92 literature call 800-637-5545. For help with an application call (408) 432-1900, Ext. 361.

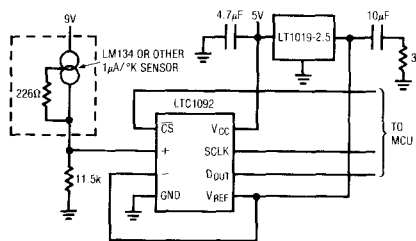
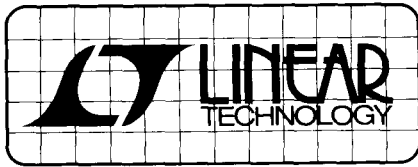


Figure 3. -55°C to +125°C Thermometer Using Current Output Silicon Sensors



DESIGN NOTES

Number 6 in a series from Linear Technology Corporation

January, 1988

Operational Amplifier Selection Guide for Optimum Noise Performance

George Erdi

The LT1028 is the lowest noise op amp available today. Its voltage noise is less than that of a 50Ω resistor. In other words, if the LT1028 is operated with source resistors in excess of 50Ω, resistor noise will dominate. If the application requires large source resistors, the LT1028's relatively high current noise will limit performance, and other op amps will provide lower overall noise.

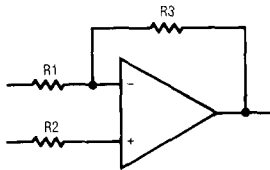
In general, the total noise of any op amp (referred to the input) is given by:

$$\text{total noise} = \sqrt{(\text{voltage noise})^2 + (\text{resistor noise})^2 + (\text{current noise} \times R_{eq})^2}$$

where,

$$\text{resistor noise} = 0.13\sqrt{R_{eq}} \text{ in nV}/\sqrt{\text{Hz}}$$

$$\text{and } R_{eq} = \text{equivalent source resistance} \\ = R2 + R1//R3$$



Several conclusions can be reached by inspection of the equation:

- (a) To minimize noise, resistor values should be minimized to make the contribution of the second and third terms of the equation negligible. Don't forget, however, that feedback resistor R3 is a load on the output.
- (b) Total noise is dominated by:
 - (i) voltage noise at low R_{eq} ,
 - (ii) resistor noise at mid R_{eq} ,
 - (iii) current noise at high R_{eq} , because resistor noise is proportional to $\sqrt{R_{eq}}$, while the current noise contribution to total noise is proportional to R_{eq} .

The table below lists which op amp gives minimum total noise for a specified equivalent source resistance. A two step procedure should be followed to optimize noise:

- (1) Reduce equivalent source resistance to a minimum allowed by the specific application.
- (2) Enter the table to find the optimum op amp.

The table actually has two sets of devices: one for low frequency (instrumentation), one for wideband applications. The slight differences between the two columns occur because voltage and current noise increase at low frequencies (below the so-called 1/f corner) while resistor noise is flat with frequency.

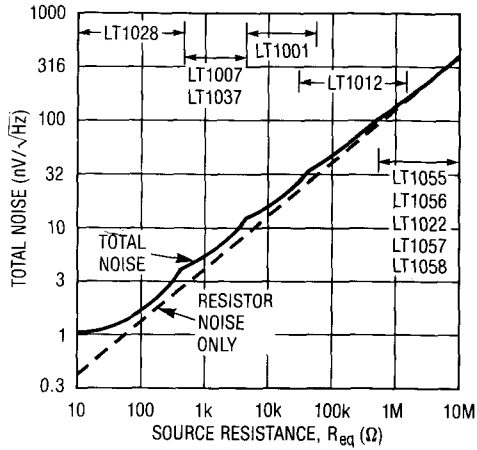
Best Op Amp for Lowest Noise vs Source Resistance

SOURCE R (R_{eq})	BEST OP AMP	
	@ LOW FREQ. (10Hz)	@ WIDEBAND (1kHz)
0Ω to 400Ω	LT1028	LT1028
400Ω to 1k	LT1007/37	LT1028
1k to 4k	LT1007/37	LT1028, LT1007/37
4k to 15k	LT1001	LT1007/37
15k to 30k	LT1001	LT1001, LT1007/37
30k to 70k	LT1001, LT1012	LT1001
70k to 150k	LT1012	LT1001, LT1012 LT1055/56/22, LT1057/58
150k to 600k	LT1012, LT1006/13/14	LT1012, LT1006/13/14 LT1055/56/22, LT1057/58
600k to 2M	LT1012 LT1055/56/22, LT1057/58	LT1012, LT1006/13/14 LT1055/56/22, LT1057/58
2M to 10M	LT1055/56/22, LT1057/58	LT1012 LT1055/56/22, LT1057/58
> 10M	LT1055/56/22, LT1057/58	LT1055/56/22, LT1057/58

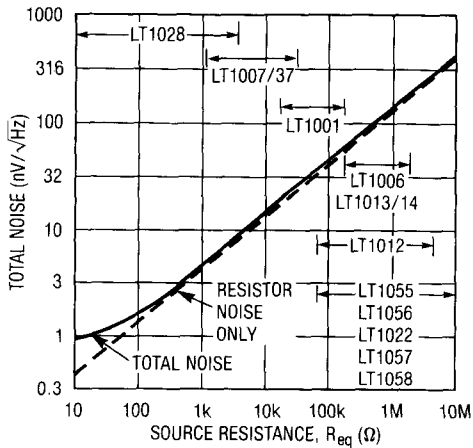
The actual achievable total noise is plotted at 10Hz and 1kHz. The striking feature of these plots is that with the proper selection of op amps total noise is dominated by equivalent source resistor noise over a five decade (100Ω to 10MΩ) range.

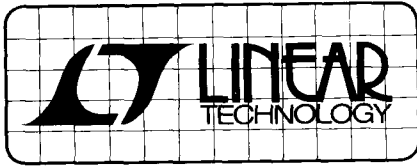
For Op Amp literature call 800-637-5545. For help with an application call (408) 432-1900, Ext. 361.

10Hz Total Noise vs Equivalent Source Resistance



1kHz Total Noise vs Equivalent Source Resistance





DESIGN NOTES

Number 7 in a series from Linear Technology Corporation

February, 1988

DC Accurate Filter Eases PLL Design

Nello Sevastopoulos
Philip Karantzalis

The LTC1062 is a versatile, DC accurate, instrumentation lowpass filter with gain and phase that closely approximate a 5th order Butterworth filter. The LTC1062 is quite different from presently available lowpass switched capacitor filters because it uses an external (R, C) to isolate the IC from the input signal DC path, thus providing DC accuracy. The DC accurate output, pin 7 of Figure 1, is buffered by an internal op amp from the switched capacitor network. The output of the switched capacitor network drives the bottom of C1. The input and output appear across an external resistor and, the IC part of the overall filter handles only the AC path of the signal. A buffered output is also provided (Figure 1) and its maximum guaranteed offset voltage over temperature is 20mV. Typically the buffered output offset is 0-5mV and drift is $1\mu\text{V}/^\circ\text{C}$. The use of an input (R, C) also provides other advantages, such as lower noise and antialiasing.

With commercially available PLLs, the loop filter is designed by the user to optimize the loop performance. For a variety of applications, a 1st or 2nd order lowpass passive or active R, C filter will do the job. When minimum output jitter and good transient response are required simultaneously, the design of the loop filter becomes more sophisticated. For instance, a fast transient response implies wide filter bandwidth and a reduced VCO output jitter implies minimum ripple at the VCO input. This is achieved by high outband attenuation of the lowpass filter. The LTC1062 provides the above requirements as well as economy and cutoff frequency programmability to be used advantageously in PLL designs.

The circuit of Figure 2 illustrates the use of the LTC1062 as a loop filter. The power supplies for the circuit are a single 5V

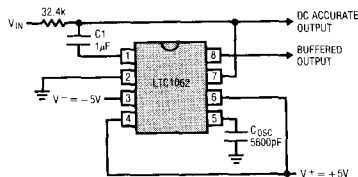


Figure 1. 8Hz 5th Order Butterworth Lowpass Filter

for the PLL and $\pm 5\text{V}$ for the LTC1062. The CMOS PLL is a CD4046B. The LTC1062 can also be used with a single 5V with some additional level shifting (see AN20). Phase detector #2 drives a diode-resistor limiter combination to make the voltage at input R of the LTC1062 swing from one diode above ground to one diode below the 5V supply. Additionally, the two 5k resistors establish a maximum AC impedance to keep the LTC1062 in its operating region and to bias the VCO input at its mid point when phase detector #2 switches into a three-state mode.

An empirical design procedure for input frequencies less than 5kHz ($f_{\text{IN}} \leq 5\text{kHz}$, Figure 2) is illustrated below:

- Given the minimum input frequency value, the cutoff frequency, f_c , of the LTC1062 should be chosen as:

$$1/6 (f_{\text{IN(MIN)}}) \leq f_c \leq 1/4 (f_{\text{IN(MIN)}})$$

The internal (or external) clock frequency of the LTC1062 should be 150 to 250 times the desired cutoff frequency, f_c .

- The capacitor C_{OSC} setting the LTC1062's internal oscillator should be chosen by:

$$C_{\text{OSC}} = \left(\frac{130\text{kHz}}{250 \times f_c} - 1 \right) \times 33\text{pF}$$

By further decreasing the value of C_{OSC} , the internal clock frequency of the LTC1062 increases and the damping of the loop also increases.

- By letting the value of $C = 0.047\mu\text{F}$, the LTC1062 input resistor R should be:

$$R = \frac{5500\text{k}\Omega}{f_c (\text{Hz})}$$

Note: For this application, the loop filter is not required to be maximum flat and, therefore, the (R, C) values of the LTC1062 can be within $\pm 5\%$ tolerance.

To illustrate the performance difference between a lowpass passive R, C loop filter and the LTC1062, the circuit of Figure 2 was tested for a PLL with a $60\text{Hz} \pm 10\%$ input fre-

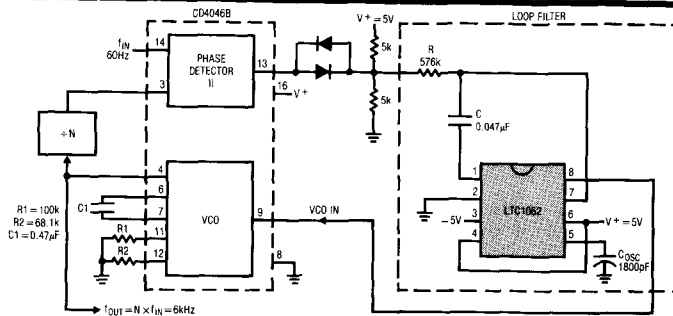
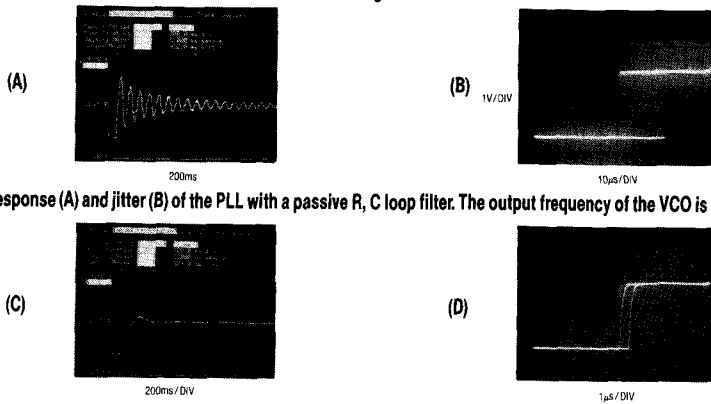


Figure 2



Transient response (A) and jitter (B) of the PLL with a passive R, C loop filter. The output frequency of the VCO is 6kHz and the $\div N = 100$.

Transient response (C) and jitter (D) of the PLL with the LTC1062 used as a loop filter. The VCO output frequency is 6kHz and the $\div N = 100$. The jitter is reduced to the internal jitter of the VCO.

Figure 3

frequency range and with $\div N = 100$. Then, the PLL's VCO output could be used to drive the clock input of a precision switched capacitor filter, such as an LTC1060A set up in a 100:1 clock to center ratio, and configured as a 60Hz sharp notch or bandpass filter. Figure 3A shows the transient response of the loop when a passive R,C loop filter, Figure 4, is used. The input frequency is shifted from 54Hz to 60Hz and the loop takes 820ms to settle within 5% of its steady state value. The corner frequency of the R, C passive filter is 22Hz. The natural frequency of the loop is approximately 10Hz and the damping factor less than 0.1. Figure 3B shows the jitter at the VCO output under the above conditions. A $30\mu\text{s}$ jitter with $f_{OUT} = 6\text{kHz}$ corresponds to 18% instantaneous frequency inaccuracy. This makes the PLL VCO output unusable as a

clock generator for a tracking switched capacitor filter. A small improvement in the VCO output jitter could be achieved by further decreasing the filter's cutoff frequency; this, however, would further penalize the circuit's settling time.

Figures 3C and 3D show the PLL performance when an LTC1062 is used as a loop filter. The corner frequency f_c of the LTC1062 was set at 9.5Hz ($\approx 1/6 f_{IN}$) and its internal clock was set for 2.4kHz ($\approx 252 \times f_c$). The settling time of the loop was 320ms and the damping factor was optimally set to 0.7. The $1\mu\text{s}$ VCO output jitter, $f_{OUT} = 6\text{kHz}$, was measured over 5 periods and it is attributed to the inherited jitter of the VCO internal circuitry. With the LTC1062 used as a loop filter, the circuit's jitter corresponds to 0.12% frequency error. This is quite adequate to drive the clock input of 0.3% accurate switched capacitor filters, such as LTC1059A or LTC1060A.

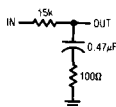


Figure 4. Lowpass R, C Filters used for PLL Example

For Filter literature call 800-637-5545. For help with an application call (408) 432-1900, Ext. 361.

Inductor Selection for LT1070 Switching Regulators

Jim Williams

A common problem area in switching regulator design is the inductor, and the most common difficulty is saturation. An inductor is saturated when it cannot hold any more magnetic flux. As an inductor arrives at saturation it begins to look more resistive and less inductive. Under these conditions current flow is limited only by the inductor's DC copper resistance and the source capacity. This is why saturation often results in destructive failures.

While saturation is a prime concern, cost, heating, size, availability and desired performance are also significant. Electromagnetic theory, although applicable to these issues, can be confusing, particularly to the non-specialist.

Practically speaking, an empirical approach is often a good way to approach inductor selection. It permits real time analysis under actual circuit operating conditions using the ultimate simulator—a breadboard. If desired, inductor design theory can be used to augment or confirm experimental results.

Figure 1 shows a typical flyback regulator utilizing the LT1070 switching regulator. A simple approach may be employed to determine the appropriate inductor. A very useful tool is the #845 inductor kit* shown in Figure 2. This kit provides a broad range of inductors for evaluation in test circuits such as Figure 1.

*Available from Pulse Engineering, Inc., P.O. Box 12235, San Diego, CA 92112, 619-268-2400

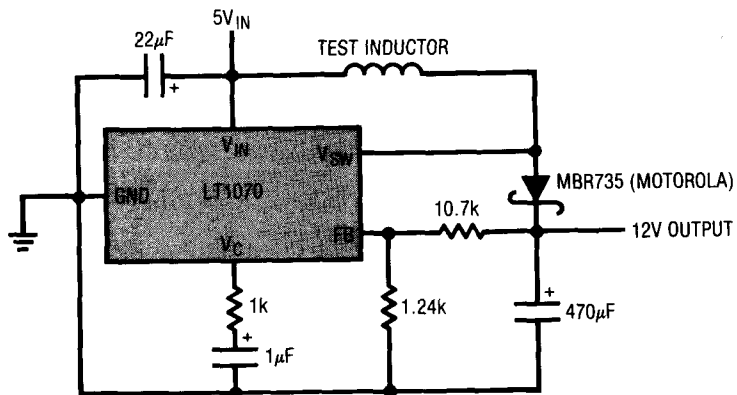


Figure 1. Basic LT1070 Flyback Regulator Test Circuit

Figure 3 was taken with a $450\mu\text{H}$ value, high core capacity inductor installed. Circuit operating conditions such as input voltage and loading are set at levels appropriate to the intended application. Trace A is the LT1070's V_{SWITCH} pin voltage while trace B shows its current. When V_{SWITCH} pin voltage is low, inductor current flows. The high inductance means current rises relatively slowly, resulting in the shallow slope observed. Behavior is linear, indicating no saturation problems. In Figure 4, a lower value unit with equivalent core characteristics is tried. Current rise is steeper, but saturation is not encountered. Figure 5's selected inductance is still lower, although core characteristics are similar. Here, the current ramp is quite pronounced, but well controlled. Figure 6 brings some informative surprises. This high value unit, wound on a low capacity core, starts out well but heads rapidly into saturation, and is clearly unsuitable.

The described procedure narrows the inductor choice within a range of devices. Several were seen to produce acceptable electrical results, and the "best" unit can be further selected on the basis of cost, size, heating and other parameters. A standard device in the kit may suffice, or a derived version can be supplied by the manufacturer.

Using the standard products in the kit minimizes specification uncertainties, accelerating the dialogue between user and inductor vendor.

References

- AN-25 "Switching Regulators for Poets", Jim Williams, Linear Technology Corporation
- AN-19 "LT1070 Design Manual", Carl Nelson, Linear Technology Corporation

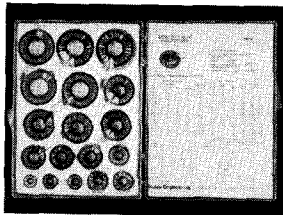


Figure 2. Model 845 Inductor Selection Kit from Pulse Engineering, Inc. (includes 18 fully specified devices)

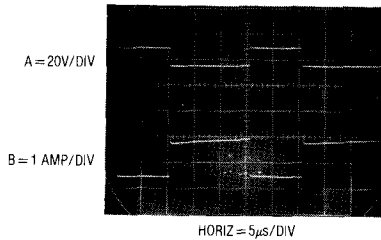


Figure 3. Waveforms for $450\mu\text{H}$, High Core Capacity Unit

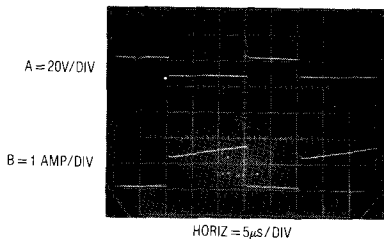


Figure 4. Waveforms for $170\mu\text{H}$, High Capacity Core Unit

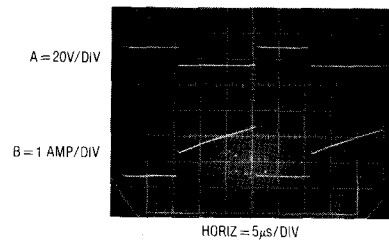


Figure 5. Waveforms for $55\mu\text{H}$, High Capacity Core Unit

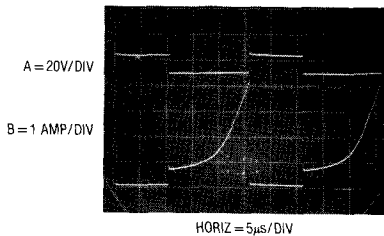


Figure 6. Waveforms for $500\mu\text{H}$, Low Capacity Core Inductor (note saturation effects)

For Switching Regulator literature call 800-637-5545. For help with an application call (408) 432-1900, Ext. 361.

Chopper Amplifiers Complement a DC Accurate Low-Pass Filter

Nello Sevastopoulos

Monolithic switched-capacitor low-pass filters, although they offer precise frequency responses, cannot usually be used for DC accurate applications because of their prohibitive DC offsets and poor gain linearity. The LTC1062, however, is quite different from currently available low-pass switched-capacitor filters because it uses an external (R, C) to isolate the IC from the input-signal DC path and to provide antialiasing for incoming signals larger than half its clock frequency. The LTC1062 is ideal when used in conjunction with high performance chopper-stabilized op amps.

The LTC1050 is an ultra low offset, low noise chopper with the sampling capacitors internal. It can remove residual clock noise without adding further DC error. Also, the internal capacitor minimizes board area.

Figure 1 shows a low cost, 7th order DC accurate, 10Hz low-pass filter where amplitude and phase response closely ap-

proximates a Bessel filter. The required clock frequency is 2kHz, thus yielding a clock to cutoff frequency ratio of 200:1.

The LTC1050 is configured as unity gain 2nd order low-pass filter which center frequency is $(1.2\pi R'C) = 1.72 \times f_{\text{CUT-OFF}} = 17.2\text{Hz}$ and $Q = 0.5$. Figure 2 shows the amplitude response of the filter, and Figure 3 shows a well behaved transient response for which Bessel filters are famous. The power supplies used were $\pm 8\text{V}$ to provide a total DC input common-mode range of $\pm 6\text{V}$. The measured wideband noise was $52\mu\text{Vrms}$. The clock, and R, C values of Figure 1 can be easily modified to provide a 7th order Butterworth 10Hz filter, such as: $f_{\text{CLK}} = 1\text{kHz}$, $R = 26.7\text{k}$, $C = 1\mu\text{F}$, $R' = 165\text{k}$, $C_1 = 0.2\mu\text{F}$ and $C_2 = 0.047\mu\text{F}$. The diode at LTC1062 pin 3 should be used to protect the device from incoming signals above the power supplies.

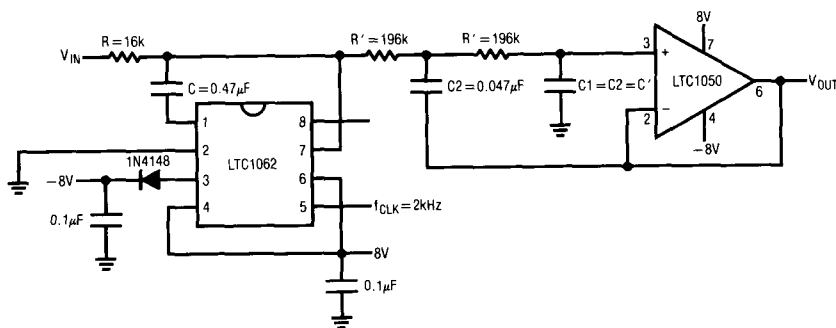


Figure 1. Combining the LTC1050 Chopper Op Amp with the LTC1062 to Provide a 10Hz, DC Accurate Low-Pass Bessel Filter

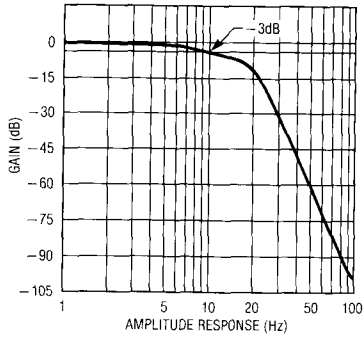


Figure 2. Amplitude Response of Figure 1, Providing a Close Approximation to a Bessel Filter

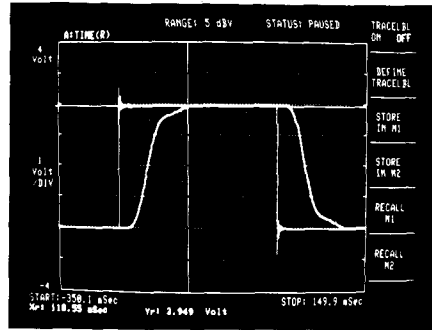


Figure 3. Transient Response of the Bessel Low-Pass Filter of Figure 1

In Figure 4, an external (R1, R2, C1) network is used at the input-output of the internal buffer of the LTC1062 (pins 7 and 8), to provide an additional 2 pole, $Q = 0.707$, high-pass filter. The filter output at pin 8 is bandpass, Figure 5, whereas the DC accurate Butterworth low-pass filter is still available at the output of the LTC1050. This circuit allows the user to separate the DC and AC components of an incoming signal, V_{IN} . Here, the LTC1050 buffers the low-pass filter section of the overall bandpass filter. For a $Q = 0.707$, the design equation for the high-pass sections are straightforward: set $R2 = 2R1$;

and then the high-pass cutoff frequency is, $f_c = (0.707 / 2\pi R1C1)$. The circuit in Figure 4 can be easily operated with a single supply, because resistor R2 and capacitor(s) C1 of the high-pass section, also DC bias pin 7 at mid supplies independently of the DC input voltage. If only a single supply is available, simply bias the bottom side of R2 at half supply.

For Filter literature call 800-637-5545. For help with an application call (408) 432-1900, Ext. 361.

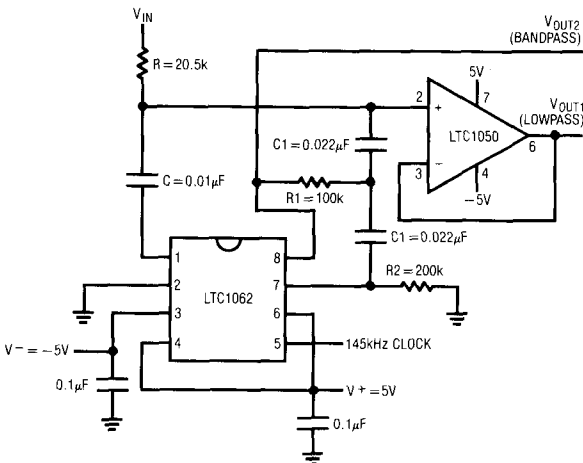


Figure 4. A Bandpass, DC Accurate Lowpass Filter Combination used to Extract the AC Information from a DC + AC Input Signal

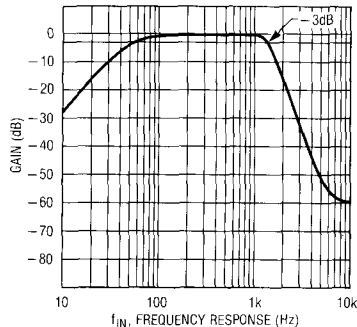
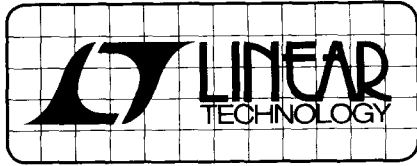


Figure 5. Frequency Response of the Bandpass Filter Output, V_{OUT2} , of Figure 4



DESIGN NOTES

Number 10 in a series from Linear Technology Corporation

May, 1988

Electrically Isolating Data Acquisition Systems

Guy Hoover
William Rempfer

Introduction

In data acquisition systems it is often necessary to electrically isolate the measurement points from the system controller. Reasons for the electrical isolation include the following: to allow floating measurements at high voltages; for safety, to reduce the danger of electrical shock, as might occur in medical applications; and to eliminate ground loops between measurement points and the system controller which can cause errors.

The data transmitted over the isolated lines can be either analog or digital. Analog signals have poor noise immunity and one isolator is required for each signal point. Traditionally, the highly noise immune, digitally encoded signals required many isolated lines for each channel. Now, with the LTC1090 family of serial data acquisition systems, it is possible to transmit eight channels of data with only four isolated lines. Each additional eight channels requires only one additional isolated line.

Both opto isolators and pulse transformers could be used to isolate the signals. However, since opto isolators tend to be smaller and less expensive than pulse transformers, they will be the only type of device considered here.

The circuit to be demonstrated is an eight channel data acquisition system with 500V of isolation that uses the LTC1090 and four opto isolators. With the addition of another opto isolator, the circuit can be battery operated, drawing only 50 μ A while taking a reading once every two seconds.

The number of channels can be increased to 16, 24, 32, etc., with one additional opto isolator used to increase the number of channels in multiples of eight. Up to 24 channels can be powered directly by the LT1021.

Circuit Description

The LT1021 powers the analog circuitry and provides an accurate reference. A 1 Ω resistor isolates the reference from power supply transients.

The 4N28s in Figure 1 are very commonly used opto isolators. They provide only 500V of isolation, however. If more isolation is desired, up to 2500V of isolation can be obtained by using 4N25s with no other circuit modifications.

PNP transistors were chosen to drive the opto isolators to optimize signal fall time and clock rate. D_{OUT} of the LTC1090 is transmitted on the falling edge of SCLK. Data is clocked into the processor on the rising edge of SCLK. It is therefore necessary that the falling edge of SCLK have as little delay as possible through the opto isolator. This insures that D_{OUT} can be output by the LTC1090 in time to be captured by the processor on the rising edge of SCLK. NPNs could be used at slower data rates or if burning more current is not objectionable.

The current limiting resistors in the collectors of the opto drivers are chosen with the Current Transfer Ratio (CTR) of the opto isolator in mind. The output transistor of the opto isolator must have enough base current to drive the desired

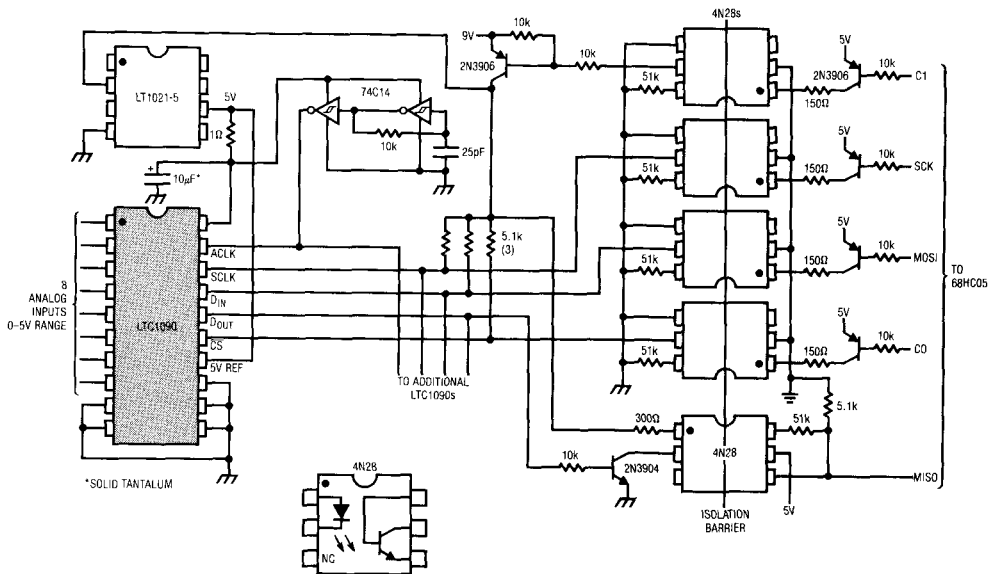


Figure 1. Micropower, 500V Opto Isolated, Multichannel, 10-Bit Data Acquisition System is Accessed Once Every Two Seconds

load. The base resistor on the opto output transistor is there to decrease the turn off time of the opto isolator.

The code written for the Motorola 68HC05 processor is available from Linear Technology. The code powers up the circuit, allows 6.0ms for the $10\mu\text{F}$ cap to charge to its final value, reads 9 channels in 12ms, and then powers down until the next set of readings is required. Nine channel readings are required because, when the LTC1090 is powered up, a dummy read is necessary to initialize the device. The frequency of the ACLK generated by the 74C14 is not too critical. The software must provide a delay of at least two ACLK cycles between the time $\overline{\text{CS}}$ goes low and the first SCLK edge is generated. Another delay of 44 ACLKs is required during the time that $\overline{\text{CS}}$ is high between data transfers.

Alternatives

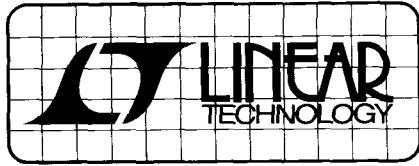
The circuit demonstrated in Figure 1 is capable of transferring serial data at about a 15kHz rate, which is fast enough for many applications. For higher data transfer rates, pulse

transformers from companies such as Sprague or Pulse Engineering, or high speed opto isolators such as Hewlett Packard's HCPL2200 are available which can transmit data at the full 1MHz rate that the LTC1090 is capable of.

Summary

The LTC1090 with its serial architecture is ideally suited for isolation applications. It requires only four isolated lines for eight channels of data and can be expanded by adding only one additional isolated line for each additional eight channels of data required. Possible applications for this and similar circuits are PC-based measurement systems, medical instrumentation and other applications where large common-mode voltages or ground loops exist.

For LTC1090 literature call **800-637-5545**. For help with an application call (408) 432-1900, Ext. 361.



DESIGN NOTES

Number 11 in a series from Linear Technology Corporation

June, 1988

Achieving Microamp Quiescent Current in Switching Regulators

Jim Williams

Many battery powered applications require very wide ranges of power supply output current. Normal conditions require currents in the ampere range, while standby or "sleep" modes draw only microamperes. A typical lap top computer may draw 1 to 2 amperes running while needing only a few hundred microamps for memory when turned off. In theory, any switching regulator designed for loop stability under no-load conditions will work. In practice, a regulator's relatively large quiescent current may cause unacceptable battery drain during low output current intervals.

Figure 1 shows a typical flyback regulator. In this case the 6V battery is converted to a 12V output by the inductive flyback voltage produced each time the LT1070's V_{SW} pin is internally switched to ground. An internal 40kHz clock produces a flyback event every 25 μ s. The energy in this event is controlled by the IC's internal error amplifier, which acts to force the feedback (FB) pin to a 1.23V reference. The error amplifier's high impedance output (the V_C pin) uses an RC damper for stable loop compensation.

This circuit works well but pulls 9mA of quiescent current. If battery capacity is limited by size or weight this may be too high. How can this figure be reduced while retaining high current performance?

A solution is suggested by considering an auxiliary V_C pin function. If the V_C pin is pulled within 150mV of ground the IC shuts down, pulling only 50 microamperes. Figure 2's special loop exploits this feature, reducing quiescent current to only 150 microamperes. Here, circuitry is placed between the feedback divider and the V_C pin. The LT1070's internal feedback amplifier and reference are not used. Figure 3 shows operating waveforms under no-load conditions. The 12V output (trace A) ramps down over a period of seconds. During this time comparator A1's output (trace B) is low, as are the paralleled inverters. This pulls the V_C pin (trace C) low, putting the IC in its 50 μ A shutdown mode. The V_{SW} pin (trace D) is high, and no inductor current flows. When the 12V output drops about 20mV, A1 triggers and the inverters (74C04) go high, pulling the V_C pin up and turning on the

regulator. The V_{SW} pin pulses the inductor at the 40kHz clock rate, causing the output to abruptly rise. This action trips A1 low, forcing the V_C pin back into shutdown. This "bang-bang" control loop keeps the 12V output within the 20mV ramp hysteresis window set by R3-R4. Diode clamps prevent V_C pin overdrive. Note that the loop oscillation period of 4-5 seconds means the R6-C2 time constant at V_C is not a significant term. Because the LT1070 spends almost all of the time in shutdown, very little quiescent current (150 μ A) is drawn.

Figure 4 shows the same waveforms with the load increased to 3mA. Loop oscillation frequency increases to keep up with the loads sink current demand. Now, the V_C pin waveform (trace C) begins to take on a filtered appearance. This is due to R6-C2's 10ms time constant. If the load continues to increase, loop oscillation frequency will also increase. The R6-C2 time constant, however, is fixed. Beyond some frequency, R6-C2 must average loop oscillations to DC.

Figure 5 plots what occurs, with a pleasant surprise. As output current rises, loop oscillation frequency also rises until about 500Hz. At this point the R6-C2 time constant filters the V_C pin to DC and the LT1070 transitions into "normal" operation. With the V_C pin at DC it is convenient to think of A1 and the inverters as a linear error amplifier with a closed loop gain set by the R1-R2 feedback divider. In fact, A1 is still duty cycle modulating, but at a rate far above R6-C2's break frequency. The phase error contributed by C1 (which was selected for low loop frequency at low output currents) is dominated by the R6-C2 roll off and the R7-C3 lead into A1. The loop is stable and responds linearly for all loads beyond 80mA. In this high current region the LT1070 behaves like Figure 1's circuit.

The loop described provides a controlled, conditional instability to lower regulator quiescent current by a factor of 60 without sacrificing high power performance. Although demonstrated in a boost converter, it is readily exportable to other configurations, (e.g., multi-output flyback, buck, etc.) allowing LT1070 use in low quiescent power applications.

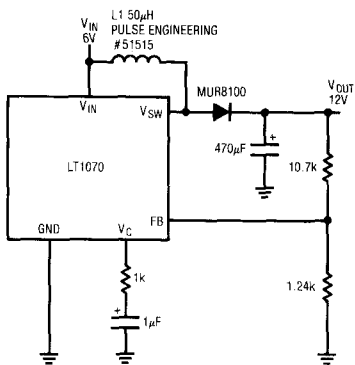
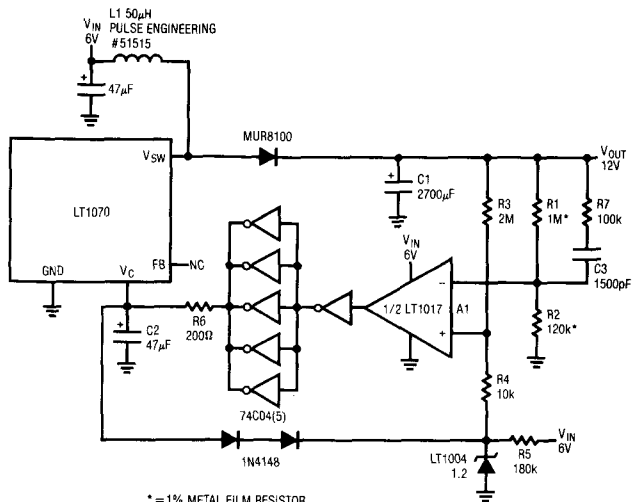


Figure 1. Typical LT1070 Flyback Regulator



* = 1% METAL FILM RESISTOR

Figure 2. Low Quiescent Current Flyback Regulator

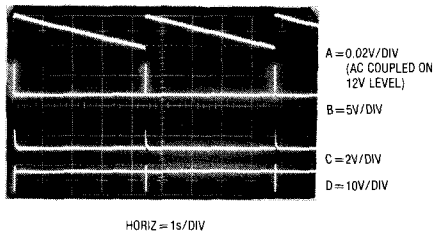


Figure 3. Waveforms at No Load for Figure 2 (Traces B and D Retouched for Clarity)

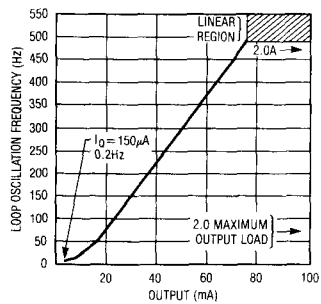


Figure 5. Output Current vs Loop Oscillation Frequency for Figure 2

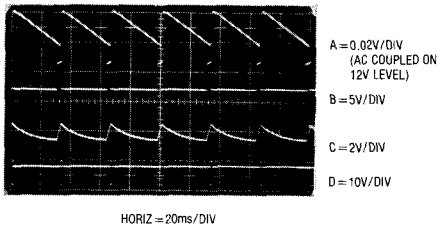


Figure 4. Waveforms at 3mA Load for Figure 2

For LT1070 literature call 800-637-5545. For help with an application call (408) 432-1900, Ext. 361.

An LT1013 and LT1014 Op Amp SPICE Macromodel

Walter G. Jung

With the advent of low cost and powerful desktop computers, present day op amp circuit designs can mature more quickly with good simulation tools. One such tool since its inception has been SPICE, the standard analog circuit simulator. However, while PCs and workstations may now be present on more and more desks, a potential bottleneck towards effective simulation has been SPICE models for the more popular parts.

The macromodel approach to simulation of an op amp is viable for many designs, with the great asset of simulation speeds far faster than that of a full device-level circuit. With this design note, Linear Technology Corporation introduces

op amp macromodels to its applications library. It is hoped that eventually most op amps in the product line will be developed as macromodels and made available to customers.

The LT1013 and LT1014 devices are popular single supply LTC op amps, and are thus logical candidates for macromodels. While existing macromodels for the generic 358 and 324 types might suffice for some applications, circuit designs which take advantage of the unique precision and functional features of the LT1013 warrant a model which reflects those features. The schematic diagram of the LT1013 and LT1014 macromodel is shown in Figure 1, and is applicable to one channel of either device.

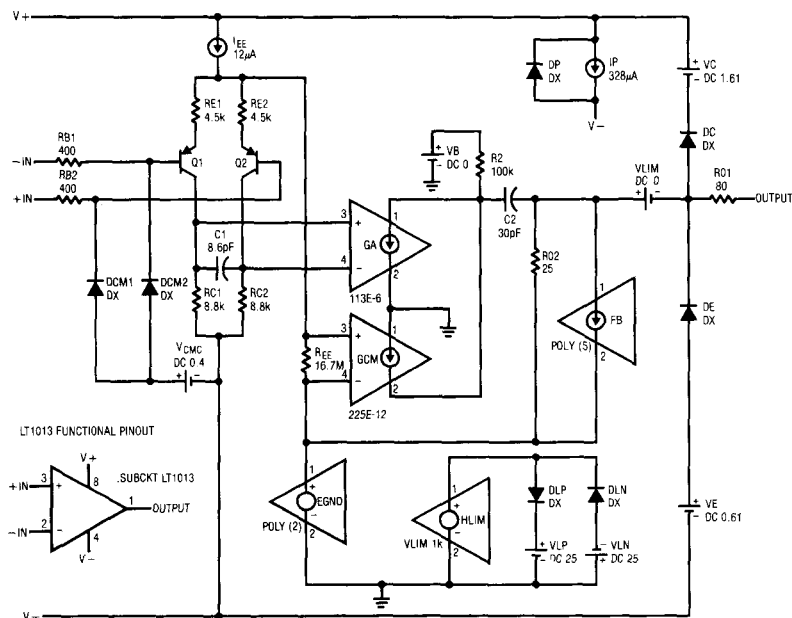


Figure 1. LT1013 Op Amp Macromodel

Key op-amp specifications for the commercial device are:
 offset voltage = $50\mu\text{V}$ (offset is not simulated)
 bias current = 8nA
 gain = 1000000
 slew rate = $0.4\text{V}/\mu\text{s}$
 bandwidth = 0.8MHz

Also, the model simulates the input common mode range (which includes ground) and the output characteristics of swinging to ground while sinking current.

This macromodel acts very much like the real LT1013 or LT1014 device which incorporates input common mode clamping, to prevent the sign-reversal errors common to the 358/324 types. For example, comparison responses for the LT1013 and the 358 are shown in Figure 2. The common conditions of this test are for an overdriven, +5V single-supply follower. In both instances, the input signal is V_{IN} , a -20V to 20V sweep fed through 10k , while the output is $V(5)$.

Note that with the 358, the output reverses sign when the input is overdriven below ground. In contrast, the LT1013 model is well behaved, simply clamping the overdrive at ground level...just like the real LT1013 device does!

The model itself is listed on this page, and can be entered by typing it in (carefully!). Registered users of MicroSim's PSPICE simulator will automatically receive this macromodel as part of the model library update with version 3.07. Interested readers may contact MicroSim at the address or phone number listed at the end of this note for further information.

This LT1013/LT1014 op amp macromodel is being supplied to users as an aid to circuit designs. While it reflects reasonably close similarity to the actual device in terms of performance, it is not suggested as a replacement for breadboarding. Simulation should be used as a forerunner or a supplement to traditional lab testing.

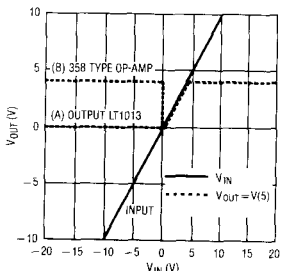


Figure 2. LT1013 Test Circuit: Single-Supply (+5V), Overdriven Follower

This more complete macromodel has been adapted from the Parts program generated LT1013/LT1014 model. This version features closer fidelity to the real part, with input common mode clamping and compensated output clamping. It can be used for large signal and/or single supply applications, where the inputs can potentially be overdriven.

SPICE List for LT1013 Macromodel

```
connections:
*      |      |      |
*      |      |      | positive power supply
*      |      |      | negative power supply
*      |      |      | output
*      |      |      |
*      |      |      |
.subckt LT1013 1 2 3 4 5
*
*
c1     11 12      8.661E-12
c2     6  7      30.00E-12
dc     8 53 dx
de     54 8 dx
dlp    90 91 dx
dlm    92 90 dx
dp     4  3 dx
egnd   99 0
fb     7 99      poly(2) (3,0) (4,0) 0 .5 .5
                    poly(5) vb vc ve vlp vin 0
                    2.475E9 -2E9 2E9 2E9 -2E9
ga     6  0 11 12 113.1E-6
gcm    0  6 10 99 225.7E-12
iee    3 10 dc   12.03E-6
hlim   90 0      vlim 1k
q1     11 102 13 qx
q2     12 101 14 qx
rb1    2 102 400
rb2    1 101 400
dcm1   105 102 dx
dcm2   105 101 dx
vcmc   105 4  dc   0.4
r2     6  9      100.0E3
rc1    4 11      8.841E3
rc2    4 12      8.841E3
re1    13 10     4.519E3
re2    14 10     4.519E3
ree    10 99     16.63E6
ro1    8  5 80
ro2    7 99 25
ip     3  4      328E-6; supply current
vb     9  0 dc  0
vc     3 53 dc  1.610
ve     54 4  dc  .61
vlim   7  8  dc  0
vlp    91 0  dc  25
vin    0 92  dc  25
.model dx D(lS=800.0E-18)
.model qx PNP(lS=800.0E-18 Bf=400)
.ends

PSPICE simulator is available from:
MicroSim
23175 La Cadena Drive
Laguna Hills, CA 92653
(714) 770-3022; (800) 826-8603
```

For LT1013/14 literature call 800-637-5545. For help with an application call (408) 432-1900, Ext. 361.



DESIGN NOTES

Number 13 in a series from Linear Technology Corporation

August, 1988

Closed Loop Control with the LTC1090 Series of Data Acquisition Systems

Guy Hoover
William Rempfer

Introduction

The use of microprocessors in process control loops is quite common. A processor based control loop requires special design considerations as compared to traditional analog loops. Often a single centrally located processor will be used to control several remotely located processes. The outputs of the remote process sensors can be digitized at the sensor location and then be transmitted to the central processor. Unfortunately, transmitting digital signals typically requires one wire for each bit of resolution and requires expensive cabling. Alternatively, the sensor output can be transmitted as an analog signal to the central processor area for digitization. However, transmitting analog signals over distances can introduce errors because of noise and voltage drops in the wires.

The solution to these control loop problems can be found in the LTC1090 series of data acquisition systems. As can be seen in the schematic of Figure 2, ten bits of data can be digitized remotely and sent to the processor with only three wires plus ground. The single supply capability and the low DC current drain (1mA typ.) also simplify remote location. The LTC1090 series provides the user with blocks of 1, 2, 6 or 8 10-bit channels which can be chosen according to how many sensors are located in each remote site.

The LTC1090 series is ideally suited for such process control loop applications as position control, temperature control, container filling and tension control.

Circuit Description

The circuit of Figure 2 is a container filling control loop which has a resolution of .03 pounds with a 30 pound full scale. It

was designed to implement an automatic filling station for the model train shown in Figure 1. When S1 is closed the MC68HC05 processor reads the LTC1092. If the weight is below the preprogrammed limit in the processor then the motor drive line which controls the pump is turned on. The LTC1092 is continually read by the processor as the truck is filled, until the limit is reached. The motor drive line is then shut off. The limit may be derived in a number of ways. A fixed limit will result in filling to an absolute weight, while relative or tare weight filling can be implemented when the measured empty weight is used in the calculation of the limit. Code for this application is available upon request from Linear Technology Corporation.

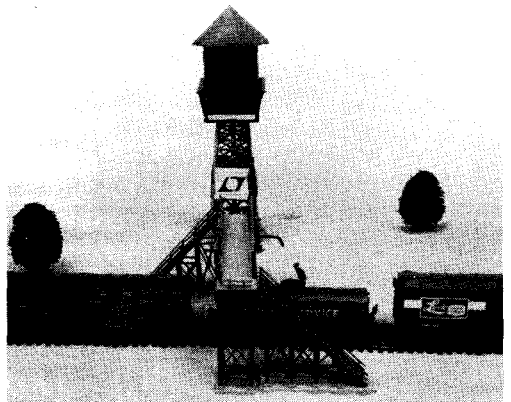
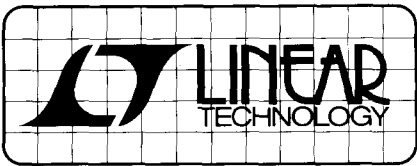


Figure 1. A Typical Application. Automatic Filling at a Railroad Siding.



DESIGN NOTES

Number 14 in a series from Linear Technology Corporation

September, 1988

Extending the Applications of 5V Powered RS232 Transceivers

High Speed Operation

Although the EIA RS232 specification is for a relatively slow communications protocol, many applications require RS232 transceivers to operate at higher frequencies. Devices such as the LT1080, LT1081, and the LT1130 series share a common design for the drivers and receivers and are capable of operating over 100 kilobaud.

Although the slew rate is controlled for all of the Linear Technology series of RS232 communications devices, for output levels limited to $\pm 6V$ the transition time is fast enough to allow high baud rates. With a slew rate of approximately 10V per microsecond, it only takes 1.2 microseconds for a 12V excursion. The two photos (Figure 1 and Figure 2) show the output waveform and delay associated with a 75kHz square wave input and a 100kHz square wave. Delay times are in the order of 0.5 microseconds and the total slew

time is approximately 1.2 microseconds. Output load is 3k. Receivers are much faster and can handle these baud rates with no problem. For higher communication rates, a differential signal is recommended.

Power Supply Tricks

The power supply generator on 5V powered devices is a charge pump circuit which generates approximately $\pm 9V$ from a single 5V supply. Parallel operation of the supply charge pumps for 5V powered transceivers is easily achieved to minimize component count. The positive and negative supply have approximately $1\mu F$ of holding capacitance for energy storage. If several devices with charge pumps are used in the same system, the output supplies may be paralleled into a single pair of common energy storage capacitors.

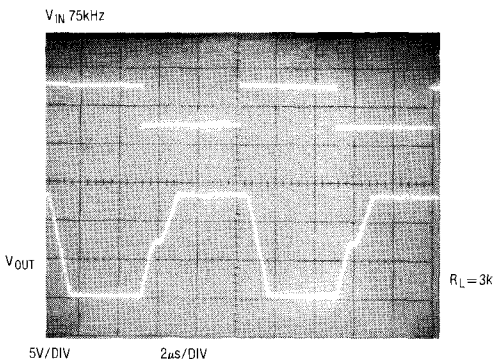


Figure 1. Operation at 75kHz

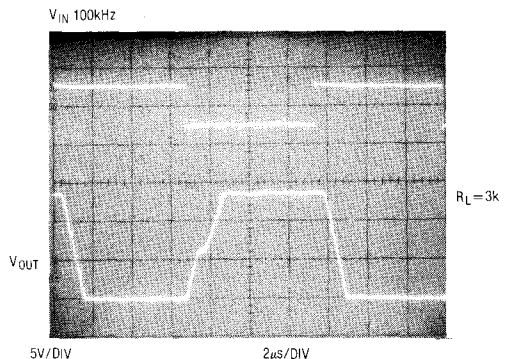


Figure 2. Operation at 100kHz

Figure 3 shows two LT1080's with common power supply capacitors for energy storage. Twice the output current is available for external use. This eliminates two capacitors from the system. Individual charge pump capacitors are still needed on each of the devices.

Operation with +5V and +12V Supplies

The charge pump circuitry takes the input 5V and doubles it. The doubled voltage is then inverted to obtain a negative output. The only reason for doubling the input is to ensure adequate positive and negative output voltage to meet RS232 specifications. In PC systems, where +12V is available, the internal voltage doubler does not need to be used. The device may be connected directly to a +5V and a +12V supply. The +12V is then inverted to obtain approximately -11V. This eliminates one charge pump capacitor and one holding capacitor for the 12V output. Figure 4 shows an LT1080 connected to a 12V and 5V power supply. The +12V is connected into one of the charge pump capacitor pins rather than the 12V output pin. Supply current also decreases to about 9mA.

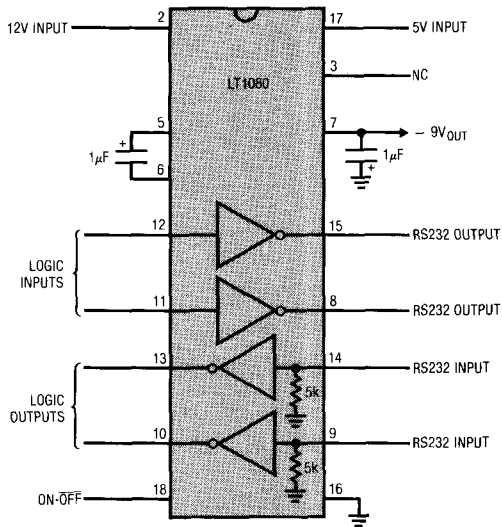


Figure 4. Operation with +12V and +5V Supplies

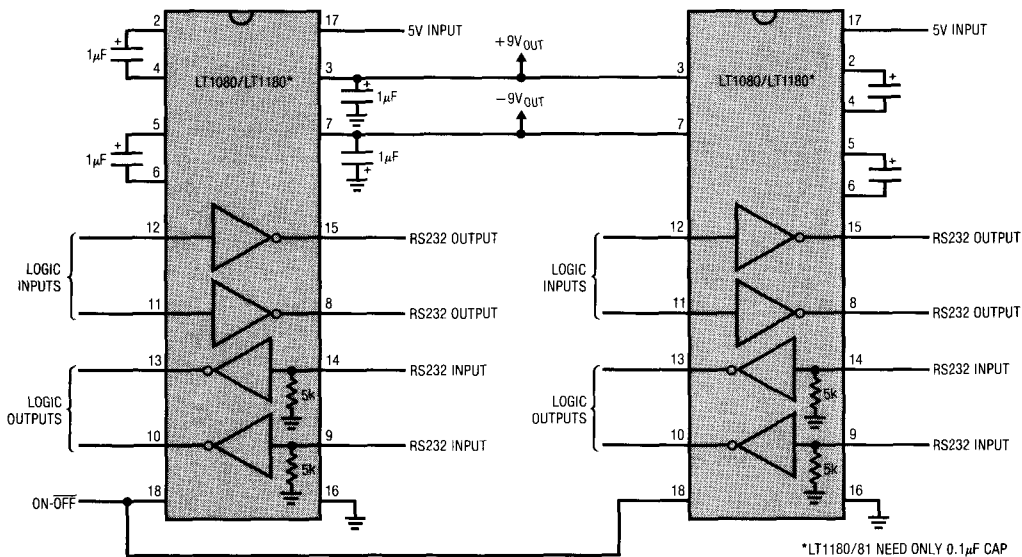


Figure 3. Paralleling Power Outputs

For literature about our complete line of RS232 products, call 800-637-5545. For help with an application, call (408) 432-1900, Ext. 357.

Noise Calculations in Op Amp Circuits

Alan Rich

Noise calculations in op amp circuits are one of the most confused calculations that an analog engineer must perform.

One cannot just look at noise specifications; the total op amp circuit including resistors and operating frequency range must be included in calculations for circuit noise. A "low" noise amplifier in one circuit will become a "high" noise amplifier in another circuit.

As a part of this Design Note, an IBM-PC or compatible computer program, NOISE, has been written to perform the noise calculations. This program allows the user to calculate circuit noise using LTC op amps, determine the best LTC op amp for a low noise application, display the noise data for LTC op amps, calculate resistor noise, and calculate circuit noise using noise specs for any op amp. At the end of this Design Note there are detailed operating instructions for the computer program NOISE.

To calculate noise for an op amp circuit, one must consider the op amp voltage and current noise density and 1/f corner frequency, the frequency range of interest, and the resistor noise.

The most comprehensive specification for voltage or current noise is the noise density frequency response curve as shown in Figure 1.

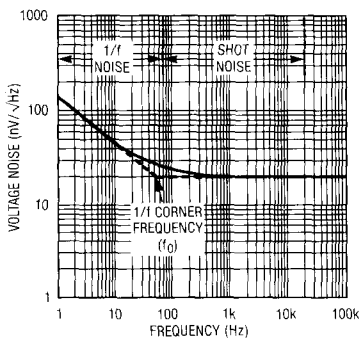


Figure 1.

There are two distinct regions to consider:

1. The high frequency part of the curve shows the shot noise and is independent of frequency.
2. The low frequency part of the curve is the 1/f noise as shown by a rapidly increasing noise density. In low frequency applications, the 1/f noise limits the minimum level of noise. The point on the curve where the asymptotes of the shot noise and 1/f noise intersect is the 1/f corner frequency.

To calculate the total RMS noise of an op amp over a bandwidth:

$$N = NO \times \sqrt{FC \times LN \left(\frac{FH}{FL} \right) + (FH - FL)} \quad (\text{Equation 1})$$

Where N is the RMS current or voltage noise measured from a lower frequency FL to an upper frequency FH and NO is the current or voltage shot noise density with a 1/f corner frequency FC.

Consider an audio preamplifier using an LT1037 as a simple inverting circuit (Figure 2) and the corresponding noise model (Figure 3).

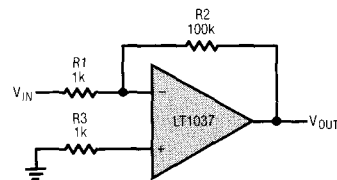


Figure 2.

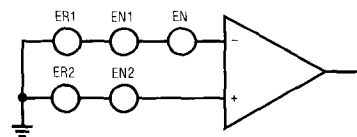


Figure 3. Noise Model

EN is the voltage noise of the op amp, EN1 is the voltage noise developed by the current noise in resistors R1 and R2, EN2 is the voltage noise developed by the current noise in resistor R3, ER1 is the voltage noise of R1 and R2, and ER2 is the voltage noise of R3.

Since we are using an LT1037 over the audio frequency range, NO = 2.5nV/√Hz, FC = 2.0Hz, FH = 20kHz, FL = 20Hz. Plugging into Equation 1:

$$EN = 2.5 \times \sqrt{2 \times LN(20kHz/20Hz) + (20kHz - 20Hz)}$$

$$EN = 354nV, RMS$$

To calculate EN1, first the current noise must be calculated using Equation 1 and a current noise density of 0.57pA/√Hz and 1/f corner frequency of 120Hz.

$$IN = 0.57 \times \sqrt{120 \times LN(20kHz/20Hz) + (20kHz - 20Hz)}$$

$$IN = 82pA, RMS$$

IN will flow into the parallel combination of R1 and R2.

$$EN1 = 82pA \times 1k \parallel 100k = 82nV, RMS$$

Similarly, EN2 results from IN flowing in R3.

$$EN2 = 82pA \times 1k = 82nV, RMS$$

The voltage noise of the resistors must be calculated next. In general, resistor noise is given by:

$$ER = \sqrt{4 \times K \times T \times R \times (FH - FL)}$$

Where K is Boltzman's Constant, 1.39×10^{-23} , T is temperature (K), R is the resistor value, FH is the upper frequency, and FL is the lower frequency of interest.

At 25°C, this equation reduces to:

$$ER = \sqrt{R \times (FH - FL)} \times 1.28 \times 10^{-10}$$

To calculate ER1 we must consider R1 in parallel with R2,

$$ER1 = \sqrt{(1k \parallel 100k) \times (20kHz - 20Hz)} \times 1.28 \times 10^{-10}$$

$$ER1 = 570nV, RMS$$

Similarly, to calculate ER2,

$$ER2 = \sqrt{1k \times (20kHz - 20Hz)} \times 1.28 \times 10^{-10}$$

$$ER2 = 570nV, RMS$$

To calculate the total noise of the audio preamplifier using an LT1037, the RMS sum of the individual terms must be calculated.

$$TOTAL\ NOISE = \sqrt{EN^2 + EN1^2 + EN2^2 + ER1^2 + ER2^2}$$

$$TOTAL\ NOISE = \sqrt{353^2 + 80^2 + 80^2 + 570^2 + 570^2} = 880nV, RMS$$

To calculate p-p noise, multiply the RMS noise times 6; the total peak-to-peak noise is 5.3μV for this preamplifier.

It is important to realize this noise is referred to the input of the circuit; to obtain the output noise level, the input noise must be multiplied by the noise gain which can be different from the circuit gain:

$$OUTPUT\ NOISE = TOTAL\ NOISE \times NOISE\ GAIN$$

$$OUTPUT\ NOISE = 880nV \times 101 = 89\mu V, RMS\ or\ 534\mu V, peak-to-peak$$

It should be noted that design techniques to optimize DC performance will frequently result in higher noise. For exam-

ple, to minimize DC errors, a balance resistor is often placed in the + Input of an op amp to compensate for an error voltage created by bias current flowing in gain setting resistors connected to the - Input. This resistor will increase the output noise since op amp noise current must flow through the resistor, and thus create a voltage noise generator. For minimum noise levels, the resistor in the + Input should be 0Ω. As a side note, for precision op amps (LT1001, LT1007, OP07) that employ bias current cancellation techniques, this resistor should be 0Ω to minimize DC errors since the bias current equals the offset current.

Instructions for Operating NOISE

NOISE is a general purpose computer program to calculate noise in op amp circuits. It will run on any IBM-PC compatible computer with a direct call from DOS.

Noise specifications and data for Linear Technology op amps (LT10XX) are contained in the program's data file. All noise specifications are based on typical specifications at 25°C.

To operate NOISE:

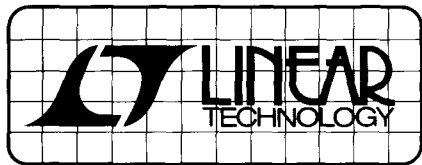
1. Boot the system with DOS and wait for DOS prompt "A >".
2. Insert the NOISE.EXE program disk into the A disk drive.
3. Type "NOISE" and <return>.

Operation in NOISE is menu driven throughout the program with default values on all parameters initially.

Best Op Amp for Lowest Noise vs Source Resistance

SOURCE R (R _{eq})	BEST OP AMP	
	@ LOW FREQ. (10Hz)	@ WIDEBAND (1kHz)
0Ω to 400Ω	LT1028	LT1028
400Ω to 1k	LT1007/37	LT1028
1k to 4k	LT1007/37	LT1028, LT1007/37
4k to 15k	LT1001	LT1007/37
15k to 30k	LT1001	LT1001, LT1007/37
30k to 70k	LT1001, LT1012	LT1001
70k to 150k	LT1012	LT1001, LT1012 LT1055/56/22, LT1057/58
150k to 600k	LT1012, LT1006/13/14	LT1012, LT1006/13/14 LT1055/56/22, LT1057/58
600k to 2M	LT1012 LT1055/56/22, LT1057/58	LT1012, LT1006/13/14 LT1055/56/22, LT1057/58
2M to 10M	LT1055/56/22, LT1057/58	LT1012 LT1055/56/22, LT1057/58
>10M	LT1055/56/22, LT1057/58	LT1055/56/22, LT1057/58

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DESIGN NOTES

Number 16 in a series from Linear Technology Corporation

October, 1988

Switched-Capacitor Low Pass Filters for Anti-Aliasing Applications

Richard Markell
Nello Sevastopoulos

INTRODUCTION

Many signal processing applications require a front end low pass filter to bandwidth limit the signal of interest. This filter is often crucial to the system designer since it determines the number of bits which the system can resolve by its noise and dynamic range. Until now, the designer rejected the use of switched-capacitor filters as being too noisy, having too much distortion, or because they were not usable at a high enough frequency. The LTC1064-1 8th order Cauer filter can compete directly with the discrete operational amplifier design. Not only that, but the cost and performance advantages are tremendous.

The LTC1064-1 is a complete 8th order, clock tunable Cauer (also known as elliptic) low pass switched-capacitor filter with internal thin film resistors. The passband ripple is $\pm 0.1\text{dB}$ and the stopband attenuation at 1.5 times the cutoff frequency is 72dB. The device is available in a 14-pin DIP or 16-pin surface mount package.

The LTC1064-1 boasts internal thin film resistors factory adjusted to optimize the Cauer 8th order response. The LTC1064-1 attains wide-band noise (2kHz-102kHz) of $150\mu\text{VRMS}$ and a total harmonic distortion of 0.03% for $V_{\text{IN}} = 3\text{VRMS}$. No external components are required for cutoff frequencies up to 20kHz. For cutoff frequencies over 20kHz two small value capacitors are required to maintain passband flatness.

By way of comparison, older switched-capacitor filters had noise in the millivolts, THD in the percents, and maximum corner frequencies limited to $< 20\text{kHz}$.

This note compares the performance of the LTC1064-1 8th order Cauer filter with internal thin film resistors to that of the equivalent filter built with operational amplifiers. The LTC1064-1 quad switched-capacitor filter competes favorably with op amp RC designs in most parameters of interest to the designer and wins easily when printed circuit board space is considered. Since it is tunable, the LTC1064-1 can replace not just one, but many op amp RC designs, if multi-frequency filtering is required. The specification comparisons become even more favorable to the LTC1064-1 as the frequencies become higher.

COMPARING THE LTC1064-1 WITH RC ACTIVE FILTERS UTILIZING OPERATIONAL AMPLIFIERS

Performance

The Cauer filter has target design specifications as follows: a cutoff frequency of 40kHz, $\pm 0.05\text{dB}$ passband ripple and a -72dB attenuation at 1.5 times the cutoff frequency. This filter is realized with stopband notches and it is considered a quite complex and selective filter realization. Figure 1 details the frequency response of this design.

An 8th order active RC was designed using a fully inverting state variable topology. This topology is considered "state-of-the-art" for active filters since all non-inverting inputs of the op amps are grounded. The discrete active RC version of the Cauer filter is quite complex requiring 16 op amps, 31 resistors and 8 capacitors. The op amps used for this comparison were TL084 quad FET input amplifiers. The circuit topology was optimized to yield the maximum useful input voltage swing.

Test Results

Figure 1 shows the frequency response of the LTC1064-1 connected as shown in Figure 3. The shape of the frequency response of the active RC state variable filter was very similar and its differences cannot

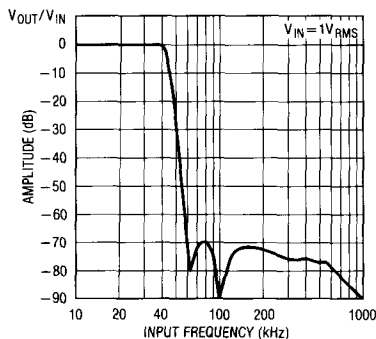


Figure 1. LTC1064-1 Frequency Response

be easily shown here. Figure 2, curve (a), details the TL084 state variable filter response near the 40kHz cutoff frequency. Laboratory "tweaking" of resistor values could not produce any better response than shown here. This is a passband ripple of approximately

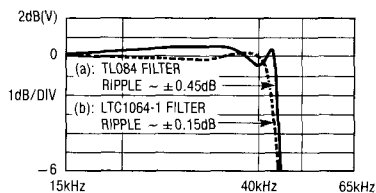


Figure 2. Passband Ripple

$\pm 0.45\text{dB}$. For comparison, the LTC1064-1 passband ripple is $\pm 0.15\text{dB}$ as shown in Figure 2, curve (b). This is for a clock to center frequency ratio of 100:1, or a 4MHz clock. The measured filter amplitude response at 1.5 times the cutoff frequency for the TL084 active RC filter was about -65dB while that of the LTC1064-1 was -68dB . The noise for the TL084 state variable implementation was $111\mu\text{V}_{\text{RMS}}$ while that for the LTC1064-1 was $145\mu\text{V}_{\text{RMS}}$. Second harmonic distortion measurements were also made on both filters and they are included on the summary chart, Table 1.

Table 1 compares the LTC1064-1, the switched capacitor implementation of the 8th order Cauer low pass filter, to the active RC. Both circuits operate with dual $\pm 7.5\text{V}$ supplies or a single 15V supply.

System Considerations

Not only does the LTC1064-1 compare favorably on individual specifications, but it wins easily when system considerations are evaluated. Suppose four sharp cutoff frequencies are needed. The

closest active RC solution is a 7th order single cutoff frequency Cauer filter. Four of these non-tunable devices (each a 2" x 3" hybrid) would be required for the four cutoff frequencies. This would be 24 square inches of PC board space. The discrete approach using operational amplifiers requires even more space. Since the LTC1064-1 is tunable, four frequencies can be selected merely by tuning the clock to the LTC1064-1. A complete LTC1064-1 system with tunable clock is estimated to occupy only 4 square inches of board space. This is a whopping savings of 6 times in board area. The LTC1064-1 wins easily in this category.

SUMMARY

In summary it can be seen from Table 1 that the LTC1064-1 is the equal of the active RC filter. In the pure specification battle there is no clear winner, but when the amazing difference in hardware complexity, the full clock tunability and the simple method of application of the LTC1064-1 device are all considered it is the sure winner.

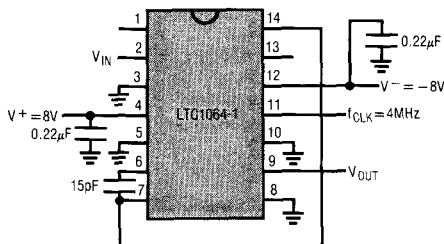


Figure 3. The LTC1064-1, Monolithic 8th Order Cauer Low Pass Filter Operating with a 4MHz Clock and Providing a 40kHz Cutoff Frequency

Table 1. 8th Order Cauer (Elliptic) LPF with a 40kHz Ripple Bandwidth

	# EXT OP AMPS	# EXT R's, 1%	# EXT CAPS, 5%	TUNABLE	WIDEBAND NOISE, RMS ⁴	DISTORTION V _{IN} = 1V _{RMS} , 3V _{RMS} (dB)	V _{OS} OUT (mV) ³	I _{SUPPLY} (mA)	ATTENUATION AT 60kHz	MEASURED PASSBAND RIPPLE	TRIMMING ²
RC Active TL084	16	31	8	No	111 μV	-87, -87	55	33	65dB	$\pm 0.45\text{dB}$	Yes
LTC1064-1	None ¹	None	1	Yes	145 μV	-70, -70	30	18	68dB	$\pm 0.15\text{dB}$	None

Note 1: An output inverting buffer (LT118) was used for driving cables during measurements.

Note 2: To obtain the $\pm 0.45\text{dB}$ ripple for the TL084, 3 resistors were trimmed.

Note 3: The output offset voltage numbers are as measured by DVM with the input of the filter grounded.

Note 4: Measurement BW (2kHz-102kHz).

For literature on our filter products, call 800-637-5545. For help with an application, call (408) 432-1900, Ext. 361.

Programming Pulse Generators for Flash Memories

Jim Williams

Recently introduced "flash" memories add electrical chip-erase and reprogramming to established EPROM technology. These features make them a cost effective and reliable alternative for updatable non-volatile memory. Utilizing the electrical program-erase capability requires linear circuitry techniques. The Intel 28F256 flash memory, built on the ETOX™ process, specifies programming operation with 12V or 12.75V (faster erase/program times) amplitude pulses. These "V_{pp}" amplitudes must fall within 1.6%, and excursions beyond 14.0V will damage the device.

Providing the V_{pp} pulse requires generating and controlling high voltages within the tightly specified limits. Figure 1's circuit does this. When the V_{pp} command pulse goes low (trace A, Figure 2) the LT1072 switching regulator drives L1, producing high voltage. DC feedback occurs via R1 and R2, with AC roll-off controlled by C1 and R3-C2. The result is a smoothly rising V_{pp} pulse (trace B) which settles to the required value. The specified R1 values allow either 12V or 12.75V outputs. The 5.6V zener permits the output to return to 0V when the V_{pp} command goes high. It may be deleted in cases where a 4.5V minimum output is acceptable (see Intel 28F256 data sheet). The 0.1% resistors combine with the LT1072's tight internal reference to eliminate circuit trimming

requirements. Additionally, this circuit will not spuriously overshoot during power-up or down.

Figure 1's repetition rate is limited because the regulator must fully rise and settle for each V_{pp} command. Figure 3's circuit serves cases which require higher repetition rate V_{pp} pulses. Here, the switching regulator runs continuously, with the V_{pp} pulses generated by the A1-A2 loop. If desired, the "V_{pp} Lock" line can be driven, shutting down the regulator to preclude any possibility of inadvertent V_{pp} outputs. When V_{pp} Lock goes low (trace A, Figure 4) the LT1072 loop comes on (trace B), stabilizing at about 17V. Pulsing the V_{pp} command line low causes the 74C04 (trace C) to bias the LT1004 reference. The LT1004 clamps at 1.23V with A1 and A2 giving a scaled output (trace D). The 680pF capacitor controls loop slewing, eliminating overshoots. Figure 5 details the V_{pp} output. Trace A is the 74C04 output, with trace B showing clean V_{pp} characteristics. As in Figure 1, spurious V_{pp} outputs are suppressed during power-up or down. The diode path around A2 prevents overshoot during short circuit recovery.

A good question might be; "Why not set the switching regulator output voltage at the desired V_{pp} level and use a simple low resistance FET or bipolar switch?" Figure 6 shows that this is a potentially dangerous approach. Figure 6A shows

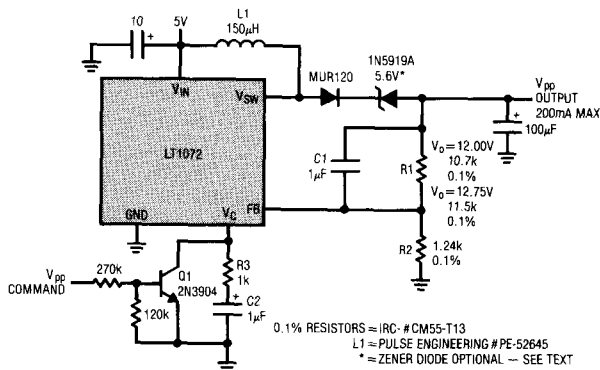


Figure 1. Basic Flash Memory V_{pp} Pulse Generator

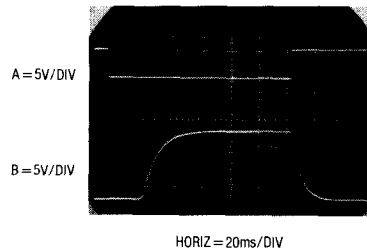


Figure 2. Waveforms for Basic Flash Memory Pulser

the clean output of a low resistance switch operating directly at the V_{pp} supply. The PC trace run to the memory chip looks like a transmission line with ill-defined termination characteristics. As such, Figure 6A's clean pulse degrades and rings badly (Figure 6B) at the memory IC's pins. Overshoot exceeds 20V, well beyond the 14V destruction level. The controlled edge times of the circuits discussed eliminate this problem. Further discussion of these and other circuits appears in LTC Application Note 31, "Linear Circuits for Digital Systems" (Available February, 1989).

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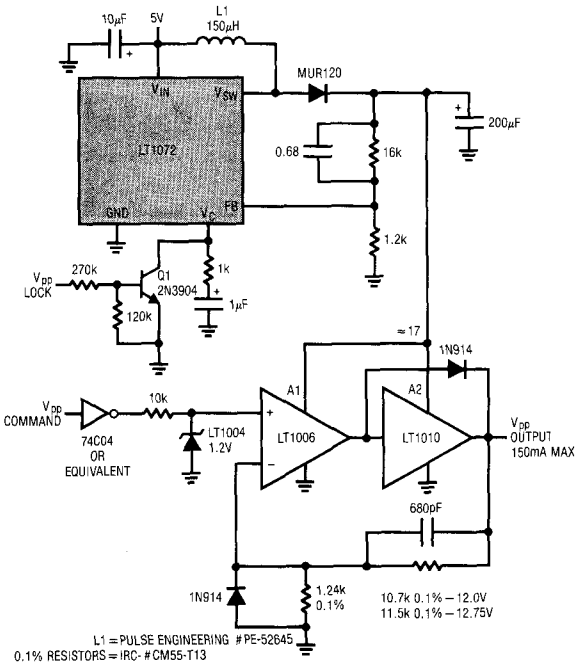


Figure 3. High Repetition Rate V_{pp} Pulse Generator

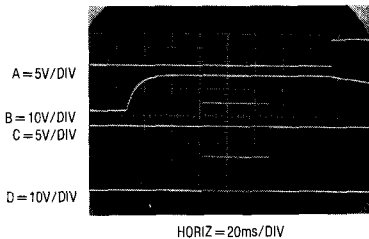


Figure 4. Operating Details of High Repetition Rate Flash Memory Pulser

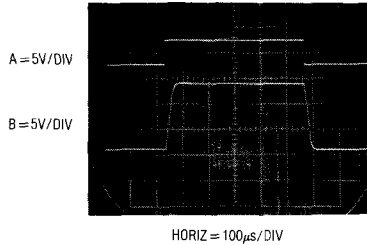


Figure 5. Expanded Scale Display of Figure 3's V_{pp} Pulse. Controlled Risetime Eliminates Overshoots.

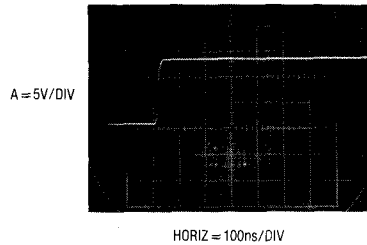
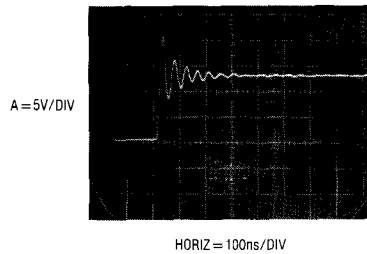


Figure 6A. An "Ideal" Flash Memory V_{pp} Pulse ...



... Figure 6B. Rings at Destructive Voltages After a PC Trace Run

For literature on LT1006, LT1010 and LT1072, call 800-637-5545. For applications help, call (408) 432-1900 Ext. 361.

A Battery Powered Lap Top Computer Power Supply

Brian Huffman

Most battery powered lap top computers require regulated multiple output potentials. Problems associated with such a supply include magnetic and snubber design, loop compensation, short circuit protection, size and efficiency. Typical output power requirements include 5V @ 1A for memory and logic circuitry and $\pm 12V$ @ 300mA to drive the analog components. Primary power may be either a 6V or 12V battery. The circuit in Figure 1 meets all these requirements. The LT1071 simplifies the power supply design by integrating most of the switching regulator building blocks. Also, the off-the-self transformer eliminates all the headaches associated with the magnetic design.

The circuit is a basic flyback regulator. The transformer transfers the energy from the 12V input to the 5V and $\pm 12V$ outputs. Figure 2 shows the voltage (trace A) and the current (trace B) waveforms at the V_{SW} pin. The V_{SW} output is a collector of a common emitter NPN, so current flows through it when it is low. The circuit's 40kHz repetition rate is set by the LT1071's internal oscillator. During the V_{SW} (trace A) "on" time, the input voltage is applied across the primary winding. Notice that the current in the primary (trace C) rises slowly as

the magnetic field builds up. The magnetic field in the core induces a voltage on the secondary windings. This voltage is proportional to the input voltage times the turns ratio. However, no power is transferred to the outputs because the catch diodes are all reversed biased. The energy is stored in the magnetic field. The amount of energy stored in the magnetic field is a function of the current level, how long the current flows, the primary inductance and the core material. When the switch is turned "off" energy is no longer transferred to the core, causing the magnetic field to collapse. The voltage on the transformer windings is proportional to time-rate-of-change of the magnetic field. Hence, the collapsing magnetic field causes the voltages on the windings to change. Now the catch diodes are forward biased and the energy is transferred to the outputs. Trace D is the voltage seen on the 5V secondary and trace E is the current flowing through it. The energy transfer is controlled by the LT1071's internal error amplifier, which acts to force the feedback (FB) pin to a 1.24V reference. The error amplifier's high impedance output (V_C pin) uses an RC damper for stable loop compensation. If a 6V input is desired, use just one primary winding and an LT1070.

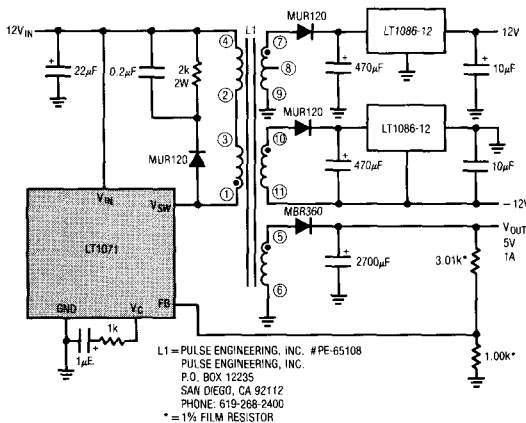


Figure 1. Multi-Output Flyback Converter

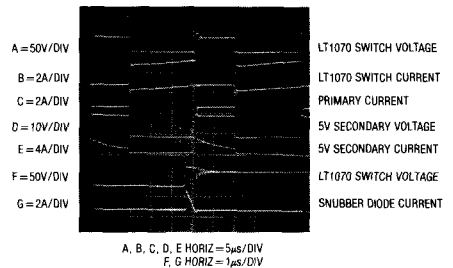


Figure 2. Waveforms for Continuous Mode Operation

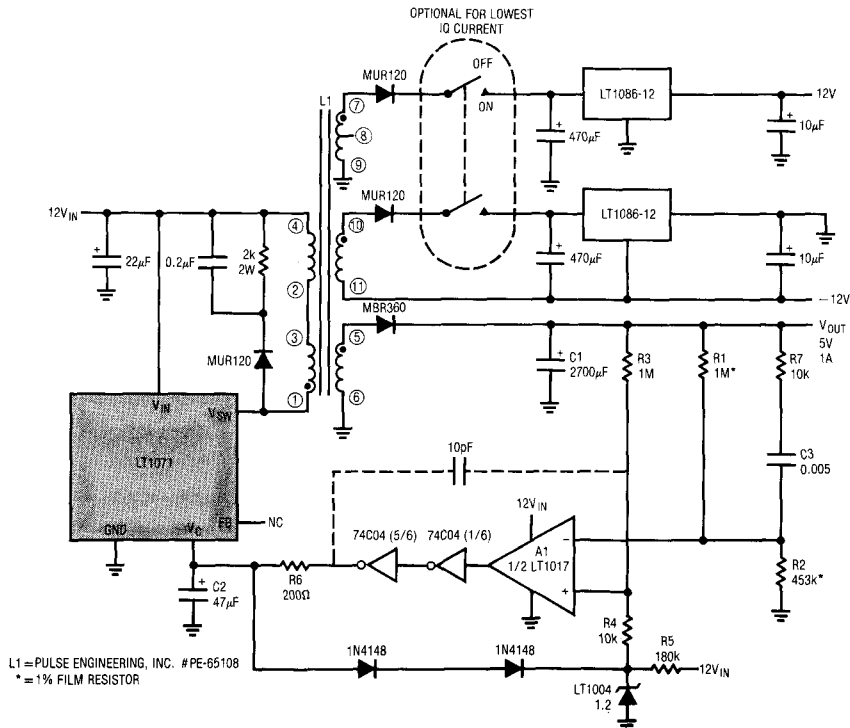


Figure 3. Multi-Output, Transformer Coupled Low Quiescent Current Converter

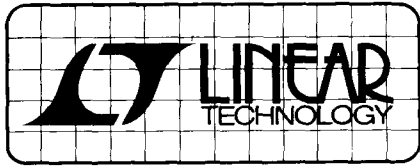
This is not an ideal transformer so not all the energy is coupled into the secondary. The energy left in the primary winding causes the overvoltage spike seen on the V_{SW} pin (trace F). This phenomenon is modeled by a leakage inductance term placed in series with the primary winding. When the switch is turned "off" current continues to flow in the inductor, causing the snubber diode to conduct (trace G). The snubber network clamps the voltage spike, preventing excessive voltage at the LT1071's V_{SW} pin. When the snubber diode current reaches zero, the V_{SW} pin voltage settles to a potential related to the turns ratio, output voltage and input voltage.

Post regulators are needed on the unregulated outputs if the cross regulation error is too great. Such error can be as much as 20% depending upon output loading conditions. Note that the floating secondaries allow a -12V output to be obtained with a positive voltage regulator. The isolation allows the input of the regulator to float above ground. The LT1086 positive voltage regulators maintain both positive and negative outputs within 1%.

If battery capacity is limited by size or weight this circuit's 9mA quiescent current may be too high. Figure 3's modification offers output current in the ampere range with only microamps of quiescent drain. Further information about this circuit can be found in LTC Application Note AN29 "Some Thoughts on DC-DC Converters," page 8.

By using standard magnetics and a simplified switching regulator the design time needed to implement this power supply is greatly reduced. Although these circuits demonstrated a flyback topology, the LT1070/LT1071/LT1072 can easily handle other configurations including buck, boost, forward and inverting. Examples are given in LTC Application Notes; AN19 "LT1070 Design Manual," AN25 "Switching Regulators for Poets," and AN29 "Some Thoughts on DC-DC Converters."

For literature on Switching Regulators, call 800-637-5545. For applications help, call (408) 432-1900, Ext. 361.



DESIGN NOTES

Number 19 in a series from Linear Technology Corporation

January, 1989

A Two Wire Isolated and Powered 10-Bit Data Acquisition System Guy Hoover and William Rempfer

Introduction

For reasons of safety or to eliminate error producing ground loops, it is often necessary to provide electrical isolation between measurement points and the microprocessor. Unfortunately, the isolated side of this measurement system must still be provided with power. One alternative is to power the isolated side of the circuit with batteries. This solution works if power consumption is low, environmental conditions are mild and the batteries are easily accessible. If these conditions are not met a separate isolated supply may be constructed. This can be both difficult and expensive. This design note describes a transformer isolated system in which one small pulse transformer provides both power and a data path.

The circuit of Figure 1 is a 10-bit data acquisition system with 700V of isolation. The circuit takes advantage of the serial architecture of the LTC1092 which allows data and power to be transmitted using only one transformer. A 10-bit conversion can be completed and the data transferred to the microprocessor in 100 μ s. Using standard ribbon cable the isolated side of this circuit has been remotely located as much as 50 feet from the transformer without affecting circuit performance.

Circuit Description

In Figure 1, a 4 μ s wide CS pulse clears the 74HC164 shift registers which will hold the D_{OUT} word of the LTC1092. Additionally, the CS signal sends a 15V pulse through the transformer which charges the 1 μ f capacitor. The CS pulse width must be in the 2–6 μ s range for the transformer shown, a small Pulse Engineering model. A pulse more than 6 μ s will saturate the transformer while a pulse width of less than 2 μ s will not transfer enough energy through the transformer to keep the isolated supply from drooping during the conversion. The CS pulse can be generated with software or hardware. The LT1021-5 produces a regulated 5V at its output once the 1 μ f capacitor is charged to approximately 7.2V. The LT1021-5 regulated output powers the isolated side of the circuit. Initially several CS pulses may be required to charge the 1 μ f capacitor to 7.2V. Once charged however, only one CS pulse

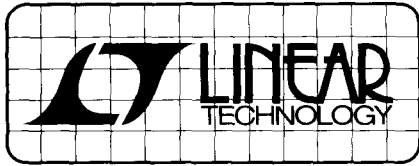
per cycle is required to keep the isolated supply from drooping as long as the cycle is repeated every 100 μ s. The 15V CS signal is also attenuated and delayed. This signal is used to reset the clock circuit and begin the conversion of the LTC1092. The delay is required to allow the transformer flyback to die out before transmitting the D_{OUT} word of the LTC1092 across it.

The clock circuit is a simple oscillator that is gated by a combination of the CS signal and the 74HC161 counter so that for each CS signal the clock circuit generates 12 pulses and then is gated off. These 12 pulses are used to perform the A/D conversion and shift the D_{OUT} word of the LTC1092 into the 74HC164 shift registers where the data can be acquired by the microprocessor.

The D_{OUT} serial data of the LTC1092 is encoded with the clock, differentiated and sent across the transformer. The encoding circuitry pulse width modulates the LTC1092 output. The encoding circuitry uses two one shots to combine the data and the clock. For each negative going clock edge a positive pulse is produced at the output of the encoding circuitry. A wide pulse at the output of the encoding circuitry represents a logical 1 and a narrow pulse represents a logical 0 as shown in the timing diagram of Figure 2. The schottky diodes on the output of the 74HC04 capacitor driver are to protect the driver from damage caused by the initial 15V pulse and the resulting flyback.

The differentiated spikes from the transformer are "integrated" by the schmitt inverters and the 74HC74. Again, schottky diodes as well as current limiting resistors are used to protect the gates from transformer excursions beyond the supplies at their inputs. The encoded data is decoded by one half of the 74HC221 which reconstructs the clock. The 74HC164s convert the data to parallel format.

The 10k Ω pull-up resistor forces the output of the LTC1092 high when the A/D is in the high impedance state. When the A/D output becomes active a start bit (logic 0) is clocked out.



DESIGN NOTES

Number 20 in a series from Linear Technology Corporation

February, 1989

Hex Level Shift Shrinks Board Space

Brian Huffman

Although simple in concept, interfacing digital levels between different logic families usually requires many parts and appreciable board space. Other applications that require some form of level shifting of the output swing have solutions just as complicated. A logic to CMOS analog switch (Figure 1) is just one example where a level shift must occur. A new device, the LTC1045, solves this and other level shift related problems conveniently. The LTC1045 is a hex level translator with a linear comparator on the front end. A latch and three-state output buffer are at the back. These features make it useful in other applications as a hex comparator or in interfacing to a data bus. Almost any input and output voltage requirements can be accommodated by simply setting the level of the appropriate power supply voltages.

The LTC1045 consists of six high speed comparators with output latches and three-state capability (see Figure 2). Each comparator's non-inverting input is brought out separately. The inverting inputs of comparators 1-4 are tied to V_{TRIP1} and 5-6 are tied to V_{TRIP2} . With these inputs the switching point of the comparators can be set anywhere within the

common-mode range of V^- to $(V^+ - 2V)$. There are four power supply pins on the LTC1045: V^+ , V^- , V_{OH} and V_{OL} . V^+ and V^- power the comparator's front end, and V_{OH} and V_{OL} power the output drivers. Almost any combination of power supply voltages can be used. There are three restrictions: V_{OH} must be less than or equal to V^+ ; there must be a minimum differential voltage of 4.5V between V^+ and V^- and 3V between V_{OH} and V_{OL} . The maximum voltage between any two pins must not exceed the 18V absolute maximum.

The supply current is programmed with an external resistor. The R_{SET} resistor allows trade-offs between speed and power consumption. The propagation delay, with the I_{SET} pin at V^- and a single 5V supply, is typically 100ns with a total supply current of 4.5mA. The quiescent current can be brought down to 100 μ A (15 microamps per comparator) with an R_{SET} of 1M and a propagation delay of only 1.2 μ s. In addition, the I_{SET} pin completely shuts off power and latches the translator output voltages. The DISABLE input sets the six outputs to a high impedance state allowing the LTC1045 to be interfaced to a data bus.

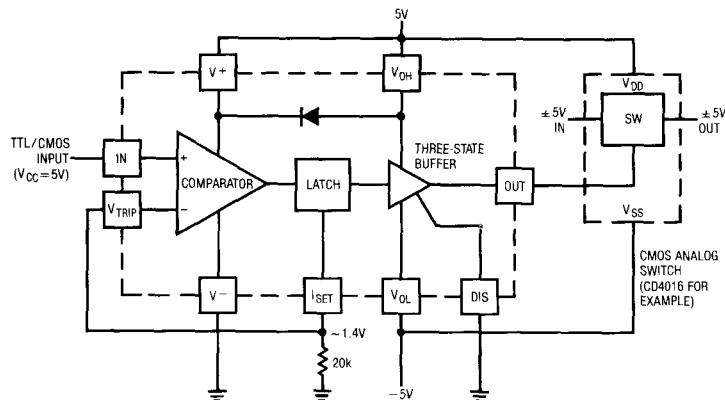


Figure 1. TTL/CMOS Logic Levels to $\pm 5V$ Analog Switch Driver

Floating Input Extends Regulator Capabilities

Brian Huffman

Many applications require circuit performance that is unachievable with conventional regulator design. This results in added complexity to the circuit. However, some problems can easily be solved by floating the input to the regulator. A floating input can either be a battery, or a secondary winding that is galvanically isolated from all other windings. With this method high efficiency negative voltage regulation, high voltage regulation, and low saturation loss positive buck switching regulator can all be achieved easily.

Low dropout negative voltage regulators are not currently available. This would seem to preclude high efficiency negative linear regulators. Such regulation is frequently desired in

switching supply post regulators; however, if the secondary windings are isolated from one another, a low dropout positive voltage regulator can be used for negative regulation (Figure 1).

In this circuit the LT1086 serves the voltage between the output and the adjust pin to 1.25V. The positive regulation is accomplished by conventional regulator design. Negative voltage regulation is achieved by connecting the output of the positive voltage regulator to ground. The V_{IN} pin floats to 1.5V or greater, above ground. This technique can be used with any positive voltage regulator, although highest efficiency occurs with low dropout types.

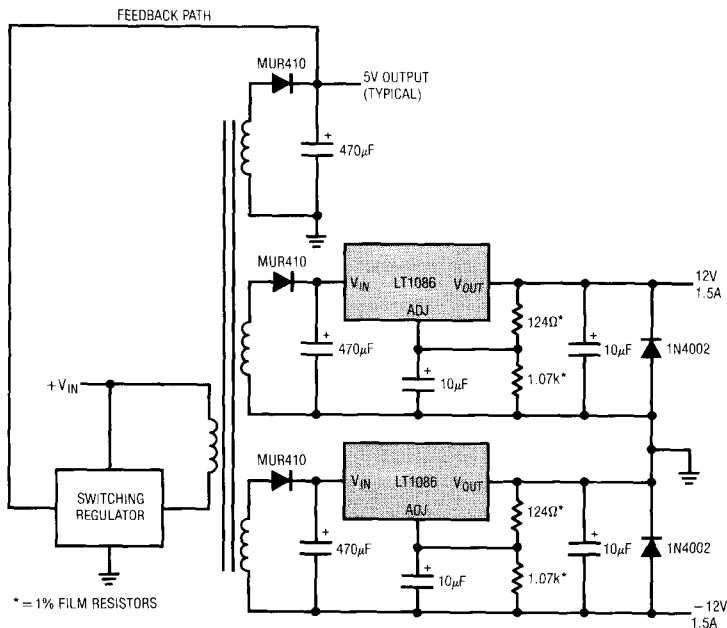


Figure 1. High Efficiency Negative Voltage Regulation

Another example where floating a linear regulator can be useful is shown in Figure 2. In this case high voltage regulation can be handled if split secondary windings are available. This allows the regulators to be connected in series. Neither regulator exceeds its maximum differential voltage even under short circuit conditions.

High current positive buck switching regulators can have excessive saturation losses since most switches are Darlingtons. As much as 2V can be dropped across a Darlington or composite PNP switching transistor. However, efficiency can be increased and power dissipation requirements greatly reduced if the input is allowed to float (Figure 3).

The circuit in Figure 3 uses an LT1070 to perform a buck conversion. The LT1070 is a current mode switching regulator. The V_{SW} pin output is a collector of a common emitter NPN, so current flows through it when it is low. The 40kHz repetition rate is set by the LT1070's internal oscillator. When the V_{SW} pin is "on," current flows through the load, the inductor, and into the V_{SW} pin. During this time a magnetic field is built up in the inductor. When the switch is turned "off," the magnetic field collapses dumping energy into the load through D1. The input of the switching regulator floats to a potential set by the output.

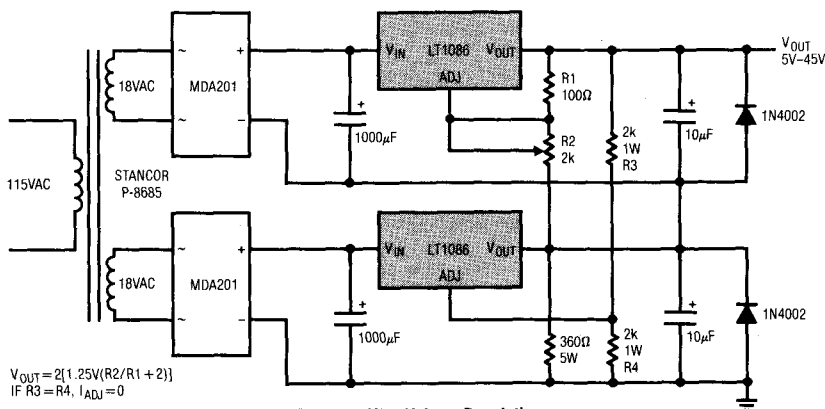


Figure 2. High Voltage Regulation

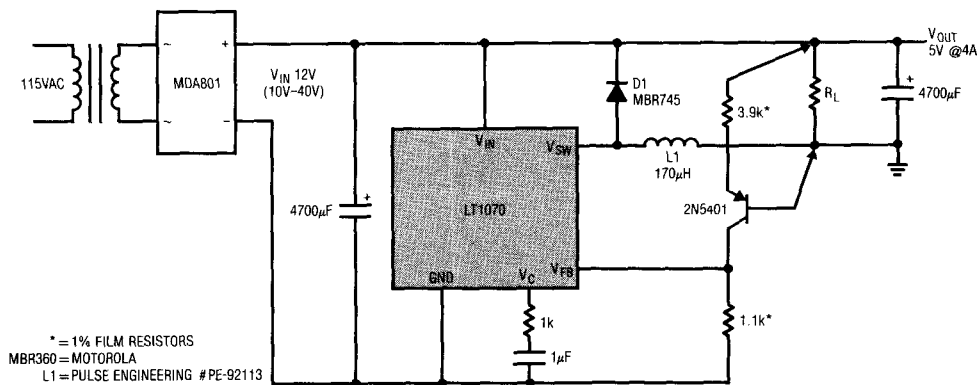
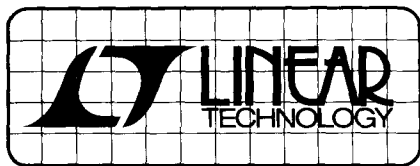


Figure 3. Floating Input Low Saturation Loss Buck Regulator

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DESIGN NOTES

Number 22 in a series from Linear Technology Corporation

May, 1989

New 12-Bit Data Acquisition Systems Communicate with Microprocessors Over 4 Wires

As board space and semiconductor package pins become more valuable, serial data transfer methods between microprocessors (MPUs) and their peripherals become more and more attractive. Not only does this save lines in the transmission medium, but, because of the savings in package pins, more function can be packed into both the MPU and the peripheral. Users are increasingly able to take advantage of these savings as more MPU manufacturers develop serial ports for their products^[1-3]. However, peripherals which are able to communicate with these MPUs must be available in order for users to take full advantage. Also, MPU serial formats are not standardized so not all peripherals can talk to all MPUs.

The LTC1290 Family

A new family of 12-bit data acquisition circuits has been developed to communicate over just 4 wires to the recently developed MPU synchronous serial formats as well as to MPUs which do not have serial ports. These circuits feature software configurable analog circuitry including analog multiplexers, sample and holds, bipolar and unipolar conversion modes and the ability to shut power completely off. They also have serial ports which can be software configured to communicate with virtually any MPU. Even the lowest grade device features guaranteed ± 0.5 LSB linearity over the full operating temperature range. Reduced span operation, accuracy over a wide temperature range and low power single supply operation make it possible to locate these circuits near remote sensors and transmit digital data back through noisy media to the MPU. Figure 1 shows a typical hookup of the LTC1290, the first member of this data acquisition family. For more detail, refer to the LTC1290 data sheet.

Included are eight analog inputs which can common-mode to both supply rails. Each can be configured for unipolar or bipolar conversions and for single-ended or differential inputs by sending a data input (D_{IN}) word from the MPU to the LTC1290 (Figure 1).

Both the power supplies are bypassed to analog ground. The V^- supply allows the device to operate with inputs which swing below ground. In single supply applications it can be tied to ground.

The span of the A/D converter is set by the reference inputs which, in this case, are driven by a 2.5V LT1009 which gives an LSB step size of 0.61mV. However, any reference voltage within the power supply range can be used.

The 4 wire serial interface consists of an active low chip select pin (CS), a shift clock (SCLK) for synchronizing the data bits, a data input (D_{IN}) and a data output (D_{OUT}). Data is transmitted and received simultaneously (full duplex), minimizing the transfer time required.

The external ACLK input controls the conversion rate and can be tied to SCLK as in Figure 1. Alternatively, it can be derived from the MPU system clock (e.g., the 8051 ALE pin) or run asynchronously. When the ACLK pin is driven at 4MHz, the conversion time is 13 μ s.

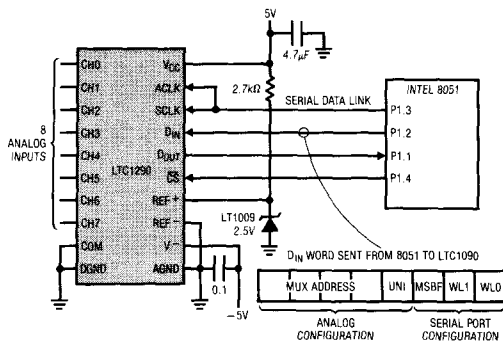


Figure 1. A Typical Hookup of the LTC1290

Advantages of Serial Communications

The LTC1290 can be located near the sensors and serial data can be transmitted back from remote locations through isolation barriers or through noisy media.

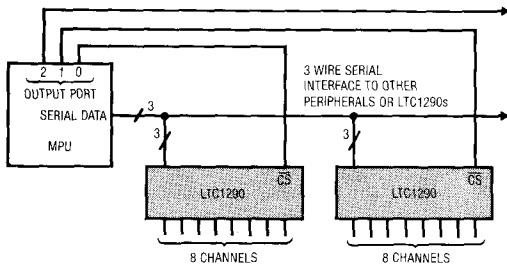


Figure 2. Several LTC1290s Sharing One 3 Wire Serial Interface

Using fewer pins for communication makes it possible to pack more function into a smaller package. LTC1290 family members are complete systems being offered in packages ranging from 20 pins to 8 pins (e.g., LTC1291, 1292, 1293, 1294).

Speed is Usually Limited by the MPU

A perceived disadvantage of the serial approach is speed. However, the LTC1290 can transfer a 12-bit A/D result in 6 μ s when clocked at its maximum rate of 2MHz. With the minimum conversion time of 13 μ s, throughput rates of 50kHz are possible. In practice, the serial transfer rate is usually limited by the MPU, not the LTC1290. Even so, throughput rates of 20kHz are not uncommon when serial port MPUs are used. For MPUs without serial ports, the transfer time is somewhat longer because the serial signals are generated with software. For example, with the Intel 8051 running at 12MHz, a complete transfer takes 96 μ s. This makes possible throughput rates of approximately 10kHz.

Talking to Serial Port MPUs

By accommodating a wide variety of transfer protocols, the LTC1290 is able to talk directly to almost all synchronous serial formats. The last 3 bits of the LTC1290 data input (D_{IN}) word define the serial format and power shutdown (see Figure 3). The MSBF bit determines the sequence in which the A/D conversion result is sent to the processor (MSB or LSB first). Figure 4 shows several popular serial formats and the appropriate D_{IN} word for each. Typically a complete data transfer cycle takes only about 15 lines of processor code.

WL1	WL2	Output Word Length
0	0	8 Bits
0	1	Power Shut Down
1	0	12 Bits
1	1	16 Bits

Figure 3. Word Length and Power Shutdown

Talking to MPUs without Serial Ports

The LTC1290 talks to serial port processors but works equally well with MPUs which do not have serial ports. In these cases, \overline{CS} , SCLK and D_{IN} are generated with software on 3 port lines. D_{OUT} is read on a fourth. Figure 4 shows the appropriate D_{IN} word for communicating with MPU parallel ports. Figure 1 shows a 4 wire interface to the popular Intel 8051. A complete transfer takes only 33 lines of code.

Sharing the Serial Interface

No matter what processor is used, the serial port can be shared by several LTC1290s or other peripherals (see Figure 2). A separate \overline{CS} line for each peripheral determines which is being addressed.

Conclusions

The LTC1290 family provides data acquisition systems which communicate via a simple 4 wire serial interface to virtually any microprocessor. By eliminating the parallel data bus they are able to provide more function in smaller packages, right down to 8 pin DIPs. Because of the serial approach, remote location of the A/D circuitry is possible and digital transmission through noisy media or isolation boundaries is made easier without a great loss in speed.

Type of Interface	LTC1090 Data Format	LTC1090 D_{IN} Word							
		Analog Configuration	MSBF	WL1	WL0				
All Parallel Port MPUs	MSB First 12 Bits	X	X	X	X	X	1	1	0
National MICROWIRE* MICROWIRE/PLUS*	MSB First 12 Bits	X	X	X	X	X	1	1	0
Motorola SPI	MSB First 16 Bits	X	X	X	X	X	1	1	1
Hitachi Synchronous SCI	LSB First 16 Bits	X	X	X	X	X	0	1	1
TI TMS7000 Serial Port		X	X	X	X	X	0	1	1

Figure 4. The LTC1290 Accommodates Both Parallel and Serial Ports

*MICROWIRE and MICROWIRE/PLUS are trademarks of National Semiconductor Corp.

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- [1] Aleaf, Abdul, and Richard Lazovick, "Microwire/Plus," National Semiconductor, Santa Clara, CA, Wescon '86, Session 21.
- [2] Derkach, Donald J., "Serial Data Transmission in MCU Systems," RCA Solid State, Somerville, NJ, Wescon '86, Session 21.
- [3] Kalinka, Theodore J., "Versatile Serial Peripheral Interface (SPI)," RCA Solid State, Somerville, NJ, Wescon '86, Session 21.

For LTC1290 literature, call 800-637-5545. For help with an application call 432-1900, Ext. 445.

Micropower, Single Supply Applications:

- (1) A Self-Biased, Buffered Reference
- (2) Megaohm Input Impedance Difference Amplifier

Walt Jung
George Erdi

A Self-Biased, Buffered Reference

Voltage reference circuits are common to precision analog designs, in a wide variety of forms. They can be either two or three terminal in basic configuration, and may or may not also provide buffering against line and/or load immunity. Micropower analog circuits are growing in both fashion as well as performance, and micropower voltage references have been available. However, it is not often that a micropower reference combines common features of very low DC errors, and line/load buffering. The circuit of Figure 1 is an unusual form of reference circuit, in that it achieves these goals.

The leading virtue of this circuit lies in how it capitalizes on some key operating features for all of the devices used. First, the LT1034, a 1.2V two terminal reference diode allows basic low TC micropower operation, by virtue of its low minimum current requirement of only 20 μ A. Normally, such a diode would be fed with a simple source resistor to V⁺, to maintain the bias current plus the load current. This standard shunt regulator type of use is unbuffered, so for higher load currents, the micropower aspect is lost. It can also be sensitive to line voltage changes.

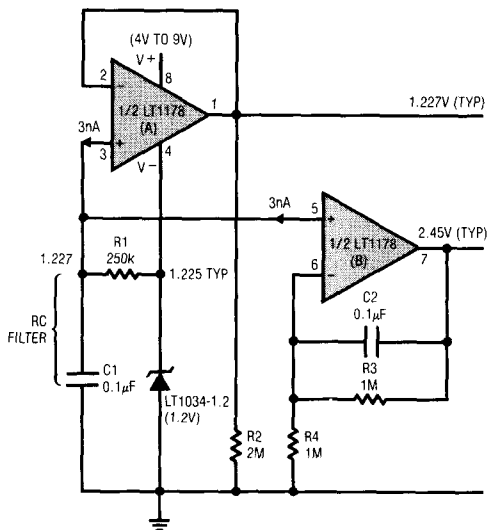


Figure 1. Self-Buffered Micropower Reference

When the LT1178 op amp enters the picture, a "free" and constant bias current source is available — *the 30 μ A quiescent supply current of the op amp itself!* To allow the op amp to self-bias as well as voltage-buffer the reference diode, the op amp used must have both input and output swings which include the amplifiers V⁻ pin potential. In the case here, this potential is nominally 1.2V above ground, by virtue of the reference diode's terminal voltage. More precisely, this will be 1.225V \pm 15mV, at the diode cathode. The overall TC of the circuit is essentially that of the LT1034 reference, or 20ppm/ $^{\circ}$ C (maximum for "B" grade).

With an op amp such as the LT1178, whose input and output swing does include the negative rail, a simple follower configuration can be set up to buffer the reference voltage. R1 feeds a filtered version of the reference voltage to the A section op amp's (+) input, which is then replicated with a low source impedance by the DC follower of the A section. The second op amp section is also connected to this node, and is shown here as a precision 2X DC amplifier, providing a buffered +2.45V output. A subtle biasing step is used, where

the two amplifier bias currents are combined in R1. This produces a drop of a few mV above the 1.225V, so as to set up the output stage of the A section in a more linear region. The output bleed resistor R2 also helps this biasing, by pulling a constant 0.6 μ A from the output of this stage.

Overall, the circuit's quiescent current is 30 μ A, which is essentially the bias current of the dual amplifier, plus the currents in R2 and R3. It can however source several mA of load current, to external loads. For example, the "A" stage output of 1.225V has a typical output impedance of 30 μ V/mA, for currents of 10mA or less.

Note that current *sinking* types of loads should be used with caution, as the sink current must necessarily flow through the reference diode. While this can be as high as 20mA for the diode itself, the saturation characteristics of the A stage as used here will add some error, proportional to the current. The circuit's greatest application advantage lies with loads which source current, and so allow the true micropower

operation. It operates from supplies of 3V greater than the reference voltage, in this case a battery stack of +4V to +9V. Typical line regulation is on the order of 10ppm/V.

More generally, the circuit will also function with the LT1078 op amp, a related micropower dual with a nominal 40 μ A/channel quiescent current, and input/output ranges similar to the LT1178. It also functions with the LT1004 type 1.2V or 2.5V references, producing proportionally scaled DC outputs, with somewhat greater drift.

If only one of the two reference outputs is needed, the LT1077 single op amp can be substituted for either side A or side B. Supply current is 45 μ A.

References

Jung, W.G. *IC Op Amp Cookbook, 3d Ed.*, Ch 4, "References" Howard W. Sams, Indianapolis, IN 1986.

Megaohm Input Impedance Difference Amplifier

The usefulness of difference amplifiers is limited by the fact that the input resistance is equal to the source resistance. The picoampere offset current and low current noise of the LT1077 allows the use of 1M Ω source resistors without degradation in performance. In addition, with megaohm resistors micropower operation can be maintained.

Typical performance is:

- Bandwidth = 25kHz
- Output Offset = 0.7mV
- Output Noise = 80 μ Vpp (0.1Hz to 10Hz)
260 μ V RMS over full bandwidth
- Supply Current = 45 μ A

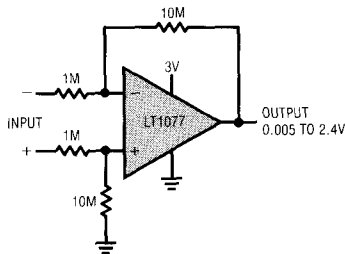


Figure 2. Gain of 10 Difference Amplifier

Although the difference amplifier operates on a single 3V battery, the input common mode range extends to 250mV below ground with proper gain of ten amplification. As the positive input is pulled further below ground to as low as -1V, the input stage saturates, but the output still stays low because the LT1077 is equipped with a unique phase reversal protection circuit. Using competitive single supply op amps in this application, the output switches high.

Another interesting feature of the LT1077 in the differential amplifier configuration is its ability to sink current while swinging to ground. Competitive micropower single supply op amps need a pull down resistor at the output to sink current, the LT1077 does not. When the input common mode voltage is 1.8V, the output has to sink a minuscule 0.16 μ A. However, competitive devices cannot sink any current, and need a 30k resistor from output to ground to pull the output to 5mV (5mV \approx 30k \times 0.16 μ A). When the output now swings to 2.4V, 80 μ A will flow in the pull down resistor, completely dominating the micropower current budget.

For literature on our complete micropower line, call (800) 637-5545. For applications help, call (408) 432-1900, Ext. 445.

Complex Data Acquisition System Uses Few Components

Richard Markell

Introduction

Sophisticated filter system designs frequently demand expensive printed circuit boards chock-full of operational amplifiers and precision capacitors. Digital filters require fewer but more expensive devices and a lot of software. However, advances in switched capacitor filters have made the design of elegant filter systems cheaper, easier and much smaller. The system shown in block diagram form in Figure 1 is a good example. It is a typical system for filtering transducer signals. Its input is a DC-to-20kHz signal; its output allows signals to be analyzed in three frequency bands.

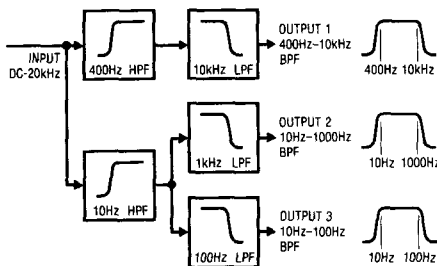


Figure 1. Filter System Block Diagram

Implementation

A system implemented using switched capacitor filters is shown in schematic form in Figure 2. This implementation uses two LTC1064 quad switched capacitor building blocks and one LTC1062 5th order Butterworth lowpass filter. The system requires the use of one operational amplifier, an LT1007.

Filter Design Specifications and Test Results

Filter 1 — a 400Hz-to-10kHz bandpass filter, with passband ripple of 1dB and passband noise of $200\mu\text{VRMS}$, Figure 3.

Filter 2 — a 10Hz-to-100Hz bandpass filter, with passband ripple of 1dB and passband noise of $500\mu\text{VRMS}$, Figure 4.

Filter 3 — a 10Hz-to-1kHz bandpass filter, with passband ripple of 1dB and passband noise of $390\mu\text{VRMS}$, Figure 5.

These wideband filters are made by cascading 4th order elliptic lowpass and highpass filters. The single exception is the 5th order Butterworth lowpass filter used in the 400Hz-to-10kHz section.

System Considerations

The LTC1064 quad switched capacitor filters used are building blocks capable of implementing up to 8th order filters. One LTC1064 implements both a 4-pole elliptic 400Hz highpass filter and a 4-pole elliptic 1kHz lowpass filter. The other LTC1064 implements a 4-pole elliptic 100Hz lowpass filter and a 4-pole elliptic 10Hz highpass filter. The LTC1062 is a 5-pole Butterworth lowpass filter set at 10kHz.

Resistors R_{11A} to R_{H2A} implement the 400Hz elliptic highpass filter in Device A. The 1kHz elliptic lowpass filter in Device A is implemented by R_{13A} to R_{44A} . Resistors R_{11B1} to R_{42B} implement the 10Hz elliptic highpass filter in Device B. The 100Hz elliptic lowpass filter in Device B is implemented by R_{13B} through R_{44B} . The LTC1062 is hardware programmed for 10kHz by R_{50} and C_{50} .

The 8th order LTC1064 devices allow the use of two sections in the 100:1 clock-to-center frequency mode and two sections in the 50:1 mode. (Resistor programming can then be used to further extend the clock-to-center frequency range to 25:1 for two sections and 250:1 for the other two sections.) This allows decade-wide bandpass filters to be built using only one LTC1064 at one clock frequency.

Conclusion

This is only one use of the new switched capacitor building blocks, the LTC1064 family of quad switched capacitor filters. These filters have wide flexibility. For example, the 10Hz-to-100Hz filter could be used at 20Hz-to-200Hz simply by doubling the clock, which sets the filter frequency. Similarly, bands of interest could be inspected by sweeping the clock. The devices work with center frequencies as high as 100kHz in circuits with similar simplicity.

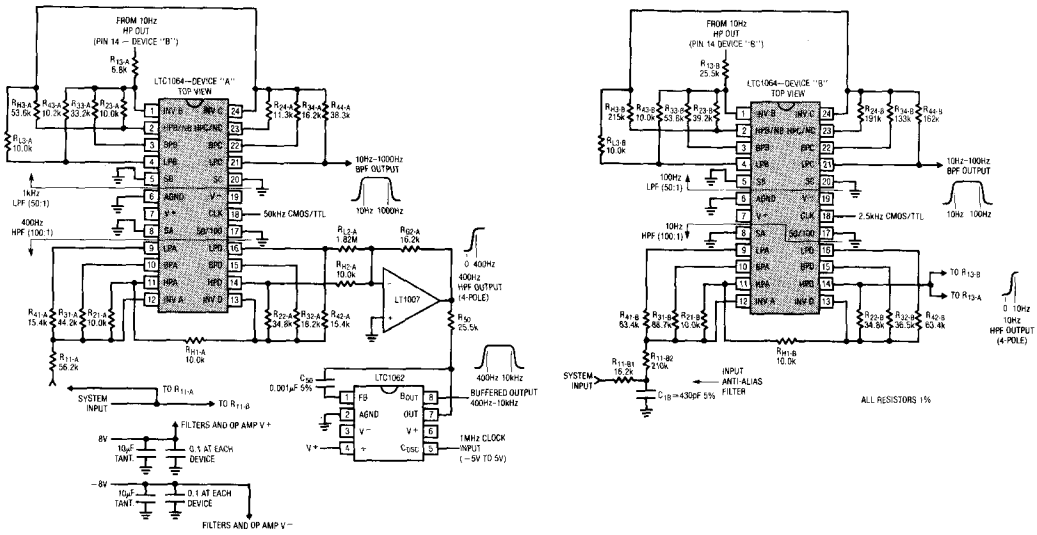


Figure 2. Schematic Diagram

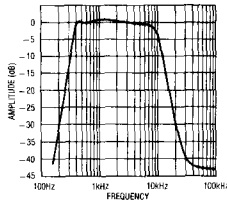


Figure 3. 400Hz-10kHz BP Filter Amplitude Response

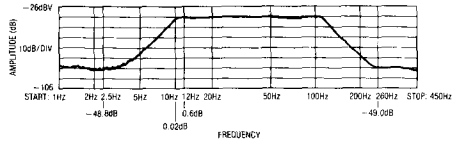


Figure 4. 10Hz-100kHz BPF Amplitude Response

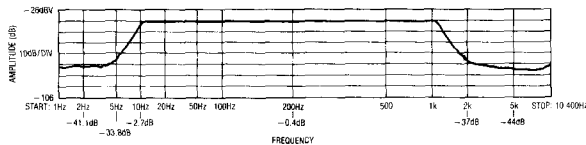
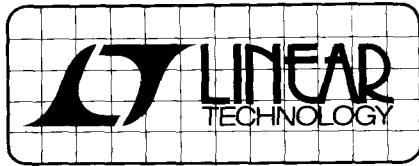


Figure 5. 10Hz-1000Hz BPF Amplitude Response

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DESIGN NOTES

Number 25 in a series from Linear Technology Corporation

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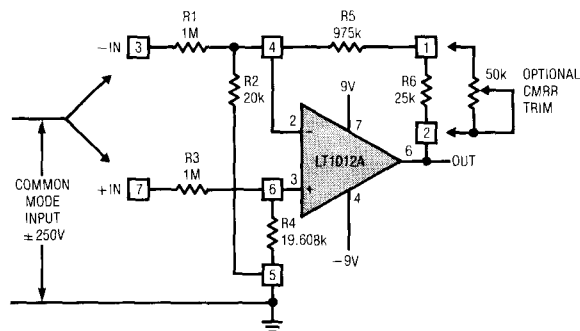
A Single Amplifier, Precision High Voltage Instrument Amp

Walt Jung
George Erdi

Instrumentation amplifier (IA) circuits abound in analog systems, in fact virtually any linear applications handbook will show many useful variations on the concept⁽¹⁾. While this may be somewhat bewildering to a newcomer, all the variations have uses which are differentiated and valuable. A good working knowledge of the alternate forms can be a powerful tool towards designing cost-effective high performance linear circuits.

A case in point is a single amplifier *precision qualified* high voltage IA. This circuit must withstand very high common

mode voltages at the input, yet it should still be relatively simple, while at the same time capable of high performance. Whereas dual summing amplifier setups can provide high input-voltage qualifications, a more simple single amp solution is often sought. An IA topology which achieves all the above objectives is shown in Figure 1, the "Precision High Voltage IA." The circuit employs the virtues of two key parts in performing its function; the resistor array and the op amp used with it.



TYPICAL PERFORMANCE:
COMMON MODE REJECTION RATIO = 74dB (RESISTOR LIMITED)
WITH OPTIONAL TRIM = 130dB
OUTPUT OFFSET (TRIMMABLE TO ZERO) = 500 μ V
OUTPUT OFFSET DRIFT = 10 μ V/ $^{\circ}$ C
INPUT RESISTANCE = 1M (CM)
2M (DIFF)
BANDWIDTH = 13kHz
BATTERY CURRENT = 370 μ A

R1-R6: VISHAY 444 ACCUTRACT THIN-FILM
SIP NETWORK
X : VISHAY 444 PIN NUMBERS

VISHAY INTERTECHNOLOGY, INC.
63 LINCOLN HIGHWAY
MALVERN, PA 19355

Figure 1. ± 250 V Common Mode Range Instrumentation Amplifier ($A_V = 1$)

Here, the resistor network is a precision high-voltage design thin-film system, comprised of R1 through R6. This array, a Vishay type 444, is a thin-film SIP with a 250V/100mW input rating for R1-R3. This high voltage rating allows direct connection to AC or DC line shunts for current monitoring, level shifting from high voltage DC rails, and other such interfacing feats normally uncommon to low voltage IC circuits. The 444 network has a basic common-mode attenuation of 50 times, thus an op amp with an input voltage range of $\pm 10V$ would allow a theoretical range at input pins 3-7 of $\pm 500V$. So, devices with standard $\pm 15V$ supplies are basically compatible with the network operating parameters. While the network has a CM attenuation of 50 times, the differential signal scaling is nominally unity, with an error of $\pm 0.1\%$. Functionally then, the differential mode input signal between pins 3-7 is referred at the output of this circuit to the local ground (pin 5 of the network), with unity gain scaling.

A second keen application point which is a large determining factor towards the overall success of this type of IA is the relative precision of the op amp A1. Indeed, this amplifier is the second "key ingredient" towards high overall performance. Because the circuit basically amplifies the input offset voltage of A1 by the same factor as the CM attenuation, both the initial offset and the drift of A1 can become limitations, as can the CMRR of the device. Here an LT1012A op amp is used, a device with a $25\mu V$ (max) input offset voltage; the output offset will then be 1.25mV or less, worst case. The overall CMRR of the circuit has two primary sources for errors, the basic ratio match of the network halves, and to a lesser degree, the CMRR of A1. The LT1012A has a minimum CMRR of

114dB, while the network is factory trimmed to a 0.02% match, corresponding to a 74dB CMRR. For 120dB or more CMRR, a 50k trimmer can be substituted for R6.

While A1 is shown operating from $\pm 9V$ battery supplies (a feature possible by virtue of the $370\mu A$ quiescent current) the LT1012 device family can also be used on standard $\pm 15V$ supplies, or on lower voltage supplies down to $\pm 1.2V$ (with reduced CM range, of course). With the 9V supplies shown, input ranges of $\pm 250V$ or more to the circuit will not tax the network.

For single battery applications (i.e. when pin 4 is grounded), the LT1012A should be replaced by a single supply op amp such as the LT1006 or the LT1077. These devices can handle about $-250mV$ of negative common mode voltage, while maintaining accuracy. Therefore, the 250V positive common mode range is unchanged, but the negative common mode range is reduced to $-12V$.

Using an LT1006, bandwidth and battery current are basically unchanged. With the LT1077 micropower op amp, battery current is reduced to $45\mu A$ but at the expense of bandwidth ($= 4.5kHz$). Offset voltage and drift specifications are degraded by approximately a factor of two using the LT1006 or the LT1077 compared to the LT1012A.

References

1. Jung, W.G. *IC Op Amp Cookbook, 3d Ed.*, Ch 7, "Amplifier Techniques," Howard W. Sams, Indianapolis, IN 1986.

For literature on our instrumentation amplifiers and precision op amps call (800) 637-5545. For applications help, call (408) 432-1900, Ext. 456.

Auto-Zeroing A/D Offset Voltage

Guy Hoover
William Rempfer

Introduction

Many A/D converters exhibit low offset errors with large full scale voltages. However, when the full scale voltage is decreased the V_{OS} , expressed in LSBs, increases. An A/D converter with 0.5 LSB of offset with a 5V full scale voltage can have 12.5 LSBs of offset with a 200mV full scale voltage. With the LTC1090 family of data acquisition systems and a few external components it is now possible to reduce the V_{OS} to only 0.25 LSB even with only a 200mV full scale voltage. This allows a user to digitize signals from low voltage transducers without the need for a gain stage.

Circuit Description

The LTC1090 is a 10-bit data acquisition system with an eight channel multiplexer. The channel to be read is software selectable and all channels can be referred to the COM pin. In the circuit of Figure 1, CH0 is used to servo the COM pin giving the user a seven channel, offset corrected data acquisition system.

Figure 2 shows how the processor servos the COM pin to eliminate the A/D offset. CH0 is set to a 0.5 LSB voltage. The COM pin is servoed (by the pulse width modulated signal on

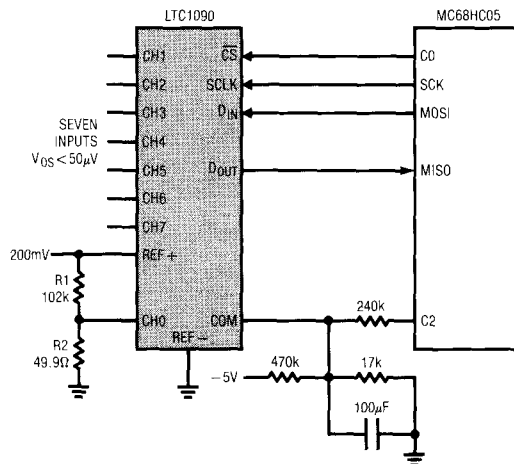


Figure 1. Circuit Provides Seven Channel 10-Bit Data Acquisition System with Less than 50µV of Offset

port C2) so that the CH0 reading dithers between 0 and 1 LSB. The 100 μ F filters the PWM signal at the COM pin. Motorola MC68HC05 code is available from LTC to correct the LTC1090 offset and read the remaining seven channels. This algorithm

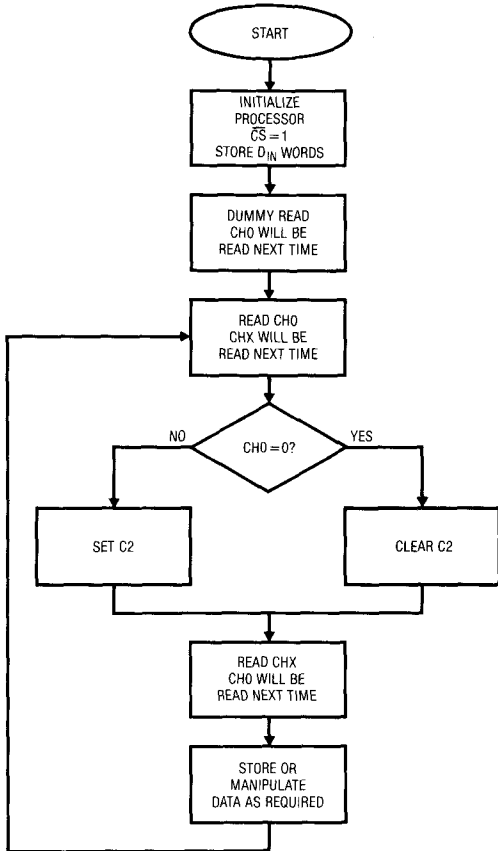


Figure 2. Auto-Zero Flowchart

will work in either unipolar or bipolar mode. (Unipolar is shown. For bipolar the 49.9 Ω resistor is changed to 100 Ω and the decision block is changed to "CH0 \leq 0?")

After initializing the processor, the code sends a D_{IN} word to the LTC1090 requesting CH0 to be read with respect to COM. The next D_{IN} word that is sent will set up the A/D for the desired channel to be read while the CH0 data previously requested is shifted into the processor. If the CH0 D_{OUT} is 0 then C2 is cleared. If the CH0 D_{OUT} is greater than 0 then C2 is set. Another D_{IN} word requesting CH0 data is sent and the D_{OUT} data from the previously requested channel is read into the processor.

As can be seen from the LTC1090 data sheet the linearity and full scale errors with a 200mV full scale voltage are still within 0.5 LSB. To fully take advantage of the reduced offset of the auto-zero circuit the noise of the LTC1090 must be reduced. This can be done by averaging the data with the processor. Figure 3 shows a dynamic cross plot of the output data near half-scale after 64 averages. The top trace is the B9 transition of the LTC1090 while the bottom trace is a binary weighted summation of B0 and B1. The horizontal scale is 1 LSB per major division. The averaged noise is much less than 1 LSB.

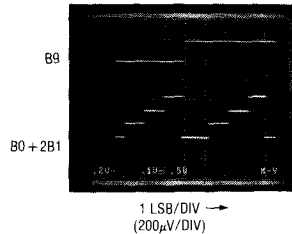
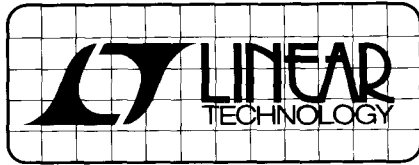


Figure 3. Dynamic Cross Plot Shows Excellent LTC1090 Performance with Only 200mV Full Scale

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DESIGN NOTES

Number 27 in a series from Linear Technology Corporation

October, 1989

Design Considerations for RS-232 Interfaces

Sean Gold

Introduction

When designing an RS-232 interface, it is necessary to conform to standards published by the Electronics Industry Association, EIA RS-232.V28. Some key specifications are summarized in Table 1. However, the EIA specifications are often just the beginning of the design. Practical problems such as generating RS-232 signal levels, providing sufficient load drive, and ensuring protection against fault conditions must also be considered.

Table 1. Key RS-232 Transceiver Specifications (EIA RS232C.V28)

SPECIFICATION	VALUE	UNITS
Signal Levels	± 15 Max; ± 5 Min	V
Cable Length	50 Max	Ft
Load Capacitance	2500 Max	pF
Cable Termination	$3k < R < 7k$	Ω
Data Rate	20k Max	Baud
Slew Rate	$3 < SR < 30$	V/ μ s
Fault Conditions	Drivers Must Tolerate:	
	* Conductor to Conductor Shorts	—
	* Line Open Circuit	—
	* ± 25 V Line Overvoltage	—

Power Supply Generators

Creating the separate RS-232 voltage levels is a common problem in systems which have only a 5V logic supply. Linear Technology has developed a family of transceivers that include an on-chip charge pump to generate the RS-232 supplies. These transceivers are available in a wide variety of configurations incorporating up to 5 drivers and 5 receivers. Some transceivers have a SHUTDOWN control which turns off the charge pump and places the drivers in a "zero" power—high impedance state.

The charge pump consists of a relaxation oscillator, a capacitive voltage doubler, and a capacitive voltage inverter. The oscillator is designed to operate at a frequency well above the signal frequencies to avoid supply degradation as charge is rapidly removed from the storage capacitors.

The LT1180/LT1181's charge pump oscillator operates at approximately 200kHz, which is two times the frequency of the LT1080 and LT1130 series transceivers. The faster oscillator permits the use of low value capacitors ($C > 0.1\mu$ F), and shortens the turn-on time from power off or SHUTDOWN state to less than 200 μ s. The LT1080 and LT1130 start up in approximately 2ms.

Load Driving

It is often desirable to exceed the 20kHz data rate or drive loads greater than 2500pF, e.g. long cables. Slew rate control in the drivers makes this objective possible without compromising the remaining specifications. When lightly loaded, the slew rate is set by an internal bias current and compensation capacitor. When heavily loaded, slew rate is limited by the output stage short circuit current and the load capacitance. The plot in Figure 1 shows the maximum load capacitance for a given data rate.

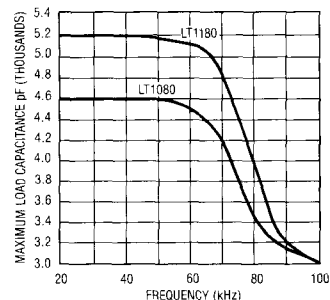


Figure 1. Max Load Capacitance vs Data Rate. Both Transceivers Use 1.0 μ F Storage Capacitors.

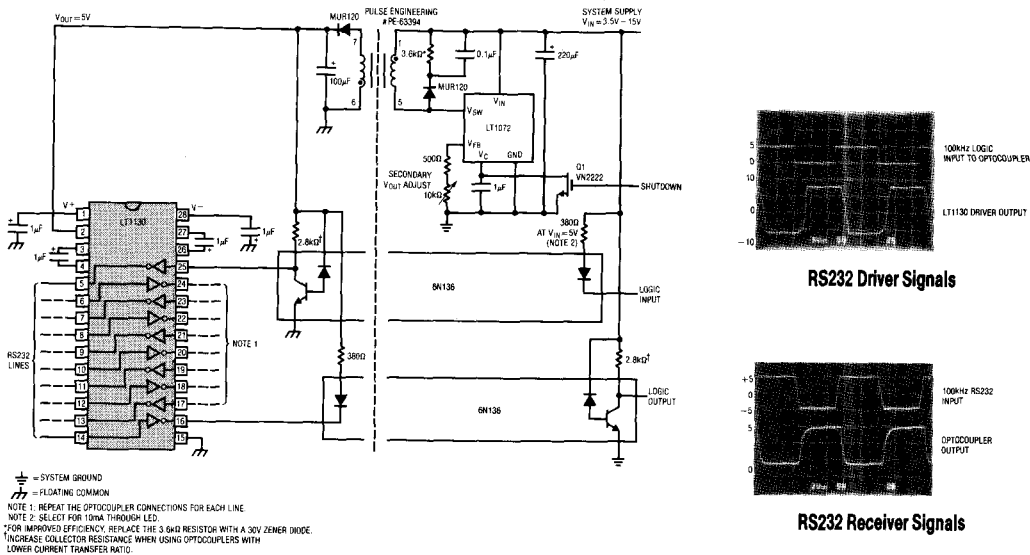


Figure 2. 2500V Isolated 5-Driver/5-Receiver RS232 Transceiver

Fault Conditions

In addition to protecting against all of the fault conditions described in Table 1, LTC transceivers are guaranteed for latchup free operation. When the drivers are turned off or SHUTDOWN, the output stage becomes a high impedance; even when the output is pulled beyond the supply rails. The small current produced by overvoltage is not directed back into the supplies. High impedance on the driver outputs also eliminates signal feedthrough between the logic inputs and the RS-232 lines.

When the device is turned on, overvoltage can, at most, pull the limited short circuit current from the supplies. The receivers are also short circuit current limited to prevent damage to unprotected logic circuitry.

Isolated Transceiver

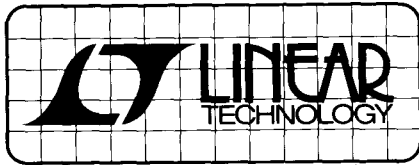
The most frequent cause of failure in interface chips is exposure to extreme fault conditions. Protection against large differences in ground potential, high ground loop currents, or accidental high voltage connections mandates a fully isolated transceiver.

The circuit in Figure 2 provides 2500V isolation with optically coupled data lines and an isolated 5V supply. A powered

transceiver eliminates the need for three supplies on both sides of the isolation transformer. High speed 6N136 optocouplers permit the LT1130 to operate at its full 100kHz bandwidth. However, slower, less expensive optoisolators, such as the 4N28, may be used when the data rate is less than 20k baud. The 5V power supply is generated with an isolated LT1072 switching regulator. The LT1072 has no electrical connection to the load; instead, the circuit derives its feedback from the transformers flyback voltage. This technique is often referred to as an isolated flyback regulator¹. The regulator needs to deliver only modest current levels (200mA max), allowing a physically small isolation transformer. The circuit accepts 3.5V to 15V unregulated inputs which are readily available in most systems. Load regulation is 5% over a 200mA range of output current (50mA-250mA), and efficiency reaches 60% under maximum load conditions. Efficiency may be improved by 10% if the 3.6kΩ snubber resistor is replaced with a 30V Zener diode. Q1 provides shutdown control, which disables the interface to a low power state.

Note 1: Refer to Linear Technology's Application Note 19, pp. 30-34.

For literature on RS-232 products, call (800) 637-5545.
For applications help, call (408) 432-1900, Ext. 453.



DESIGN NOTES

Number 28 in a series from Linear Technology Corporation

November, 1989

A SPICE Op Amp Macromodel for the LT1012

Walt Jung

Introduction

The Boyle, et al.¹, SPICE macromodel for op amps has proven to be quite useful for fast and efficient computer-based IC circuit analysis, used within its limitations. Critics of this type of model point out that it is not optimum for precise transient analysis of amplifiers using complex compensation. On the other hand, the Boyle macromodel may have little match in terms of the computational speed and performance it can achieve, plus how quickly it can be implemented. These virtues are particularly true for lower frequency op amps, or where DC performance parameters are more important.

The Boyle model can be set up to give realistic and quite reasonable working approximations to a variety of IC op amps which use various types of differential transconductance pair front ends. Two fundamental advantages of this model are the relative simplicity and the simulation speed (particularly when a minimum number of junctions are used). Further, the prudent use of the appropriate transistors at the input can simulate real input offset voltage and bias current effects, as well as such IC-unique features as input common-mode clamping², making the overall model much more realistic and akin to real-world ICs. While the original Boyle paper used an NPN bipolar input example (the 741), the topology of the macromodel is also readily adaptable to PNP bipolars as well as JFETs, as design options.

The LT1012

The LT1012 op amp is a popular "universal" high performance internally compensated precision op amp, available in a variety of electrical grades and packages. It uses a

rather unique input stage, comprised of a bias current compensated Super-Beta NPN differential pair. This allows the desirably low drift of an NPN pair to be realized, but with typical bias currents of only 30pA, due to the use of both the Super-Beta process and bias current cancellation. Importantly, the low bias currents are *not* achieved at the expense of poor drift and high voltage noise, as the LT1012 (C grade) accomplishes a $1\mu\text{V}/^\circ\text{C}$ Max. drift, and a $14\text{nV}/\text{Hz}^{1/2}$ Typ. voltage noise.

The LT1012 has recently been broadened in terms of performance grades, with the addition of a premium "LT1012A" grade part, featuring $25\mu\text{V}$ Max. V_{OS} , $0.6\mu\text{V}/^\circ\text{C}$ Max. drift, and $500\mu\text{A}$ Max. supply current. The added "LT1012D" part has a $140\mu\text{V}$ Max. V_{OS} , a $1.7\mu\text{V}/^\circ\text{C}$ Max. drift, and an $800\mu\text{A}$ Max. supply current. All device grades have the unusual combination of performance characteristics which allow use as a low-voltage ($\pm 1.2\text{V}$), low supply current micropower op amp as well as a full $\pm 20\text{V}$ supply range general purpose part. The LT1012 actually exceeds the performance of the industry standard OP-07, doing so at 1/20 the bias/offset currents, and 1/8 of the supply current.

The LT1012 Macromodel

While all of the above may be interesting enough to a designer, how the model imitates the real part is more so. The LT1012 macromodel listed in Figure 1 has a number of features worthy of mention. Note that it is based on the LT1012C room temperature typical specs, taken from the data sheet.

V_{OS} , the input offset voltage of the input pair, is modeled by using two slightly different NPN transistor models, qm1 and qm2. The ratio of their two saturation currents will produce an offset voltage, which is:

$$V_{OS} = KT/q \ln(I_{s1}/I_{s2})$$

With the ratio as shown, this produces the typical $10\mu V$ offset for the LT1012C.

Bias and offset currents are modeled by using a different Bf for the two input pair halves, as:

$$Bf1 = I_{c1}/I_{b1} \text{ and } Bf2 = I_{c2}/I_{b2}$$

The Bf values shown for qm1 and qm2 are those which correspond to $I_b = 30pA$; $I_{OS} = 20pA$. While the gains listed are enormously high (even for Super-Beta transistors) this is not a problem for SPICE, so bias currents in the range of a typical LT1012C are produced.

Other additions to the generic Boyle macromodel are the optional input diode clamps, ddm1 and ddm2, as in the real part (they can be deleted, if not used). The substitution of a current source, I_p , in the place of the R_p of the original model simulates quiescent power supply current. The LT1012, like

many modern day ICs, has a quiescent supply current which is quite constant with supply voltage, thus I_p is more appropriate than a fixed resistor.

The remaining specifications modeled are shown at the head of the listing, consistent with the LT1012C. The model can also be used for the LT1024 (dual LT1012), if the "x" call is added at the end as shown. A sample small signal pulse response waveform of the model is shown in Figure 2, which can be compared to the similar condition scope photo, from the LT1012 data sheet (pg. 7).

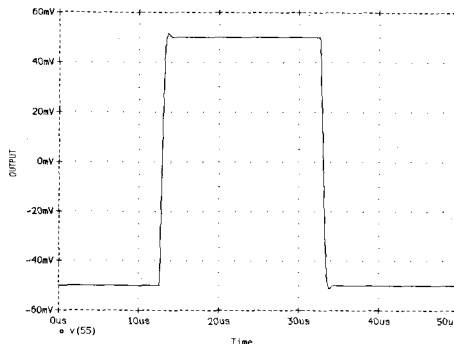


Figure 2. Small Signal Transient Response

References

- Boyle, G.R., Cohn, B.M., Pederson, D.O., Solomon, J.E., "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, Vol. SC-9, #6, December 1974.
- Jung, W.G., "An LT1013 Op Amp Macromodel," Linear Technology Design Note Number 13, July 1988.

Obtaining This Macromodel

This model can be entered onto a given computer type simply by typing it in (very carefully!) using an ASCII text editor. Optionally, interested readers may contact LTC at the address or phone number below, for a copy of a PC data disc containing the most recent collection of macromodels (including this model and all those previously released).

For literature on the LT1012 op amp, or a 5 1/4" macromodel disk, call (800) 637-5545. For applications help, call (408) 432-1900, Ext. 456.

```
*
* Linear Technology LT1012 op amp model (with calls for LT1024)
* Written: 08-17-1989 10:16:25 Type: Bipolar npn input, internal comp.
* Typical specs:
* Vos=1.0E-05, Ib=3.0E-11, Ios=2.0E-11, GBP=6.0E+05Hz, Phase mar.= 70 deg,
* SR(+)=2.0E-01V/us, SR(-)=1.9E-01V/us, Avc= 126 dB, CMRR= 132 dB,
* Vsat(+)= 1 V, Vsat(-)= -1 V, Isc= +/- 12.5 mA, Iqs= 380 uA
* (input differential mode clamp active)
*
* Connections: + - V+V-O
*subckt LT1012 3 2 7 4 6
* input
rc1 7 80 8.842E+03
rc2 7 90 8.842E+03
d1 80 2 10 qm1
d2 90 3 13 qm2
ddm1 2 3 ddm2
ddm2 3 2 ddm1
c1 80 90 5.460E-12
re1 10 12 2.246E+02
re2 11 12 2.246E+02
lee 12 4 6.000E-06
re 12 0 3.333E+07
ce 12 0 1.579E-12
* intermediate
qcm 0 8 12 0 2.841E-11
qa 8 0 80 90 1.131E-04
r2 8 0 1.000E+05
c2 1 8 3.000E-11
gp 1 0 8 0 1.960E+02
* output
rc1 1 6 1.000E+02
rc2 1 0 9.000E+02
rc 17 0 1.063E-04
gc 0 17 6 0 9.408E+03
d1 1 17 dml
d2 17 1 dml
d3 6 13 ddm2
d4 14 6 ddm2
vc 7 13 1.785E+00
ve 14 4 1.785E+00
ip 7 4 3.740E-04
dsub 4 7 dms
* models
.model qm1 npn (is=8.000E-16 bf=7.500E+04)
.model qm2 npn (is=8.003E-16 bf=1.500E+05)
.model dml d (is=1.179E-19)
.model ddm2 d (is=8.000E-16)
.ends LT1012
*
*subckt LT1024 3 2 7 4 6
xLT1024 3 2 7 4 6 LT1012
.ends LT1024
*
* - - - - - fini LT1012 family * - - - - - (*comm vnl 8/89)
```

Figure 1.

A Single Supply RS232 Interface for Bipolar A to D Converters

Sean Gold

Designing circuitry for single supply operation is often an attractive simplification for reducing production costs. Yet many applications call for just a few additional supplies to solve simple interface problems. The example presented here describes how an advanced RS232 interface can simplify an A to D converter which processes bipolar signals.

The LT1180 RS232 transceiver includes a charge pump which produces low ripple supplies with sufficient surplus current to drive a CMOS A to D converter and precision voltage reference. The circuit in Figure 1 operates from a single 5V supply, and draws a total quiescent current of only 37mA. These features make the circuit ideal for applications which must process bipolar signals with minimal support electronics.

The LTC1094 serial A to D converter requires both a low noise supply and reference voltage for accurate operation.¹ These design problems are solved with an LT1021 precision reference, which delivers a stable, low noise, 5V signal from the LT1180's V⁺ output. Relatively large storage and filter capacitors must be used with the LT1180 to reduce the noise in the system below 1mV for a 12 bit system. Construction also re-

quires close attention to the layout of the system grounds and other aspects of circuit board design to avoid noise problems.²

To accommodate bipolar inputs ($-5 < V_{IN} < 5$), the LTC1094's negative rail must be biased beyond the extreme signal swing, but below absolute maximum ratings for the supplies. A 5.6V Zener diode, D1, provides a sufficient bias because the V⁻ pin draws very little current.

The A to D converter communicates with a remote controller via three wires, which carry the clock, the configuration word, and the output data. The chip select signal, CS, is generated from the incoming clock with a peak detector, constructed with a single PNP transistor. R and C are designed to hold the CS pin low for at least one clock period. Assuming the logic

Note 1: Refer to the data sheets for the LTC1094/LTC1294.

Note 2: An excellent reference on the subject of grounding and low noise circuit design is: "An IC Amplifier User's Guide to Decoupling, Grounding, and Making Things Go Right for A Change," by Paul Brokaw, Analog Devices Application Note.

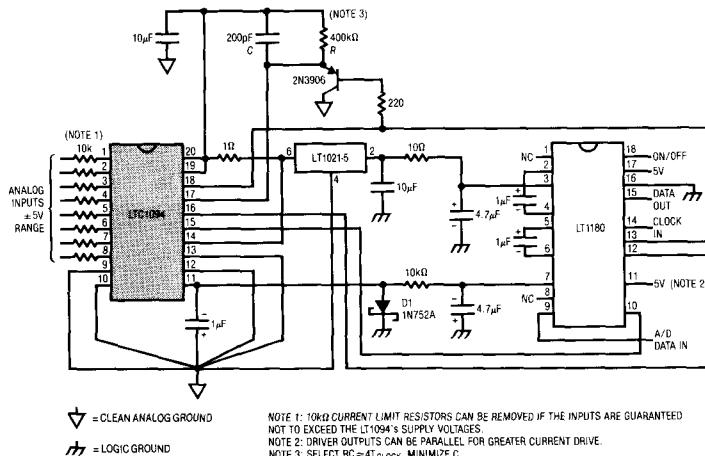


Figure 1. A/D Converter Interface

threshold in the LTC1094 is 1.4V, two useful rules of thumb for selecting R and C are: Design RC to be at least four times the clock period. And select C as small as possible to start the converter quickly. Minor aberrations in the \overline{CS} signal are unimportant because the \overline{CS} pin is level sensitive. The PNP is biased from the clean reference supply so very little noise is coupled into the A to D. Additional buffers are unnecessary because the peak detector drives a CMOS input.

The operating sequence for the LTC1094 is shown in Figure 2. The \overline{CS} signal switches to a low state less than $1\mu\text{s}$ after receiving the system clock, and the configuration word may be transmitted after one clock cycle. After the 18 clock cycles required to complete the conversion, the clock must shut off

to allow \overline{CS} to switch to a high state for at least $2\mu\text{s}$ — the minimum time between conversions. The operating sequence may then be repeated.

A single conversion cycle is shown in Figure 3. The LT1180's maximum data rate limits the clock speed to 100k baud. The input voltage is 3.33V which generates a bit pattern of alternating 1's and 0's. Trace B shows the Chip Select signal, and Trace C shows the gating pulse for the system clock. The complete conversion cycle for a 12-bit converter using an LTC1294 is listed in Figure 4. For this example, the gating signals are adjusted to allow for the two extra bits of data.³

Note 3: The LTC1094 in Figure 1 was directly replaced with an LTC1294, with no changes to the circuit.

MSB First Data (MSBF = 1)

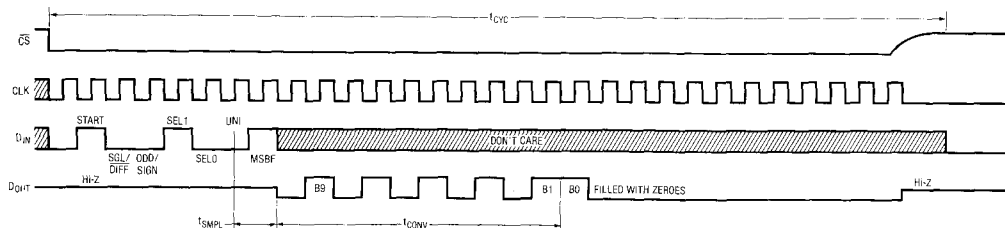


Figure 2. LTC1093/4 Operating Sequence Example: Differential Inputs (CH4+, CH5-), Bipolar Mode

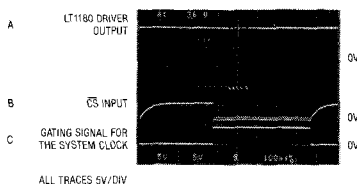


Figure 3. 10 Bit Converter Interface

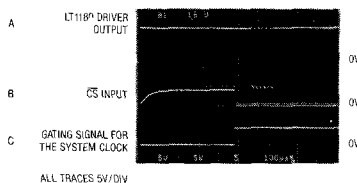
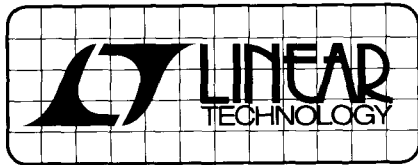


Figure 4. 12 Bit Converter Interface

For literature on RS232 products, call (800) 637-5545.
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DESIGN NOTES

Number 30 in a series from Linear Technology Corporation

January, 1990

RS232 Transceiver with Automatic Power Shutdown Control

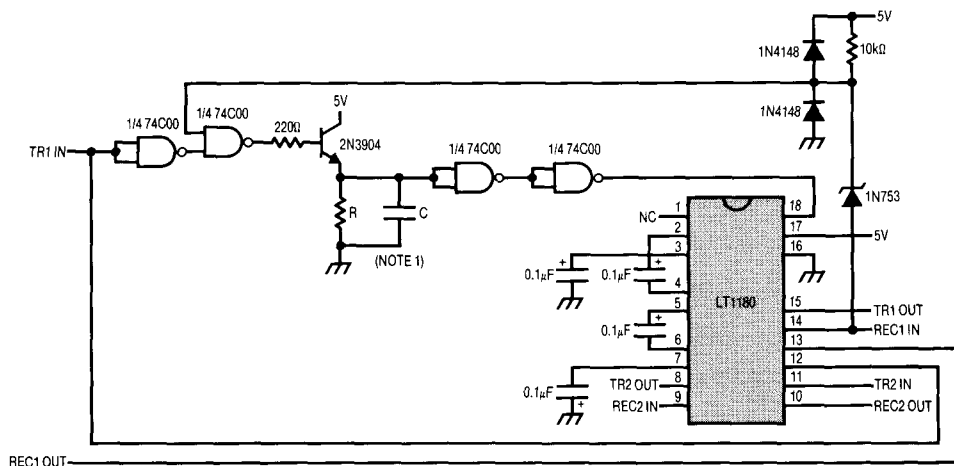
Sean Gold

The LT1180/81 RS232 transceivers with on-chip charge pumps offer some unique features that greatly enhance serial interface performance. Like the LT1080 and LT1130 series transceivers, the LT1180 is fully compliant with all RS232 specifications. The LT1180 is unique since it utilizes a charge pump which oscillates at 150kHz to 200kHz — about twice the frequency of the standard transceivers. In addition to providing excellent current delivery capability, the high speed charge pump can operate with storage capacitors as small as 0.1 μ F.

Reducing storage capacitor size to 0.1 μ F shrinks board space, thereby lowering production costs. Small capacitors also shorten the transceiver turn-on time to less than 200 μ s, which makes the LT1180 ideal for applications which must address the RS232 transceiver quickly. The interface de-

scribed here takes advantage of fast turn-on to reduce power dissipation.

The circuit shown in Figure 1 automatically shuts down when there is no data flow through the interface. A data stream on either the RS232 or logic inputs activates the transceiver. The data must begin with a logic 1 preamble, and the data stream must contain a sufficient number of 1's to keep the transceiver active. The preamble may be as short as 50 μ s. Alternatively, the input to the Automatic SHUTDOWN circuit could be an RS232 handshake signal, such as Data Set Ready (DSR) or Clear to Send (CTS), which remain high during the data transfer. The LT1180's 200 μ s turn-on delay does not limit the data rate in the transceiver. Once the LT1180 is active, it can process data at the maximum 100k baud data rate.



NOTE 1: SELECT RC BASED ON CLOCK SPEED AND REQUIRED DROP OUT TIME.
 $\tau = RC = 2 \cdot T_{\text{PROP OUT}}$. FOR THIS EXAMPLE, $R = 100k\Omega$ AND $C = 1\mu F$.
 C SHOULD NOT EXCEED $1\mu F$ UNLESS THE 2N3904 CURRENT LIMITED WITH A COLLECTOR RESISTOR.

Figure 1. Fast Turn-On Transceiver with Automatic SHUTDOWN Control

A peak detector senses data flow. The extra CMOS gates are buffers which ensure the time constant is relatively independent of input signal level. The drop out time, i.e. the duration of inactivity prior to SHUTDOWN, is approximately 0.5RC. More specifically, drop out occurs when the voltage on the peak detector decays from $V_{CC} - 0.7V$ to the logic switch point of $V_{CC}/2$. The RS232 input to the control circuit is clamped to protect the logic inputs. The zener diode, D3, forces the turn-on threshold on the RS232 side to $-3.5V$, which prevents the transceiver from turning on when the cable is grounded.

Figures 2 through 4 demonstrate the automatic SHUTDOWN control's response to logic and RS232 signals, as well as zero data flow. The minimum pulse width is $50\mu s$ and the drop out time is set to 50ms. The power supply outputs — the lower two traces in Figures 2 and 3 — become active in less than $200\mu s$. When active, the circuit consumes 16mA of quiescent current. In SHUTDOWN state, the Q-current drops to $50\mu A$.

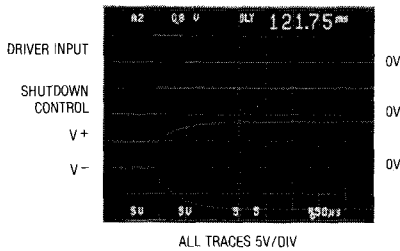


Figure 2. Transceiver Turn-On Via Logic Input

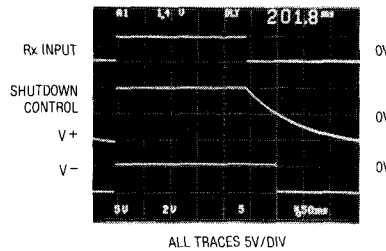


Figure 3. Transceiver Turn-On Via Receiver Input

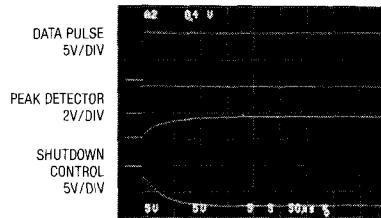


Figure 4. SHUTDOWN After 50ms Without Data Transmission

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Isolated Power Supplies for Local Area Networks

Sean Gold

Introduction

Local Area Networks such as Ethernet™ or Cheapernet™, require low cost isolated power supplies with modest line and load regulation. Table 1 summarizes the objective design specifications based on IEEE 802.3 and ECMA 200-V. The LT1072 high efficiency switching regulator can be used in isolated flyback mode to satisfy these requirements with minimal support circuitry.¹

Table 1. Power Supply Specifications for Figure 1

PARAMETER	VALUE	COMMENTS
V _{OUT}	-9V	Ethernet 11.4V < V _{IN} < 12.6V Cheapernet 4.55V < V _{IN} < 5.45V
Ripple	V _n < 10mVp-p	
I _{LOAD}	150mA	40mA Min, 250mA Max
Load Reg	5%	
Line Reg	5%	
Efficiency	e > 70%	
Isolation	3000V 500V	Ethernet Cheapernet

Circuit Design

Figure 1 illustrates the design approach. In isolated flyback mode, the LT1072 has no electrical connection to the load; instead, the regulator obtains a feedback signal from the transformer's flyback voltage during the switch off-time. The voltage sense occurs after a 1.5μs delay, which prevents the internal error amplifier from regulating the voltage spike due to transformer leakage inductance. The LT1072 compares the feedback signal with a reference voltage, which is set at the feedback pin with a resistor to ground. The primary voltage is regulated to 16V + (V_{FB}/R_{FB})7k. The feedback pin voltage V_{FB}, clamps to about 400mV, and the term (V_{FB}/R_{FB})7k is nominally set to 2V, making the total flyback voltage 18V. The circuit is programmed for -9V output by setting the transformer turns ratio to 2 to 1. The feedback resistor R_{FB}, includes a 500Ω trim to take into account variations in the clamp voltage and gain within the LT1072.

Note 1: LTC's Application Note 19, the LT1070 Design Manual, presents a detailed discussion of isolated flyback mode and general information on switching regulator design.

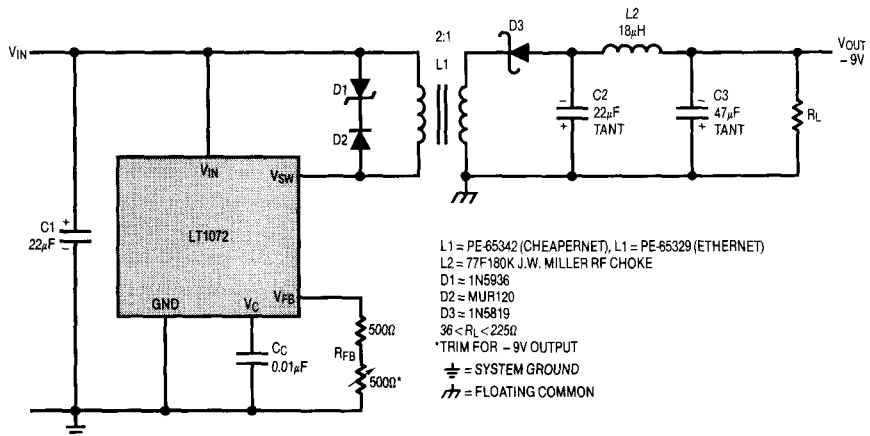


Figure 1. Isolated Switching Regulator for LAN

A snubber network consisting of a fast turn-on, high break-down diode and a 36V Zener diode, limits the magnitude of the leakage inductance spike. This snubber configuration improves efficiency because it minimizes the duration of the inductance spike. A Schottky diode in the secondary reduces the voltage loss to the output and increases efficiency.

Specifications for power supply filters are application dependent. When noise levels of 150mV are tolerable, a single 100µF tantalum capacitor is a suitable supply filter. When output noise below 10mV is required, the use of large output capacitors is often impractical. An LC filter is an appropriate recourse. The optional LC filter in Figure 1 contains an RF choke L2, and tantalum filter capacitors C1 and C2. These components have low effective series resistance (ESR) which helps maintain 5% load regulation.

Figure 2 shows the voltage on the switch pin, trace A, and the current flowing through the inductor, trace B. Trace C is a magnified view of trace A, which more clearly shows regulation of the primary voltage after the switch off-time. Figure 3 shows the voltage and current noise at the output.

Transformer Design

The circuit design for 12V to -9V (Ethernet) and 5V to -9V (Cheapernet) circuits are identical except for the transformer specifications. Both circuits develop a regulated 18V primary voltage, but the available input voltage determines the required primary inductance.

$$L_{PRI} = \frac{V_{IN}}{(\Delta I) (f) (1 + V_{IN}/V_{PRI})}$$

$$= \frac{5V}{(0.3A) (40kHz) (1 + 5/18)}$$

$$= 326\mu H \text{ (Minimum)}$$

Where,

- ΔI = Magnetizing Current
- f = Switching Frequency
- V_{IN} = Input Voltage
- V_{PRI} = Primary Voltage

Ethernet requires a larger primary inductance than Cheapernet, which implies a larger transformer. Increased isolation also mandates a larger core to accommodate additional

insulation. The transformers used in both applications are shown in Figure 4. The PE-65329 for Ethernet (right) achieves 3700V isolation, while the PE-65342 for Cheapernet (left) provides 500V isolation.² These transformers are constructed with low loss core material and low resistance wire, to further improve efficiency.

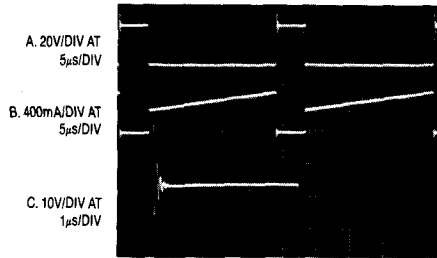


Figure 2. Switching Waveforms

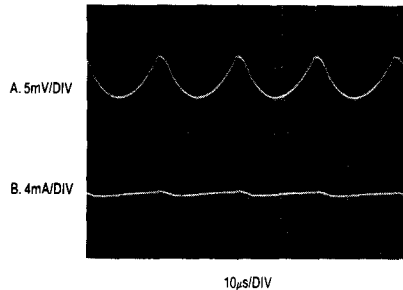


Figure 3. Voltage and Current Noise

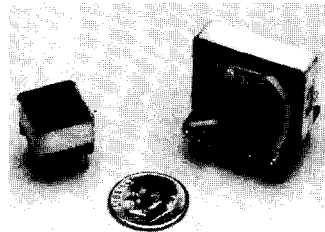


Figure 4. LAN Transformers. PE-65342 (Left), PE-65329 (Right)

For additional literature on switching regulators, call (800) 637-5545. For applications help, call (408) 432-1900, Ext. 445.

Note 2: A 500V version of the Ethernet transformer (PE-65330) is available in the 0.5 inch package in Figure 4.

A Simple Ultra-Low Dropout Regulator

Jim Williams

Linear voltage regulators with low dropout characteristics are a frequent requirement, particularly in battery powered applications. It is desirable to maintain regulation until the battery is almost entirely depleted. Regulator dropout limits significantly impact useful battery life, and as such should be minimized. Figure 1 shows dropout characteristics for a monolithic regulator, the LT1085. The <math><1.5V</math> dropout performance is about twice as good as standard monolithic regulators. In many cases this device will serve nicely, but applications requiring lower dropout mandate a different approach.

Figure 2's simple regulator has only 85mV dropout at 2.5A — a 13x improvement. At lower currents dropout decreases to vanishingly small values. This circuit is particularly applicable in battery driven lap top computers, where multi-output

power supplies are used. In operation, the LT1431 shunt regulator adjusts its output ("collector") to whatever value is required to force circuit output to 5V. The LT1431's internal trimming eliminates the usual feedback resistors and trim-pots. Q1, the pass element, runs as a voltage overdriven source follower. This configuration offers the lowest possible dropout voltage,* although it does require a +12V bias source for Q1's gate. This +12V source is commonly present in lap top computers and similar devices because of disc drive and peripheral power requirements. Power drain on the +12V supply is a few milliamperes.

*A detailed discussion of various methods for achieving low dropout appears as Appendix A ("Achieving Low Dropout") in LTC Application Note 32, "High Efficiency Linear Regulators."

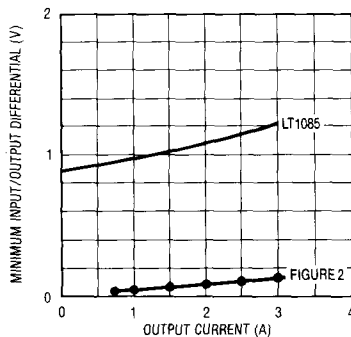
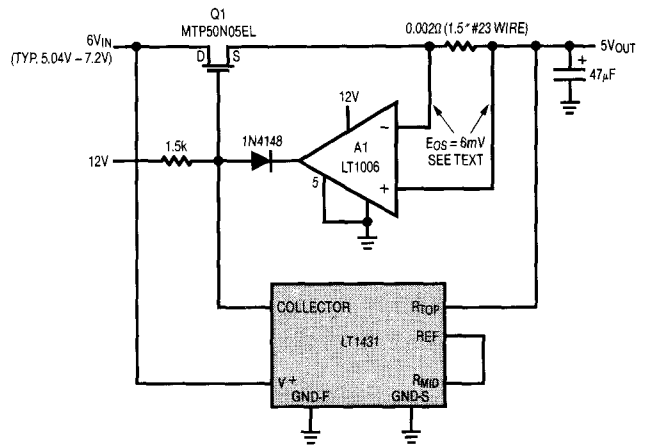


Figure 1. Dropout Performance for a Low Dropout Monolithic Regulator vs Figure 2



CONNECT ALL ± LABELED RETURNS TO A SINGLE POINT AT THE 6VIN SOURCE

Figure 2. Ultra-Low Dropout Regulator

Providing short circuit protection without introducing significant loss requires care. A1 achieves this by sensing across a 0.002Ω shunt (1.5" of #23 wire). This introduces only 6mV of drop at the circuits 3A current limit threshold. A 6mV current limit trip point is derived by grounding A1's offset pin 5. The 6mV input offset generated at A1 by doing this is stable over time, temperature and unit-unit variation, and substitutions for A1 are not advisable. Currents beyond 3A cause A1 to pull low, stealing Q1's gate drive and shutting off the regulators output. Under overload conditions A1 and Q1 form a well controlled linear current control loop with smooth limiting. Figure 3 details dropout characteristics. Results for the MTP50N05EL MOSFET specified for Q1 show only 85mV dropout, decreasing to just 8mV at 0.25A. For comparison, data for some higher resistance transistors also appears.

Q1's source follower connection makes regulator dynamics quite good compared to common source/emitter approaches. Figure 4 shows no load (Trace A low) to full load (Trace A high) response. Regulator output (Trace B) dips only 200mV and recovers quickly with clean damping. The positive slew recovery time is due to the 1.5k Ω bias resistor acting against Q1's

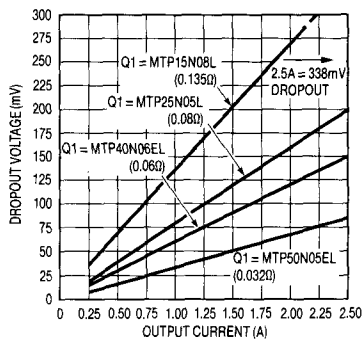


Figure 3. Dropout Characteristics for Figure 2. Q1's Saturation Directly Influences Performance.

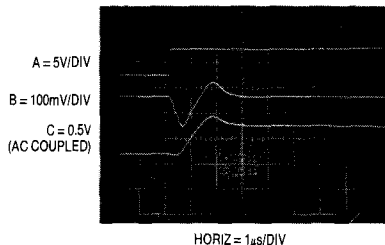


Figure 4. Transient Response for a Full Load Step. Follower Connection Provides Clean Dynamics.

input capacitance (Trace C is Q1's gate). Quicker response is possible by a reduction in this value, although current drain from the +12V supply will increase. The value used represents a good compromise. Transient recovery for load removal is also well controlled.

This regulator offers a simple solution to applications requiring extremely low dropout over a range of output currents. The performance, low parts count and lack of trimming make it an attractive alternative to other approaches. For reference, pertinent information on construction of wire shunts appears in Figures 5 and 6.

WIRE GAUGE	$\mu\Omega$ /INCH
10	83
11	100
12	130
13	160
14	210
15	265
16	335
17	421
18	530
19	670
20	890
21	1000
22	1300
23	1700
24	2100
25	2700

Figure 5. Resistance vs Size for Various Copper Wire Types

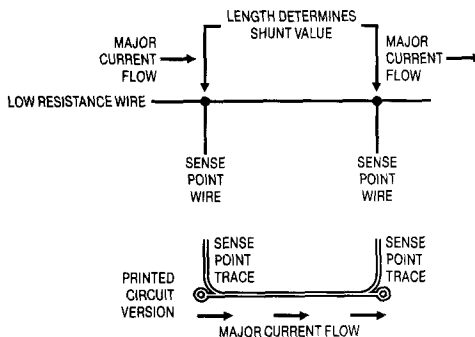


Figure 6. Detail of a Low Resistance Current Shunt

For literature on low dropout regulators, call (800) 637-5545. For applications help, call (408) 432-1900, Ext. 445.

SECTION 3—MACROMODELS

SECTION 3—MACROMODELS

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LM101A Macromodel

```
*
* Linear Technology LM101A op amp model
* Written: 08-23-1989 15:55:44 Type: Bipolar npn input, external comp.
* Typical specs:
* Vos=7.0E-04, Ib=3.0E-08, Ios=1.5E-09, GBP=9.0E+05Hz, Phase mar.= 70 deg,
* SR(+)=5.0E-01V/us, SR(-)=4.8E-01V/us, Av= 104 dB, CMMR= 96 dB,
* Vsat(+)=1.00V, Vsat(-)=1.00V, Isc=+/-30.0mA, Iq= 1800uA
*
* Connections: + - V+V-0 CaCb
.subckt LM101A 3 2 7 4 6 1 8 ; Use C=30 pF in main circuit (Ca to Cb).
* input
rc1 7 80 5.895E+03
rc2 7 90 5.895E+03
q1 80 2 10 qm1
q2 90 3 11 qm2
c1 80 90 5.460E-12
re1 10 12 2.438E+03
re2 11 12 2.438E+03
iee 12 4 1.506E-05
re 12 0 1.328E+07
ce 12 0 1.579E-12
* intermediate
gcm 0 8 12 0 2.689E-09
ga 8 0 80 90 1.696E-04
r2 8 0 1.000E+05
* external comp cap used for c2 (see note above).
gb 1 0 8 0 1.401E+02
* output
ro1 1 6 3.333E+01
ro2 1 0 6.667E+01
rc 17 0 4.758E-05
gc 0 17 6 0 2.102E+04
d1 1 17 dm1
d2 17 1 dm1
d3 6 13 dm2
d4 14 6 dm2
vc 7 13 1.808E+00
ve 14 4 1.808E+00
ip 7 4 1.785E-03
dsub 4 7 dm2
* models
.model qm1 npn (is=8.000E-16 bf=2.439E+02)
.model qm2 npn (is=8.220E-16 bf=2.564E+02)
.model dm1 d (is=3.337E-15)
.model dm2 d (is=8.000E-16)
.ends LM101A
*
* - - - - - * fini LM101A * - - - - - * [oamm vnl 8/89]
```

LM107 Macromodel

```
*
* Linear Technology LM107 op amp model
* Written: 08-23-1989 15:53:34 Type: Bipolar npn input, internal comp.
* Typical specs:
* Vos=7.0E-04, Ib=3.0E-08, Ios=1.5E-09, GBP=9.0E+05Hz, Phase mar.= 70 deg,
* SR(+)=5.0E-01V/us, SR(-)=4.8E-01V/us, Av= 104 dB, CMMR= 96 dB,
* Vsat(+)=1.00V, Vsat(-)=1.00V, Isc=+/-30.0mA, Iq= 1800uA
*
* Connections: + - V+V-0
.subckt LM107 3 2 7 4 6
* input
rc1 7 80 5.895E+03
rc2 7 90 5.895E+03
q1 80 2 10 qm1
q2 90 3 11 qm2
c1 80 90 5.460E-12
re1 10 12 2.438E+03
re2 11 12 2.438E+03
iee 12 4 1.506E-05
re 12 0 1.328E+07
ce 12 0 1.579E-12
* intermediate
gcm 0 8 12 0 2.689E-09
ga 8 0 80 90 1.696E-04
r2 8 0 1.000E+05
c2 1 8 3.000E-11
gb 1 0 8 0 1.401E+02
* output
ro1 1 6 3.333E+01
ro2 1 0 6.667E+01
rc 17 0 4.758E-05
gc 0 17 6 0 2.102E+04
d1 1 17 dm1
d2 17 1 dm1
d3 6 13 dm2
d4 14 6 dm2
vc 7 13 1.808E+00
ve 14 4 1.808E+00
ip 7 4 1.785E-03
dsub 4 7 dm2
* models
.model qm1 npn (is=8.000E-16 bf=2.439E+02)
.model qm2 npn (is=8.220E-16 bf=2.564E+02)
.model dm1 d (is=3.337E-15)
.model dm2 d (is=8.000E-16)
.ends LM107
*
* - - - - * fini LM107 * - - - - * [oamm vnl 8/89]
```

LM108 Macromodel

```

*
* Linear Technology LM108 op amp model (with calls for LH2108)
* Written: 08-23-1989 15:42:36 Type: Bipolar npn input, external comp.
* Typical specs:
* Vos=7.0E-04, Ib=5.0E-10, Ios=5.0E-11, GBP=6.0E+05Hz, Phase mar.= 70 deg,
* SR(+)=2.0E-01V/us, SR(-)=1.9E-01V/us, Av= 110 dB, CMMR= 100 dB,
* Vsat(+)=1.00V, Vsat(-)=1.00V, Isc=+/- 6.0mA, Iq= 300uA
* (input differential mode clamp active)
*
* Connections: + - V+V-0 CaCb
.subckt LM108 3 2 7 4 6 1 8 ; Use C=30 pF in main circuit (Ca to Cb).
* input
rc1 7 80 8.842E+03
rc2 7 90 8.842E+03
q1 80 2 10 qm1
q2 90 3 11 qm2
dcm1 2 3 dm2
ddm2 3 2 dm2
c1 80 90 5.460E-12
re1 10 12 2.246E+02
re2 11 12 2.246E+02
iee 12 4 6.001E-06
re 12 0 3.333E+07
ce 12 0 1.579E-12
* intermediate
gcm 0 8 12 0 1.131E-09
ga 8 0 80 90 1.131E-04
r2 8 0 1.000E+05
* external comp cap used for c2 (see note above).
gb 1 0 8 0 3.146E+01
* output
ro1 1 6 1.111E+02
ro2 1 0 8.889E+02
rc 17 0 3.533E-04
gc 0 17 6 0 2.830E+03
d1 1 17 dm1
d2 17 1 dm1
d3 6 13 dm2
d4 14 6 dm2
vc 7 13 1.766E+00
ve 14 4 1.766E+00
ip 7 4 2.940E-04
dsub 4 7 dm2
* models
.model qm1 npn (is=8.000E-16 bf=5.714E+03)
.model qm2 npn (is=8.220E-16 bf=6.316E+03)
.model dm1 d (is=1.192E-10)
.model dm2 d (is=8.000E-16)
.ends LM108
*
.subckt LH2108 3 2 7 4 6 1 8
x_LH2108 3 2 7 4 6 1 8 LM108
.ends LH2108
*
* - - - - - * fini LM108 family * - - - - - * [oamm vn1 8/89]

```


LM108A Macromodel

```

*
* Linear Technology LM108A op amp model (with calls for LH2108A)
* Written: 08-23-1989 15:40:03 Type: Bipolar npn input, external comp.
* Typical specs:
* Vos=3.0E-04, Ib=5.0E-10, Ios=5.0E-11, GBP=6.0E+05Hz, Phase mar.= 70 deg,
* SR(+)=2.0E-01V/us, SR(-)=1.9E-01V/us, Av= 110 dB, CMMR= 110 dB,
* Vsat(+)=1.00V, Vsat(-)=1.00V, Isc=+/- 6.0mA, Iq= 300uA
* (input differential mode clamp active)
*
* Connections: + - V+V-O CaCb
.subckt LM108A 3 2 7 4 6 1 8 ; Use C=30 pF in main circuit (Ca to Cb).
* input
rc1 7 80 8.842E+03
rc2 7 90 8.842E+03
q1 80 2 10 qm1
q2 90 3 11 qm2
ddm1 2 3 dm2
ddm2 3 2 dm2
c1 80 90 5.460E-12
re1 10 12 2.246E+02
re2 11 12 2.246E+02
iee 12 4 6.001E-06
re 12 0 3.333E+07
ce 12 0 1.579E-12
* intermediate
gcm 0 8 12 0 3.576E-10
ga 8 0 80 90 1.131E-04
r2 8 0 1.000E+05
* external comp cap used for c2 (see note above).
gb 1 0 8 0 3.146E+01
* output
ro1 1 6 1.111E+02
ro2 1 0 8.889E+02
rc 17 0 3.533E-04
gc 0 17 6 0 2.830E+03
d1 1 17 dm1
d2 17 1 dm1
d3 6 13 dm2
d4 14 6 dm2
vc 7 13 1.766E+00
ve 14 4 1.766E+00
ip 7 4 2.940E-04
dsub 4 7 dm2
* models
.model qm1 npn (is=8.000E-16 bf=5.714E+03)
.model qm2 npn (is=8.093E-16 bf=6.316E+03)
.model dm1 d (is=1.192E-10)
.model dm2 d (is=8.000E-16)
.ends LM108A
*
.subckt LH2108A 3 2 7 4 6 1 8
x_LH2108A 3 2 7 4 6 1 8 LM108A
.ends LH2108A
*
* - - - - - * fini LM108A family * - - - - - * [oamm vn1 8/89]

```

LM118 Macromodel

```

*
* Linear Technology LM118 op amp model
* Written: 11-21-1989 Type: Bipolar npn input, internal comp.
* Typical specs:
*   Ref. LM118 data sheet, LTC 1990 databook p2-313
* Comments:
*   Uses extended phase compensation; input differential mode clamp.
*
* Connections: + - V+V-0
.subckt LM118 3 2 7 4 6
* input
rc1 7 80 7.074E+02
rc2 7 90 7.074E+02
q1 80 2 10 qm1
q2 90 3 11 qm1
*
c1 80 91 300e-12
rxcl 91 90 1e3
cxcl 91 90 15e-12
c2 1 8 5.000E-12
*
rb1 2 102 1.0000E+00
rb2 3 103 1.0000E+00
ddm1 102 104 dm2
vz1 104 103 5.5
ddm2 103 105 dm2
vz2 105 102 5.5
re1 10 12 6.209E+02
re2 11 12 6.209E+02
iee 12 4 6.000E-04
re 12 0 3.332E+05
ce 12 0 2.632E-13
*
gcm 0 8 12 0 1.414E-08
ga 8 0 80 90 1.414E-03
r2 8 0 1.000E+05
gb 1 0 8 0 5.318E+01
ro2 1 0 7.4000E+01
*
rs 1 6 1
ec1 18 0 1 6 3.172e+01
gc1 0 8 20 0 1
rc1 20 0 1e3
d1 18 20 dm1
d2 20 18 dm1
d3a 131 70 dm3
d3b 13 131 dm3
gp1 0 8 70 7 1
vc 13 6 3.6473
rpla 7 70 1e4
rplb 7 131 1e5
d4a 60 141 dm3
d4b 141 14 dm3
gn1 0 8 60 4 1
ve 6 14 3.6473
rnla 60 4 1e4
rn1b 141 4 1e5
*
ip 7 4 4.400E-03
dsub 4 7 dm2
* models
.model qm1 npn (is=8.0000E-16
bf=2.4390E+03)
.model qm2 npn (is=8.6435E-16
bf=2.5641E+03)
*
.model dml d (is=1.000e-19)
.model dm2 d (is=8.000E-16)
.model dm3 d (is=1.000e-20)
.ends LM118
*
* - - - - - * fini LM118 * - - - - - *

```

LM308 Macromodel

```

*
* Linear Technology LM308 op amp model
* Written: 08-23-1989 15:46:51 Type: Bipolar npn input, external comp.
* Typical specs:
* Vos=2.0E-03, Ib=1.5E-09, Ios=2.0E-10, GBP=6.0E+05Hz, Phase mar.= 70 deg,
* SR(+)=2.0E-01V/us, SR(-)=1.9E-01V/us, Av= 110 dB, CMMR= 100 dB,
* Vsat(+)=1.00V, Vsat(-)=1.00V, Isc=+/- 6.0mA, Iq= 300uA
* (input differential mode clamp active)
*
* Connections: + - V+V-0 CaCb
.subckt LM308 3 2 7 4 6 1 8 ; Use C=30 pF in main circuit (Ca to Cb).
* input
rc1 7 80 8.842E+03
rc2 7 90 8.842E+03
q1 80 2 10 qm1
q2 90 3 11 qm2
ddm1 2 3 dm2
ddm2 3 2 dm2
c1 80 90 5.460E-12
re1 10 12 2.245E+02
re2 11 12 2.245E+02
iee 12 4 6.003E-06
re 12 0 3.332E+07
ce 12 0 1.579E-12
* intermediate
gcm 0 8 12 0 1.131E-09
ga 8 0 80 90 1.131E-04
r2 8 0 1.000E+05
* external comp cap used for c2 (see note above).
gb 1 0 8 0 3.146E+01
* output
ro1 1 6 1.111E+02
ro2 1 0 8.889E+02
rc 17 0 3.533E-04
gc 0 17 6 0 2.830E+03
d1 1 17 dm1
d2 17 1 dm1
d3 6 13 dm2
d4 14 6 dm2
vc 7 13 1.766E+00
ve 14 4 1.766E+00
ip 7 4 2.940E-04
dsub 4 7 dm2
* models
.model qm1 npn (is=8.000E-16 bf=1.875E+03)
.model qm2 npn (is=8.643E-16 bf=2.143E+03)
.model dm1 d (is=1.192E-10)
.model dm2 d (is=8.000E-16)
.ends LM308
*
* - - - - * fini LM308 * - - - - * [oamm vnl 8/89]

```

LM308A Macromodel

```

*
* Linear Technology LM308A op amp model
* Written: 08-23-1989 15:45:03 Type: Bipolar npn input, external comp.
* Typical specs:
* Vos=3.0E-04, Ib=1.5E-09, Ios=2.0E-10, GBP=6.0E+05Hz, Phase mar.= 70 deg,
* SR(+)=2.0E-01V/us, SR(-)=1.9E-01V/us, Av= 110 dB, CMMR= 110 dB,
* Vsat(+)=1.00V, Vsat(-)=1.00V, Isc=+/- 6.0mA, Iq= 300uA
* (input differential mode clamp active)
*
* Connections: + - V+V-0 CaCb
.subckt LM308A 3 2 7 4 6 1 8 ; Use C=30 pF in main circuit (Ca to Cb).
* input
rc1 7 80 8.842E+03
rc2 7 90 8.842E+03
q1 80 2 10 qm1
q2 90 3 11 qm2
ddm1 2 3 dm2
ddm2 3 2 dm2
c1 80 90 5.460E-12
re1 10 12 2.245E+02
re2 11 12 2.245E+02
iee 12 4 6.003E-06
re 12 0 3.332E+07
ce 12 0 1.579E-12
* intermediate
gcm 0 8 12 0 3.576E-10
ga 8 0 80 90 1.131E-04
r2 8 0 1.000E+05
* external comp cap used for c2 (see note above).
gb 1 0 8 0 3.146E+01
* output
ro1 1 6 1.111E+02
ro2 1 0 8.889E+02
rc 17 0 3.533E-04
gc 0 17 6 0 2.830E+03
d1 1 17 dm1
d2 17 1 dm1
d3 6 13 dm2
d4 14 6 dm2
vc 7 13 1.766E+00
ve 14 4 1.766E+00
ip 7 4 2.940E-04
dsub 4 7 dm2
* models
.model qm1 npn (is=8.000E-16 bf=1.875E+03)
.model qm2 npn (is=8.093E-16 bf=2.143E+03)
.model dml d (is=1.192E-10)
.model dm2 d (is=8.000E-16)
.ends LM308A
*
* - - - - - * fini LM308A * - - - - - * [oamm vnl 8/89]

```

LT1001 Macromodel

```

*
* Linear Technology LT1001 op amp model (with calls for LT1002)
* Written: 10-16-1989 15:04:20 Type: Bipolar npn input, internal comp.
* Typical specs:
* Vos=1.80E-05, Ib=7.00E-10, Ios=4.00E-10, GBP=8.0E+05Hz, Phase mar.=60.0deg,
* SR(+)=3.3E-01V/us, SR(-)=3.1E-01V/us, Av=118dB, CMMR=126dB,
* Vsat(+)=1.00V, Vsat(-)=1.00V, Isc=+/-25.0mA, Iq=1600uA
* (input differential mode clamp active)
*
* Connections: + - V+V-0
.subckt LT1001 3 2 7 4 6
* input
rc1 7 80 6.631E+03      .model qm1 npn (is=8.000E-16 bf=5.500E+03)
rc2 7 90 6.631E+03      .model qm2 npn (is=8.006E-16 bf=9.900E+03)
q1 80 102 10 qm1        .model dm1 d (is=2.331E-08)
q2 90 103 11 qm2        .model dm2 d (is=8.000E-16)
rb1 2 102 5.000E+02     .ends LT1001
rb2 3 103 5.000E+02     *
ddm1 102 104 dm2
ddm3 104 103 dm2
ddm2 103 105 dm2
ddm4 105 102 dm2
c1 80 90 8.660E-12      *.subckt LT1002 3 2 7 4 6
re1 10 12 1.409E+03     x_LT1002 3 2 7 4 6 LT1001
re2 11 12 1.409E+03     .ends LT1002
iee 12 4 9.901E-06      *
re 12 0 2.020E+07
ce 12 0 1.579E-12
* intermediate
gcm 0 8 12 0 7.558E-11
ga 8 0 80 90 1.508E-04
r2 8 0 1.000E+05
c2 1 8 3.000E-11
gb 1 0 8 0 1.538E+03
* output
ro1 1 6 2.575E+01
ro2 1 0 3.425E+01
rc 17 0 4.228E-06
gc 0 17 6 0 2.365E+05
d1 1 17 dm1
d2 17 1 dm1
d3 6 13 dm2
d4 14 6 dm2
vc 7 13 1.803E+00
ve 14 4 1.803E+00
ip 7 4 1.590E-03
dsub 4 7 dm2

```

LT1007 Macromodel

```

*
* Linear Technology LT1007 op amp model
* Written: 11-21-1989 Type: Bipolar npn input, internal comp.
* Typical specs:
*   Ref. LT1007 data sheet, LTC 1990 databook p2-57
* Comments:
*   Uses extended phase compensation; input differential mode clamp.
*
* Connections: + - V+V-0
.subckt LT1007 3 2 7 4 6
rc1 7 80 6.6315E+02
rc2 7 90 6.6315E+02
q1 80 2 10 qm1
q2 90 3 11 qm2
*
c1 80 91 200e-12
rxcl 91 90 50
cxc1 91 90 500e-12
c2 8 98 4.000e-12
rxc2 8 98 4.00k
cxc2 1 98 27.000e-12
*
cin 3 2 5e-12
ddm1 2 104 dm2
ddm3 104 3 dm2
ddm2 3 105 dm2
ddm4 105 2 dm2
re1 10 12 -2.6233E+01
re2 11 12 -2.6233E+01
iee 12 4 7.5030E-05
re 12 0 2.666E+06
ce 12 0 1.579E-12
gcm 0 8 12 0 7.558E-10
ga 8 0 80 90 1.5080E-03
r2 8 0 1.000E+05
gb 1 0 8 0 1.9176E+03
ro2 1 0 6.900E+01
*
rs 1 6 1
ec1 18 0 1 6 2.828e+01
gc1 0 8 20 0 1
rc1 20 0 1e3
d1 18 20 dm1
d2 20 18 dm1
*
d3a 131 70 dm3
d3b 13 131 dm3
gpl 0 8 70 7 1
vc 13 6 3.0909
rpla 7 70 1e4
rplb 7 131 1e5
d4a 60 141 dm3
d4b 141 14 dm3
gnl 0 8 60 4 1
ve 6 14 3.0909
rnla 60 4 1e4
rnlb 141 4 1e5
*
ip 7 4 2.625E-03
dsub 4 7 dm2
* models
.model qm1 npn (is=8.0000E-16
bf=1.7857E+03)
.model qm2 npn (is=8.0062E-16
bf=4.1667E+03)
.model dml d (is=1.000e-19)
.model dm2 d (is=8.000E-16)
.model dm3 d (is=1.000e-20)
.ends LT1007
*
* - - - - - * fini LT1007 * - - - - - *

```

LT1008 Macromodel

```

*
* Linear Technology LT1008 op amp model
* Written: 08-18-1989 17:38:46 Type: Bipolar npn input, external comp.
* Typical specs:
* Vos=3.0E-05, Ib=3.0E-11, Ios=3.0E-11, GBP=6.0E+05Hz, Phase mar.= 60 deg,
* SR(+)=2.0E-01V/us, SR(-)=1.9E-01V/us, Av= 126 dB, CMMR= 132 dB,
* Vsat(+)=1.00V, Vsat(-)=1.00V, Isc=+/- 8.0mA, Iq= 380uA
* (input differential mode clamp active)
*
* Connections: + - V+V-0 CaCb
.subckt LT1008 3 2 7 4 6 1 8 ; Use C=30 pF in main circuit (Ca to Cb).
* input
rc1 7 80 8.842E+03
rc2 7 90 8.842E+03
q1 80 2 10 qm1
q2 90 3 11 qm2
ddm1 2 3 dm2
ddm2 3 2 dm2
c1 80 90 8.660E-12
re1 10 12 2.246E+02
re2 11 12 2.246E+02
iee 12 4 6.000E-06
re 12 0 3.333E+07
ce 12 0 1.579E-12
* intermediate
gcm 0 8 12 0 2.841E-11
ga 8 0 80 90 1.131E-04
r2 8 0 1.000E+05
* external comp cap used for c2 (see note above).
gb 1 0 8 0 1.960E+02
* output
ro1 1 6 1.000E+02
ro2 1 0 9.000E+02
rc 17 0 6.802E-05
gc 0 17 6 0 1.470E+04
d1 1 17 dm1
d2 17 1 dm1
d3 6 13 dm2
d4 14 6 dm2
vc 7 13 1.774E+00
ve 14 4 1.774E+00
ip 7 4 3.740E-04
dsub 4 7 dm2
* models
.model qm1 npn (is=8.000E-16 bf=6.667E+04)
.model qm2 npn (is=8.009E-16 bf=2.000E+05)
.model dm1 d (is=4.276E-12)
.model dm2 d (is=8.000E-16)
.ends LT1008
*
* - - - - - * fini LT1008 * - - - - - * [oamm vnl 8/89]

```

LT1012 Macromodel

```

*
* Linear Technology LT1012 op amp model (with calls for LT1024)
* Written: 09-05-1989 16:53:38 Type: Bipolar npn input, internal comp.
* Typical specs:
* Vos=1.0E-05, Ib=3.0E-11, Ios=2.0E-11, GBP=6.0E+05Hz, Phase mar.= 70 deg,
* SR(+)=2.0E-01V/us, SR(-)=1.9E-01V/us, Av= 126 dB, CMMR= 132 dB,
* Vsat(+)=1.00V, Vsat(-)=1.00V, Isc=+/-12.5mA, Iq= 380uA
* (input differential mode clamp active)
*
* Connections: + - V+V-0
.subckt LT1012 3 2 7 4 6
* input
rc1 7 80 8.842E+03      * models
rc2 7 90 8.842E+03      .model qm1 npn (is=8.000E-16 bf=7.500E+04)
q1 80 2 10 qm1          .model qm2 npn (is=8.003E-16 bf=1.500E+05)
q2 90 3 11 qm2          .model dml d (is=1.179E-19)
ddm1 2 3 dm2           .model dm2 d (is=8.000E-16)
ddm2 3 2 dm2           .ends LT1012
c1 80 90 5.460E-12      *
re1 10 12 2.246E+02     .subckt LT1024 3 2 7 4 6
re2 11 12 2.246E+02     x_LT1024 3 2 7 4 6 LT1012
iee 12 4 6.000E-06     .ends LT1024
re 12 0 3.333E+07      *
ce 12 0 1.579E-12      * - - - - * fini LT1012 family * - - - - * [oamm vn01 9/89]
* intermediate
gcm 0 8 12 0 2.841E-11
ga 8 0 80 90 1.131E-04
r2 8 0 1.000E+05
c2 1 8 3.000E-11
gb 1 0 8 0 1.960E+02
* output
ro1 1 6 1.000E+02
ro2 1 0 9.000E+02
rc 17 0 1.063E-04
gc 0 17 6 0 9.408E+03
d1 1 17 dm1
d2 17 1 dm1
d3 6 13 dm2
d4 14 6 dm2
vc 7 13 1.785E+00
ve 14 4 1.785E+00
ip 7 4 3.740E-04
dsub 4 7 dm2

```


LT1013/LT1014 Macromodel

* This more complete macromodel has been adapted from the Parts
 * generated LT1013/LT1014 model. This version features closer
 * fidelity to the real part, with input common-mode clamping, and
 * compensated output clamping. It can be used for large signal
 * and/or single supply applications, where the inputs can
 * potentially be overdriven. Since it uses more active devices,
 * it may run more slowly than will a conventional macromodel.

```
* connections:  non-inverting input
*               | inverting input
*               | | positive power supply
*               | | | negative power supply
*               | | | | output
*               | | | | |
```

```
.subckt LT1013 1 2 3 4 5
```

```
*
*
c1 11 12 8.661E-12
c2 6 7 30.00E-12
dc 8 53 dx
de 54 8 dx
dlp 90 91 dx
dln 92 90 dx
dp 4 3 dx
egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5
fb 7 99 poly(5) vb vc ve vlp vln 0 2.475E9 -2E9 2E9 2E9 -2E9
ga 6 0 11 12 113.1E-6
gcm 0 6 10 99 225.7E-12
iee 3 10 dc 12.03E-6
hlim 90 0 vlim 1K
q1 11 102 13 qx
q2 12 101 14 qx
rb1 2 102 400
rb2 1 101 400
dcm1 105 102 dx
dcm2 105 101 dx
vcmc 105 4 dc 0.4
r2 6 9 100.0E3
rc1 4 11 8.841E3
rc2 4 12 8.841E3
rel 13 10 4.519E3
re2 14 10 4.519E3
ree 10 99 16.63E6
ro1 8 5 80
ro2 7 99 25
ip 3 4 328E-6
vb 9 0 dc 0
vc 3 53 dc 1.610
ve 54 4 dc .61
vlim 7 8 dc 0
vlp 91 0 dc 25
vln 0 92 dc 25
.model dx D(Is=800.0E-18)
.model qx PNP(Is=800.0E-18 Bf=400)
.ends
```

```
*-----
* connections:  non-inverting input
*               | inverting input
*               | | positive power supply
*               | | | negative power supply
*               | | | | output
*               | | | | |
.subckt LT1014 1 2 3 4 5
```

```
*
* x_LT1014 1 2 3 4 5 LT1013
.ends
```

```
*-----
* connections:  non-inverting input
*               | inverting input
*               | | positive power supply
*               | | | negative power supply
*               | | | | output
*               | | | | |
.subckt LT1006 1 2 3 4 5
*
* x_LT1006 1 2 3 4 5 LT1013
.ends
*-----
```

LT1028 Macromodel

```

*
* Linear Technology LT1028 op amp model
* Written: 11-28-1989 Type: Bipolar npn input, internal comp.
* Typical specs:
*   Ref. LT1028 data sheet, LTC 1990 databook p2-161
* Comments:
*   Uses extended phase compensation; input differential mode clamp.
*
* Connections: + - V+V-O
.subckt LT1028 3 2 7 4 6
rcl 7 80 7.0736E+01
rc2 7 90 7.0736E+01
q1 80 2 10 qm1
q2 90 3 11 qm2
*
c1 80 91 750e-12
rxcl 91 90 50
cxc1 91 90 400e-12
c2 1 98 30.000E-12
rxc2 98 8 1k
cxc2 98 8 10.000E-12
*
cin 2 3 15e-12
rin 2 3 2e4
ddm1 2 104 dm2
ddm3 104 3 dm2
ddm2 3 105 dm2
ddm4 105 2 dm2
rel 10 12 -4.4157E+01
re2 11 12 -4.4157E+01
iee 12 4 4.5006E-04
re 12 0 4.4439E+05
ce 12 0 1.5789E-12
gcm 0 8 12 0 7.0854E-09
ga 8 0 80 90 1.4137E-02
r2 8 0 1.0000E+05
gb 1 0 8 0 2.6731E+02
ro2 1 0 7.9000E+01
*
rs 1 6 1
ecl 18 0 1 6 2.7910e+01
gcl 0 8 20 0 1
rcl 20 0 1e3
d1 18 20 dm1
d2 20 18 dm1
*
d3a 131 70 dm3
d3b 13 131 dm3
gpl 0 8 70 7 1
vc 13 6 3.6394
rpla 7 70 1e4
rplb 7 131 1e5
d4a 60 141 dm3
d4b 141 14 dm3
gnl 0 8 60 4 1
ve 6 14 3.6394
rnla 60 4 1e4
rnlb 141 4 1e5
*
ip 7 4 7.450E-03
dsub 4 7 dm2
* models
.model qm1 npn (is=8.0000E-16 bf=5.7692E+03)
.model qm2 npn (is=8.0062E-16 bf=1.0714E+04)
.model dm1 d (is=1.000e-19)
.model dm2 d (is=8.000E-16)
.model dm3 d (is=1.000e-20)
.ends LT1028
*
* - - - - - * fini LT1028 * - - - - - *

```

LT1037 Macromodel

```

*
* Linear Technology LT1037 op amp model
* Written: 11-21-1989 Type: Bipolar npn input, internal comp.
* Typical specs:
*   Ref. LT1037 data sheet, LTC 1990 databook p2-57
* Comments:
*   Uses extended phase compensation; input differential mode clamp.
*
* Connections: + - V+V-0
.subckt LT1037 3 2 7 4 6
rc1 7 80 6.6315E+02
rc2 7 90 6.6315E+02
q1 80 2 10 qm1
q2 90 3 11 qm2
*
c1 80 91 200e-12
rxcl 91 90 200
cxc1 91 90 200e-12
c2 8 98 1.000e-12
rxc2 8 98 10.00k
cxc2 1 98 5.000e-12
*
cin 3 2 5e-12
ddm1 2 104 dm2
ddm3 104 3 dm2
ddm2 3 105 dm2
ddm4 105 2 dm2
re1 10 12 -2.6233E+01
re2 11 12 -2.6233E+01
iee 12 4 7.5030E-05
re 12 0 2.666E+06
ce 12 0 1.579E-12
gcm 0 8 12 0 7.558E-10
ga 8 0 80 90 1.5080E-03
r2 8 0 1.000E+05
gb 1 0 8 0 1.9176E+03
ro2 1 0 6.900E+01
*
rs 1 6 1
ec1 18 0 1 6 2.828e+01
gc1 0 8 20 0 1
rc1 20 0 1e3
dl 18 20 dm1
d2 20 18 dm1
*
d3a 131 70 dm3
d3b 13 131 dm3
gpl 0 8 70 7 1
vc 13 6 3.0909
rpla 7 70 1e4
rplb 7 131 1e5
d4a 60 141 dm3
d4b 141 14 dm3
gn1 0 8 60 4 1
ve 6 14 3.0909
rnla 60 4 1e4
rn1b 141 4 1e5
*
ip 7 4 2.625E-03
dsub 4 7 dm2
* models
.model qm1 npn (is=8.0000E-16 bf=1.7857E+03)
.model qm2 npn (is=8.0062E-16 bf=4.1667E+03)
.model dm1 d (is=1.000e-19)
.model dm2 d (is=8.000E-16)
.model dm3 d (is=1.000e-20)
.ends LT1037
*
* - - - - * fini LT1037 * - - - - *

```

LT1055 Macromodel

```

*
* Linear Technology LT1055 op amp model
* Written: 11-30-1989 Type: PFET input, internal comp.
* Typical specs:
*   Ref. LT1055 data sheet, LTC 1990 databook p2-219
* Comments:
*   Uses input common-mode clamp (comment out if not desired).
*
* Connections: + - V+V-0
.subckt LT1055 3 2 7 4 6
*
rd1 4 80 9.474E+02      d3a 131 70 dm3
rd2 4 90 9.474E+02      d3b 13 131 dm3
j1 80 102 10 jm1        gpl 0 8 70 7 1
j2 90 103 11 jm2        vc 13 6 2.9515
rg1 2 102 2.000E+00     rpla 7 70 1e4
rg2 3 103 2.000E+00     rplb 7 131 1e5
** cm clamp
dcm1 107 103 dm4        d4a 60 141 dm3
dcm2 105 107 dm4        d4b 141 14 dm3
vcmc 105 4 4.1e0        gnl 0 8 60 4 1
ecmp 106 4 103 4 1      ve 6 14 2.9515
rcmp 107 106 1e4        rnla 60 4 1e4
dcm3 109 102 dm4        rnlb 141 4 1e5
dcm4 105 109 dm4        *
ecmn 108 4 102 4 1      ip 7 4 2.38e-3
rcmn 109 108 1e4        dsub 4 7 dm2
**
c1 80 90 1.5e-11        * models
rs1 10 12 1e0           .model jm1 pjf (is=10e-12 beta=1.5e-3 vto=-1.0000e+00)
rs2 11 12 1e0           .model jm2 pjf (is=5e-12 beta=1.5e-3 vto=-9.9988e-01)
iss 7 12 4.200E-04      .model dml d (is=1.000e-15)
rs 12 0 4.762E+05       .model dm2 d (is=8.000E-16)
cs 12 0 1.579E-12       .model dm3 d (is=1.000e-16)
*                         .model dm4 d (is=1.000e-09)
gcm 0 8 12 0 1.329E-08  .ends LT1055
ga 8 0 80 90 1.056E-03  *
r2 8 0 1.000E+05        * - - - - * fini LT1055 * - - - - *
c2 1 8 3.6e-11
gb 1 0 8 0 5.097E+01
ro2 1 0 7.400E+01
*
rso 1 6 1.000E+00
ec1 18 0 1 6 1.712e+01
gc1 0 8 20 0 1
rc1 20 0 1e3
dl 18 20 dm1
d2 20 18 dm1

```

LT1056 Macromodel

```

*
* Linear Technology LT1056 op amp model
* Written: 11-30-1989 Type: PFET input, internal comp.
* Typical specs:
*   Ref. LT1056 data sheet, LTC 1990 databook p2-219
* Comments:
*   Uses input common-mode clamp (comment out if not desired).
*
* Connections: + - V+V-0
.subckt LT1056 3 2 7 4 6
*
rd1 4 80 9.474E+02
rd2 4 90 9.474E+02
j1 80 102 10 jm1
j2 90 103 11 jm2
rg1 2 102 2.000E+00
rg2 3 103 2.000E+00
** cm clamp
dcm1 107 103 dm4
dcm2 105 107 dm4
vcmc 105 4 4.1e0
ecmp 106 4 103 4 1
rcmp 107 106 1e4
dcm3 109 102 dm4
dcm4 105 109 dm4
ecmn 108 4 102 4 1
rcmn 109 108 1e4
**
c1 80 90 1.5e-11
rs1 10 12 1e0
rs2 11 12 1e0
iss 7 12 4.200E-04
rs 12 0 4.762E+05
cs 12 0 1.579E-12
*
gcm 0 8 12 0 1.329E-08
ga 8 0 80 90 1.056E-03
r2 8 0 1.000E+05
c2 1 8 3.000E-11
gb 1 0 8 0 5.097E+01
ro2 1 0 7.400E+01
*
rso 1 6 1.000E+00
ec1 18 0 1 6 1.712e+01
gcl 0 8 20 0 1
rc1 20 0 1e3
d1 18 20 dm1
d2 20 18 dm1
*
d3a 131 70 dm3
d3b 13 131 dm3
gpl 0 8 70 7 1
vc 13 6 2.9515
rpla 7 70 1e4
rplb 7 131 1e5
d4a 60 141 dm3
d4b 141 14 dm3
gnl 0 8 60 4 1
ve 6 14 2.9515
rnla 60 4 1e4
rnlb 141 4 1e5
*
ip 7 4 4.080E-03
dsub 4 7 dm2
* models
.model jm1 pjf (is=10e-12 beta=1.5e-3 vto=-1.0000e+00)
.model jm2 pjf (is=5e-12 beta=1.5e-3 vto=-9.9986e-01)
.model dm1 d (is=1.000e-15)
.model dm2 d (is=8.000E-16)
.model dm3 d (is=1.000e-16)
.model dm4 d (is=1.000e-09)
.ends LT1056
*
* - - - - * fini LT1056 * - - - - *

```

LT1057 Macromodel

```

*
* Linear Technology LT1057 op amp model
* Written: 11-30-1989 Type: PFET input, internal comp.
* Typical specs:
*   Ref. LT1057 data sheet, LTC 1990 databook p2-235
* Comments:
*   Uses input common-mode clamp (comment out if not desired).
*
* Connections: + - V+V-0
.subckt LT1057 3 2 7 4 6
*
rd1 4 80 9.474E+02      rso 1 6 1.000E+00
rd2 4 90 9.474E+02      ecl 18 0 1 6 2.569e+01
j1 80 102 10 jm1        gcl 0 8 20 0 1
j2 90 103 11 jm2        rcl 20 0 1e3
rg1 2 102 2.000E+00     d1 18 20 dm1
rg2 3 103 2.000E+00     d2 20 18 dm1
** cm clamp
dcm1 107 103 dm4        d3a 131 70 dm3
dcm2 105 107 dm4        d3b 13 131 dm3
vcmc 105 4 4.1e0        gpl 0 8 70 7 1
ecmp 106 4 103 4 1     vc 13 6 3.1515
rcmp 107 106 1e4        rpla 7 70 1e4
dcm3 109 102 dm4        rplb 7 131 1e5
dcm4 105 109 dm4        d4a 60 141 dm3
ecmn 108 4 102 4 1     d4b 141 14 dm3
rcmn 109 108 1e4        gnl 0 8 60 4 1
**                       ve 6 14 3.1515
c1 80 90 1.5e-11        rnla 60 4 1e4
rs1 10 12 1e0           rnlb 141 4 1e5
rs2 11 12 1e0           *
iss 7 12 4.200E-04      ip 7 4 1.28e-3
rs 12 0 4.762E+05       dsub 4 7 dm2
cs 12 0 1.579E-12       * models
*                       .model jm1 pjf (is=10e-12 beta=1.5e-3 vto=-1.0000e+00)
gcm 0 8 12 0 1.329E-08  .model jm2 pjf (is=5e-12 beta=1.5e-3 vto=-9.9978e-01)
ga 8 0 80 90 1.056E-03  .model dm1 d (is=1.000e-15)
r2 8 0 1.000E+05        .model dm2 d (is=8.000E-16)
c2 1 8 3.3e-11          .model dm3 d (is=1.000e-16)
gb 1 0 8 0 5.097E+01    .model dm4 d (is=1.000e-09)
ro2 1 0 7.400E+01      .ends LT1057
*
.subckt LT1058 3 2 7 4 6
x_LT1058 3 2 7 4 6 LT1057
.ends LT1058
*
* - - - - - * fini LT1057 family * - - - - - *

```

LT1078 Macromodel

```

*
* Linear Technology LT1078 op amp model (with calls for LT1079, LT1077)
* Written: 10-17-1989 10:20:02 Type: Bipolar pnp input, internal comp.
* Typical specs:
* Vos=4.0E-05, Ib=6.0E-09, Ios=5.0E-11, GBP=2.0E+05Hz, Phase mar.= 60 deg,
* SR(-)=8.0E-02V/us, SR(+)=7.6E-02V/us, Av= 120 dB, CMMR= 108 dB,
* Vsat(+)=1.00V, Vsat(-)=0.00V, Isc=+/-15.0mA, Iq=45uA.
* (input common mode clamp active)
* (3 for 1!)
*
* Connections: + - V+V-0
.subckt LT1078 3 2 7 4 6
* input
rc1 4 80 2.653E+04      .model qm1 pnp (is=8.000E-16 bf=1.992E+02)
rc2 4 90 2.653E+04      .model qm2 pnp (is=8.012E-16 bf=2.008E+02)
q1 80 102 10 qm1        .model dm1 d (is=2.119E-24)
q2 90 103 11 qm2        .model dm2 d (is=8.000E-16)
rb1 2 102 6.000E+02     .ends LT1078
rb2 3 103 6.000E+02     *
dcm1 105 102 dm2       .subckt LT1079 3 2 7 4 6
dcm2 105 103 dm2       x_LT1079 3 2 7 4 6 LT1078
vcmc 105 4 4.000E-01   .ends LT1079
c1 80 90 8.660E-12      *
re1 10 12 4.958E+03     .subckt LT1077 3 2 7 4 6
re2 11 12 4.958E+03     x_LT1077 3 2 7 4 6 LT1078
iee 7 12 2.412E-06      .ends LT1077
re 12 0 8.292E+07      *
ce 12 0 1.579E-12       * - - - - - * fini LT1078 family * - - - - - * [oamm vp01 10/89]
* intermediate
gcm 0 8 12 0 1.501E-10
ga 8 0 80 90 3.770E-05
r2 8 0 1.000E+05
c2 1 8 3.000E-11
gb 1 0 8 0 1.396E+02
* output
ro1 1 110 1.000E+02
ro2a 1 0 1.083E+03
ro2b 6 110 8.170E+02
ec 17 0 110 0 1
d1 1 17 dm1
d2 17 1 dm1
d3 110 13 dm2
d4 14 110 dm2
d5 6 110 dm2
d6 110 6 dm2
vc 7 13 1.790E+00
ve 14 4 7.901E-01
ip 7 4 4.259E-05
dsub 4 7 dm2

```

LT1097 Macromodel

```

*
* Linear Technology LT1097 op amp model
* Written: 12-05-1989 Type: Bipolar npn input, internal comp.
* Typical specs:
* Vos=1.0E-05, Ib=5.0e-11, Ios=2.0E-11, GBP=6.0E+05Hz, Phase mar.= 70 deg,
* SR(+)=2.0E-01V/us, SR(-)=1.9E-01V/us, Av= 126 dB, CMMR= 132 dB,
* Vsat(+)=1.00V, Vsat(-)=1.00V, Isc=+/-12.5mA, Iq= 380uA
* (input differential mode clamp active)
*
* Connections: + - V+V-0
.subckt LT1097 3 2 7 4 6
* input
rc1 7 80 8.842E+03
rc2 7 90 8.842E+03
q1 80 2 10 qm1
q2 90 3 11 qm2
ddm1 2 3 dm2
ddm2 3 2 dm2
c1 80 90 5.460E-12
re1 10 12 2.246E+02
re2 11 12 2.246E+02
iee 12 4 6.000E-06
re 12 0 3.333E+07
ce 12 0 1.579E-12
* intermediate
gcm 0 8 12 0 2.841E-11
ga 8 0 80 90 1.131E-04
r2 8 0 1.000E+05
c2 1 8 3.000E-11
gb 1 0 8 0 1.960E+02
* output
ro1 1 6 1.000E+02
ro2 1 0 9.000E+02
rc 17 0 1.063E-04
gc 0 17 6 0 9.408E+03
d1 1 17 dm1
d2 17 1 dm1
d3 6 13 dm2
d4 14 6 dm2
vc 7 13 1.785E+00
ve 14 4 1.785E+00
ip 7 4 3.740E-04
dsub 4 7 dm2
* models
.model qm1 npn (is=8.000E-16 bf=5.000e+04)
.model qm2 npn (is=8.003E-16 bf=7.500e+05)
.model dm1 d (is=1.179E-19)
.model dm2 d (is=8.000E-16)
.ends LT1097
*
* - - - - * fini LT1097 * - - - - *

```


LT1101 Macromodel

```
*
* Linear Technology LT1101 instrumentation amplifier model
* Written: 10-23-89 Type: Bipolar pnp input, single supply.
* Typical specs:
* Ref. LT1101 data sheet, LTC 1990 databook p13-36
*
* Comments: Uses nested LT1078 model. Edit path of ".lib" below, or
*           use ".inc" function to call LT1078 model.
*
* Connections: Gnd G10a(-) V- V+ (+) G10b Out
.subckt LT1101 1 2 3 4 5 6 7 8
*
r90a 1 2 828e3
r9a 2 100 82.8e3
ra 100 101 9.2e3
rb 101 102 9.2e3
r9b 102 7 82.8e3
r90b 7 8 828e3
*
xa 3 100 5 4 101 LT1078
xb 6 102 5 4 8 LT1078
*
rina 3 0 7e9
rinb 6 0 7e9
*
.ends LT1101
* /- edit for LT1078 path
.lib LT1078
* - - - - - * fini LT1101 * - - - - - *
```

LT1115 Macromodel

```

*
* Linear Technology LT1115 op amp model
* Written: 11-28-1989 Type: Bipolar npn input, internal comp.
* Typical specs:
*   Ref. LT1115 data sheet, LTC Dec 1989
* Comments:
*   Uses extended phase compensation; input differential mode clamp.
*
* Connections: + - V+V-0
.subckt LT1115 3 2 7 4 6
rcl 7 80 7.0736E+01
rc2 7 90 7.0736E+01
q1 80 2 10 qm1
q2 90 3 11 qm2
*
c1 80 91 750e-12
rxcl 91 90 50
cxc1 91 90 400e-12
c2 1 98 30.000E-12
rxc2 98 8 1k
cxc2 98 8 10.000E-12
*
cin 2 3 15e-12
rin 2 3 2e4
ddm1 2 104 dm2
ddm3 104 3 dm2
ddm2 3 105 dm2
ddm4 105 2 dm2
rel 10 12 -4.4157E+01
re2 11 12 -4.4157E+01
iee 12 4 4.5006E-04
re 12 0 4.4439E+05
ce 12 0 1.5789E-12
gcm 0 8 12 0 7.0854E-09
ga 8 0 80 90 1.4137E-02
r2 8 0 1.0000E+05
gb 1 0 8 0 2.6731E+02
ro2 1 0 7.9000E+01
*
rs 1 6 1
ecl 18 0 1 6 2.7910e+01
gcl 0 8 20 0 1
rcl 20 0 1e3
d1 18 20 dm1
d2 20 18 dm1
*
d3a 131 70 dm3
d3b 13 131 dm3
gpl 0 8 70 7 1
vc 13 6 3.6394
rpla 7 70 1e4
rplb 7 131 1e5
d4a 60 141 dm3
d4b 141 14 dm3
gnl 0 8 60 4 1
ve 6 14 3.6394
rnla 60 4 1e4
rnlb 141 4 1e5
*
ip 7 4 7.450E-03
dsub 4 7 dm2
* models
.model qm1 npn (is=8.0000e-16 bf=3.4615e+03)
.model qm2 npn (is=8.0155e-16 bf=6.4286e+03)
.model dm1 d (is=1.000e-19)
.model dm2 d (is=8.000E-16)
.model dm3 d (is=1.000e-20)
.ends LT1115
*
* - - - - * fini LT1115 * - - - - *

```

LT1178 Macromodel

```

*
* Linear Technology LT1178 op amp model (with calls for LT1179)
* Written: 11-02-1989 13:20:10 Type: Bipolar pnp input, internal comp.
* Typical specs:
* Vos=4.0E-05, Ib=3.0E-09, Ios=5.0E-11, GBP=6.0E+04Hz, Phase mar.= 60 deg,
* SR(-)=2.5E-02V/us, SR(+)=2.4E-02V/us, Av= 117 dB, CMMR= 102 dB,
* Vsat(+)=1.00V, Vsat(-)=0.00V, Isc=+/- 5.0mA, Iq=14uA.
* (input common mode clamp active)
* (2 for 1)
*
* Connections: + - V+V-0
.subckt LT1178 3 2 7 4 6
* input
rc1 4 80 8.842E+04
rc2 4 90 8.842E+04
q1 80 102 10 qm1
q2 90 103 11 qm2
rb1 2 102 6.000E+02
rb2 3 103 6.000E+02
dcm1 105 102 dm2
dcm2 105 103 dm2
vcmc 105 4 4.000E-01
c1 80 90 8.660E-12
re1 10 12 1.933E+04
re2 11 12 1.933E+04
iee 7 12 7.560E-07
re 12 0 2.646E+08
ce 12 0 1.579E-12
* intermediate
gcm 0 8 12 0 8.984E-11
ga 8 0 80 90 1.131E-05
r2 8 0 1.000E+05
c2 1 8 3.000E-11
gb 1 0 8 0 1.647E+02
* output
ro1 1 110 2.000E+02
ro2a 1 0 2.166E+03
ro2b 6 110 1.634E+03
ec 17 0 110 0 1
d1 1 17 dm1
d2 17 1 dm1
d3 110 13 dm2
d4 14 110 dm2
d5 6 110 dm2
d6 110 6 dm2
vc 7 13 1.762E+00
ve 14 4 7.617E-01
ip 7 4 1.324E-05
dsub 4 7 dm2
* models
.model qm1 pnp (is=8.000E-16 bf=1.240E+02)
.model qm2 pnp (is=8.012E-16 bf=1.261E+02)
.model dm1 d (is=1.961E-16)
.model dm2 d (is=8.000E-16)
.ends LT1178
*
.subckt LT1179 3 2 7 4 6
x_LT1179 3 2 7 4 6 LT1178
.ends LT1179
*
* - - - - * fini LT1178 family * - - - - * [oamm vp01 10/89]

```

LT118A Macromodel

```

*
* Linear Technology LT118A op amp model
* Written: 11-21-1989 Type: Bipolar npn input, internal comp.
* Typical specs:
*   Ref. LT118A data sheet, LTC 1990 databook p2-313
* Comments:
*   Uses extended phase compensation; input differential mode clamp.
*
* Connections: + - V+V-0
.subckt LT118A 3 2 7 4 6
* input
rc1 7 80 7.074E+02
rc2 7 90 7.074E+02
q1 80 2 10 qm1
q2 90 3 11 qm1
*
c1 80 91 300e-12
rxcl 91 90 1e3
cxcl 91 90 15e-12
c2 1 8 5.000E-12
*
rb1 2 102 1.0000E+00
rb2 3 103 1.0000E+00
ddm1 102 104 dm2
vz1 104 103 5.5
ddm2 103 105 dm2
vz2 105 102 5.5
re1 10 12 6.209E+02
re2 11 12 6.209E+02
iee 12 4 6.000E-04
re 12 0 3.332E+05
ce 12 0 2.632E-13
*
gcm 0 8 12 0 1.414E-08
ga 8 0 80 90 1.414E-03
r2 8 0 1.000E+05
gb 1 0 8 0 5.318E+01
ro2 1 0 7.4000E+01
*
rs 1 6 1
ec1 18 0 1 6 3.172e+01
gc1 0 8 20 0 1
rc1 20 0 1e3
dl 18 20 dm1
d2 20 18 dm1
*
d3a 131 70 dm3
d3b 13 131 dm3
gpl 0 8 70 7 1
vc 13 6 3.6473
rpla 7 70 1e4
rplb 7 131 1e5
d4a 60 141 dm3
d4b 141 14 dm3
gn1 0 8 60 4 1
ve 6 14 3.6473
rnla 60 4 1e4
rn1b 141 4 1e5
*
ip 7 4 4.400E-03
dsub 4 7 dm2
* models
.model qm1 npn (is=8.0000E-16 bf=2.4390E+03)
.model qm2 npn (is=8.1562E-16 bf=2.5641E+03)
*
.model dm1 d (is=1.000e-19)
.model dm2 d (is=8.000E-16)
.model dm3 d (is=1.000e-20)
.ends LT118A
*
* - - - - - * fini LT118A * - - - - - *

```

OP-05 Macromodel

```

*
* Linear Technology OP05 op amp model
* Written: 08-23-1989 15:59:46 Type: Bipolar npn input, internal comp.
* Typical specs:
* Vos=2.0E-04, Ib=1.0E-09, Ios=1.0E-09, GBP=6.0E+05Hz, Phase mar.= 70 deg,
* SR(+)=3.0E-01V/us, SR(-)=2.9E-01V/us, Av= 114 dB, CMMR= 126 dB,
* Vsat(+)=2.00V, Vsat(-)=2.00V, Isc=+/-25.0mA, Iq= 3000uA
* (input differential mode clamp active)
*
* Connections: + - V+V-0
.subckt OP05 3 2 7 4 6
* input
rc1 7 80 8.842E+03
rc2 7 90 8.842E+03
q1 80 102 10 qm1
q2 90 103 11 qm2
rb1 2 102 5.000E+02
rb2 3 103 5.000E+02
ddm1 102 104 dm2
ddm3 104 103 dm2
ddm2 103 105 dm2
ddm4 105 102 dm2
c1 80 90 5.460E-12
re1 10 12 3.097E+03
re2 11 12 3.097E+03
iee 12 4 9.002E-06
re 12 0 2.222E+07
ce 12 0 1.579E-12
* intermediate
gcm 0 8 12 0 5.668E-11
ga 8 0 80 90 1.131E-04
r2 8 0 1.000E+05
c2 1 8 3.000E-11
gb 1 0 8 0 6.647E+02
* output
ro1 1 6 3.333E+01
ro2 1 0 6.667E+01
rc 17 0 1.393E-05
gc 0 17 6 0 7.179E+04
d1 1 17 dm1
d2 17 1 dm1
d3 6 13 dm2
d4 14 6 dm2
vc 7 13 2.803E+00
ve 14 4 2.803E+00
ip 7 4 2.991E-03
dsub 4 7 dm2
* models
.model qm1 npn (is=8.000E-16 bf=3.000E+03)
.model qm2 npn (is=8.062E-16 bf=9.000E+03)
.model dm1 d (is=5.991E-12)
.model dm2 d (is=8.000E-16)
.ends OP05
*
* - - - - - * fini OP05 * - - - - - * [oamm vnl 8/89]

```

OP-07 Macromodel

```

*
* Linear Technology OP07 op amp model
* Written: 08-24-1989 12:35:59 Type: Bipolar npn input, internal comp.
* Typical specs:
* Vos=3.0E-05, Ib=1.0E-09, Ios=4.0E-10, GBP=6.0E+05Hz, Phase mar.= 70 deg,
* SR(+)=2.5E-01V/us, SR(-)=2.4E-01V/us, Av= 114 dB, CMMR= 126 dB,
* Vsat(+)=2.00V, Vsat(-)=2.00V, Isc=+/-25.0mA, Iq=2500uA
* (input differential mode clamp active)
*
* Connections: + - V+V-0
.subckt OP07 3 2 7 4 6
* input
rc1 7 80 8.842E+03
rc2 7 90 8.842E+03
q1 80 102 10 qm1
q2 90 103 11 qm2
rb1 2 102 5.000E+02
rb2 3 103 5.000E+02
ddm1 102 104 dm2
ddm3 104 103 dm2
ddm2 103 105 dm2
ddm4 105 102 dm2
c1 80 90 5.460E-12
re1 10 12 1.948E+03
re2 11 12 1.948E+03
iee 12 4 7.502E-06
re 12 0 2.666E+07
ce 12 0 1.579E-12
* intermediate
gcm 0 8 12 0 5.668E-11
ga 8 0 80 90 1.131E-04
r2 8 0 1.000E+05
c2 1 8 3.000E-11
gb 1 0 8 0 1.294E+03
* output
ro1 1 6 2.575E+01
ro2 1 0 3.425E+01
rc 17 0 6.634E-06
gc 0 17 6 0 1.507E+05
dl 1 17 dm1
d2 17 1 dm1
d3 6 13 dm2
d4 14 6 dm2
vc 7 13 2.803E+00
ve 14 4 2.803E+00
ip 7 4 2.492E-03
dsub 4 7 dm2
* models
.model qm1 npn (is=8.000E-16 bf=3.125E+03)
.model qm2 npn (is=8.009E-16 bf=4.688E+03)
.model dm1 d (is=1.486E-08)
.model dm2 d (is=8.000E-16)
.ends OP07
*
* - - - - - * fini OP07 * - - - - - * [oamm vn1 8/89]

```

OP-27 Macromodel

```

*
* Linear Technology OP27 op amp model (with calls for OP227)
* Written: 11-21-1989 Type: Bipolar npn input, internal comp.
* Typical specs:
*   Ref. OP-27 data sheet, LTC 1990 databook p2-345
* Comments:
*   Uses extended phase compensation; input differential mode clamp.
*
* Connections: + - V+V-0
.subckt OP27 3 2 7 4 6
rc1 7 80 6.6315E+02
rc2 7 90 6.6315E+02
q1 80 2 10 qm1
q2 90 3 11 qm2
*
c1 80 91 200e-12
rxc1 91 90 50
cxc1 91 90 500e-12
c2 8 98 4.000e-12
rxc2 8 98 4.00k
cxc2 1 98 27.000e-12
*
cin 3 2 5e-12
ddm1 2 104 dm2
ddm3 104 3 dm2
ddm2 3 105 dm2
ddm4 105 2 dm2
rel 10 12 -2.6233E+01
re2 11 12 -2.6233E+01
iee 12 4 7.5030E-05
re 12 0 2.666E+06
ce 12 0 1.579E-12
gcm 0 8 12 0 7.558E-10
ga 8 0 80 90 1.5080E-03
r2 8 0 1.000E+05
gb 1 0 8 0 1.9176E+03
ro2 1 0 6.900E+01
*
rs 1 6 1
ec1 18 0 1 6 2.828e+01
gc1 0 8 20 0 1
rc1 20 0 1e3
d1 18 20 dml
d2 20 18 dml
*
d3a 131 70 dm3
d3b 13 131 dm3
gp1 0 8 70 7 1
vc 13 6 3.0909
rpla 7 70 1e4
rplb 7 131 1e5
d4a 60 141 dm3
d4b 141 14 dm3
gn1 0 8 60 4 1
ve 6 14 3.0909
rnla 60 4 1e4
rnlb 141 4 1e5
*
ip 7 4 2.625E-03
dsub 4 7 dm2
* models
.model qm1 npn (is=8.0000E-16 bf=2.0000E+03)
.model qm2 npn (is=8.0093E-16 bf=4.6667E+03)
.model dml d (is=1.000e-19)
.model dm2 d (is=8.000E-16)
.model dm3 d (is=1.000e-20)
.ends OP27
*
.subckt OP227 3 2 7 4 6
x_OP227 3 2 7 4 6 OP27
.ends OP227
*
* - - - - - * fini OP27 family * - - - - - *

```

OP-37 Macromodel

```

*
* Linear Technology OP37 op amp model (with calls for OP237)
* Written: 11-21-1989 Type: Bipolar npn input, internal comp.
* Typical specs:
*   Ref. OP-37 data sheet, LTC 1990 databook p2-345
* Comments:
*   Uses extended phase compensation; input differential mode clamp.
*
* Connections: + - V+V-0
.subckt OP37 3 2 7 4 6
rc1 7 80 6.6315E+02
rc2 7 90 6.6315E+02
q1 80 2 10 qm1
q2 90 3 11 qm2
*
c1 80 91 200e-12
rxcl 91 90 200
cxcl 91 90 200e-12
c2 8 98 1.000e-12
rxcl 8 98 10.00k
cxcl 1 98 5.000e-12
*
cin 3 2 5e-12
ddm1 2 104 dm2
ddm3 104 3 dm2
ddm2 3 105 dm2
ddm4 105 2 dm2
re1 10 12 -2.6233E+01
re2 11 12 -2.6233E+01
iee 12 4 7.5030E-05
re 12 0 2.666E+06
ce 12 0 1.579E-12
gcm 0 8 12 0 7.558E-10
ga 8 0 80 90 1.5080E-03
r2 8 0 1.000E+05
gb 1 0 8 0 1.9176E+03
ro2 1 0 6.900E+01
*
rs 1 6 1
ec1 18 0 1 6 2.828e+01
gc1 0 8 20 0 1
rcl 20 0 1e3
d1 18 20 dm1
d2 20 18 dm1
*
d3a 131 70 dm3
d3b 13 131 dm3
gpl 0 8 70 7 1
vc 13 6 3.0909
rpla 7 70 1e4
rplb 7 131 1e5
d4a 60 141 dm3
d4b 141 14 dm3
gnl 0 8 60 4 1
ve 6 14 3.0909
rnla 60 4 1e4
rnlb 141 4 1e5
*
ip 7 4 2.625E-03
dsub 4 7 dm2
* models
.model qm1 npn (is=8.0000E-16 bf=2.0000E+03)
.model qm2 npn (is=8.0093E-16 bf=4.6667E+03)
.model dm1 d (is=1.000e-19)
.model dm2 d (is=8.000E-16)
.model dm3 d (is=1.000e-20)
.ends OP37
*
.subckt OP237 3 2 7 4 6
x_OP237 3 2 7 4 6 OP37
.ends OP237
*
* - - - - * fini OP37 family * - - - - *

```


OP-97 Macromodel

```

*
* Linear Technology OP97 op amp model
* Written: 12-06-89 Type: Bipolar npn input, internal comp.
* Typical specs:
* Vos=3.0e-05, Ib=3.0E-11, Ios=2.0E-11, GBP=6.0E+05Hz, Phase mar.= 70 deg,
* SR(+)=2.0E-01V/us, SR(-)=1.9E-01V/us, Av= 126 dB, CMMR= 132 dB,
* Vsat(+)=1.00V, Vsat(-)=1.00V, Isc=+/-12.5mA, Iq= 380uA
* (input differential mode clamp active)
*
* Connections: + - V+V-0
.subckt OP97 3 2 7 4 6
* input
rc1 7 80 8.842E+03
rc2 7 90 8.842E+03
q1 80 2 10 qm1
q2 90 3 11 qm2
ddm1 2 3 dm2
ddm2 3 2 dm2
c1 80 90 5.460E-12
re1 10 12 2.246E+02
re2 11 12 2.246E+02
iee 12 4 6.000E-06
re 12 0 3.333E+07
ce 12 0 1.579E-12
* intermediate
gcm 0 8 12 0 2.841E-11
ga 8 0 80 90 1.131E-04
r2 8 0 1.000E+05
c2 1 8 3.000E-11
gb 1 0 8 0 1.960E+02
* output
ro1 1 6 1.000E+02
ro2 1 0 9.000E+02
rc 17 0 1.063E-04
gc 0 17 6 0 9.408E+03
d1 1 17 dm1
d2 17 1 dm1
d3 6 13 dm2
d4 14 6 dm2
vc 7 13 1.785E+00
ve 14 4 1.785E+00
ip 7 4 3.740E-04
dsub 4 7 dm2
* models
.model qm1 npn (is=8.000E-16 bf=7.500E+04)
.model qm2 npn (is=8.008e-16 bf=1.500E+05)
.model dm1 d (is=1.179E-19)
.model dm2 d (is=8.000E-16)
.ends OP97
*
* - - - - * fini OP97 * - - - - *

```

SECTION 4—REFERENCE READING

SECTION 4—REFERENCE READING

Understanding Interference-Type Noise	RR1-1
Shielding and Guarding	RR2-1
Mounting Considerations for Power Semiconductors	RR3-1

solution is inappropriate, it may only make the noise problem worse! Different noise problems require different solutions; adding a capacitor or a shield will not solve every such problem.

TYPES OF SYSTEM NOISE

Noise in any electronic system can originate at a large number of sources, including computers, fans, power supplies, adjacent equipment, test devices; noise sources can even include improperly connected shields and ground wires that were intended to combat noise. Our discussion of noise sources and coupling mechanisms will include the following topics:

- Common-impedance noise
- Capacitively coupled noise
- Magnetically coupled noise
- Power-line transients
- Miscellaneous noise sources

Common-Impedance Noise. As the name implies, common-impedance noise is developed by an impedance that is common to several circuits. Figure 3 shows the basic configuration, which might occur when a pulse output source and an op amp's reference terminal are both connected to a "ground" point having tangible impedance to the power-supply return terminal. The noise current (the noisy return current of Circuit 1) will develop across impedance, Z , a voltage, V_{noise} , which will appear as a noise signal to Circuit 2.

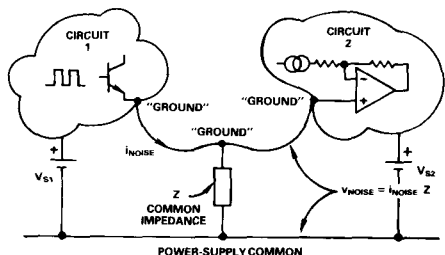


Figure 3. How noise is developed by a common circuit impedance.

Typically, this type of noise has a repetition rate that is set by the rate of the noise source. The actual waveshape is determined by the characteristics of the impedance, Z . For example, if Z is purely resistive, the noise voltage will be proportional to the noise current and of similar shape (Figure 4a). If Z is an R-L-C, the noise voltage will ring at a frequency, $1/(2\pi\sqrt{LC})$ and decay exponentially at a rate set by L/R (b).

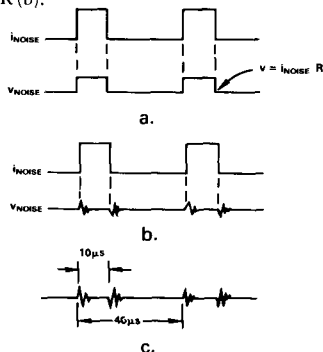


Figure 4. Noise effects in a common impedance. (a) Resistance. (b) An R-L-C circuit. (c) Switching-supply noise response.

If noise of this kind is found in a circuit, its origin may be readily deduced from the repetition rate and waveshape. The *repetition rate* will point to the source of noise, since the noise and its source are synchronized. For example, a noise waveform like that shown in (c), at a 25kHz repetition rate and a 25% duty cycle, might be typical of a switching power supply containing a regulating loop using pulse-width modulation.

The *waveshape* will help identify the impedance that is actually generating the undesired noise. If, for example, the waveform of the noise is the simple damped sinusoid shown in Figure 5, the following features allow us to deduce the nature of Z :

- A constant resistance, R , is in series with the line. The voltage change, V_1 , is the product of R and a current step, I_1 .
- The natural frequency of the oscillation, f_1 , is determined by the series L and shunt C , $f = 1/(2\pi\sqrt{LC})$.
- The damping time constant, τ , is determined by L/R .

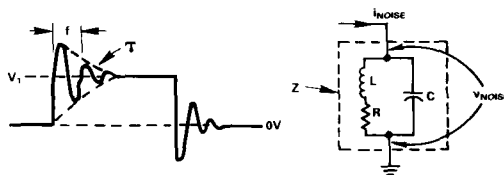


Figure 5. Waveshape for an underdamped R-L-C circuit.

Capacitively Coupled Noise. Noise is also produced by capacitive coupling from a noise source to another circuit. This type of noise is often seen when signals with fast rise-and-fall times or high frequency content are in close proximity to high-impedance circuits. Stray capacitance couples the fast edges of the signal into adjacent circuits, as the circuit model of Figure 6 shows. The nature of the impedance, Z , determines the shape of the response. Typical capacitances are listed in Table 1.

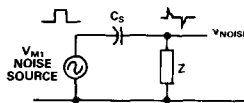


Figure 6. Stray capacitance couples noise into high-impedance circuits.

Table 1. Typical capacitances.¹

Condition	Capacitance
Human standing on an insulator to earth	700 pF
Power input (ac) to output (dc) of ± 15 -V dc supply	100 pF
Two-conductor shielded cable:	
Conductor to conductor	40 pF/ft
Conductor to shield	65 pF/ft
RG58 coaxial cable, center conductor to shield	33 pF/ft
Connector, pin to pin	2 pF
Optical isolator, LED to photodetector	2 pF
1/2-watt resistor (end to end)	1.5 pF

Capacitive pickup can occur in many ways, shapes, and sizes. Here are a few examples:

- A TTL digital signal produces fast edges, with a typical rise time of 10 nanoseconds and voltage swings of 5 volts. If Z is a 1-megohm resistor, even 0.1pF will produce 5-volt spikes with decay time constants of 100 nanoseconds.

¹Sources: Excerpts from Ralph Morrison, *Grounding and Shielding Techniques in Instrumentation*, Second Edition (New York: John Wiley & Sons, 1977), p.30, and actual measurements.

•Crosstalk may result between two adjacent wires. For example, if two wires in a 10-foot (3-meter) length of cable have a capacitance of 40 pF/ft, the total capacitance is 400 pF. If a test voltage of 10 V at 1 kHz is on one conductor, 250 mV at 1 kHz will be coupled into the adjacent wire if Z is a 10 k resistance.

•Noise on the ac power line, developed through common impedances, will couple into other circuits. A common case is when transients couple through the interwinding capacitance of power-supply transformers.

It is amazing how little capacitance can cause serious problems. For example, consider the situation where high noise-immunity CMOS logic is used in an industrial circuit where 2500-volt, 1.5 MHz noise transients (IEEE Standard 472-1974) are present. Suppose that stray capacitance of only 0.1 pF exists between a CMOS input and the noise source, as shown in Figure 7. The calculated noise voltage, V_c , will be 2.4 volts, steady state, with an initial 50-V transient, which will cause improper logic operation or worse!

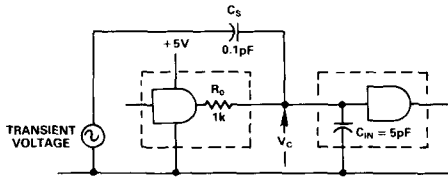


Figure 7. Coupling of high-voltage transients from test generator to logic.

Magnetically Coupled Noise. Strong magnetic fields are found where cables carry current, where ac power is distributed, and near machinery, power transformers, fans, etc. There is an analogous relationship between circuits coupled magnetically and those coupled capacitively, as shown in Figure 8 and Table 2.

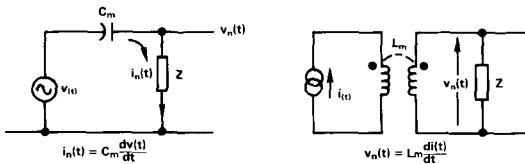


Figure 8. Comparison of magnetic and capacitive noise coupling.

Table 2. Characteristics of capacitive and magnetic coupling.

	Capacitive Coupling	Magnetic Coupling
Noise Source	Voltage change (dV/dt)	Current change (dI/dt)
Coupling Medium	Mutual capacitance	Mutual inductance
Coupled Noise	Current (frequently converted to voltage by Z)	Voltage

This analogy helps us consider some differences between capacitively and magnetically coupled noise:

•When the noise is magnetically coupled, voltage noise (V_n) appears in series with the receiver circuit; in the capacitive situation, the voltage noise produced between the receiver and ground is the voltage in Z caused by the noise current, i_n .

•Reducing the receiver impedance, Z, will reduce capacitively coupled noise. This is not the case in magnetically coupled circuits; lowering Z will not dramatically reduce voltage noise.

The voltage, V_n , induced in a closed loop (single turn) by a magnetic field is given by

$$V_n = 2\pi fBA \cos\theta \times 10^{-8} \quad (1)$$

volts, where f is the frequency of the sinusoidally varying flux density, B is the rms value of the flux density (gauss), A is the area of the closed loop (cm^2), and θ is the angle of B to area A.

For example, consider the circuit of Figure 9. It shows the calculation for two one-foot conductors, separated by 1 inch, in a 10-gauss 60-Hz magnetic field (typical of fans, power wiring, transformers). The maximum voltage induced in the wires is 3 mV.

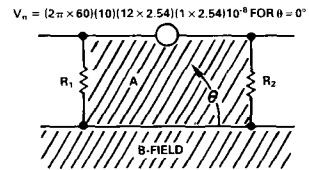


Figure 9. Example demonstrating magnitude of magnetic pickup.

The equation tells us that the noise voltage can be reduced by reducing B, A, or $\cos\theta$. The B term can be reduced by increasing the distance from the source of the field or—if the field is caused by currents flowing through nearby pairs of wires—twisting those wires to reduce the net field to zero by alternating its direction.

The loop area, A, can be reduced by placing the conductors closer together. For example, if the conductors in the example were placed 0.1" apart (separated only by insulation), the noise voltage would be reduced to 0.3mV. If they can be twisted together, the area is, in effect, reduced to small positive and negative increments that cancel, practically nullifying the magnetic pickup.

The $\cos\theta$ term can be reduced by proper orientation of the receiving wires to the field. For example, if the conductors were perpendicular to the field, the pickup would be minimized, while if they were run together in the same cable ($\theta = 0$), pickup would be maximized.

The rms induced voltage, V_n , in a conductor in parallel with a second conductor, carrying a current I_2 at an angular frequency $\omega = 2\pi f$, with a given mutual inductance, M, is

$$V_n = \omega M I_2 \quad (2)$$

The application of this relationship shown in Figure 10 illustrates why only one end of a shield should be grounded. A 100-ft length of shielded cable is used to carry a high-level low-impedance signal

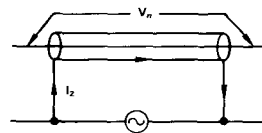


Figure 10. Magnetic pickup from current flowing through a cable shield.

(10V) to a 12-bit data-acquisition system (1 LSB \approx 2.4 mV). The shield, which has series resistance of 0.01 ohms per foot and mutual inductance to the conductor of $0.6\mu\text{H}/\text{ft}$, has been grounded at both the source and the destination. A potential of 1 volt at 60 Hz exists between the two ground points, causing a current of 1 ampere to flow in the 1-ohm total resistance of the shield. By (2), the noise voltage induced in the conductor is

$$V_n = (2\pi 60 \text{ Hz})(100 \times 0.6 \times 10^{-6} \text{ H})(1 \text{ A}) \\ = 23 \text{ mV,}$$

or 10 LSBs, thereby reducing the effective resolution of the system to less than 9 bits. This noise voltage is a direct consequence of the large current flowing in the shield because it is grounded at both ends. And the 1-volt potential assumed between the grounds was conservative! In heavy-industry environments, 10 to 50 volts between earth grounds is not uncommon.

Power-Line Transients. Another type of system noise is that generated by high-voltage transients in inductive circuits, such as relays, solenoids, and motors, when they are turned on and off. When devices having high self-inductance are turned off, the collapsing fields can generate transients of the order of kilovolts, with frequencies from 0.1 to 3 megahertz, that appear on the power line.

Besides creating noise in sensitive circuitry, via capacitive and conductive coupling and radiated energy, these transients are hazardous to equipment and people. Standards exist to characterize certain transient waveforms for the purpose of protection; however, besides being designed to withstand them, systems should also be designed to deal with their potential interference with signals. Figure 11 shows 4 typical waveforms existing in industry standards.

Miscellaneous Noise Sources Finally, there is a group of noise sources that can be considered as miscellaneous—or just “flakey.”

For low-level signals at high impedance, the cable itself can become a noise source. A charge can be produced on the dielectric material within the cable; if the dielectric does not maintain contact with the conductors, this charge will act as a noise source within the cable, unless the cable can be kept rigid. This noise is highly dependent on any motion of the cable; noise levels of 5 to 100 mV were reported by Belden Corporation. Noise of similar character (5 to 25 mV) was observed in the laboratory for RG188 coaxial cable, as it was moved and flexed.

Another type of motion-related noise occurs when a cable is moved through a magnetic field. Voltage will be induced in the cable as the cable cuts fixed flux lines or the flux density, B , changes. This kind of noise is troublesome in a high-vibration environment, where the cables can be in rapid motion. If the cable can be kept from vibrating relative to the field, this noise will not occur.

Finally, if instrumentation is operating in close proximity to a radio or television station, signals may be picked up from the transmissions. In addition to AM, FM, and television transmitters, the RFI may come from CB radios, amateur radios, walkie-talkies, paging systems, etc. High-frequency noise should be considered as a possible source of mysterious drifts in dc circuitry, due to rectification of picked-up rf; investigations of drift should always be conducted with a wideband oscilloscope.

SUMMARY

We have described here the different types of interference noise that will exist in any electronic system. Table 3 lists the noise sources discussed above and some effective approaches to solving the pickup problem. It is important to understand the complete noise system (source, coupling medium, receiver, and relationships) before noise-reduction techniques are employed.

Noise reduction is not a mystical job for wizards; it is a practical and analytical job for engineers. Needless to say, the most effective

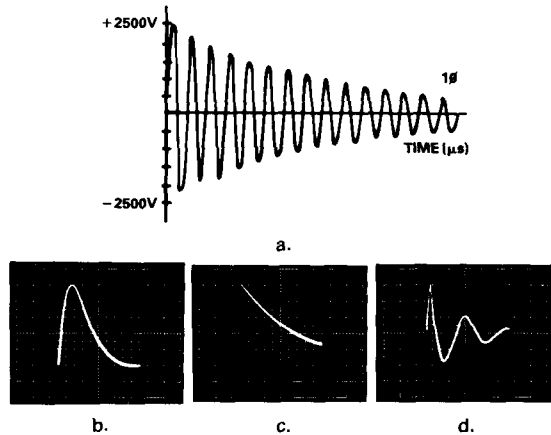
approach is *prevention*—applying noise-reduction analysis and minimization techniques *before the system is built*.

In part 2 of this article, we will describe the proper application of shielding and guarding techniques for noise reduction.

Further Reading:

Ralph Morrison, *op. cit.*

Henry W. Ott, *Noise Reduction Techniques in Electronic Systems* (New York: John Wiley & Sons, 1976). ▶



Courtesy of Key Tek Instrument Corp., Burlington, MA

Figure 11. Examples of transients existing in standards for industrial power-line equipment. (a) IEEE Standard 472-1974 “Guide for Surge Withstand Capability.” (b) Impulse wave, 8×20 , 1000V peak, $5\mu\text{s}/\text{div}$. (c) Impulse wave, 10×1000 , 1500V peak, $0.2\text{ms}/\text{div}$. (d) 100kHz ac surge, 6kV peak (500kHz leading edge); successive peaks down by 40% ($1\text{kV}/\text{div}$, $2\mu\text{s}/\text{div}$).

Table 3. Noise sources and possible solutions.

Common-Impedance Noise

- Proper circuits for distributing power
- Isolation transformers, optical isolators, analog isolators
- Shielding of sensitive circuits

Capacitively Coupled Noise

- Reducing noise sources
- Properly implemented shields (very effective)
- Reducing stray capacitance

Magnetically Coupled Noise

- Careful routing of wiring
- High-permeability (mumetal) shields (the most effective)
- Reducing area of receiver circuit (twisted pairs, physical wire placement)
- Reducing the noise source (twisted pairs, driven shields to cancel field)

Power-Line Transients

- Coil suppression on relays, solenoids, etc.
- Zero-crossing turnoff for relays, solenoids, etc.
- Shielding
- Reducing stray capacitance

Miscellaneous

- Rigid wiring
- Low-noise cable
- Shielding from RFI source

SHIELDING AND GUARDING

How to Exclude Interference-Type Noise What to Do and Why to Do It—A Rational Approach

by Alan Rich

This is the second of two articles dealing with interference noise. In the last issue of *Analog Dialogue* (Vol. 16, No. 3, pp. 16-19), we discussed the nature of interference, described the relationship between sources, coupling channels, and receivers, and considered means of combatting interference in systems by reducing or eliminating one of those three elements.

One of the means of reducing noise coupling is *shielding*. Our purpose in this article is to describe the correct uses of shielding to reduce noise. The major topics we will discuss include noise due to capacitive coupling, noise due to magnetic coupling, and driven shields and guards. A set of guidelines will be included, with do's and don'ts.

From the outset, it should be noted that shielding problems are always rational and do not involve the occult; but they are not always straightforward. Each problem must be analyzed carefully. It is important first to identify the noise source, the receiver, and the coupling medium. Improper shielding and grounding, based on faulty identification of any of these elements, may only make matters worse or create a new problem.

You can think of shielding as serving two purposes. First, shielding can be used to confine noise to a small region; this will prevent noise from extending its reach and getting into a nearby critical circuit. However, the problem with such shields is that noise captured by the shield can still cause problems if the return path the noise takes is not carefully planned and implemented by understanding of the ground system and making the connections correctly.

Second, if noise is present in a system, shields can be placed around critical circuits to prevent the noise from getting into sensitive portions of the circuits. These shields can consist of metal boxes around circuit regions or cables with shields around the center conductors. Again, where and how the shields are connected is important.

CAPACITIVELY COUPLED NOISE

If the noise results from an electric field, a shield works because a charge, Q_2 , resulting from an external potential, V_1 , cannot exist on the interior of a closed conducting surface (Figure 1).

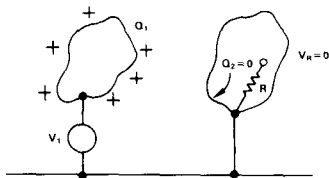


Figure 1. Charge Q_1 cannot create charge inside a closed metal shell.

Coupling by mutual, or stray, capacitance can be modeled by the circuit of Figure 2. Here, V_n is a noise source (switching transistor, TTL gate, etc.), C_s is the stray capacitance, Z is the impedance of a receiver (for example, a bypass resistor connected between the input of a high-gain amplifier and ground), and V_{no} is the output noise developed across Z .

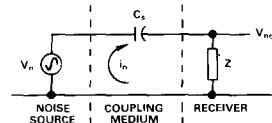


Figure 2. Equivalent circuit of capacitive coupling between a source and a nearby impedance.

A noise current, $i_n = V_n / (Z + Z_{Cs})$, will result, producing a noise voltage, $V_{no} = V_n / (1 + Z_{Cs} / Z)$. For example, if $C_s = 2.5$ pF, $Z = 10$ k Ω (resistive), and $V_n = 100$ mV at 1.3 MHz, the output noise will be 20 mV (0.2% of 10V, i.e., 8 LSBs of 12 bits).

It is important to recognize the effect that very small amounts of stray capacitance will have on sensitive circuits. This becomes increasingly critical as systems are being designed to combine circuits operating at lower power (implying higher impedance levels), higher speed (implying lower nodal stray capacitance, faster edges, and higher frequencies), and higher resolution (much less output noise permitted).

When a shield is added, the change to the situation of Figure 2 is exemplified by the circuit model of Figure 3. With the assumption that the shield has zero impedance, the noise current in loop A-B-D-A will be V_n / Z_{Cs1} , but the noise current in loop D-B-C-D will be zero, since there is no driving source in that loop. And, since no current flows, there will be no voltage developed across Z . The sensitive circuit has thus been shielded from the noise source, V_n .

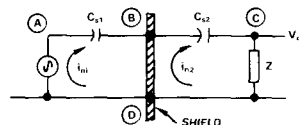


Figure 3. Equivalent circuit of the situation of Figure 2, with a shield interposed between the source and the impedance.

Guidelines for Applying Electrostatic Shields

- An electrostatic shield, to be effective, should be connected to the reference potential of any circuitry contained within the shield. If the signal is earthed or grounded (i.e., connected to a metal chassis or frame, and/or to earth), the shield must be earthed or grounded. But grounding the shield is useless if the signal is not grounded.
- The shield conductor of a shielded cable should be connected to the reference potential at the signal-reference node (Figure 4).
- If the shield is split into sections, as might occur if connectors are used, the shield for each segment must be tied to those for the

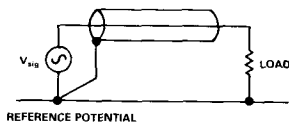


Figure 4. Grounding a cable shield.

adjoining segments, and ultimately connected (only) to the signal-reference node (Figure 5).

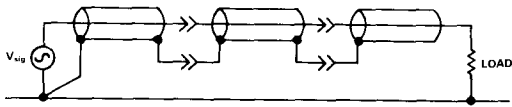


Figure 5. Shields must be interconnected if interrupted.

•The number of separate shields required in a system is equal to the number of independent signals that are being measured. Each signal should have its own shield, with no connections to other shields in the system, unless they share a common reference potential (signal "ground"). If there is more than one signal ground (Figure 6), each shield should be connected to its own reference potential.

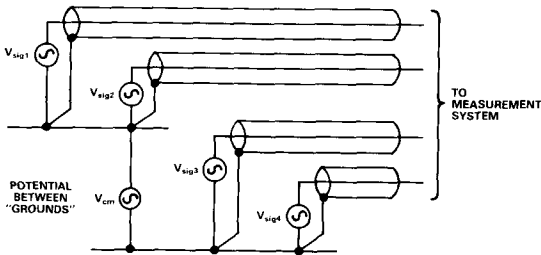


Figure 6. Each signal should have its own shield connected to its own reference potential.

•Don't connect both ends of the shield to "ground". The potential difference between the two "grounds" will cause a shield current to flow (Figure 7). The shield current will induce a noise voltage into the center conductor via magnetic coupling. An example of this can be found in Part 1 of this series, *Analog Dialogue* 16-3, page 18, Figure 10.

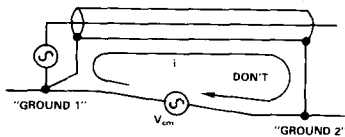
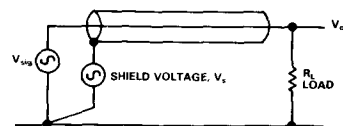


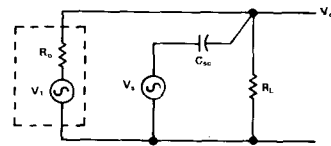
Figure 7. Don't connect the shield to ground at more than one point.

•Don't allow shield current to exist (except as noted later in this article). The shield current will induce a voltage in the center conductor.

•Don't allow the shield to be at a voltage with respect to the reference potential (except in the case of a guard shield, to be described). The shield voltage will couple capacitively to the center conductor (or conductors in a multiple-conductor shield). With a noise voltage, V_s , on the shield, the situation is as shown in Figure 8.



a. Shield at potential V_s .



b. Equivalent circuit.

Figure 8. Don't permit the shield to be at a potential with respect to the signal.

The fraction of V_s appearing at the output will be

$$V_o = \frac{V_s}{\sqrt{1 + \frac{1}{(2\pi f R_{eq} C_{sc})^2}}} \quad (1)$$

where V_1 is the open-circuit signal voltage, R_o is the signal's source impedance, C_{sc} is the cable's shield-to-conductor capacitance, and R_{eq} is the equivalent parallel resistance of R_o and R_L . For example, if $V_s = 1V$ at 1.5MHz, $C_{sc} = 200pF$ (10 feet of cable), $R_o = 1000$ ohms, and $R_L = 10k\Omega$, the output noise voltage will be 0.86 volts.

This is an often-ignored guideline; serious noise problems can be created by inadvertently applying undesired potentials to the shield.

•Know by careful study how the noise current that has been captured by the shield returns to "ground." An improperly returned shield can cause shield voltages, can couple into other circuits, or couple into other shields. The shield return should be as short as possible to minimize inductance.

Here is an example that illustrates the problems that can arise in relation to these last two guidelines: Consider the improperly configured shield system shown in Figure 9, in which a precision voltage source, V_1 , and a digital logic gate share a common shield connection. This situation can occur in a large system where analog and digital signals are cabled together.

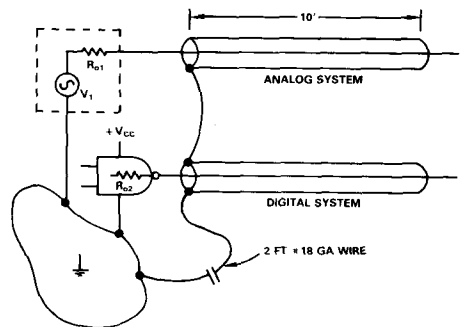


Figure 9. A situation that generates transient shield voltages.

A step voltage change in the output of the logic circuit couples capacitively to its shield, creating a current in the common 2-foot

shield return. This, in turn, develops a shield voltage common to both the analog and digital shields. An equivalent circuit is shown in Figure 10, in which $V(t)$ is a 5-volt step from a TTL logic gate, R_{o2} is the 13-ohm output impedance of the logic gate, C_{ws} is the 470-pF capacitance from the shield to the center conductor of the shielded cable, and R_s and L_s are the 0.1-ohm resistance and 1-microhenry inductance of the 2-foot wire connecting the shield to the system ground.

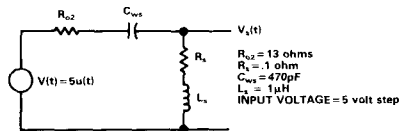


Figure 10. Equivalent circuit for generating shield voltage.

The shield voltage, $V_s(t)$, can be solved for by conventional circuit-analysis techniques, or simulated by actually building and carefully making measurements on a circuit with the given parameters. For the purpose of demonstration, the calculated response waveform, illustrated in Figure 11, with a 5-volt initial spike, resonant frequency of 7.3 MHz, and damping time constant of 0.15 μ s, is sufficient to illustrate the nature of the voltage that appears on the shield and is capacitively coupled to the analog input. If the voltage is looked at with a wideband oscilloscope, it will look like a noise "spike." We can see that this transient will couple a fast damped waveform of significant peak amplitude to the analog system input.

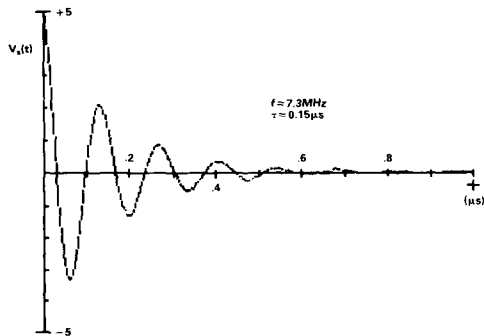


Figure 11. Computed response of circuit of Figure 10.

Even in a purely digital system, noise glitches can be caused to appear in apparently remote portions of a system having the kind of situation shown. This can often explain some otherwise inexplicable system bugs.

In quite a few cases, the proper choice of shield connection among the many possibilities may not be immediately obvious, and the guidelines may not provide us with a clear choice. There is no alternative but to analyze the various possibilities and choose the approach for which the lowest noise may be calculated.

For example, consider the case illustrated in Figure 12, in which the measurement system and the source have differing ground potentials. Should we connect the shield to A: the low side at the measurement-system input, B: ground at the system input, C: ground at the signal source, or D: the low side at the source?

A is a poor choice, since noise current is allowed to flow in a signal

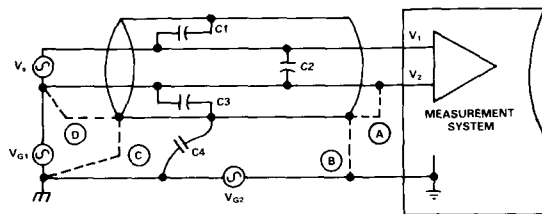


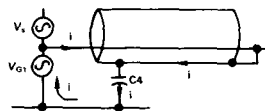
Figure 12. Possible grounds where system and source have differing ground potentials.

conductor. The path of the noise current due to V_{G1} , as it returns through C_4 , is shown in Figure 13a.

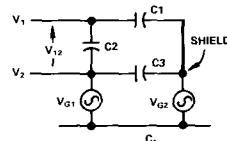
B is also a poor choice, since the two noise sources in series, V_{G1} and V_{G2} , produce a component across the two signal wires, developed by the source impedance in parallel with C_2 , in series with C_1 , as shown in Figure 13b.

C is poor, too, since V_{G1} produces a voltage across the two signal wires, by the same mechanism as (B), as Figure 13c shows.

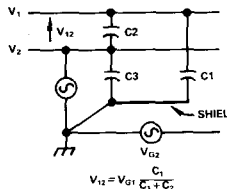
D is the best choice, under the given assumptions, as can be seen in Figure 13d. It also tends to confirm the grounding guideline to connect the shield at the signal's reference potential.



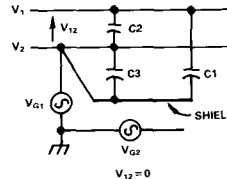
a. Return path A.



b. Return path B.



c. Return path C.



d. Return path D.

Figure 13. Equivalent circuits.

NOISE RESULTING FROM A MAGNETIC FIELD

Noise in the form of a magnetic field induces voltage in a conductor or circuit; it is much more difficult to shield against than elec-

tric fields because it can penetrate conducting materials. A typical shield placed around a conductor and grounded at one end has little if any effect on the magnetically induced voltage in that conductor.

As a magnetic field, B , penetrates a shield, its amplitude decreases exponentially (Figure 14). The skin depth, δ , of the shield material, is defined as the depth of penetration required for the field to be attenuated to 37% ($\exp(-1)$) of its value in free air. Table 1¹ lists typical values of δ for several materials at various frequencies. You can see that any of the materials will be more effective as a shield at high frequency, because δ decreases with frequency, and that steel provides at least an order of magnitude more effective shielding at any frequency than copper or aluminum.

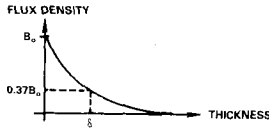


Figure 14. Magnetic field in a shield as a function of penetration depth.

Figure 15 compares absorption loss as a function of frequency for two thicknesses of copper and steel. 1/8-inch steel becomes quite effective for frequencies above 200 Hz, and even a 20-mil (0.5 mm) thickness of copper is effective at frequencies above 1 MHz. However, all show a glaring weakness at lower frequencies, including 50-60-Hz line frequencies—the principal source of magnetically coupled noise at low frequency.

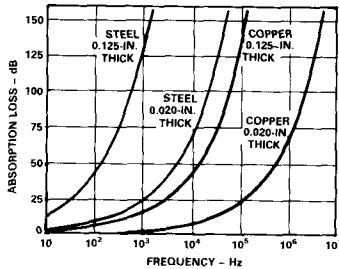


Figure 15. Absorption loss vs. frequency for two thicknesses of copper and steel.

For improved low-frequency magnetic shielding, a shield consisting of a high-permeability magnetic material (e.g., Mumetal)

Table 1. Skin depth, δ , vs. frequency

Frequency	δ for Copper		δ for Aluminum		δ for Steel	
	(in.)	(mm)	(in.)	(mm)	(in.)	(mm)
60Hz	0.335	8.5	0.429	10.9	0.034	0.86
100Hz	0.260	6.6	0.333	8.5	0.026	0.66
1kHz	0.082	2.1	0.105	2.7	0.008	0.2
10kHz	0.026	0.66	0.033	0.84	0.003	0.08
100kHz	0.008	0.2	0.011	0.3	0.0008	0.02
1MHz	0.003	0.08	0.003	0.08	0.0003	0.008

¹Table 1 and Figures 15 and 16 are from Ott, H.W., *Noise Reduction Techniques in Electronic Systems* (New York: John Wiley & Sons, © 1976).

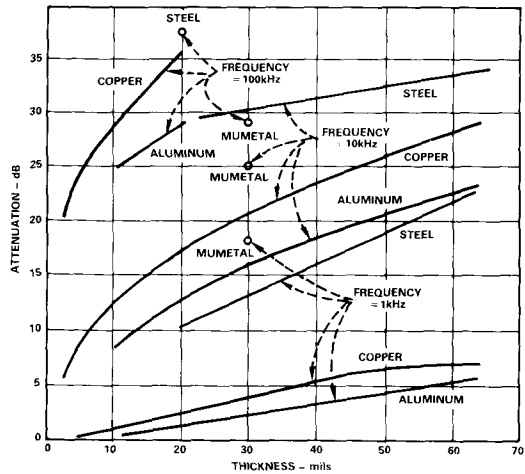
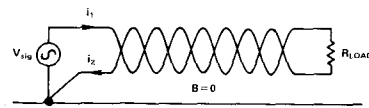


Figure 16. Shielding attenuation of Mumetal and other materials at several frequencies.

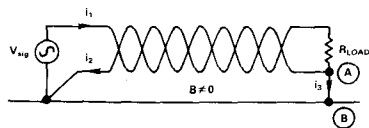
should be considered. Figure 16 compares a 30-mil thickness of Mumetal with various materials at several frequencies. It shows that, below 1 kHz, Mumetal is more effective than any of the other materials, while at 100kHz it is the least effective. However, Mumetal is not especially easy to apply, and if it is saturated by an excessively strong field, it will no longer provide an advantage.

As you can see, it is very difficult to shield against magnetic fields, i.e., to modify the coupling medium by shielding. Therefore, the most effective approaches at low frequency are to minimize the strength of the interfering magnetic field, minimize the receiver loop area, and minimize coupling by optimizing wiring geometries. Here are some guidelines:

- Locate the receiving circuits as far as possible from the source of the magnetic field.
- Avoid running wires parallel to the magnetic field; instead, cross the magnetic field at right angles.
- Shield the magnetic field with an appropriate material for the frequency and field strength.
- Use a twisted pair of wires for conductors carrying the high-level current that is the source of the magnetic field. If the currents in the two wires are equal and opposite, the net field in any direction



a. Correct connection with balanced currents.



b. Incorrect connection forming ground loop.

Figure 17. Connections to a twisted pair.

over each cycle of twist will be zero (Figure 17a). For this arrangement to work, none of the current can be shared with another conductor, for example, a ground plane. Figure 17b shows what can happen if a ground loop is formed; if part of the current flows through the ground plane (depending on the ratio of conductor resistance to ground resistance), it will form a loop with the twisted pair, generating a field determined by i_3 ($= i_1 - i_2$).

The ground connection between A and B need not be as simple as a short circuit to cause trouble. Any stray unbalanced capacitance or resistance from R_{load} circuits to the ground plane will also unbalance the currents and produce a net current through the wires and the ground plane, producing a ground loop and a related magnetic field. For this reason, it is also good practice to run the twisted pair close to the ground plane to tend to balance the capacitances from each side to ground, as well as to minimize loop area.

● Use a shielded cable with the high-level source circuit's return current carried in the shield (Figure 18). If the shield current, I_2 is equal and opposite to that in the center conductor, the center-conductor field and the shield field will cancel, producing a zero net field. In this case, which seems to violate the "no shield current" rule for receiver circuits, the concentric cable is not used to shield the center lead; instead, the geometry produces cancellation.

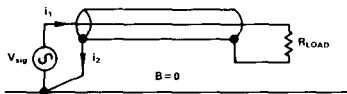


Figure 18. Use of shield for return current to noisy source.

This scheme can be usefully employed in an ATE system where accurate measurements must be performed on devices with high power-supply currents that may be noisy. For example, Figure 19 shows the application of this technique to the connections for the high-current logic supply for an a/d converter under test—at the end of a test cable.

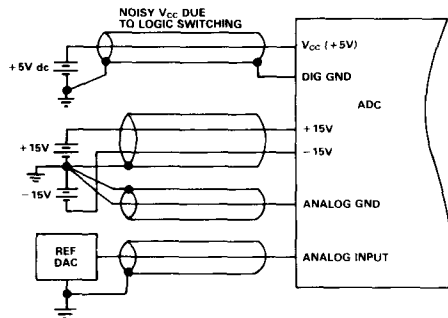


Figure 19. Application of circuit of Figure 18 in a test system.

● Since magnetically induced noise depends on the area of the receiver loop, the induced voltage due to magnetic coupling can be reduced by reducing the loop's area. What is the receiver loop? In the example shown in Figure 20, the signal source and its load are connected by a pair of conductors of length L and separation D . The circuit (assuming it has a rectangular configuration) forms a loop with area $D \cdot L$.

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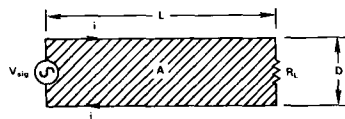


Figure 20. Area of a loop that receives magnetically coupled noise.

The voltage induced in series with the loop is proportional to the area and the cosine of its angle to the field. Thus, to minimize noise, the loop should be oriented at right angles to the field, and its area should be minimized.

The area can be reduced by decreasing the length of and/or decreasing the distance between the conductors. This is easily accomplished with a twisted pair, or at least a tightly cabled pair, of conductors. It is good practice to pair conductors so that the circuit wire and its return path will always be together. To do this, the designer must be certain of the actual path that the return current takes in getting back to the signal source. Quite often, the current returns by a path not intended in the original design layout.

If wires are moved (for example, by a technician troubleshooting some other problem), the loop area and orientation to the field may change, so that yesterday's acceptable noise level may be transformed to tomorrow's disastrous noise level. Which may lead to a service call . . . and another repetition of the cycle. The bottom line: Know the loop area and orientation, do what must be done to minimize noise—and permanently secure the wiring!

DRIVEN SHIELDS AND GUARDING

We have discussed the role of a current-driven shield carrying an equal and opposite current to reduce generated noise by reducing the magnetic field around a conductor.

Guarding is similar, in that it involves driving a shield, at low impedance, with a potential essentially equal to the common-mode voltage on the signal wire contained within the shield. Guarding has many useful purposes: It reduces common-mode capacitance, improves common-mode rejection, and eliminates leakage currents in high-impedance measurement circuits.

Figure 21 shows an example of an op amp with negligible bias current connected as a high-impedance non-inverting amplifier with gain. The purpose of the cable is to shield the high input-impedance signal conductor from capacitively coupled noise and to minimize leakage currents. The signal comes from a 10-megohm source, and the cable is assumed to have 1000 megohms of leakage resistance (which may change as a function of temperature, humidity, etc.) from conductor to shield. If connected as shown, the equivalent input circuit is an attenuator which loses 1% of the

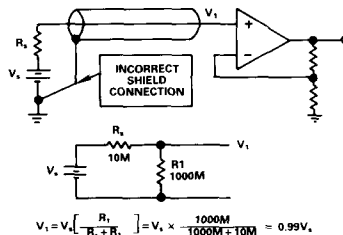


Figure 21. Op amp connected as high-impedance non-inverting amplifier with gain, with shielded input lead.

signal at the time it is measured, and an unknown fraction at other times. Also, the cable capacitance produces a substantial lag time constant, $R_s C_c$.

Figure 22 has the same players, but the shield is connected to the tap of the gain divider (usually at low impedance). Being connected to the inverting input of the op amp, it should be at the same potential as the amplifier's non-inverting input. Since there is no voltage across the cable's leakage resistance, there is no current through it and its resistance value doesn't matter; V_1 must therefore be equal to V_s , since bias current was assumed negligible.

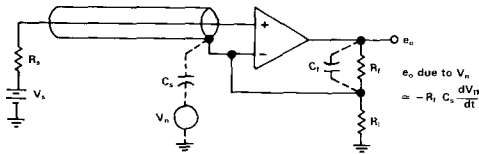


Figure 22. Same as Figure 21, but cable shield connected as a guard.

Also, there is no voltage across the cable capacitance, hence no charging or discharging of the cable; thus the lag time constant depends mainly on circuit strays and the amplifier's input capacitance. For stability, capacitance should be connected between the output and the negative input, such that $C_f R_f = C_s R_s$, where C_s is sum of the stray capacitance between shield and ground and the input capacitance.

There must be no noise voltage applied to the guard. In noisy systems, as Figure 22 shows, capacitively coupled noise will be differentiated, emphasizing the higher-frequency components. This can be avoided (Figure 23) by either using a buffer follower with fast response and low output impedance to drive the guard (a) or a second shield, around the guard, grounded to the signal common (b).

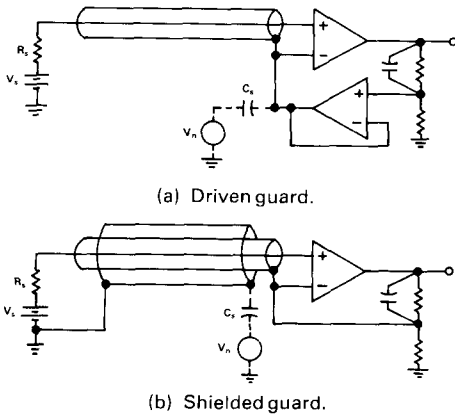


Figure 23. Avoiding noise pickup on the guard.

In high-impedance current-input inverting configurations, where a length of shielded wire is used to guard the lead from the current source to the amplifier's inverting input, the guard should either be driven by a buffer at the same potential as the non-inverting input (and connected nowhere else), or be tied directly to the non-

inverting input, with a second outer shield connected to the signal's reference point.

SUMMARY

Table 2 summarizes the important points made in this article. All are important to maintaining a high-integrity shield system. However, we cannot emphasize too strongly the two subjects that are most-often ignored: appearance of noise voltage on signal shields and proper disposition of shield noise currents. *Noise voltage must not exist on the shield*; shield-to-conductor capacitance will couple the noise directly to the center conductor. *If shield currents are not returned properly, they can show up in a remote part of the system and perhaps cause trouble in a location totally unrelated to the shielding problem that was "solved."* ▀

Table 2. Applicability of shielding considerations

Consideration	Universal	Electric	Magnetic
Know the noise source, coupling medium, and receiver.	X	X	X
Different shielding techniques are required for different noise sources, coupling channels, and receivers.	X	X	X
In most situations, conventional circuit analysis using lumped elements can be used.	X	X	X
Connect the shield at the signal-source end only.		X	
Carry shields through connectors.		X	
Individual shields should not be tied together.		X	
Do not ground both ends of a shield.		X	
Do not allow shield current to flow, except for driven shields - to cancel magnetic fields		X	X
Do not allow voltage on a shield, except for guarding.		X	
Know <i>exactly</i> where noise current from the shield will flow.		X	
Use short connections to return noise current from the shield.		X	
Electrostatic shields have little effect in reducing noise resulting from magnetic fields.			X
Reduce magnetic fields by physical separation proper orientation, twisted pairs, and/or driven shields.			X
Know the receiver loop area and orientation to the field. Keep field at right angles and reduce the loop area by using paired conductors, preferably twisted pairs, and minimize wire lengths.			X
Use guarding in high-impedance circuits	X	X	
In high-impedance circuits, be extremely careful of shield noise	X	X	

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Mounting Considerations for Power Semiconductors

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INTRODUCTION

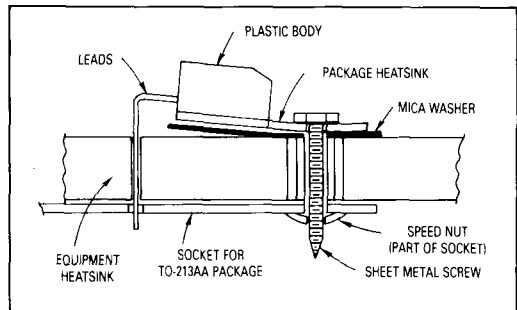
Current and power ratings of semiconductors are inseparably linked to their thermal environment. Except for lead-mounted parts used at low currents, a heat exchanger is required to prevent the junction temperature from exceeding its rated limit, thereby running the risk of a high failure rate. Furthermore, the semiconductor industry's field history indicated that the failure rate of most silicon semiconductors decreases approximately by one-half for a decrease in junction temperature from 160°C to 135°C.⁽¹⁾ Guidelines for designers of military power supplies impose a 110°C limit upon junction temperature.⁽²⁾ Proper mounting minimizes the temperature gradient between the semiconductor case and the heat exchanger.

Most early life field failures of power semiconductors can be traced to faulty mounting procedures. With metal packaged devices, faulty mounting generally causes unnecessarily high junction temperature, resulting in reduced component lifetime, although mechanical damage has occurred on occasion from improperly mounting to a warped surface. With the widespread use of various plastic-packaged semiconductors, the prospect of mechanical damage is very significant. Mechanical damage can impair the case moisture resistance or crack the semiconductor die.

(1) MIL-HANDBOOK — 2178, SECTION 2.2.
(2) "Navy Power Supply Reliability — Design and Manufacturing Guidelines" NAVMAT P4855-1, Dec. 1982 NAVPUBFORCEN, 5801 Tabor Ave., Philadelphia, PA 19120.

Cho-Therm is a registered trademark of Chromerics, Inc.
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Figure 1 shows an example of doing nearly everything wrong. A tab mount TO-220 package is shown being used as a replacement for a TO-213AA (TO-66) part which was socket mounted. To use the socket, the leads are bent — an operation which, if not properly done, can crack the package, break the internal bonding wires, or crack the die. The package is fastened with a sheet-metal screw through a 1/4" hole containing a fiber-insulating sleeve. The force used to tighten the screw tends to pull the package into the hole, possibly causing enough distortion to crack the die. In addition the contact area is small because of the area consumed by the large hole and the bowing of the package; the result is a much higher junction temperature than expected. If a rough heatsink surface and/or burrs around the hole were displayed in the illustration, most but not all poor mounting practices would be covered.



**Figure 1. Extreme Case of Improper Mounting
A Semiconductor (Distortion Exaggerated)**



In many situations the case of the semiconductor must be electrically isolated from its mounting surface. The isolation material is, to some extent, a thermal isolator as well, which raises junction operating temperatures. In addition, the possibility of arc-over problems is introduced if high voltages are present. Various regulating agencies also impose creepage distance specifications which further complicates design. Electrical isolation thus places additional demands upon the mounting procedure.

Proper mounting procedures usually necessitate orderly attention to the following:

1. Preparing the mounting surface
2. Applying a thermal grease (if required)
3. Installing the insulator (if electrical isolation is desired)
4. Fastening the assembly
5. Connecting the terminals to the circuit

In this note, mounting procedures are discussed in general terms for several generic classes of packages. As newer packages are developed, it is probable that they will fit into the generic classes discussed in this note. Unique requirements are given on data sheets pertaining to the particular package. The following classes are defined:

- Stud Mount
- Flange Mount
- Pressfit
- Plastic Body Mount
- Tab Mount
- Surface Mount

Appendix A contains a brief review of thermal resistance concepts. Appendix B discusses measurement difficulties with interface thermal resistance tests. Appendix C indicates the type of accessories supplied by a number of manufacturers.

MOUNTING SURFACE PREPARATION

In general, the heatsink mounting surface should have a flatness and finish comparable to that of the semiconductor package. In lower power applications, the heatsink surface is satisfactory if it appears flat against a straight edge and is free from deep scratches. In high-power applications, a more detailed examination of the surface is required. Mounting holes and surface treatment must also be considered.

Surface Flatness

Surface flatness is determined by comparing the variance in height (Δh) of the test specimen to that of a reference standard as indicated in Figure 2. Flatness is normally specified as a fraction of the Total Indicator Reading (TIR). The mounting surface flatness, i.e. $\Delta h/TIR$, if less than 4 mils per inch, normal for extruded aluminum, is satisfactory in most cases.

Surface Finish

Surface finish is the average of the deviations both above and below the mean value of surface height. For minimum interface resistance, a finish in the range of 50 to 60 microinches is satisfactory; a finer finish is costly to achieve and does not significantly lower contact resis-

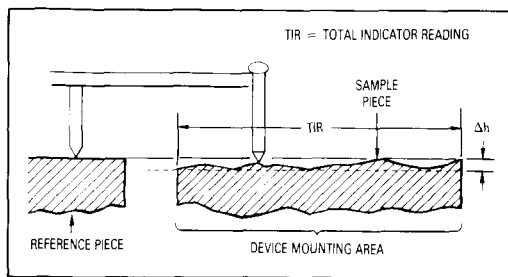


Figure 2. Surface Flatness Measurement

tance. Tests conducted by Thermalloy using a copper TO-204 (TO-3) package with a typical 32-microinch finish, showed that heatsink finishes between 16 and 64 μ -in caused less than $\pm 2.5\%$ difference in interface thermal resistance when the voids and scratches were filled with a thermal joint compound.⁽³⁾ Most commercially available cast or extruded heatsinks will require spotfacing when used in high-power applications. In general, milled or machined surfaces are satisfactory if prepared with tools in good working condition.

Mounting Holes

Mounting holes generally should only be large enough to allow clearance of the fastener. The larger thick flange type packages having mounting holes removed from the semiconductor die location, such as the TO-3, may successfully be used with larger holes to accommodate an insulating bushing, but many plastic encapsulated packages are intolerant of this condition. For these packages, a smaller screw size must be used such that the hole for the bushing does not exceed the hole in the package.

Punched mounting holes have been a source of trouble because if not properly done, the area around a punched hole is depressed in the process. This "crater" in the heatsink around the mounting hole can cause two problems. The device can be damaged by distortion of the package as the mounting pressure attempts to conform it to the shape of the heatsink indentation, or the device may only bridge the crater and leave a significant percentage of its heat-dissipating surface out of contact with the heatsink. The first effect may often be detected immediately by visual cracks in the package (if plastic), but usually an unnatural stress is imposed, which results in an early-life failure. The second effect results in hotter operation and is not manifested until much later.

Although punched holes are seldom acceptable in the relatively thick material used for extruded aluminum heatsinks, several manufacturers are capable of properly utilizing the capabilities inherent in both fine-edge blanking or sheared-through holes when applied to sheet metal as commonly used for stamped heatsinks. The holes are pierced using Class A progressive dies mounted on four-post die sets equipped with proper pressure pads and holding fixtures.

(3) Catalog #87-HS-9 (1987), page 8, Thermalloy, Inc., P.O. Box 810839, Dallas, Texas 75381-0839.

When mounting holes are drilled, a general practice with extruded aluminum, surface cleanup is important. Chamfers must be avoided because they reduce heat transfer surface and increase mounting stress. However, the edges must be broken to remove burrs which cause poor contact between device and heatsink and may puncture isolation material.

Surface Treatment

Many aluminum heatsinks are black-anodized to improve radiation ability and prevent corrosion. Anodizing results in significant electrical but negligible thermal insulation. It need only be removed from the mounting area when electrical contact is required. Heatsinks are also available which have a nickel plated copper insert under the semiconductor mounting area. No treatment of this surface is necessary.

Another treated aluminum finish is iridite, or chromate-acid dip, which offers low resistance because of its thin surface, yet has good electrical properties because it resists oxidation. It need only be cleaned of the oils and films that collect in the manufacture and storage of the sinks, a practice which should be applied to all heatsinks.

For economy, paint is sometimes used for sinks; removal of the paint where the semiconductor is attached is usually required because of paint's high thermal resistance. However, when it is necessary to insulate the semiconductor package from the heatsink, hard anodized or painted surfaces allow an easy installation for low voltage applications. Some manufacturers will provide anodized or painted surfaces meeting specific insulation voltage requirements, usually up to 400 volts.

It is also necessary that the surface be free from all foreign material, film, and oxide (freshly bared aluminum forms an oxide layer in a few seconds). Immediately prior to assembly, it is a good practice to polish the mounting area with No. 000 steel wool, followed by an acetone or alcohol rinse.

INTERFACE DECISIONS

When any significant amount of power is being dissipated, something must be done to fill the air voids between mating surfaces in the thermal path. Otherwise the interface thermal resistance will be unnecessarily high and quite dependent upon the surface finishes.

For several years, thermal joint compounds, often called grease, have been used in the interface. They have a resistivity of approximately 60°C/W/in whereas air has 1200°C/W/in. Since surfaces are highly pock-marked with minute voids, use of a compound makes a significant reduction in the interface thermal resistance of the joint. However, the grease causes a number of problems, as discussed in the following section.

To avoid using grease, manufacturers have developed dry conductive and insulating pads to replace the more traditional materials. These pads are conformal and therefore partially fill voids when under pressure.

Thermal Compounds (Grease)

Joint compounds are a formulation of fine zinc or other conductive particles in a silicone oil or other synthetic base fluid which maintains a grease-like consistency with time and temperature. Since some of these compounds do not spread well, they should be evenly applied in a

very thin layer using a spatula or lintless brush, and wiped lightly to remove excess material. Some cyclic rotation of the package will help the compound spread evenly over the entire contact area. Some experimentation is necessary to determine the correct quantity; too little will not fill all the voids, while too much may permit some compound to remain between well mated metal surfaces where it will substantially increase the thermal resistance of the joint.

To determine the correct amount, several semiconductor samples and heatsinks should be assembled with different amounts of grease applied evenly to one side of each mating surface. When the amount is correct a very small amount of grease should appear around the perimeter of each mating surface as the assembly is slowly torqued to the recommended value. Examination of a dismantled assembly should reveal even wetting across each mating surface. In production, assemblers should be trained to slowly apply the specified torque even though an excessive amount of grease appears at the edges of mating surfaces. Insufficient torque causes a significant increase in the thermal resistance of the interface.

To prevent accumulation of airborne particulate matter, excess compound should be wiped away using a cloth moistened with acetone or alcohol. These solvents should not contact plastic-encapsulated devices, as they may enter the package and cause a leakage path or carry in substances which might attack the semiconductor chip.

The silicone oil used in most greases has been found to evaporate from hot surfaces with time and become deposited on other cooler surfaces. Consequently, manufacturers must determine whether a microscopically thin coating of silicone oil on the entire assembly will pose any problems. It may be necessary to enclose components using grease. The newer synthetic base greases show far less tendency to migrate or creep than those made with a silicone oil base. However, their currently observed working temperature range are less, they are slightly poorer on thermal conductivity and dielectric strength and their cost is higher.

Data showing the effect of compounds on several package types under different mounting conditions is shown in Table 1. The rougher the surface, the more valuable the grease becomes in lowering contact resistance; therefore, when mica insulating washers are used, use of grease is generally mandatory. The joint compound also improves the breakdown rating of the insulator.

Conductive Pads

Because of the difficulty of assembly using grease and the evaporation problem, some equipment manufacturers will not, or cannot, use grease. To minimize the need for grease, several vendors offer dry conductive pads which approximate performance obtained with grease. Data for a greased bare joint and a joint using Grafoil, a dry graphite compound, is shown in the data of Figure 3. Grafoil is claimed to be a replacement for grease when no electrical isolation is required; the data indicates it does indeed perform as well as grease. Another conductive pad available from Aavid is called KON-DUX. It is made with a unique, grain oriented, flake-like structure (patent pending). Highly compressible, it becomes

Table 1
Approximate Values for Interface Thermal Resistance Data from Measurements Performed
in Motorola Applications Engineering Laboratory

Dry interface values are subject to wide variation because of extreme dependence upon surface conditions. Unless otherwise noted the case temperature is monitored by a thermocouple located directly under the die reached through a hole in the heatsink. (See Appendix B for a discussion of Interface Thermal Resistance Measurements.)

Package Type and Data		Interface Thermal Resistance (°C/W)						
JEDEC Outlines	Description	Test Torque In-Lb	Metal-to-Metal		With Insulator			See Note
			Dry	Lubed	Dry	Lubed	Type	
DO-203AA, TO-210AA TO-208AB	10-32 Stud 7/16" Hex	15	0.3	0.2	1.6	0.8	3 mil Mica	
DO-203AB, TO-210AC TO-208	1/4-28 Stud 11/16" Hex	25	0.2	0.1	0.8	0.6	5 mil Mica	
DO-208AA	Pressfit, 1/2"	—	0.15	0.1	—	—	—	
TO-204AA (TO-3)	Diamond Flange	6	0.5	0.1	1.3	0.36	3 mil Mica	1
TO-213AA (TO-66)	Diamond Flange	6	1.5	0.5	2.3	0.9	2 mil Mica	
TO-126	Thermopad 1/4" x 3/8"	6	2.0	1.3	4.3	3.3	2 mil Mica	
TO-220AB	Thermowatt	8	1.2	1.0	3.4	1.6	2 mil Mica	1, 2

NOTES: 1. See Figures 3 and 4 for additional data on TO-3 and TO-220 packages.
2. Screw not insulated. See Figure 12.

formed to the surface roughness of both the heatsink and semiconductor. Manufacturer's data shows it to provide an interface thermal resistance better than a metal interface with filled silicone grease. Similar dry conductive pads are available from other manufacturers. They are a fairly recent development; long term problems, if they exist, have not yet become evident.

INSULATION CONSIDERATIONS

Since most power semiconductors use vertical device construction it is common to manufacture power semiconductors with the output electrode (anode, collector or drain) electrically common to the case; the problem of isolating this terminal from ground is a common one. For lowest overall thermal resistance, which is quite important when high power must be dissipated, it is best to isolate the entire heatsink/semiconductor structure from ground, rather than to use an insulator between the semiconductor and the heatsink. Heatsink isolation is not always possible, however, because of EMI requirements, safety reasons, instances where a chassis serves as a heatsink or where a heatsink is common to several non-isolated packages. In these situations insulators are used to isolate the individual components from the heatsink. Newer packages, such as the Motorola Full Pak and EMS modules, contain the electrical isolation material within, thereby saving the equipment manufacturer the burden of addressing the isolation problem.

Insulator Thermal Resistance

When an insulator is used, thermal grease is of greater importance than with a metal-to-metal contact, because two interfaces exist instead of one and some materials,

such as mica, have a hard, markedly uneven surface. With many isolation materials reduction of interface thermal resistance of between 2 to 1 and 3 to 1 are typical when grease is used.

Data obtained by Thermalloy, showing interface resistance for different insulators and torques applied to TO-204 (TO-3) and TO-220 packages, are shown in Figure 3, for bare and greased surfaces. Similar materials to those shown are available from several manufacturers. It is obvious that with some arrangements, the interface thermal resistance exceeds that of the semiconductor (junction to case).

Referring to Figure 3, one may conclude that when high power is handled, beryllium oxide is unquestionably the best. However, it is an expensive choice. (It should not be cut or abraded, as the dust is highly toxic.) Thermafilm is a filled polyimide material which is used for isolation (variation of Kapton). It is a popular material for low power applications because of its low cost ability to withstand high temperatures, and ease of handling in contrast to mica which chips and flakes easily.

A number of other insulating materials are also shown. They cover a wide range of insulation resistance, thermal resistance and ease of handling. Mica has been widely used in the past because it offers high breakdown voltage and fairly low thermal resistance at a low cost but it certainly should be used with grease.

Silicone rubber insulators have gained favor because they are somewhat conformal under pressure. Their ability to fill in most of the metal voids at the interface reduces the need for thermal grease. When first introduced, they suffered from cut-through after a few years in service. The ones presently available have solved this problem by having imbedded pads of Kapton or fiberglass. By

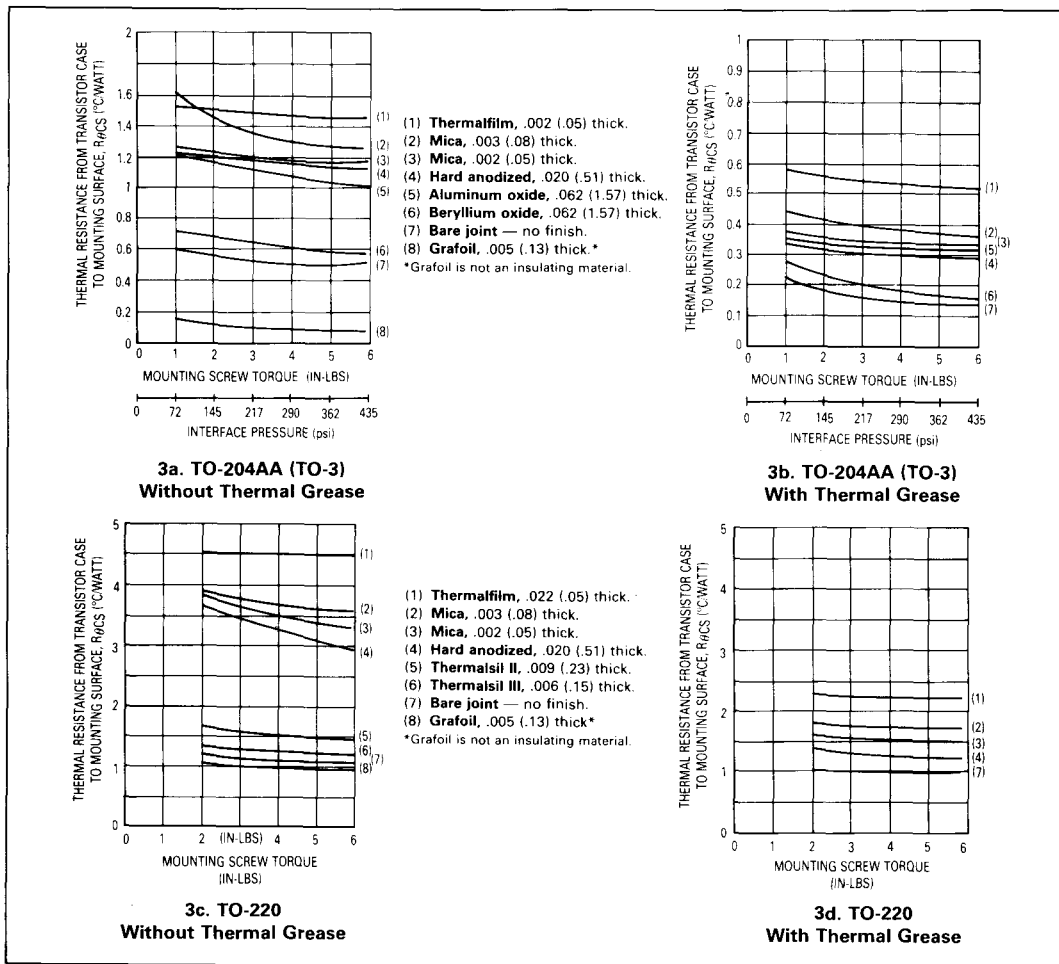


Figure 3. Interface Thermal Resistance for TO-204, TO-3 and TO-220 Packages using Different Insulating Materials as a Function of Mounting Screw Torque (Data Courtesy Thermalloy)

comparing Figures 3c and 3d, it can be noted that Thermasil, a filled silicone rubber, without grease, has about the same interface thermal resistance as greased mica for the TO-220 package.

A number of manufacturers offer silicone rubber insulators. Table 2 shows measured performance of a number of these insulators under carefully controlled, nearly identical conditions. The interface thermal resistance extremes are over 2:1 for the various materials. It is also clear that some of the insulators are much more tolerant than others of out-of-flat surfaces. Since the tests were performed, newer products have been introduced. The Bergquist K-10 pad, for example, is described as having about 2/3 the interface resistance of the Sil Pad 1000 which would place its performance close to the Chomerics 1671 pad. AAVID also offers an isolated pad called

Table 2. Thermal Resistance of Silicone Rubber Pads

Manufacturer	Product	R _{θCS} @ 3 Mil's*	R _{θCS} @ 7.5 Mil's*
Wakefield	Delta Pad 173-7	.790	1.175
Bergquist	Sil Pad K-4	.752	1.470
Stockwell Rubber	1867	.742	1.015
Bergquist	Sil Pad 400-9	.735	1.205
Thermalloy	Thermasil II	.680	1.045
Shin-Etsu	TC-30AG	.664	1.260
Bergquist	Sil Pad 400-7	.633	1.060
Chomerics	1674	.592	1.190
Wakefield	Delta Pad 174-9	.574	.755
Bergquist	Sil Pad 1000	.529	.935
Ablestik	Thermal Wafers	.500	.990
Thermalloy	Thermasil III	.440	1.035
Chomerics	1671	.367	.655

*Test Fixture Deviation from flat from Thermalloy EIR86-1010.

Rubber-Duc, however it is only available vulcanized to a heatsink and therefore was not included in the comparison. Published data from AAVID shows $R_{\theta CS}$ below $0.3^{\circ}\text{C}/\text{W}$ for pressures above 500 psi. However, surface flatness and other details are not specified so a comparison cannot be made with other data in this note.

The thermal resistance of some silicone rubber insulators is sensitive to surface flatness when used under a fairly rigid base package. Data for a TO-204AA (TO-3) package insulated with Thermasil is shown on Figure 4. Observe that the "worst case" encountered (7.5 mils) yields results having about twice the thermal resistance of the "typical case" (3 mils), for the more conductive insulator. In order for Thermasil III to exceed the performance of greased mica, total surface flatness must be under 2 mils, a situation that requires spot finishing.

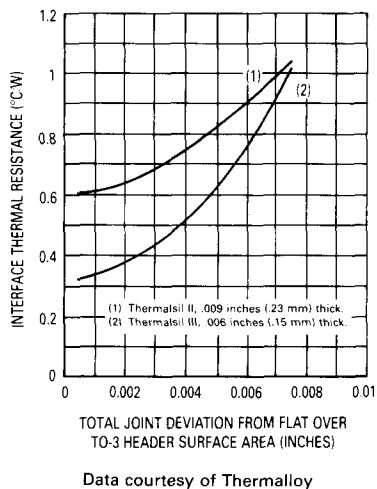


Figure 4. Effect of Total Surface Flatness on Interface Resistance Using Silicon Rubber Insulators

Silicon rubber insulators have a number of unusual characteristics. Besides being affected by surface flatness and initial contact pressure, time is a factor. For example, in a study of the Cho-Therm 1688 pad thermal interface impedance dropped from $0.90^{\circ}\text{C}/\text{W}$ to $0.70^{\circ}\text{C}/\text{W}$ at the end of 1000 hours. Most of the change occurred during the first 200 hours where $R_{\theta CS}$ measured $0.74^{\circ}\text{C}/\text{W}$. The torque on the conventional mounting hardware had decreased to 3 in-lb from an initial 6 in-lb. With non-conformal materials, a reduction in torque would have increased the interface thermal resistance.

Because of the difficulties in controlling all variables affecting tests of interface thermal resistance, data from different manufacturers is not in good agreement. Table 3 shows data obtained from two sources. The relative performance is the same, except for mica which varies widely in thickness. Appendix B discusses the variables which need to be controlled. At the time of this writing ASTM Committee D9 is developing a standard for interface measurements.

The conclusions to be drawn from all this data is that some types of silicon rubber pads, mounted dry, will out perform the commonly used mica with grease. Cost may be a determining factor in making a selection.

Insulation Resistance

When using insulators, care must be taken to keep the mating surfaces clean. Small particles of foreign matter can puncture the insulation, rendering it useless or seriously lowering its dielectric strength. In addition, particularly when voltages higher than 300 V are encountered, problems with creepage may occur. Dust and other foreign material can shorten creepage distances significantly; so having a clean assembly area is important. Surface roughness and humidity also lower insulation resistance. Use of thermal grease usually raises the withstand voltage of the insulation system but excess must be removed to avoid collecting dust. Because of these factors, which are not amenable to analysis, hi-pot testing should be done on prototypes and a large margin of safety employed.

Insulated Electrode Packages

Because of the nuisance of handling and installing the accessories needed for an insulated semiconductor mounting, equipment manufacturers have longed for cost-effective insulated packages since the 1950's. The first to appear were stud mount types which usually have a layer of beryllium oxide between the stud hex and the can. Although effective, the assembly is costly and requires manual mounting and lead wire soldering to terminals on top of the case. In the late eighties, a number of electrically isolated parts became available from various semiconductor manufacturers. These offerings presently consist of multiple chips and integrated circuits as well as the more conventional single chip devices.

The newer insulated packages can be grouped into two categories. The first has insulation between the semiconductor chips and the mounting base; an exposed area of the mounting base is used to secure the part. The EMS (Energy Management Series) Modules, shown on Figure 8, Case 806 (ICePAK) and Case 388A (TO-258AA) (see Figure 11) are examples of parts in this category. The second category contains parts which have a plastic over-mold covering the metal mounting base. The Full Pak,

Table 3. Performance of Silicon Rubber Insulators Tested per MIL-I-49456

Material	Measured Thermal Resistance ($^{\circ}\text{C}/\text{W}$)	
	Thermalloy Data(1)	Berquist Data(2)
Bare Joint, greased	0.033	0.008
BeO, greased	0.082	—
Cho-Therm, 1617	0.233	—
Q Pad (non-insulated)	—	0.009
Sil-Pad, K-10	0.263	0.200
Thermasil III	0.267	—
Mica, greased	0.329	0.400
Sil-Pad 1000	0.400	0.300
Cho-therm 1674	0.433	—
Thermasil II	0.500	—
Sil-Pad 400	0.533	0.440
Sil-Pad K-4	0.583	0.440

(1) From Thermalloy EIR 87-1030
(2) From Berquist Data Sheet

Case 221C, illustrated in Figure 13, is an example of parts in the second category.

Parts in the first category — those with an exposed metal flange or tab — are mounted the same as their non-insulated counterparts. However, as with any mounting system where pressure is bearing on plastic, the over-molded type should be used with a conical compression washer, described later in this note.

FASTENER AND HARDWARE CHARACTERISTICS

Characteristics of fasteners, associated hardware, and the tools to secure them determine their suitability for use in mounting the various packages. Since many problems have arisen because of improper choices, the basic characteristics of several types of hardware are discussed next.

Compression Hardware

Normal split ring lock washers are not the best choice for mounting power semiconductors. A typical #6 washer flattens at about 50 pounds, whereas 150 to 300 pounds is needed for good heat transfer at the interface. A very useful piece of hardware is the conical, sometimes called a Belleville washer, compression washer. As shown in Figure 5, it has the ability to maintain a fairly constant pressure over a wide range of its physical deflection — generally 20% to 80%. When installing, the assembler applies torque until the washer depresses to half its original height. (Tests should be run prior to setting up the assembly line to determine the proper torque for the fastener used to achieve 50% deflection.) The washer will absorb any cyclic expansion of the package, insulating washer or other materials caused by temperature changes. Conical washers are the key to successful mounting of devices requiring strict control of the mounting force or when plastic hardware is used in the mounting scheme. They are used with the large face contacting the packages. A new variation of the conical washer includes it as part of a nut assembly. Called a Sync Nut, the patented device can be soldered to a PC board and the semiconductor mounted with a 6-32 machine screw.⁽⁴⁾

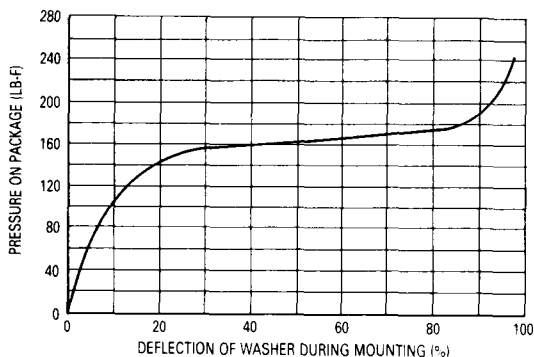


Figure 5. Characteristics of the Conical Compression Washers Designed for Use with Plastic Body Mounted Semiconductors

(4) ITW Shakeproof, St. Charles Road, Elgin, IL 60120.

Clips

Fast assembly is accomplished with clips. When only a few watts are being dissipated, the small board-mounted or free-standing heat dissipators with an integral clip, offered by several manufacturers, result in a low cost assembly. When higher power is being handled, a separate clip may be used with larger heatsinks. In order to provide proper pressure, the clip must be specially designed for a particular heatsink thickness and semiconductor package.

Clips are especially popular with plastic packages such as the TO-220 and TO-126. In addition to fast assembly, the clip provides lower interface thermal resistance than other assembly methods when it is designed for proper pressure to bear on the top of the plastic over the die. The TO-220 package usually is lifted up under the die location when mounted with a single fastener through the hole in the tab because of the high pressure at one end.

Machine Screws

Machine screws, conical washers, and nuts (or sync-nuts) can form a trouble-free fastener system for all types of packages which have mounting holes. However, proper torque is necessary. Torque ratings apply when dry; therefore, care must be exercised when using thermal grease to prevent it from getting on the threads as inconsistent torque readings result. Machine screw heads should not directly contact the surface of plastic packages types as the screw heads are not sufficiently flat to provide properly distributed force. Without a washer, cracking of the plastic case may occur.

Self-Tapping Screws

Under carefully controlled conditions, sheet-metal screws are acceptable. However, during the tapping-process with a standard screw, a volcano-like protrusion will develop in the metal being threaded; an unacceptable surface that could increase the thermal resistance may result. When standard sheet metal screws are used, they must be used in a clearance hole to engage a speed-nut. If a self tapping process is desired, the screw type must be used which roll-forms machine screw threads.

Rivets

Rivets are not a recommended fastener for any of the plastic packages. When a rugged metal flange-mount package or EMS module is being mounted directly to a heatsink, rivets can be used provided press-riveting is used. Crimping force must be applied slowly and evenly. Pop-riveting should never be used because the high crimping force could cause deformation of most semiconductor packages. Aluminum rivets are much preferred over steel because less pressure is required to set the rivet and thermal conductivity is improved.

The hollow rivet, or eyelet, is preferred over solid rivets. An adjustable, regulated pressure press is used such that a gradually increasing pressure is used to pan the eyelet. Use of sharp blows could damage the semiconductor die.

Solder

Until the advent of the surface mount assembly technique, solder was not considered a suitable fastener for power semiconductors. However, user demand has led to the development of new packages for this application. Acceptable soldering methods include conventional belt-

furnace, irons, vapor-phase reflow, and infrared reflow. It is important that the semiconductor temperature not exceed the specified maximum (usually 260°C) or the die bond to the case could be damaged. A degraded die bond has excessive thermal resistance which often leads to a failure under power cycling.

Adhesives

Adhesives are available which have coefficients of expansion compatible with copper and aluminum.⁽⁵⁾ Highly conductive types are available; a 10 mil layer has approximately 0.3°C/W interface thermal resistance. Different types are offered: high strength types for non-field-serviceable systems or low strength types for field-serviceable systems. Adhesive bonding is attractive when case mounted parts are used in wave soldering assembly because thermal greases are not compatible with the conformal coatings used and the greases foul the solder process.

Plastic Hardware

Most plastic materials will flow, but differ widely in this characteristic. When plastic materials form parts of the fastening system, compression washers are highly valuable to assure that the assembly will not loosen with time and temperature cycling. As previously discussed, loss of contact pressure will increase interface thermal resistance.

FASTENING TECHNIQUES

Each of the various classes of packages in use requires different fastening techniques. Details pertaining to each type are discussed in following sections. Some general considerations follow.

To prevent galvanic action from occurring when devices are used on aluminum heatsinks in a corrosive atmosphere, many devices are nickel- or gold-plated. Consequently, precautions must be taken not to mar the finish.

Another factor to be considered is that when a copper based part is rigidly mounted to an aluminum heatsink, a bimetallic system results which will bend with temperature changes. Not only is the thermal coefficient of expansion different for copper and aluminum, but the temperature gradient through each metal also causes each component to bend. If bending is excessive and the package is mounted by two or more screws the semiconductor chip could be damaged. Bending can be minimized by:

1. Mounting the component parallel to the heatsink fins to provide increased stiffness.
2. Allowing the heatsink holes to be a bit oversized so that some slip between surfaces can occur as temperature changes.
3. Using a highly conductive thermal grease or mounting pad between the heatsink and semiconductor to minimize the temperature gradient and allow for movement.

Stud Mount

Parts which fall into the stud-mount classification are shown in Figure 6. Mounting errors with non-insulated stud-mounted parts are generally confined to application

(5) Robert Batson, Elliot Fraunglass and James P. Moran, "Heat Dissipation Through Thermalloy Conductive Adhesives," EMTAS '83, Conference, February 1-3, Phoenix, AZ; Society of Manufacturing Engineers, One SME Drive, P.O. Box 930, Dearborn, MI 48128.

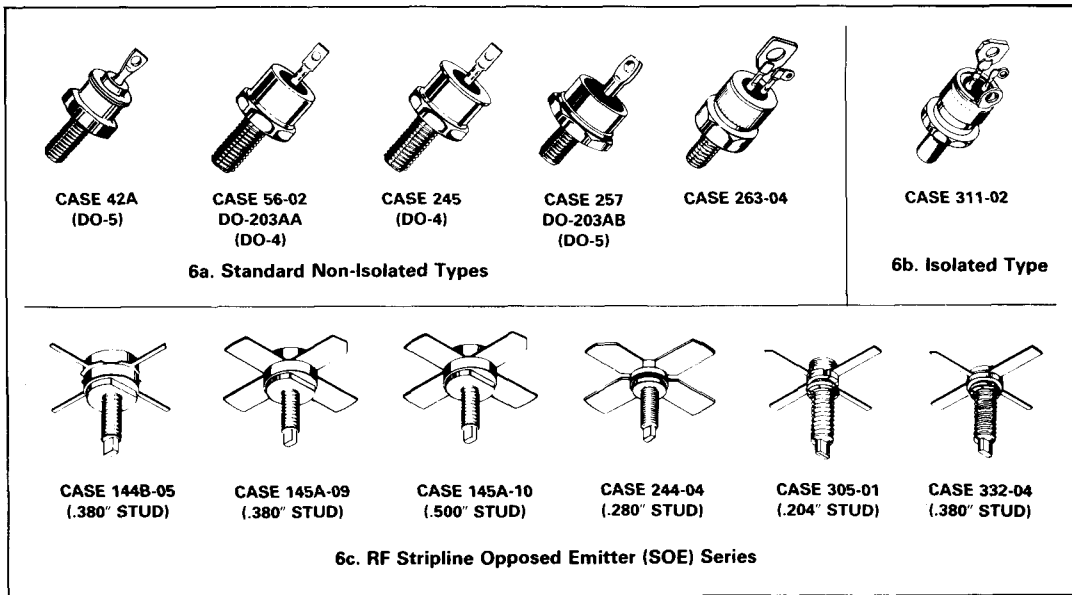


Figure 6. A Variety of Stud-Mount Parts

of excessive torque or tapping the stud into a threaded heatsink hole. Both these practices may cause a warpage of the hex base which may crack the semiconductor die. The only recommended fastening method is to use a nut and washer; the details are shown in Figure 7.

Insulated electrode packages on a stud mount base require less hardware. They are mounted the same as their non-insulated counterparts, but care must be exercised to avoid applying a shear or tension stress to the insulation layer, usually a beryllium oxide (BeO) ceramic. This requirement dictates that the leads must be attached to the circuit with flexible wire. In addition, the stud hex should be used to hold the part while the nut is torqued.

R.F. transistors in the stud-mount stripline opposed emitter (SOE) package impose some additional constraints because of the unique construction of the package. Special techniques to make connections to the strip-line leads and to mount the part so no tension or shear forces are applied to any ceramic — metal interface are discussed in the section entitled "Connecting and Handling Terminals."

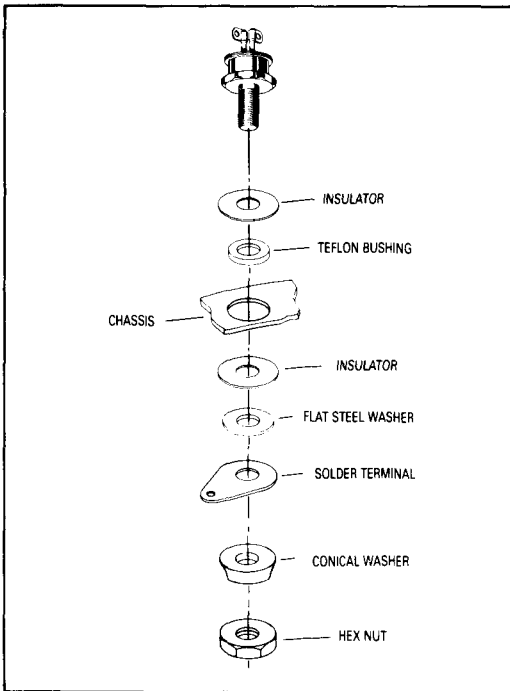


Figure 7. Isolating Hardware Used for a Non-Isolated Stud-Mount Package

Press Fit

For most applications, the press-fit case should be mounted according to the instructions shown in Figure 8. A special fixture meeting the necessary requirements must be used.

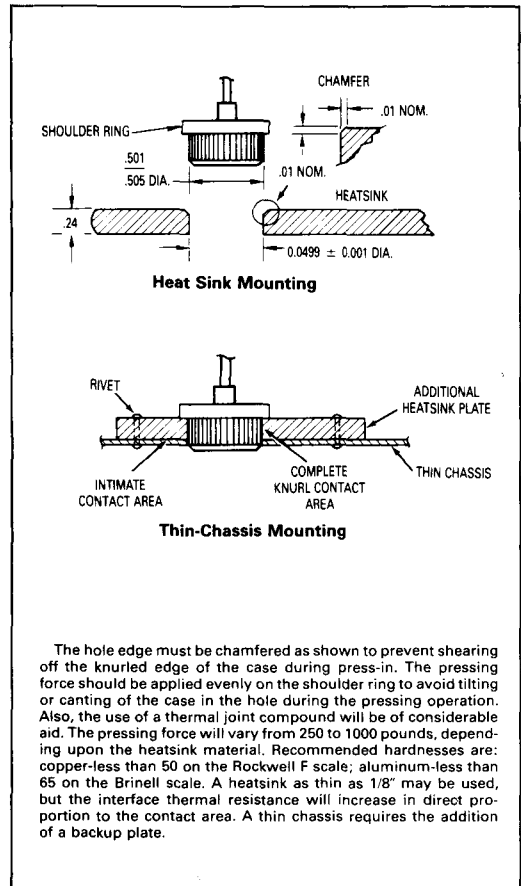


Figure 8. Press-Fit Package

The hole edge must be chamfered as shown to prevent shearing off the knurled edge of the case during press-in. The pressing force should be applied evenly on the shoulder ring to avoid tilting or canting of the case in the hole during the pressing operation. Also, the use of a thermal joint compound will be of considerable aid. The pressing force will vary from 250 to 1000 pounds, depending upon the heatsink material. Recommended hardnesses are: copper-less than 50 on the Rockwell F scale; aluminum-less than 65 on the Brinell scale. A heatsink as thin as 1/8" may be used, but the interface thermal resistance will increase in direct proportion to the contact area. A thin chassis requires the addition of a backup plate.

Flange Mount

A large variety of parts fit into the flange mount category as shown in Figure 9. Few known mounting difficulties exist with the smaller flange mount packages, such as the TO-204 (TO-3). The rugged base and distance between die and mounting holes combine to make it extremely difficult to cause any warpage unless mounted on a surface which is badly bowed or unless one side is tightened excessively before the other screw is started. It is therefore good practice to alternate tightening of the screws so that pressure is evenly applied. After the screws are finger-tight the hardware should be torqued to its final specification in at least two sequential steps. A typical mounting installation for a popular flange type part is shown in Figure 10. Machine screws (preferred) self-tapping screws, eyelets, or rivets may be used to secure the package using guidelines in the previous section. "Fastener and Hardware Characteristics."

The copper flange of the Energy Management Series (EMS) Modules is very thick. Consequently, the parts are rugged and indestructible for all practical purposes. No

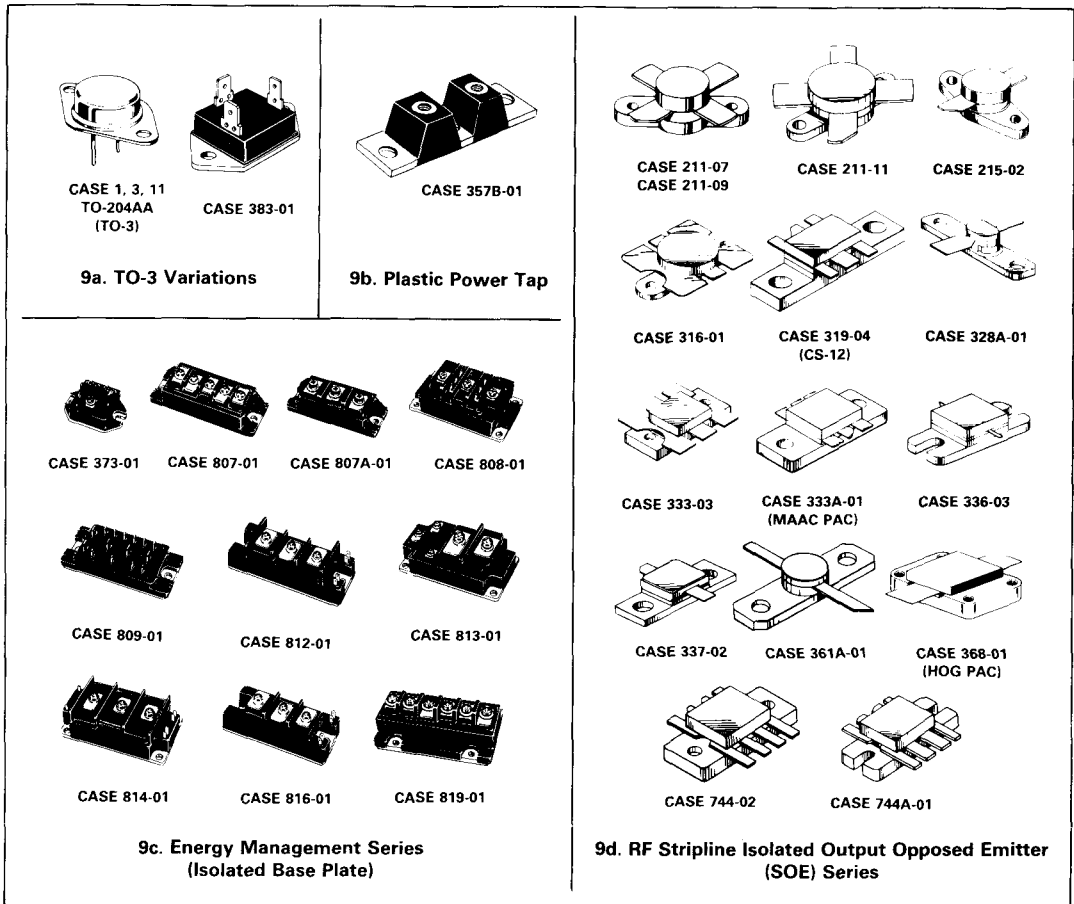


Figure 9. A Large Array of Parts Fit into the Flange-Mount Classification

special precautions are necessary when fastening these parts to a heatsink.

Some packages specify a tightening procedure. For example, with the Power Tap package, Figure 9b, final torque should be applied first to the center position.

The RF power modules (MHW series) are more sensitive to the flatness of the heatsink than other packages because a ceramic (BeO) substrate is attached to a relatively thin, fairly long, flange. The maximum allowable flange bending to avoid mechanical damage has been determined and presented in detail in EB107 "Mounting Considerations for Motorola RF Power Modules." Many of the parts can handle a combined heatsink and flange deviation from flat of 7 to 8 mils which is commonly available. Others must be held to 1.5 mils, which requires that the heatsink have nearly perfect flatness.

Specific mounting recommendations are critical to RF devices in isolated packages because of the internal ceramic substrate. The large area Case 368-1 (HOG PAC) will be used to illustrate problem areas. It is more sen-

sitive to proper mounting techniques than most other RF power devices.

Although the data sheets contain information on recommended mounting procedures, experience indicates that they are often ignored. For example, the recommended maximum torque on the 4-40 mounting screws is 5 in/lbs. Spring and flat washers are recommended. Over torquing is a common problem. In some parts returned for failure analysis, indentions up to 10 mils deep in the mounting screw areas have been observed.

Calculations indicate that the length of the flange increases in excess of two mils with a temperature change of 75°C. In such cases, if the mounting screw torque is excessive, the flange is prevented from expanding in length, instead it bends upwards in the mid-section, cracking the BeO and the die. A similar result can also occur during the initial mounting of the device if an excessive amount of thermal compound is applied. With sufficient torque, the thermal compound will squeeze out of the mounting hole areas, but will remain under the center

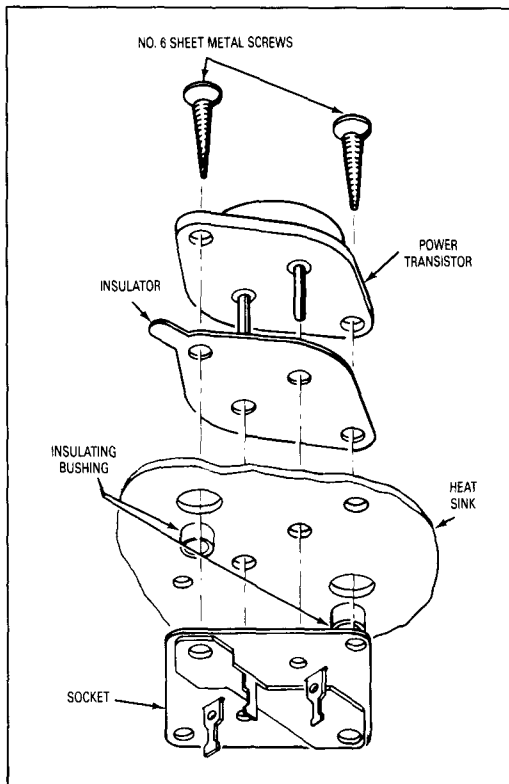


Figure 10. Hardware Used for a TO-204AA (TO-3) Flange Mount Part

of the flange, deforming it. Deformations of 2-3 mils have been measured between the center and the ends under such conditions (enough to crack internal ceramic).

Another problem arises because the thickness of the flange changes with temperature. For the 75°C temperature excursion mentioned, the increased amount is around 0.25 mils which results in further tightening of the mounting screws, thus increasing the effective torque from the initial value. With a decrease in temperature, the opposite effect occurs. Therefore thermal cycling not only causes risk of structural damage but often causes the assembly to loosen which raises the interface resistance. Use of compression hardware can eliminate this problem.

Tab Mount

The tab mount class is composed of a wide array of packages as illustrated in Figure 11. Mounting considerations for all varieties are similar to that for the popular TO-220 package, whose suggested mounting arrangements and hardware are shown in Figure 12. The rectangular washer shown in Figure 12a is used to minimize distortion of the mounting flange; excessive distortion could cause damage to the semiconductor chip. Use of

the washer is only important when the size of the mounting hole exceeds 0.140 inch (6-32 clearance). Larger holes are needed to accommodate the lower insulating bushing when the screw is electrically connected to the case; however, the holes should not be larger than necessary to provide hardware clearance and should never exceed a diameter of 0.250 inch. Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 inch-pounds is suggested when using a 6-32 screw.

Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. To minimize this problem, Motorola TO-220 packages have a chamfer on one end. TO-220 packages of other manufacturers may need a spacer or combination spacer and isolation bushing to raise the screw head above the top surface of the plastic.

The popular TO-220 Package and others of similar construction lift off the mounting surface as pressure is applied to one end. (See Appendix B, Figure B1.) To counter this tendency, at least one hardware manufacturer offers a hard plastic cantilever beam which applies more even pressure on the tab.⁽⁶⁾ In addition, it separates

(6) Catalog, Edition 18, Richco Plastic Company, 5825 N. Tripp Ave., Chicago, IL 60546.

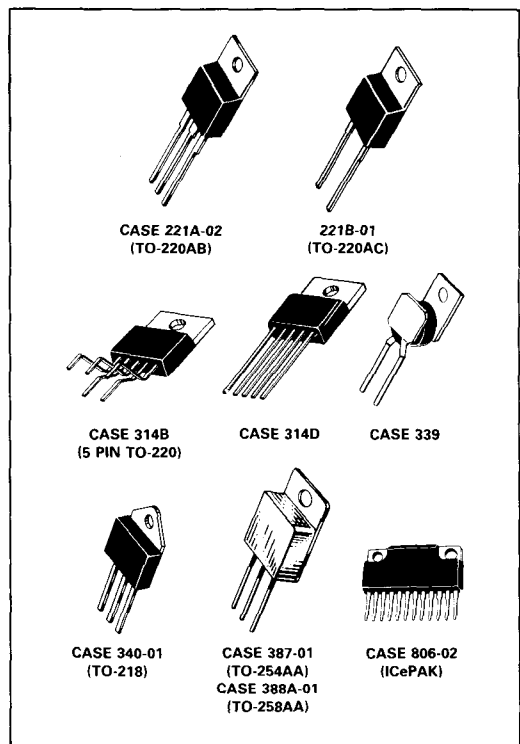


Figure 11. Several Types of Tab-Mount Parts

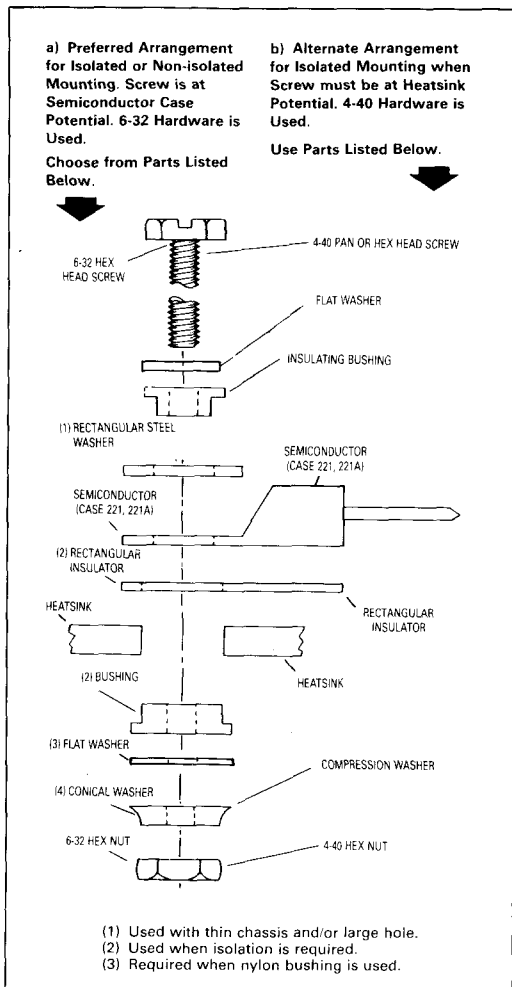


Figure 12. Mounting Arrangements for Tab Mount TO-220

the mounting screw from the metal tab. Tab mount parts may also be effectively mounted with clips as shown in Figure 15c. To obtain high pressure without cracking the case, a pressure spreader bar should be used under the clip. Interface thermal resistance with the cantilever beam or clips can be lower than with screw mounting.

The ICePAK (Case 806-02) is basically an elongated TO-220 package with isolated chips. The mounting precautions for the TO-220 consequently apply. In addition, since two mounting screws are required, the alternate tightening procedure described for the flange mount package should be used.

In situations where a tab mount package is making direct contact with the heatsink, an eyelet may be used, provided sharp blows or impact shock is avoided.

Plastic Body Mount

The Thermopad and Full Pak plastic power packages shown in Figure 13 are typical of packages in this group. They have been designed to feature minimum size with no compromise in thermal resistance. For the Thermopad (Case 77) parts this is accomplished by die-bonding the silicon chip on one side of a thin copper sheet; the opposite side is exposed as a mounting surface. The copper sheet has a hole for mounting; plastic is molded enveloping the chip but leaving the mounting hole open. The low thermal resistance of this construction is obtained at the expense of a requirement that strict attention be paid to the mounting procedure.

The Full Pak (Case 221C-01) is similar to a TO-220 except that the tab is encased in plastic. Because the mounting force is applied to plastic, the mounting procedure differs from a standard TO-220 and is similar to that of the Thermopad.

Several types of fasteners may be used to secure these packages; machine screws, eyelets, or clips are preferred. With screws or eyelets, a conical washer should be used which applies the proper force to the package over a fairly wide range of deflection and distributes the force over a fairly large surface area. Screws should not be tightened with any type of air-driven torque gun or equipment which may cause high impact. Characteristics of a suitable conical washer is shown in Figure 5.

Figure 14 shows details of mounting Case 77 devices. Clip mounting is fast and requires minimum hardware, however, the clip must be properly chosen to insure that the proper mounting force is applied. When electrical isolation is required with screw mounting, a bushing inside the mounting hole will insure that the screw threads do not contact the metal base.

The Full Pak, (Case 221C, 221D and 340B) permits the mounting procedure to be greatly simplified over that of a standard TO-220. As shown in Figure 15c, one properly chosen clip, inserted into two slotted holes in the heat-sink, is all the hardware needed. Even though clip pressure is much lower than obtained with a screw, the thermal resistance is about the same for either method. This occurs because the clip bears directly on top of the die and holds the package flat while the screw causes the package to lift up somewhat under the die. (See Figure B1 of Appendix B.) The interface should consist of a layer of thermal grease or a highly conductive thermal pad. Of course, screw mounting shown in Figure 15b may also be used but a conical compression washer should be included. Both methods afford a major reduction in hardware as compared to the conventional mounting method with a TO-220 package which is shown in Figure 15a.

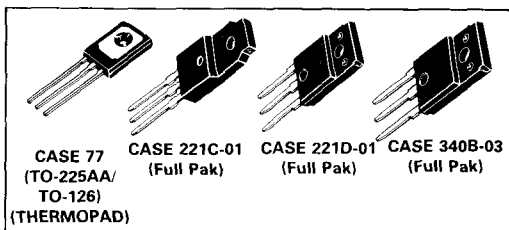


Figure 13. Plastic Body-Mount Packages

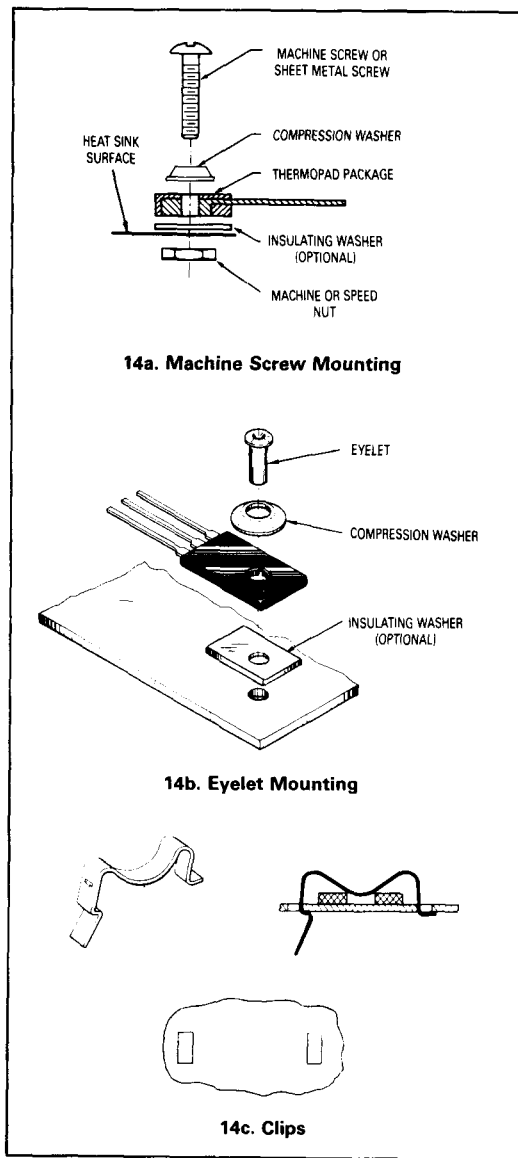


Figure 14. Recommended Mounting Arrangements for TO-225AA (TO-126) Thermopad Packages

Surface Mount

Although many of the tab mount parts have been surface mounted, special small footprint packages for mounting power semiconductors using surface mount assembly techniques have been developed. The DPAK, shown in Figure 16, for example, will accommodate a die up to 112 mils x 112 mils, and has a typical thermal resistance around 2°C/W junction to case. The thermal resis-

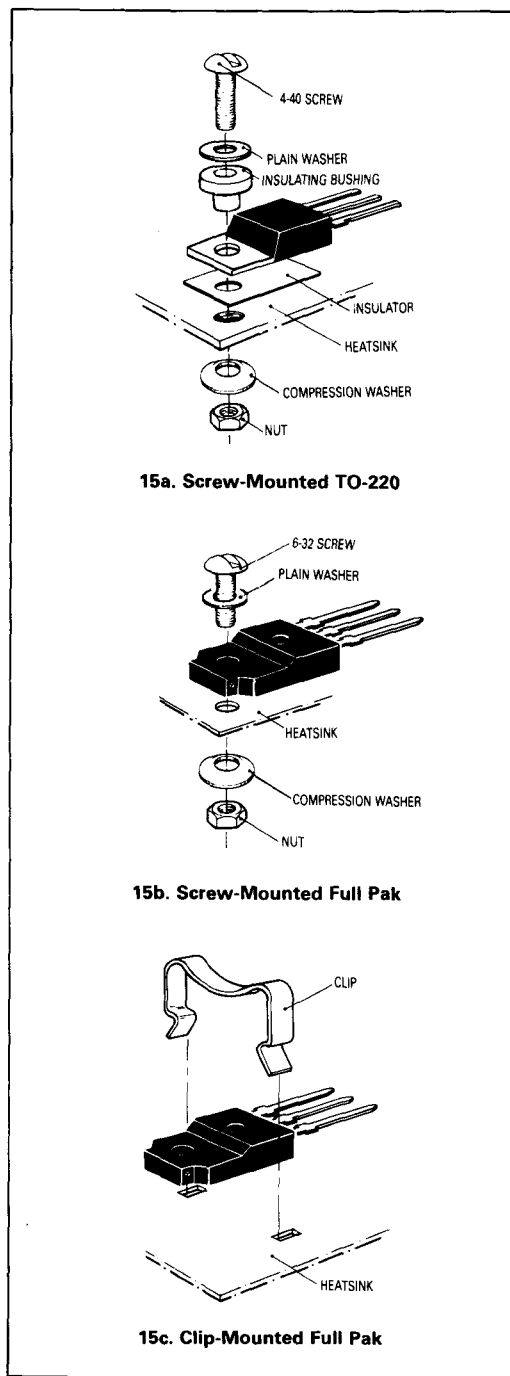


Figure 15. Mounting Arrangements for the Full Pak as Compared to a Conventional TO-220

tance values of the solder interface is well under 1°C/W. The printed circuit board also serves as the heatsink.

Standard Glass-Epoxy 2-ounce boards do not make very good heatsinks because the thin foil has a high thermal resistance. As Figure 17 shows, thermal resistance asymptotes to about 20°C/W at 10 square inches of board area, although a point of diminishing returns occurs at about 3 square inches.

Boards are offered that have thick aluminum or copper substrates. A dielectric coating designed for low thermal resistance is overlaid with one or two ounce copper foil for the preparation of printed conductor traces. Tests run on such a product indicate that case to substrate thermal resistance is in the vicinity of 1°C/W, exact values depending upon board type.⁽⁷⁾ The substrate may be an effective heatsink itself, or it can be attached to a conventional finned heatsink for improved performance.

Since DPAK and other surface mount packages are designed to be compatible with surface mount assembly techniques, no special precautions are needed other than to insure that maximum temperature/time profiles are not exceeded.

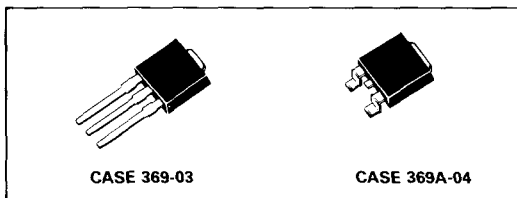


Figure 16. Surface Mount D-PAK Parts

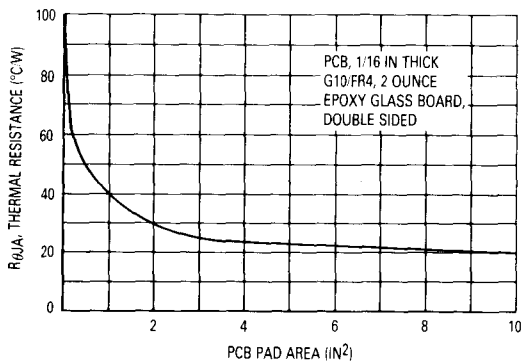


Figure 17. Effect of Footprint Area on Thermal Resistance of DPAK Mounted on a Glass-Epoxy Board

FREE AIR AND SOCKET MOUNTING

In applications where average power dissipation is on the order of a watt or so, most power semiconductors may be mounted with little or no heatsinking. The leads

(7) Herb Fick, "Thermal Management of Surface Mount Power Devices," Powerconversion and Intelligent Motion, August 1987.

of the various metal power packages are not designed to support the packages; their cases must be firmly supported to avoid the possibility of cracked seals around the leads. Many plastic packages may be supported by their leads in applications where high shock and vibration stresses are not encountered and where no heatsink is used. The leads should be as short as possible to increase vibration resistance and reduce thermal resistance. As a general practice however, it is better to support the package. A plastic support for the TO-220 Package and other similar types is offered by heatsink accessory vendors.

In many situations, because its leads are fairly heavy, the CASE 77 (TO-225AA) (TO-127) package has supported a small heatsink; however, no definitive data is available. When using a small heatsink, it is good practice to have the sink rigidly mounted such that the sink or the board is providing total support for the semiconductor. Two possible arrangements are shown in Figure 18. The arrangement of part (a) could be used with any plastic package, but the scheme of part (18b) is more practical

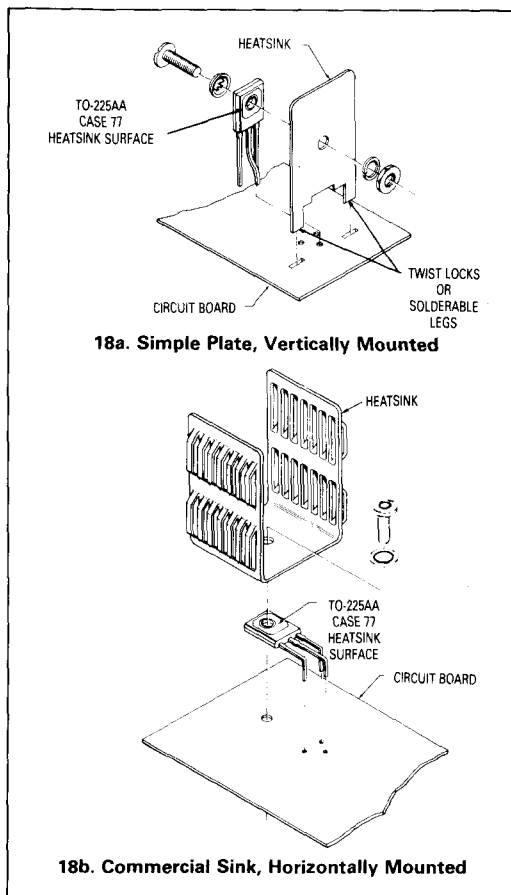


Figure 18. Methods of Using Small Heatsinks With Plastic Semiconductor Packages

with Case 77 Thermopad devices. With the other package types, mounting the transistor on top of the heatsink is more practical.

In certain situations, in particular where semiconductor testing is required or prototypes are being developed, sockets are desirable. Manufacturers have provided sockets for many of the packages available from Motorola. The user is urged to consult manufacturers' catalogs for specific details. Sockets with Kelvin connections are necessary to obtain accurate voltage readings across semiconductor terminals.

CONNECTING AND HANDLING TERMINALS

Pins, leads, and tabs must be handled and connected properly to avoid undue mechanical stress which could cause semiconductor failure. Change in mechanical dimensions as a result of thermal cycling over operating temperature extremes must be considered. Standard metal, plastic, and RF stripline packages each have some special considerations.

Metal Packages

The pins and lugs of metal packaged devices using glass to metal seals are not designed to handle any significant bending or stress. If abused, the seals could crack. Wires may be attached using sockets, crimp connectors or solder, provided the data sheet ratings are observed. When wires are attached directly to the pins, flexible or braided leads are recommended in order to provide strain relief.

EMS Modules

The screw terminals of the EMS modules look deceptively rugged. Since the flange base is mounted to a rigid heatsink, the connection to the terminals must allow some flexibility. A rigid buss bar should not be bolted to terminals. Lugs with braid are preferred.

Plastic Packages

The leads of the plastic packages are somewhat flexible and can be reshaped although this is not a recommended procedure. In many cases, a heatsink can be chosen which makes lead-bending unnecessary. Numerous lead- and tab-forming options are available from Motorola on large quantity orders. Preformed leads remove the users risk of device damage caused by bending.

If, however, lead-bending is done by the user, several basic considerations should be observed. When bending the lead, support must be placed between the point of bending and the package. For forming small quantities of units, a pair of pliers may be used to clamp the leads at the case, while bending with the fingers or another pair of pliers. For production quantities, a suitable fixture should be made.

The following rules should be observed to avoid damage to the package.

1. A lead bend radius greater than 1/16 inch is advisable for TO-225AA (CASE 77) and 1/32 inch for TO-220.
2. No twisting of leads should be done at the case.
3. No axial motion of the lead should be allowed with respect to the case.

The leads of plastic packages are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement imposes axial stress on the leads, a condition which may be caused by thermal cycling, some method of strain relief should be devised. When wires are used for connections, care should be

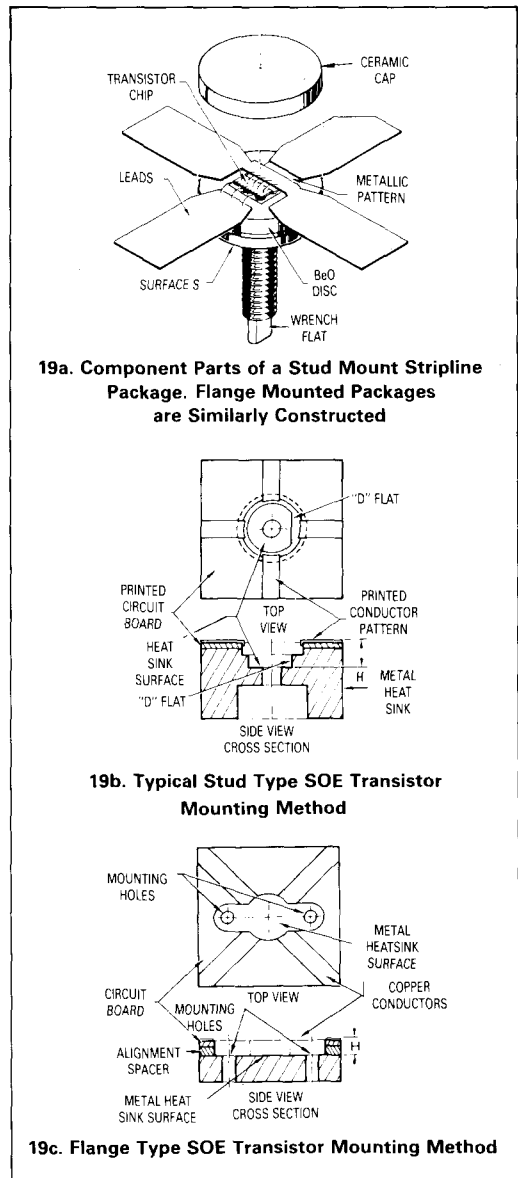


Figure 19. Mounting Details for SOE Transistors

exercised to assure that movement of the wire does not cause movement of the lead at the lead-to-plastic junctions. Highly flexible or braided wires are good for providing strain relief.

Wire-wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. The leads may be soldered; the maximum soldering temperature, however, must not exceed 260°C and must be applied for not more than 5 seconds at a distance greater than 1/8 inch from the plastic case.

Stripline Packages

The leads of stripline packages normally are soldered into a board while the case is recessed to contact a heatsink as shown in Figure 19. The following rules should be observed:

1. The device should never be mounted in such a manner as to place ceramic-to-metal joints in tension.
2. The device should never be mounted in such a manner as to apply force on the strip leads in a vertical direction towards the cap.
3. When the device is mounted in a printed circuit board with the copper stud and BeO portion of the header passing through a hole in the circuit boards, adequate clearance must be provided for the BeO to prevent shear forces from being applied to the leads.
4. Some clearance must be allowed between the leads and the circuit board when the device is secured to the heatsink.
5. The device should be properly secured into the heatsinks before its leads are attached into the circuit.
6. The leads on stud type devices must not be used to prevent device rotation during stud torque application. A wrench flat is provided for this purpose.

Figure 19b shows a cross-section of a printed circuit board and heatsink assembly for mounting a stud type stripline device. H is the distance from the top surface of the printed circuit board to the D-flat heatsink surface. If H is less than the minimum distance from the bottom of the lead material to the mounting surface of the package, there is no possibility of tensile forces in the copper stud — BeO ceramic joint. If, however, H is greater than the package dimension, considerable force is applied to the cap to BeO joint and the BeO to stud joint. Two occurrences are possible at this point. The first is a cap joint failure when the structure is heated, as might occur during the lead-soldering operation; while the second is BeO to stud failure if the force generated is high enough. Lack of contact between the device and the heatsink surface will occur as the differences between H and the package dimension become larger, this may result in device failure as power is applied.

Figure 19c shows a typical mounting technique for flange-type stripline transistors. Again, H is defined as the distance from the top of the printed circuit board to the heatsink surface. If distance H is less than the minimum distance from the bottom of transistor lead to the bottom surface of the flange, tensile forces at the various joints in the package are avoided. However, if distance H exceeds the package dimension, problems similar to those discussed for the stud type devices can occur.

CLEANING CIRCUIT BOARDS

It is important that any solvents or cleaning chemicals used in the process of degreasing or flux removal do not affect the reliability of the devices. Alcohol and unchlorinated Freon solvents are generally satisfactory for use with plastic devices, since they do not damage the package. Hydrocarbons such as gasoline and chlorinated Freon may cause the encapsulant to swell, possibly damaging the transistor die.

When using an ultrasonic cleaner for cleaning circuit boards, care should be taken with regard to ultrasonic energy and time of application. This is particularly true if any packages are free-standing without support.

THERMAL SYSTEM EVALUATION

Assuming that a suitable method of mounting the semiconductor without incurring damage has been achieved, it is important to ascertain whether the junction temperature is within bounds.

In applications where the power dissipated in the semiconductor consists of pulses at a low duty cycle, the instantaneous or peak junction temperature, not average temperature, may be the limiting condition. In this case, use must be made of transient thermal resistance data. For a full explanation of its use, see Motorola Application Note, AN569.

Other applications, notably RF power amplifiers or switches driving highly reactive loads, may create severe current crowding conditions which render the traditional concepts of thermal resistance or transient thermal impedance invalid. In this case, transistor safe operating area, thyristor di/dt limits, or equivalent ratings as applicable, must be observed.

Fortunately, in many applications, a calculation of the average junction temperature is sufficient. It is based on the concept of thermal resistance between the junction and a temperature reference point on the case. (See Appendix A.) A fine wire thermocouple should be used, such as #36 AWG, to determine case temperature. Average operating junction temperature can be computed from the following equation:

$$T_J = T_C + R_{\theta JC} \times P_D$$

where T_J = junction temperature (°C)

T_C = case temperature (°C)

$R_{\theta JC}$ = thermal resistance junction-to-case as specified on the data sheet (°C/W)

P_D = power dissipated in the device (W)

The difficulty in applying the equation often lies in determining the power dissipation. Two commonly used empirical methods are graphical integration and substitution.

Graphical Integration

Graphical integration may be performed by taking oscilloscope pictures of a complete cycle of the voltage and current waveforms, using a limit device. The pictures should be taken with the temperature stabilized. Corresponding points are then read from each photo at a suitable number of time increments. Each pair of voltage and current values are multiplied together to give instanta-

neous values of power. The results are plotted on linear graph paper, the number of squares within the curve counted, and the total divided by the number of squares along the time axis. The quotient is the average power dissipation. Oscilloscopes are available to perform these measurements and make the necessary calculations.

Substitution

This method is based upon substituting an easily measurable, smooth dc source for a complex waveform. A switching arrangement is provided which allows operating the load with the device under test, until it stabilizes

in temperature. Case temperature is monitored. By throwing the switch to the "test" position, the device under test is connected to a dc power supply, while another pole of the switch supplies the normal power to the load to keep it operating at full power level. The dc supply is adjusted so that the semiconductor case temperature remains approximately constant when the switch is thrown to each position for about 10 seconds. The dc voltage and current values are multiplied together to obtain average power. It is generally necessary that a Kelvin connection be used for the device voltage measurement.

APPENDIX A THERMAL RESISTANCE CONCEPTS

The basic equation for heat transfer under steady-state conditions is generally written as:

$$q = hA\Delta T \quad (1)$$

where q = rate of heat transfer or power dissipation (P_D)
 h = heat transfer coefficient,
 A = area involved in heat transfer,
 ΔT = temperature difference between regions of heat transfer.

However, electrical engineers generally find it easier to work in terms of thermal resistance, defined as the ratio of temperature to power. From Equation 1, thermal resistance, R_θ , is

$$R_\theta = \Delta T/q = 1/hA \quad (2)$$

The coefficient (h) depends upon the heat transfer mechanism used and various factors involved in that particular mechanism.

An analogy between Equation (2) and Ohm's Law is often made to form models of heat flow. Note that T could be thought of as a voltage thermal resistance corresponds to electrical resistance (R); and, power (q) is analogous to current (I). This gives rise to a basic thermal resistance model for a semiconductor as indicated by Figure A1.

The equivalent electrical circuit may be analyzed by using Kirchoff's Law and the following equation results:

$$T_J = P_D(R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) + T_A \quad (3)$$

where T_J = junction temperature,
 P_D = power dissipation
 $R_{\theta JC}$ = semiconductor thermal resistance (junction to case),
 $R_{\theta CS}$ = interface thermal resistance (case to heatsink),
 $R_{\theta SA}$ = heatsink thermal resistance (heatsink to ambient),
 T_A = ambient temperature.

The thermal resistance junction to ambient is the sum of the individual components. Each component must be minimized if the lowest junction temperature is to result.

The value for the interface thermal resistance, $R_{\theta CS}$, may be significant compared to the other thermal-resistance terms. A proper mounting procedure can minimize $R_{\theta CS}$.

The thermal resistance of the heatsink is not absolutely constant; its thermal efficiency increases as ambient temperature increases and it is also affected by orientation of the sink. The thermal resistance of the semiconductor is also variable; it is a function of biasing and temperature. Semiconductor thermal resistance specifications are normally at conditions where current density is fairly uniform. In some applications such as in RF power amplifiers and short-pulse applications, current density is not uniform and localized heating in the semiconductor chip will be the controlling factor in determining power handling ability.

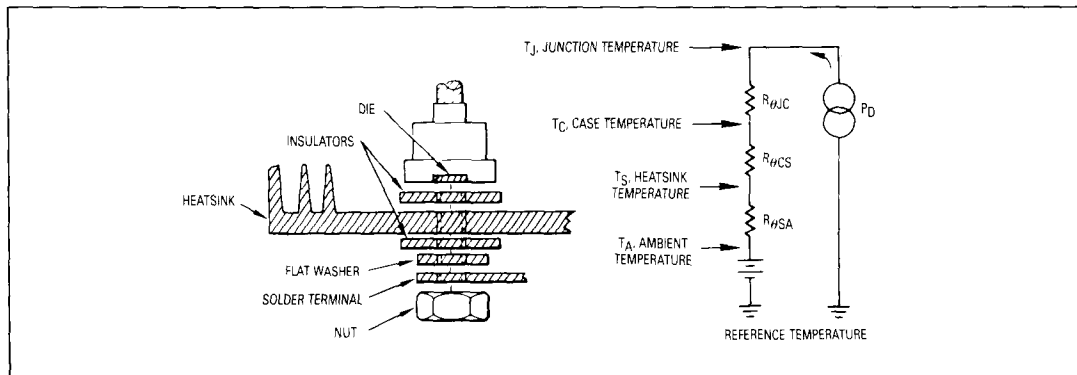


Figure A1. Basic Thermal Resistance Model Showing Thermal to Electrical Analogy for a Semiconductor

APPENDIX B MEASUREMENT OF INTERFACE THERMAL RESISTANCE

Measuring the interface thermal resistance $R_{\theta CS}$ appears deceptively simple. All that's apparently needed is a thermocouple on the semiconductor case, a thermocouple on the heatsink, and a means of applying and measuring DC power. However, $R_{\theta CS}$ is proportional to the amount of contact area between the surfaces and consequently is affected by surface flatness and finish and the amount of pressure on the surfaces. The fastening method may also be a factor. In addition, placement of the thermocouples can have a significant influence upon the results. Consequently, values for interface thermal resistance presented by different manufacturers are not in good agreement. Fastening methods and thermocouple locations are considered in this Appendix.

When fastening the test package in place with screws, thermal conduction may take place through the screws, for example, from the flange ear on a TO-3 package directly to the heatsink. This shunt path yields values which are artificially low for the insulation material and dependent upon screw head contact area and screw material. MIL-I-49456 allows screws to be used in tests for interface thermal resistance probably because it can be argued that this is "application oriented."

Thermalloy takes pains to insulate all possible shunt conduction paths in order to more accurately evaluate insulation materials. The Motorola fixture uses an insulated clamp arrangement to secure the package which also does not provide a conduction path.

As described previously, some packages, such as a TO-220, may be mounted with either a screw through the tab or a clip bearing on the plastic body. These two methods often yield different values for interface thermal resistance. Another discrepancy can occur if the top of the package is exposed to the ambient air where radiation and convection can take place. To avoid this, the package should be covered with insulating foam. It has been estimated that a 15 to 20% error in $R_{\theta CS}$ can be incurred from this source.

Another significant cause for measurement discrepancies is the placement of the thermocouple to measure

the semiconductor case temperature. Consider the TO-220 package shown in Figure B1. The mounting pressure at one end causes the other end — where the die is located — to lift off the mounting surface slightly. To improve contact, Motorola TO-220 Packages are slightly concave. Use of a spreader bar under the screw lessens the lifting, but some is inevitable with a package of this structure. Three thermocouple locations are shown:

a. The Motorola location is directly under the die reached through a hole in the heatsink. The thermocouple is held in place by a spring which forces the thermocouple into intimate contact with the bottom of the semi's case.

b. The JEDEC location is close to the die on the top surface of the package base reached through a blind hole drilled through the molded body. The thermocouple is swaged in place.

c. The Thermalloy location is on the top portion of the tab between the molded body and the mounting screw. The thermocouple is soldered into position.

Temperatures at the three locations are generally not the same. Consider the situation depicted in the figure. Because the only area of direct contact is around the mounting screw, nearly all the heat travels horizontally along the tab from the die to the contact area. Consequently, the temperature at the JEDEC location is hotter than at the Thermalloy location and the Motorola location is even hotter. Since junction-to-sink thermal resistance must be constant for a given test setup, the calculated junction-to-case thermal resistance values decrease and case-to-sink values increase as the "case" temperature thermocouple readings become warmer. Thus the choice of reference point for the "case" temperature is quite important.

There are examples where the relationship between the thermocouple temperatures are different from the previous situation. If a mica washer with grease is installed between the semiconductor package and the heatsink, tightening the screw will not bow the package; instead, the mica will be deformed. The primary heat conduction path is from the die through the mica to the heatsink. In this case, a small temperature drop will exist across the vertical dimension of the package mounting base so that the thermocouple at the EIA location will be the hottest. The thermocouple temperature at the Thermalloy location will be lower but close to the temperature at the EIA location as the lateral heat flow is generally small. The Motorola location will be coolest.

The EIA location is chosen to obtain the highest temperature on the case. It is of significance because power ratings are supposed to be based on this reference point. Unfortunately, the placement of the thermocouple is tedious and leaves the semiconductor in a condition unfit for sale.

The Motorola location is chosen to obtain the highest temperature of the case at a point where, hopefully, the case is making contact to the heatsink. Once the special heatsink to accommodate the thermocouple has been fabricated, this method lends itself to production testing and does not mark the device. However, this location is not easily accessible to the user.

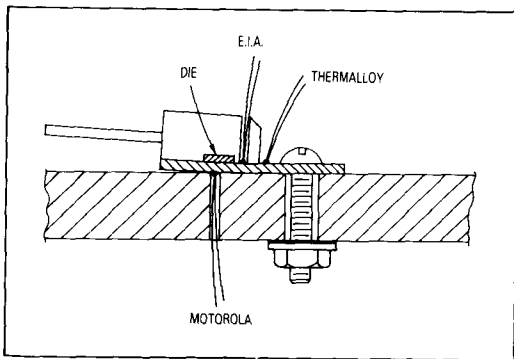


Figure B1. JEDEC TO-220 Package Mounted to Heatsink Showing Various Thermocouple Locations and Lifting Caused by Pressure at One End

The Thermalloy location is convenient and is often chosen by equipment manufacturers. However, it also blemishes the case and may yield results differing up to 1°C W for a TO-220 package mounted to a heatsink without thermal grease and no insulator. This error is small when compared to the thermal resistance of heat dissipaters often used with this package, since power dissipation is usually a few watts. When compared to the specified junction-to-case values of some of the higher power semiconductors becoming available, however, the difference becomes significant and it is important that the semiconductor manufacturer and equipment manufacturer use the same reference point.

Another EIA method of establishing reference temper-

atures utilizes a soft copper washer (thermal grease is used) between the semiconductor and the heatsink. The washer is better than 63 μ -inch, and has an imbedded thermocouple near its center. This reference includes the interface resistance under nearly ideal conditions and is therefore application-oriented. It is also easy to use but has not become widely accepted.

A good way to improve confidence in the choice of case reference point is to also test for junction-to-case thermal resistance while testing for interface thermal resistance. If the junction-to-case values remain relatively constant as insulators are changed, torque varied, etc., then the case reference point is satisfactory.

APPENDIX C Sources of Accessories

Manufacturer	Joint Compound	Adhesives	Insulators						Heatsinks
			BeO	AlO ₂	Anodize	Mica	Plastic Film	Silicone Rubber	
Aavid Eng.	X	X	—	—	—	—	—	X	X
AHAM-TOR	—	—	—	—	—	—	—	—	X
Astrodynamicis	X	—	—	—	—	—	—	—	X
Delbert Blinn	—	—	X	—	X	X	X	X	X
IERC	X	—	—	—	—	—	—	—	X
Staver	—	—	—	—	—	—	—	—	X
Thermalloy	X	X	X	X	X	X	X	X	X
Tran-tec	—	—	X	X	X	X	—	X	X
Wakefield Eng.	X	X	X	—	X	—	—	X	X

Other sources for silicone rubber pads: Chomerics, Berquist

Suppliers Addresses

Aavid Engineering, Inc., 30 Cook Court, Laconia, New Hampshire 03246 (603) 524-4443

AHAM-TOR Heatsinks, 27901 Front Street, Rancho, California 92390 (714) 676-4151

Astro Dynamics, Inc., 2 Gill St., Woburn, Massachusetts 01801 (617) 935-4944

Berquist, 5300 Edina Industrial Blvd., Minneapolis, Minnesota 55435 (612) 835-2322

Chomerics, Inc., 16 Flagstone Drive, Hudson, New Hampshire 03051 1-800-633-8800

Delbert Blinn Company, P.O. Box 2007, Pomona, California 91769 (714) 629-3900

International Electronic Research Corporation, 135 West Magnolia Boulevard, Burbank, California 91502

(213) 849-2481

The Staver Company, Inc., 41-51 Saxon Avenue, Bay Shore, Long Island, New York 11706 (516) 666-8000

Thermalloy, Inc., P.O. Box 34829, 2021 West Valley View Lane, Dallas, Texas 75234 (214) 243-4321

Tran-tec Corporation, P.O. Box 1044, Columbus, Nebraska 68601 (402) 564-2748

Wakefield Engineering, Inc., Wakefield, Massachusetts 01880 (617) 245-5900

PACKAGE INDEX

PREFACE

When the JEDEC registration system for package outlines started in 1957, numbers were assigned sequentially whenever manufacturers wished to establish a package as an industry standard. As minor variations developed from these industry standards, either a new, non-related number was issued by JEDEC or manufacturers would attempt to relate the part to an industry standard via some appended description.

In an attempt to ease confusion, JEDEC established the present system in late 1968 in which new packages are assigned into a category, based on their general physical appearance. Differences between specific packages in a category are denoted by suffix letters. The older package

designations were re-registered to the new system as time permitted.

For example the venerable TO-3 has many variations. Can heights differ and it is available with 30, 40, 50, and 60 mil pins, with and without lugs. It is now classified in the TO-204 family. The TO-204AA conforms to the original outline for the TO-3 having 40 mil pins while the TO-204AE has 60 mil pins, for example.


The new numbers for the old parts really haven't caught on very well. It seems that the DO-4, DO-5 and TO-3 still convey sufficient meaning for general verbal communication.

Motorola Case Number	JEDEC Outline		Notes	Mounting Class	See Page
	Original System	Revised System			
001	TO-3	TO-204AA		Flange	9
003	TO-3		2	Flange	9
009	TO-61	TO-210AC		Stud	8
011	TO-3	TO-204AA	—	Flange	9
011A	TO-3	—	2	Flange	9
012	TO-3	—	2	Flange	9
036	TO-60	TO-210AB	—	Stud	8
042A	DO-5	DO-203AB	—	Stud	8
044	DO-4	DO-203AA	—	Stud	8
054	TO-3	—	2	Flange	9
056	DO-4	—	—	Stud	8
058	DO-5	—	2	Stud	8
61-03				Flange	9
63-02	TO-64	TO-208AB		Stud	8
63-03	TO-64	TO-208AB		Stud	8
077	TO-126	TO-225AA	—	Plastic	12
080	TO-66	TO-213AA	—	Flange	9
086	—	TO-208	1	Stud	8
086L	—	TO-298	1	Stud	8
144B-05				Stud	8
145A-09				Stud	8
145A-10				Stud	8
145C	TO-232		1	Stud	8
157	—	DO-203	1	Stud	8
160-03	TO-59	TO-210AA	—	Stud	8
167	—	DO-203	1	Stud	8
174-04				Pressfit	9
175-03				Stud	8
197	—	TO-204AE	—	Flange	9
211-07				Flange	9
211-09				Flange	9

Motorola Case Number	JEDEC Outline		Notes	Mounting Class	See Page
	Original System	Revised System			
211-11				Flange	9
215-02				Flange	9
221	—	TO-220AB	—	Tab	11
221C-02				Plastic	12
221D-01	—	—	Isolated TO-220	Plastic	12
235	—	TO-208	1	Stud	8
235-03				Stud	8
238	—	TO-208	1	Stud	8
239	—	TO-208	—	Stud	8
244-04				Stud	8
245	DO-4	—	—	Stud	8
257-01	DO-5	—	—	Stud	8
263	—	TO-208	—	Stud	8
263-04				Stud	8
283	DO-4	—	—	Stud	8
289	—	TO-209	1	Stud	8
305-01				Stud	8
310-02				Pressfit	9
311-01			Isolated	Stud	8
311-02				Pressfit	9
311-02				Stud	8
314B-01				Tab	11
314D-01				Tab	11
316-01				Flange	9
319-04				Flange	9
328A-01				Flange	9
332-04				Stud	8
333-03				Flange	9
333A-01				Flange	9
336-03				Flange	9

Motorola Case Number	JEDEC Outline		Notes	Mounting Class	See Page
	Original System	Revised System			
337-02				Flange	9
340		TO-218AC		Tab	11
340A-02				Plastic	12
340B-03			Isolated TO-218	Plastic	12
342-01				Flange	9
357B-01				Flange	9
361-01				Flange	9
368-01				Flange	9
369-03		TO-251		Insertion	14
369A-04		TO-252		Surface	13
373-01			Isolated	Flange	9
383-01			Isolated	Flange	10
387-01		TO-254AA	Isolated 2	Tab	11
388A-01		TO-258AA	Isolated 2	Tab	11
744-02				Flange	9
744A-01				Flange	9
806-02			Isolated	Flange	9
807-01			Isolated	Flange	9
807-02			Isolated	Flange	9
807A-01			Isolated	Flange	9
808-01			Isolated	Flange	9
809-01			Isolated	Flange	9
812-01			Isolated	Flange	9
813-01			Isolated	Flange	9
814-01			Isolated	Flange	9
814A-01			Isolated	Flange	9
084B-01			Isolated	Flange	9
816-01			Isolated	Flange	9
819-01			Isolated	Flange	9
043-02	DO-21	DO-208AA		Pressfit	9

Notes: 1. Would fit within this family outline if registered with JEDEC.
2. Not within all JEDEC dimensions.

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